# Belle2 TRG System

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TRG/DAQ Workshop
2011/01/25
Zhongguanyuan Global Village, PKU

# Requirements and Strategy

- **Requirements (☑ = ok, ☒ = under study or unknown)**
  - ☑ **High efficiency** — **almost 100% for Upsilon 4S events**
    - No deadtime -> pipeline
    - Redundant and independent TRG logics -> 3 main TRG
  - ☒ **Max. average rate** — **30 kHz @ $8 \times 10^{35}$ $cm^{-2}s^{-1}$**
    - Limit from DAQ
    - Good background reduction
      - Flexible TRG logics to manage BG rates
      - Low level event reconstruction to identify BG
  - ☑ **Latency** — **~5 usec**
    - Limit from SVD front-end
  - ☑ **Timing precision** — **less than 10 nsec**
    - Request from SVD front-end
  - ☒ **Event separation** — **200 nsec**
    - Request from DAQ
- **Belle triggering scheme is employed again**
  - Sub-Triggers + Global Decision Logic
  - Basic idea is same, but each components will be improved

    Data flow : parallel -> high-speed serial

    Data rate : 16 Mbps -> 190 Mbps (CDC wire case)

    Logic : hard-coded -> FPGA

    #cables and modules : O(1000) -> O(100)

# Physics Processes and TRG Logics

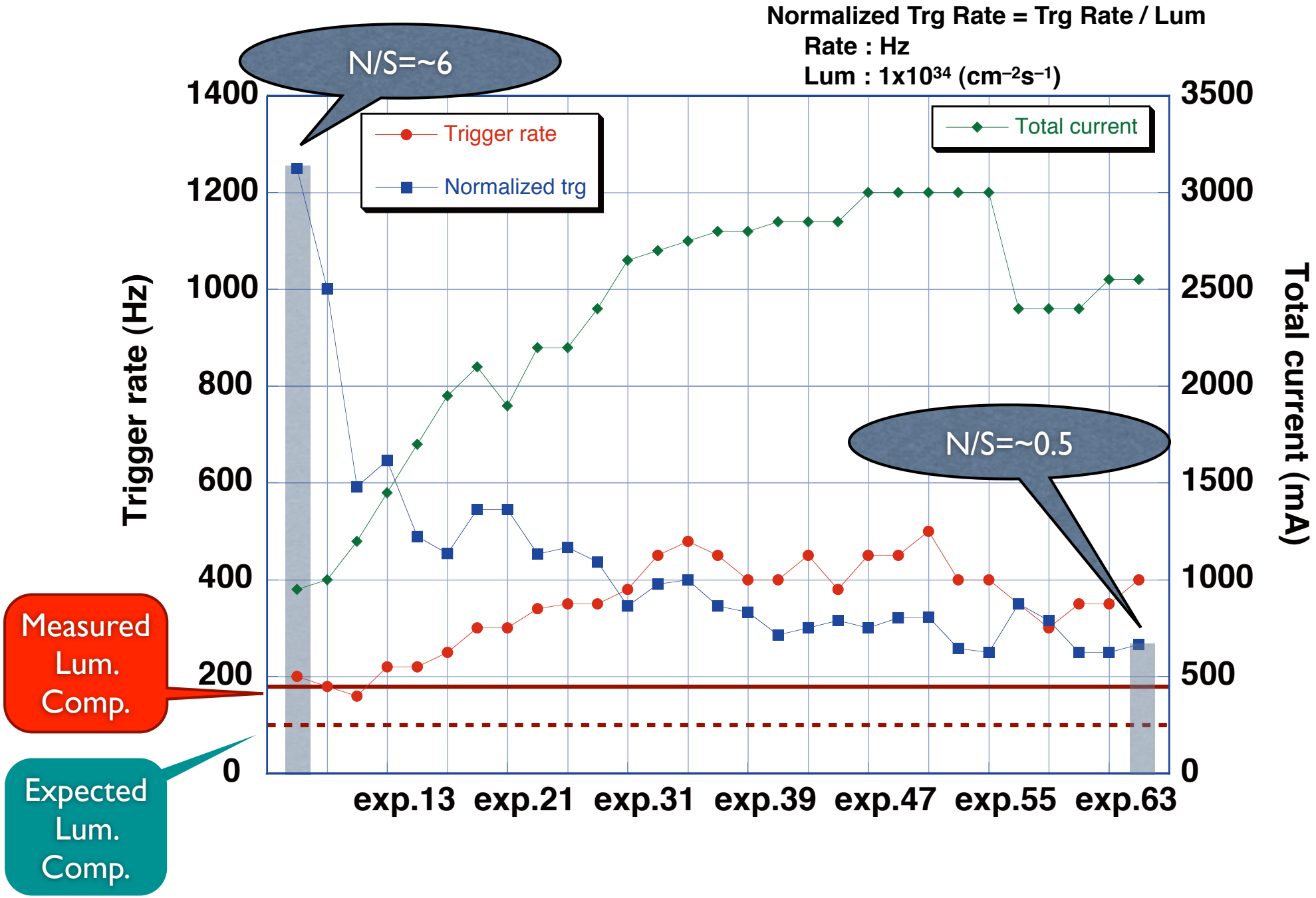
| Process | σ (nb) | Rate (Hz) @ L=8x10$^{35}$ |
|---|---|---|
| Upsilon(4S) | 1.2 | 960 |
| Continuum | 2.8 | 2200 |
| μμ | 0.8 | 640 |
| ττ | 0.8 | 640 |
| Bhabha * | 44 | 350 |
| γ-γ * | 2.4 | 19 |
| Two photon ** | 80 | 15000 |
| Total | 67 | ~20000 |

* Rate of Bhabha and γ-γ are pre-scaled by factor 100

** Rates are estimated by the luminosity component in Belle L1 trigger rate

- **Physics triggers**
  - **Upsilon 4S + continuum**
    - **Three-track**
    - **Total energy**
    - **Isolated cluster**
  - **Tau pair**
    - **Two-track**
- **Calibration triggers**
  - **Bhabha**
    - **Pre-scaled by Bhabha trigger (ECL)**
  - **γ-γ**
    - **Pre-scaled by γ-γ trigger (ECL)**
  - **Mu pair**
    - **Two-track**
  - **Random trigger**
- **Veto**
  - **Beam injection**
  - **Two photon events if necessary**
    - **Low level reconstruction is necessary**

# TRG History in Belle



# TRG Rate Estimation

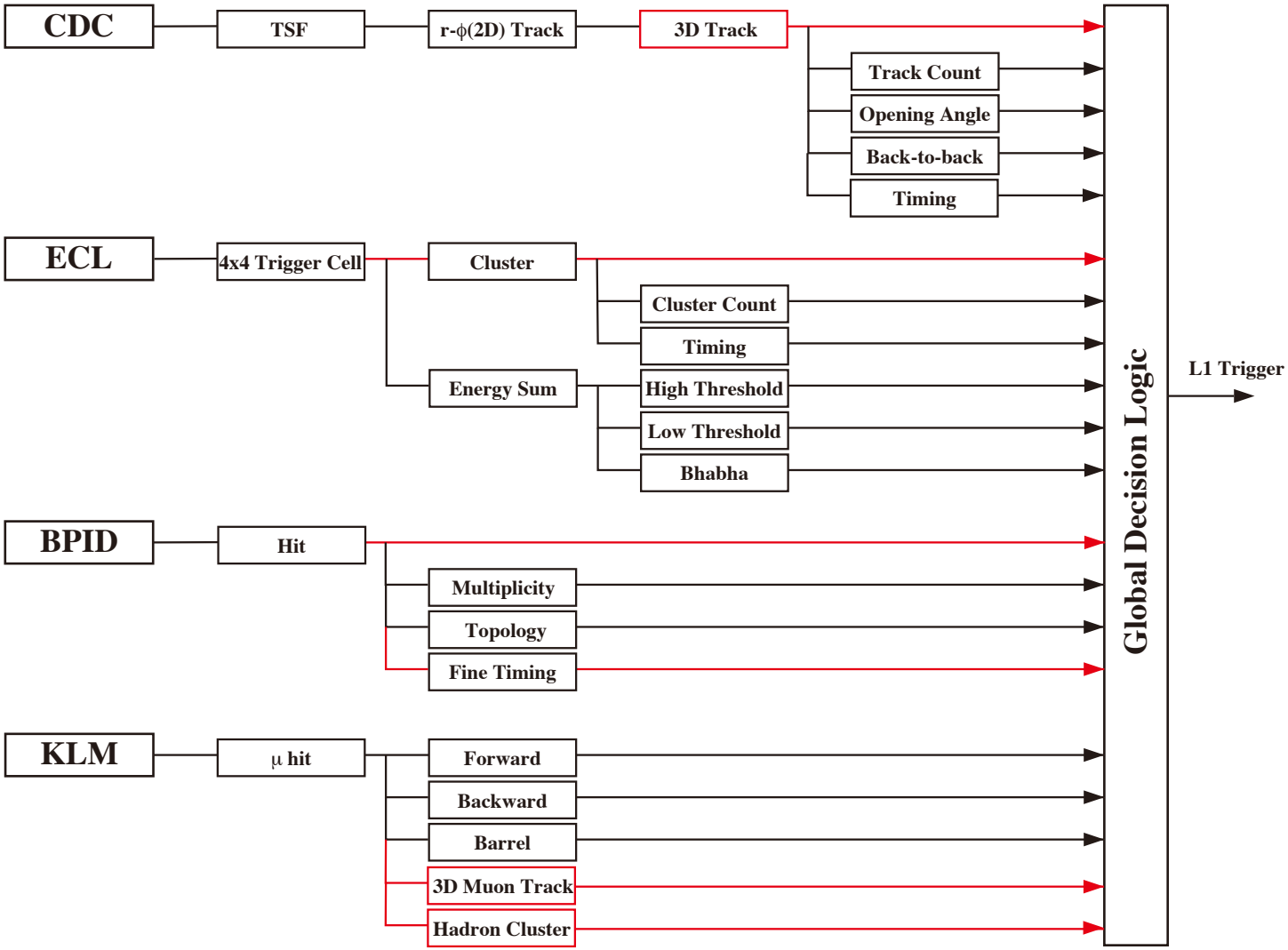
Based on Belle History

| Lum ($cm^{-2}s^{-1}$) | Lum. Comp. | N/S=~0.5 | | N/S=~6 | |
|---|---|---|---|---|---|
| | | BG | Total | BG | Total |
| $1x10^{34}$ | 190 Hz | 100 Hz | 290 Hz | 1100 Hz | 1300 Hz |
| $1x10^{35}$ | 1.9 kHz | 1.0 kHz | 2.9 kHz | 11 kHz | 13 kHz |
| $8x10^{35}$ | 7.2 kHz | 8 kHz | 15 kHz | 88 kHz | 95 kHz |

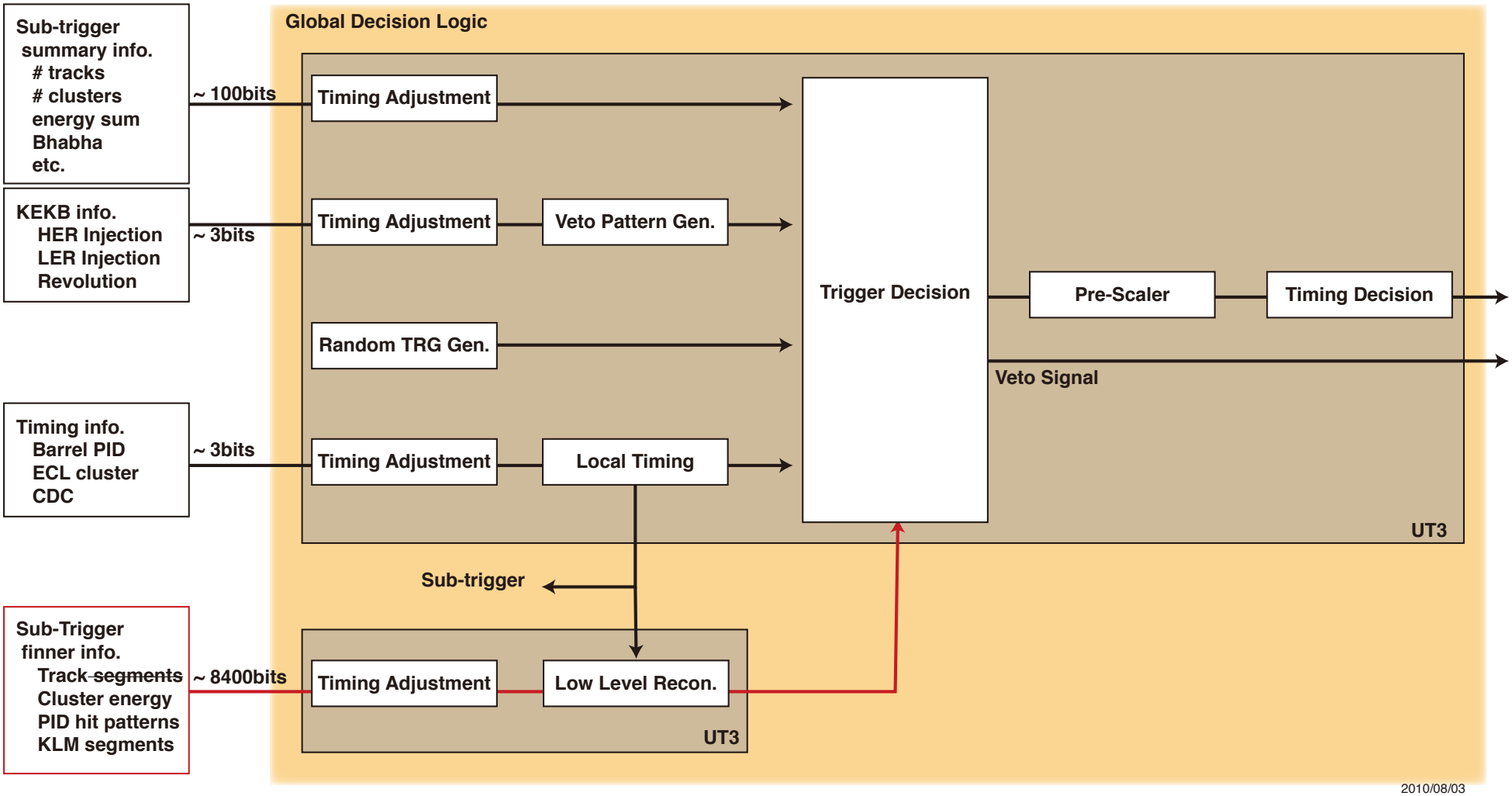
- **No reliable estimation**
  - **for the beam induced background**
  - **We will simulate spent beams when IR in KEKB is fixed**
- **If history repeats,**
  - **Early stage : lower currents with bad vacuum → N/S = ~ 6**
  - **Final stage : high currents with good vacuum → N/S = ~ 0.5**
- **We can tighten the TRG conditions**
  - **New tools : CDC 3D tracking, low level reconstruction for BG reduction**
  - **Suppress two-photon events : these are the signal in Belle**

# Belle2 TRG System

Belle II Trigger System
Version 3.4 : 2011/01/19
Y.Iwasaki



# GDL




2010/08/03
GDLS Schematic
Version 1.07
Y. Iwasaki

# Sub-Trigger Summary Info.

| Sub-Trigger | Type | Bit Width | Clock (MHz) |
|---|---|---|---|
| CDC | # Low Pt Tracks | 3 | 62.5 |
| | # Middle Pt Tracks | 3 | |
| | # High Pt Tracks | 3 | |
| | Charge Sum | 3 | |
| | Back-to-Back | 1 | |
| | Opening Angle | 1 | |
| ECL | E Low | 1 | |
| | E High | 1 | |
| | E Lum | 1 | |
| | # Isolated Clusters | 4 | |
| | Bhabha | 1 | |
| | Cosmic | 1 | |
| | Timing | 5 * | |
| TOP | Timing | 5 * | |
| | # Hits | 3 | |
| KLM | # Muon Hits | 3 | |
| | # Hadron Hits | 1 | |
| | Cosmic | 1 | |
| Total | | 30 | |

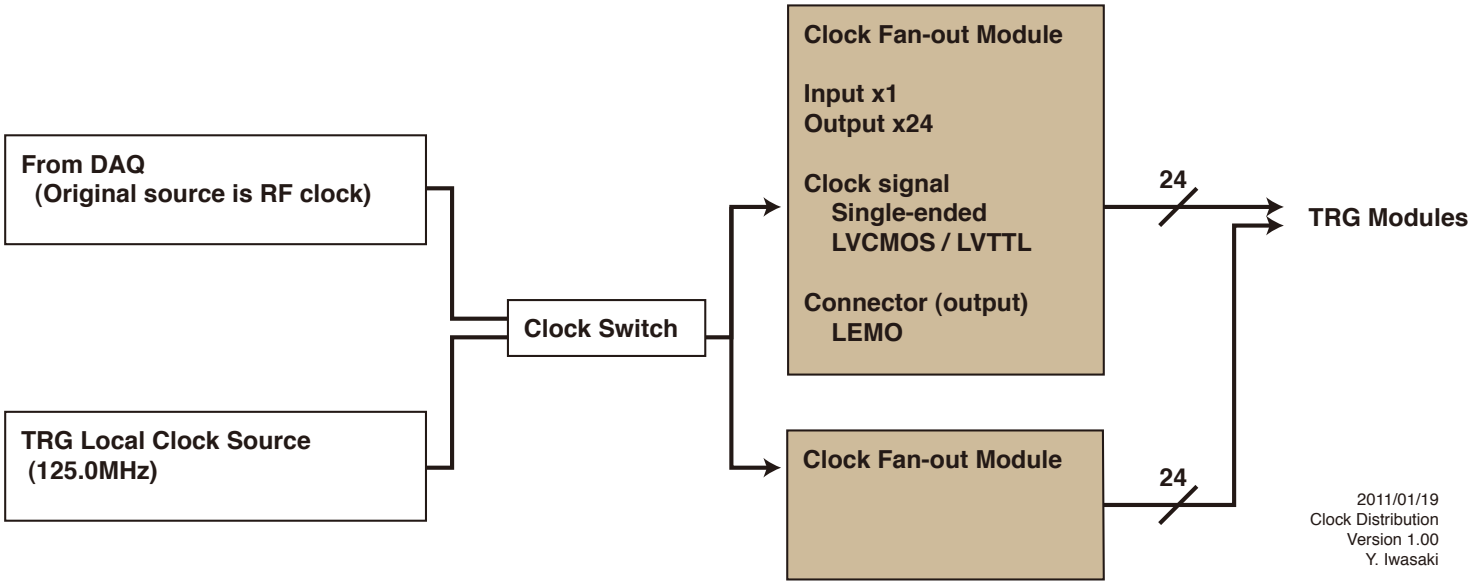
* 1 bit : hit or not, 4 bit : time counts (LSB 1ns)

# Sub-Trigger Finer Info.

| Sub-Trigger | Type | Bit Width | Channels | Clock (MHz) | Flow (Gbps) |
|---|---|---|---|---|---|
| CDC | Low Pt Tracks | 2 * | 64 # | 62.5 | 8 |
| | Middle Pt Tracks | 2 * | 64 | | 8 |
| | High Pt Tracks | 2 * | 64 | | 8 |
| ECL | Trigger Cell | 12 ** | 576 | 16 | 110 |
| Barrel PID | Hit Pattern | 1 | 128 | 62.5 | 8 |
| KLM *** | Track Segments | 1 | ~ 300 | 62.5 | ~ 20 |
| | | | | | ~ 180 (in total) |

- *** : for charge + and charge –**
- **** : energy deposit in a trigger cell**
- ***** : under discussion**
- **# : 1 bit / wedge, 64 wedges**

# Clock for TRG




- **Usage**
  - Trigger system clock
  - Reference clock for the high-speed serial links (RocketIO and HSSIO)
    - Bad clock quality kills entire TRG system
- **Clock sources**
  - DAQ group : 127 MHz (source is RF clock)
    - For normal operation
  - TRG local : 125.0 MHz
    - For development and debugging
- **All sub-trigger masters should use TRG clock**
  - If sub-trigger uses DAQ clock directly, no guarantee to communicate with GDL all the time

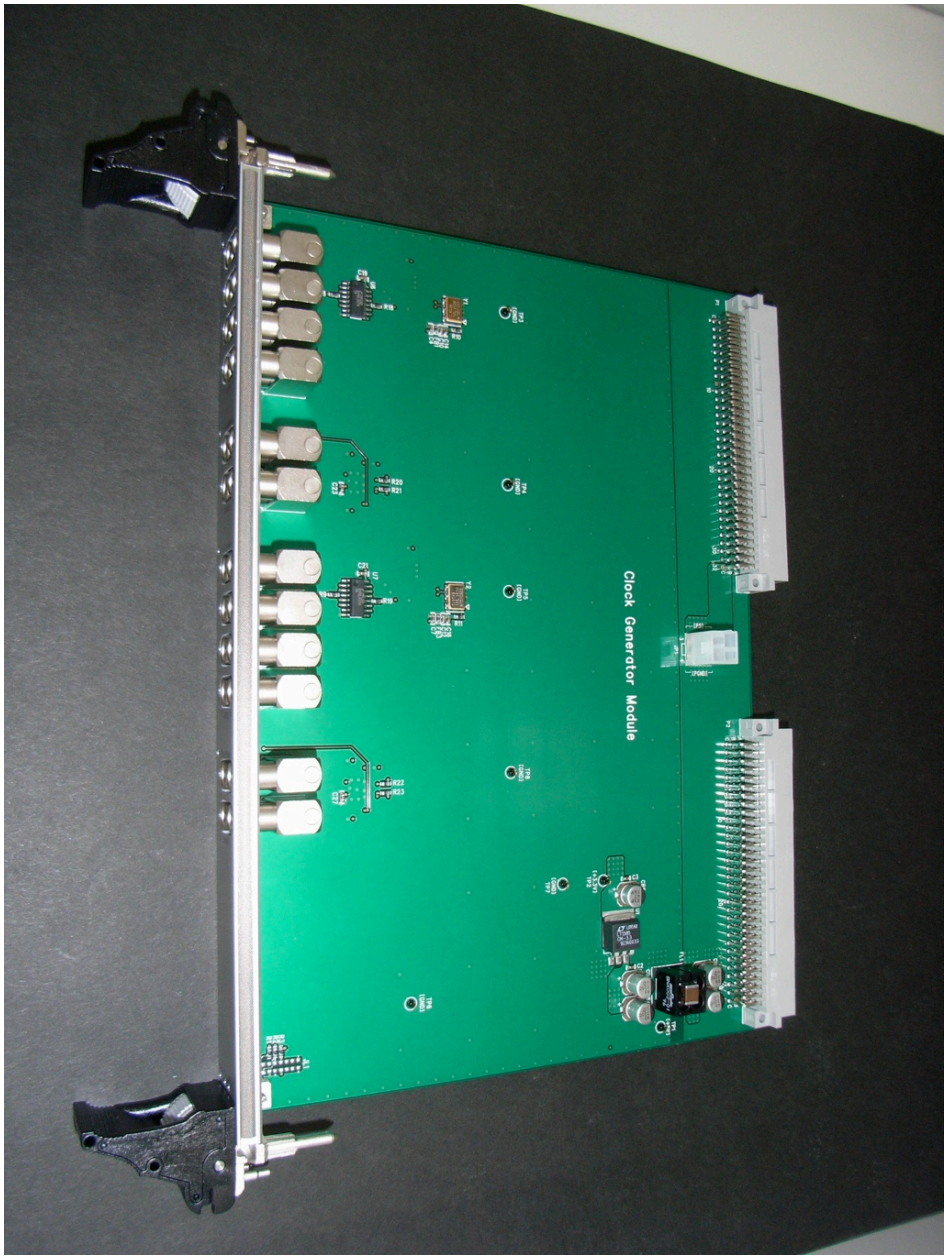
# Clock : To Be Checked / Tested

- **Clock signal from DAQ**
  - **Level ? : we prefer LVCMOS or LVTTL (single-ended)**
  - **Connector type : we prefer LEMO with NIM cable**
- **# receivers of TRG clock**
  - **At least one in each sub-trigger**
  - **How do you receive TRG clock?**
  - **Do you need the clock distributors(fan-out module)?**
- **TRG clock with serial links**
  - **We have to test TRG clock distribution with two clock sources**
    - **RocketIO(GTP, GTX, GTH), HSSIO**
    - **Cable length (up to 5m?)**

| Sub-TRG | #TRG clock |
|---|---|
| GDL | 2 |
| CDC | 19 |
| ECL | 1 ? |
| TOP | 1 ? |
| KLM | 1 ? |

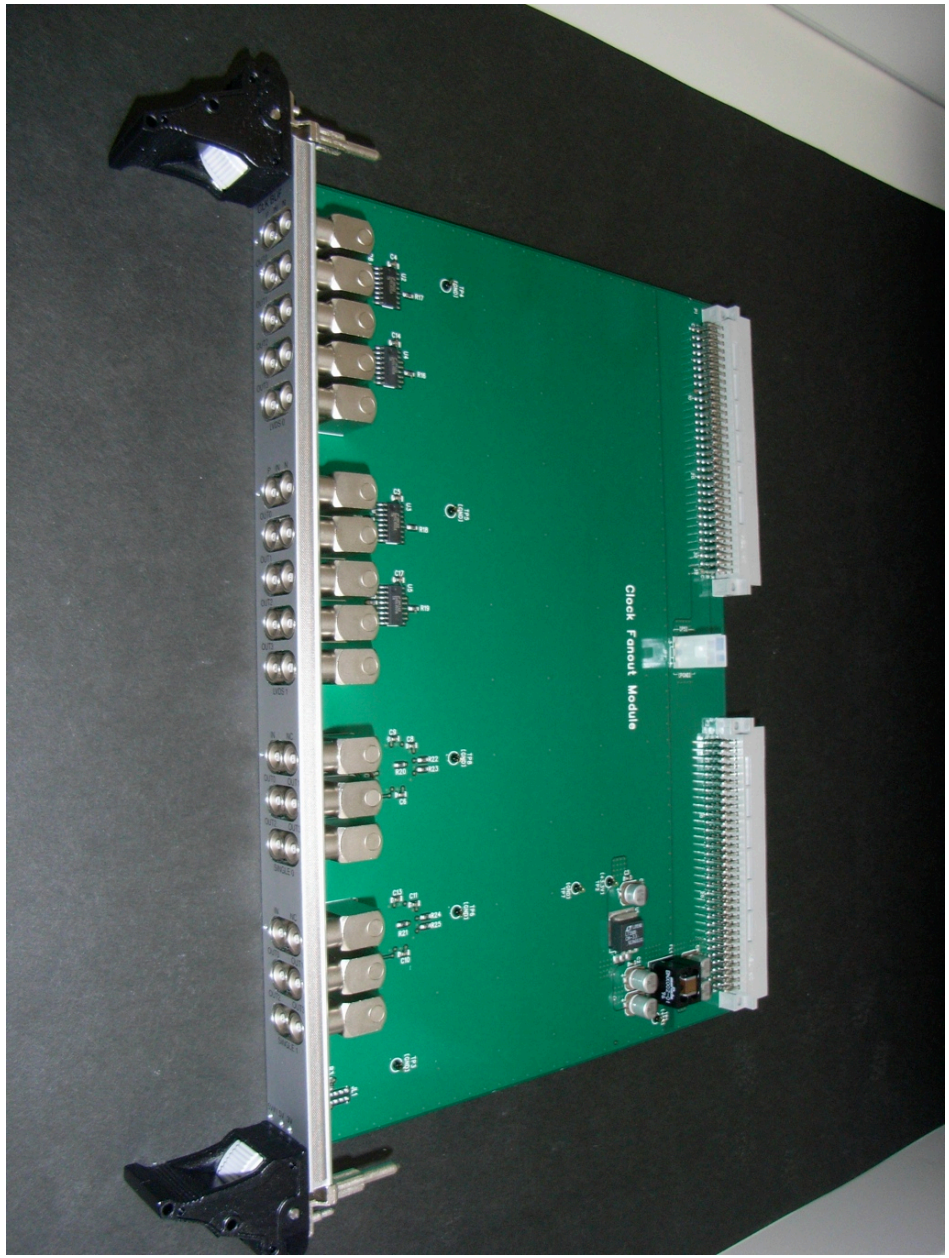
| | GTP (3.2 Gbps) | GTX (6.4 Gbps) | GTH (11 Gbps) |
|---|---|---|---|
| TRG local clock | ok | ok | not yet |
| DAQ clock | not yet | not yet | not yet |

# TRG Local Clock Generator Proto-type




- 6U VME w/o J0
- Clocks
  - 125 MHz x 4
  - 152 MHz x 4
  - Each has differential and single-ended output
- Production type
  - 125 MHz only
  - Single-ended output only
  - # output : 32ch

# Clock Distributor Proto-type



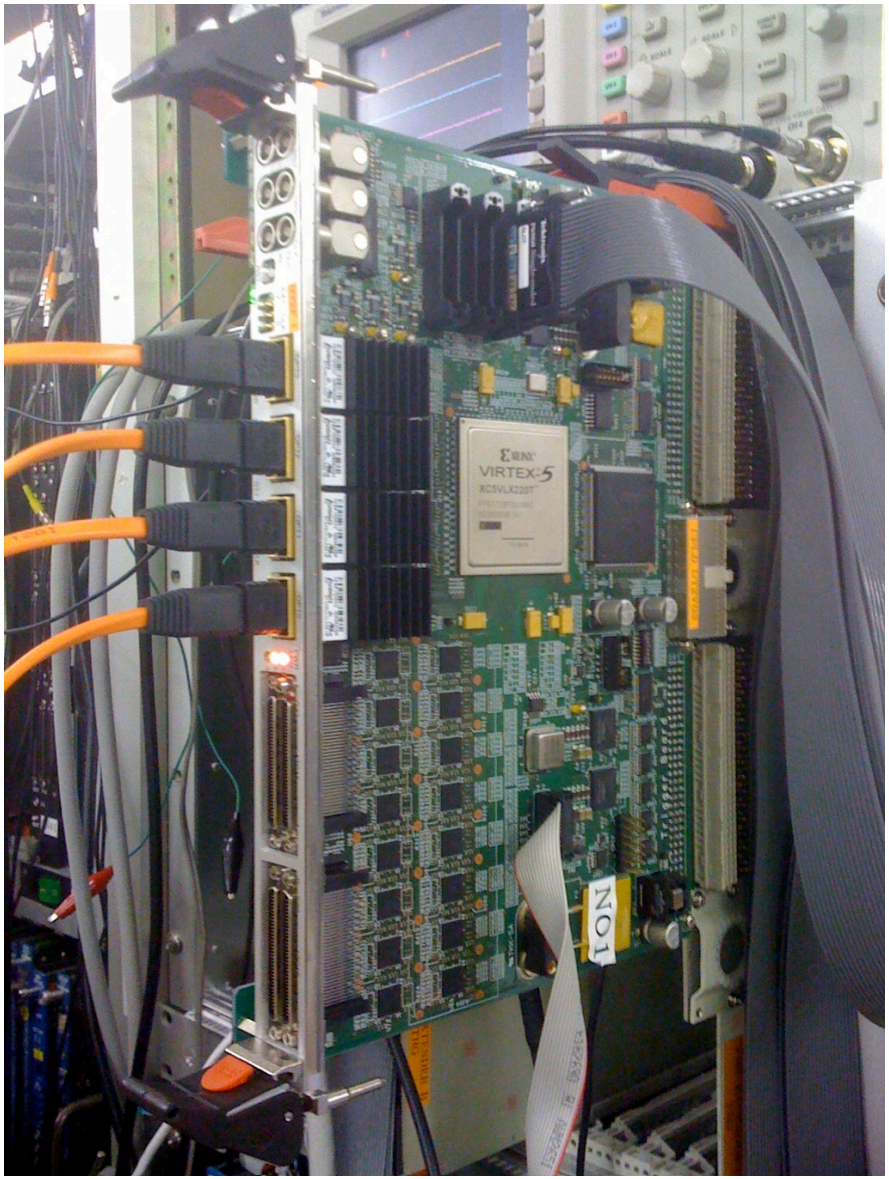

- 6U VME w/o J0
- 2 differential input
  - 8 differential fanout
- 2 single-ended input
  - 8 single-ended fanout

- Production version
  - Single-ended only
  - 1 input
  - 32 ch fanout

# TRG Read-Out

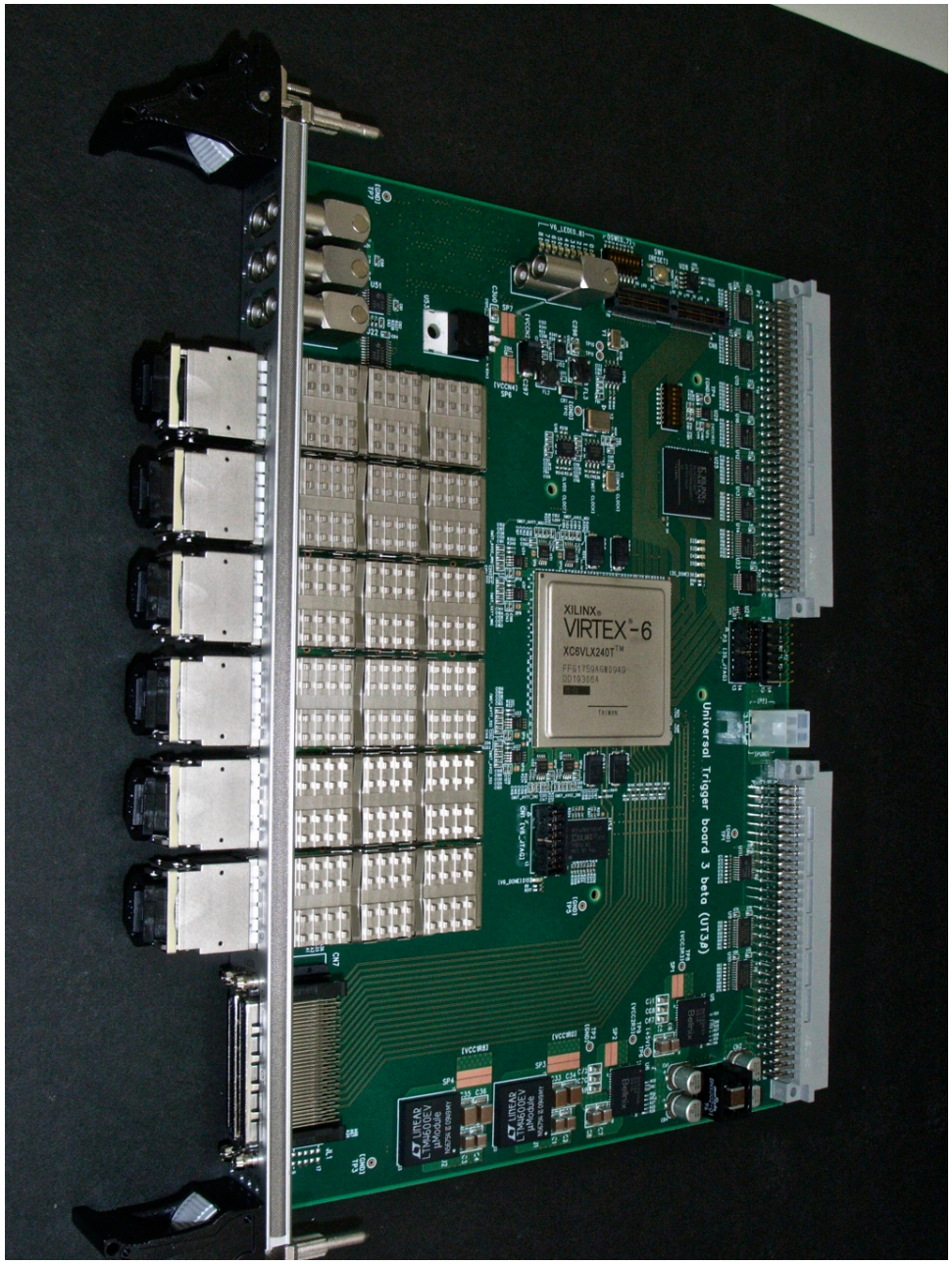
- **Data to be read (from GDL)**
  - **Edge timing of input and output**
    - **Summary info. from sub-triggers : $N_{TDC}$ ～100**
    - **Summary info. of GDL : $N_{TDC}$ ～200**
    - **Total TDC : ～ 300 channel**
- **TDC data**
  - **Clock : 125MHz (= GDL system clock)**
  - **16 bits for one edge**
    - **15 bits for time counter, 1 bit for edge type**
  - **Time window : ～33 usec**
- **Data size**
  - **16 bits x 300 TDC x 4 edges = 2.5 kB / event**
- **For debug, we like to read all sub-trigger finer info.**
  - **Not for normal runs**
  - **O(1000)**
  - **Is it possible?**
    - **Do we need special lines?**

# Universal Trigger board 2 (UT2)




- 6U VME board
- FPGA is Virtex5(XC5VLX220T)
- Optical RocketIO
  - 3Gbps x 16 I/O pairs
    ... 5000 channels in 16MHz
    ... 2000 channels in 40MHz
- Differential I/O x 64 pairs
- NIM x 3 I/O pairs
- Delivered in 2009 March
  - Three boards were fabricated
  - There were many minor troubles but fixed almost
  - RocketIO BERT ... $10^{-12}$ level

# UT3β

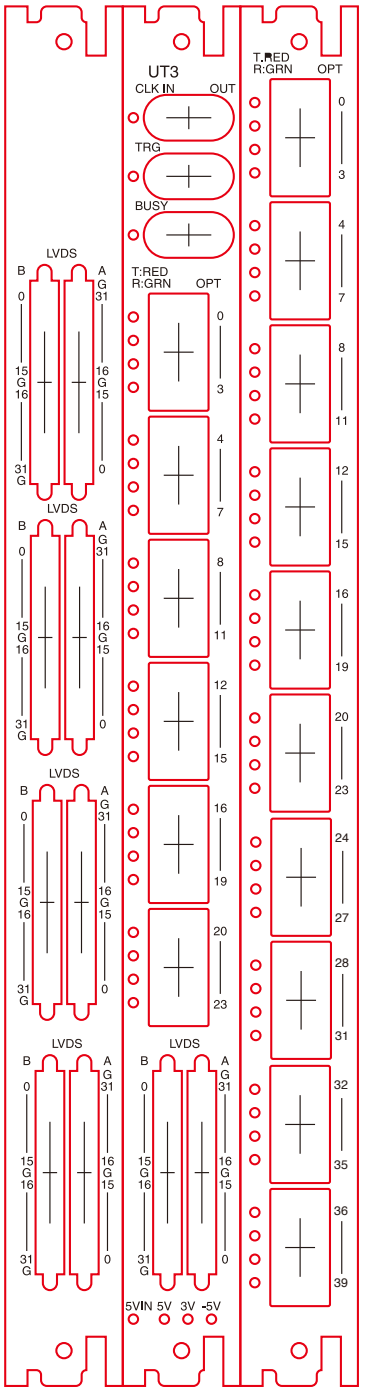



- Universal Trigger Board 3 beta
  - 6U VME module w/o J0
  - +5V only
- Xilinx Virtex-6 LX240T
- 24 GTX
  - 150 (6.25 x 24) Gbps IO
  - 6 optical connectors
    - 1 opt. connector has 4 opt. links
- Clock IO
  - Internal and external for GTX
- NIM IO
  - 2 in, 2 out
- LVDS IO
  - 32 x 2 in/out
- 3 boards fabricated
  - 2 boards delivered

# UT3γ

- **Final proto-type of the Universal Trigger board**
- **FPGA : Virtex-6 HXT (FF1923 package)**
  - **3 FPGA choices**
- **IO**
  - **Clock : 1 in, 1 out**
  - **NIM : 2 in, 2 out**
  - **LVDS : 64(32x2) in/out,**
    **256(32x8) in/out optional daughter board**
  - **RocketIO**
    - **24 GTH (268 Gbps)**
    - **40 GTX (264 Gbps) on the optional daughter board**
- **Waiting for V6HX delivery (early 2011)**

| Board | UT3β | UT3γ | | |
|---|---|---|---|---|
| FPGA | V6LX240T | V6HX255T | V6HX380T | V6HX566T |
| Logic Cells | 241,152 | 253,440 | 382,464 | 566,784 |
| GTX (max 6.6 Gbps) | 24 | 24 | 40 | 40 |
| GTH (max 11.18 Gbps) | 0 | 24 | 24 | 24 |



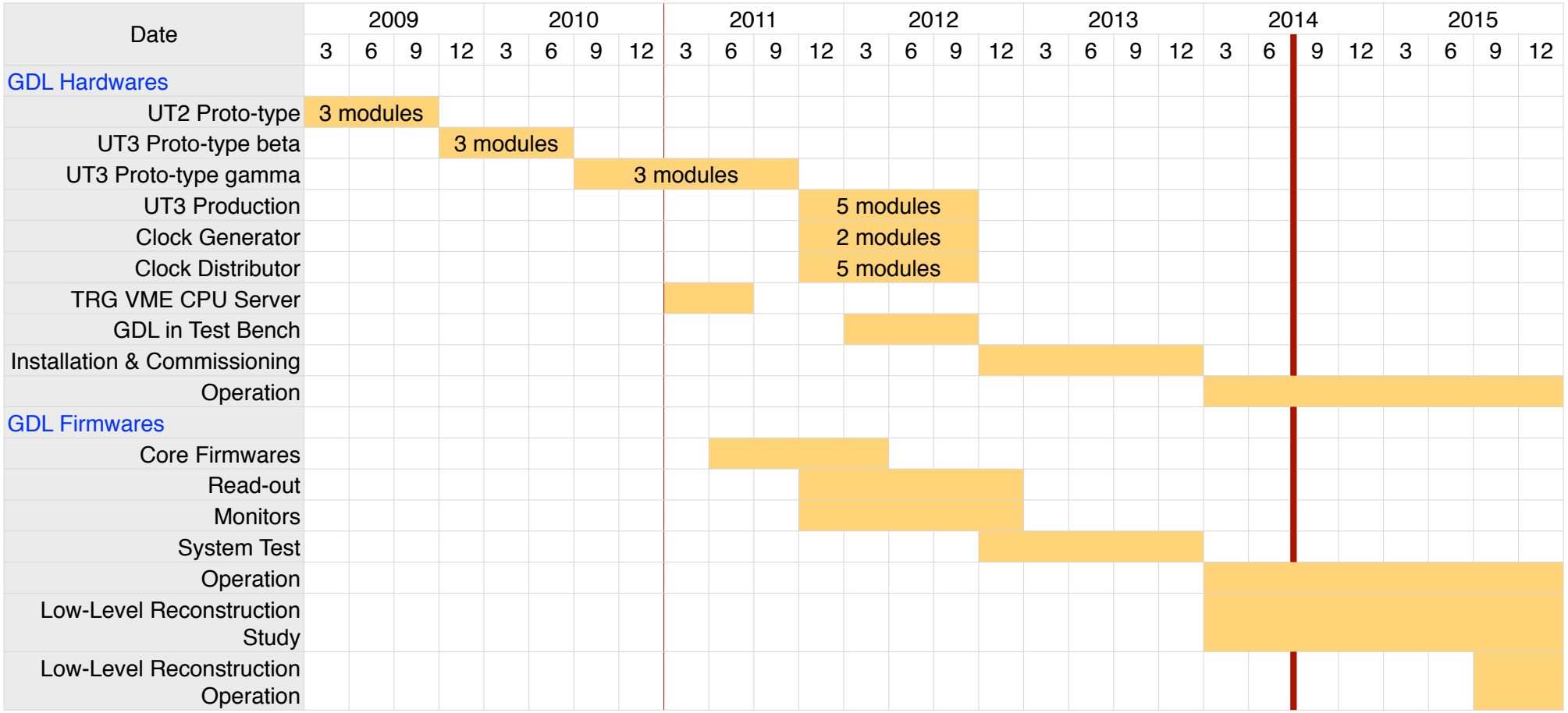
E. Won
Korea U.

# VME CPU

- **VME CPUs are necessary to control trigger modules**
  - **Disk-less CPU with network boot or USB based one?**
  - **One CPU / crate, O(10) CPU are necessary**
- **Server for VME CPU**
  - **Main server and back-up server**
  - **What has to be done when the main server dies?**
    - **Detailed procedure should be defined and practiced**
- **Requirements**
  - **Cheap, no fast CPU, stable, Intel CPU**
  - **Network booting from a server PC**
- **KU is responsible**
  - **We will experiment with exiting VME boards from GE (KU had some experience with it)**
  - **We will (eventually) setup a prototype system by summer of 2011 (one server +a couple of VME cpus) but try on Feb 2011 when EW visits KEK**
  - **If server can be near to VME cpus and not scattered too much: we can think of cpu-less usb based VME master (KU has one module)**
  - **For our study we plan to use Scientific Linux: let us know if you have other recommendations**

To GV: it may be too late to move to cPCI due to UT3 design

# Schedule

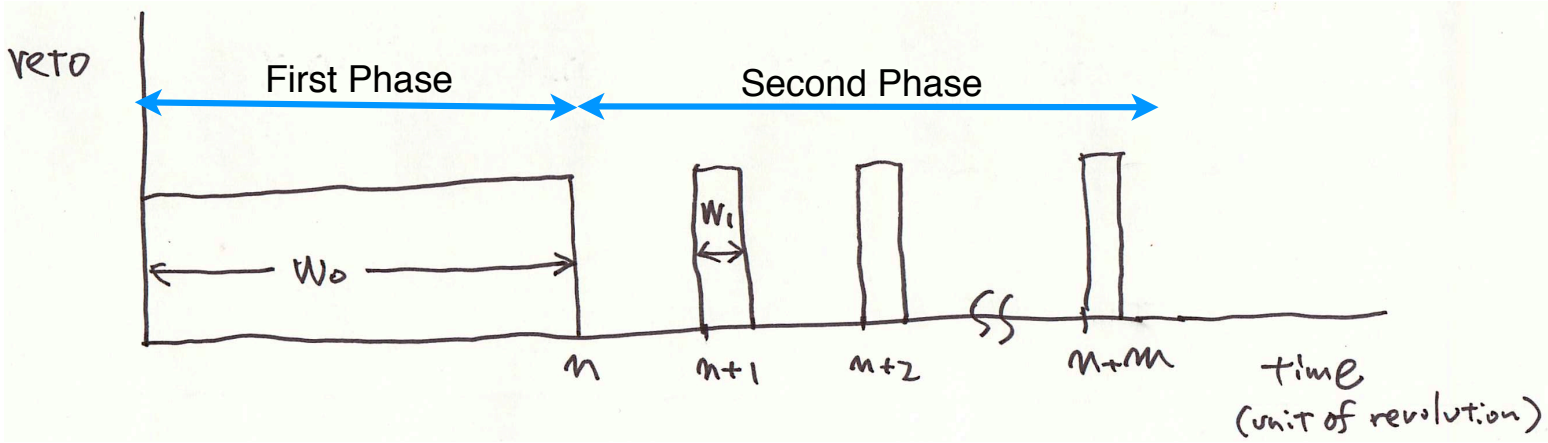

Date
2009
2010
2011
2012
2013
2014
2015
3 6 9 12 3 6 9 12 3 6 9 12 3 6 9 12 3 6 9 12 3 6 9 12 3 6 9 12
GDL Hardwares
UT2 Proto-type
3 modules
UT3 Proto-type beta
3 modules
UT3 Proto-type gamma
3 modules
UT3 Production
5 modules
Clock Generator
2 modules
Clock Distributor
5 modules
TRG VME CPU Server
GDL in Test Bench
Installation & Commissioning
Operation
GDL Firmwares
Core Firmwares
Read-out
Monitors
System Test
Operation
Low-Level Reconstruction Study
Low-Level Reconstruction Operation

# Summary

- **TRG in Belle2 is similar to that in Belle**
  - **All components will be replaced with recent technologies**
    - **FPGA with high-speed serial links is our core technology**
    - **Amount of data flow is O(100) larger than that in Belle**
  - **Hardware development is on schedule**
    - **Production will be started in next fiscal year for some modules**
- **For background reduction, we will try to reconstruct events with CDC and ECL**
  - **CDC TRG will give 3D track parameters**
  - **CDC track will be matched to ECL clusters**
  - **How powerful to reduce BG ?**

# Appendix

# Injection Veto




- **Two phases**
  - **First phase : veto n turns completely**
    **W0 = n * 10 usec**
    **n = 10～100**
  - **Second phase : veto periodically**
    **W1 = ～1 usec**
    **m ～ 300**
  - **Three parameters (n, m, W1) : SKEKB dependence**
- **Veto pattern is generated in GDL**
- **The first phase only in Belle case (n=350)**
- **Veto signal is sent to SEQ to calculate dead-time**