ECL trigger status

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On behalf of **B.G. Cheon (Hanyang U) and Y.Unno**

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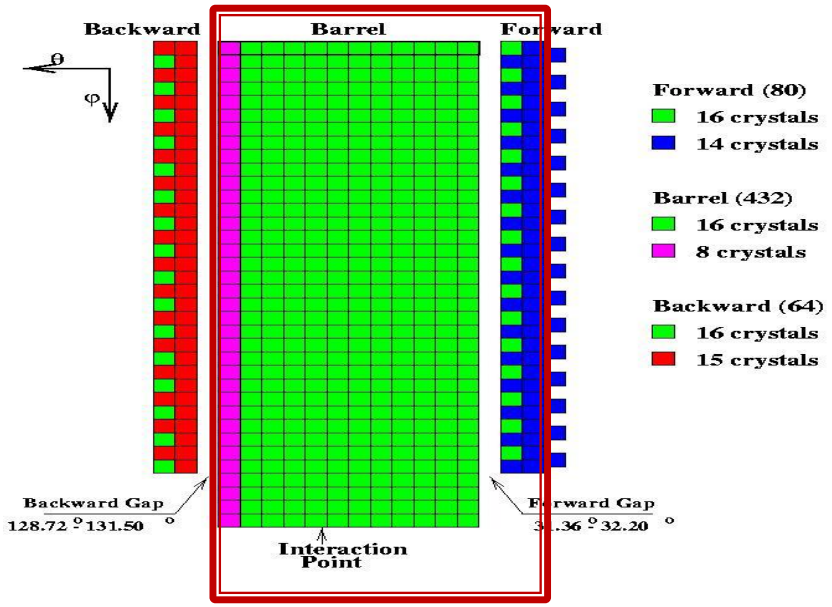
TRG/DAQ workshop

Belle II ECL Trigger

- **Requirement**
  - Suppression of beam-background events
  - Separation of hadronic and Bhabha events
  - Trigger latency $< 5\ \mu s$
  - Timing resolution $< 20ns\ (1\sigma)$ @ Belle
- **Basic element: Trigger Cell (4x4 counters sum)**
- **Main hadronic event triggers**
  - Energy trigger : $E_{TOT} > 1GeV$ & Bhabha-veto
  - Cluster trigger : ICN > 3 & Bhabha-veto
  - Redundancy with Energy and Cluster methods

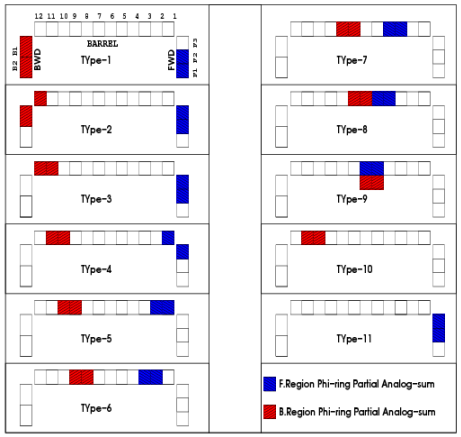
Belle II ECL Trigger (Cont'd)

- **In case of high trigger rate due to harsh Beam-BG ;**
  - Increase TC threshold (100MeV →)
  - Increase Total Energy threshold (1GeV →)
  - Increase ICN clusters (3 →)
  - Reduce physics trigger region
  - Turn on cosmic veto trigger
    - Since Rate(cosmic)
      << Rate(Beam BG)

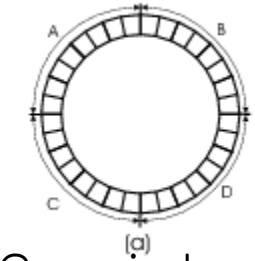


Physics trigger region

ECL Trigger output to GDL



Bhabha based on θ

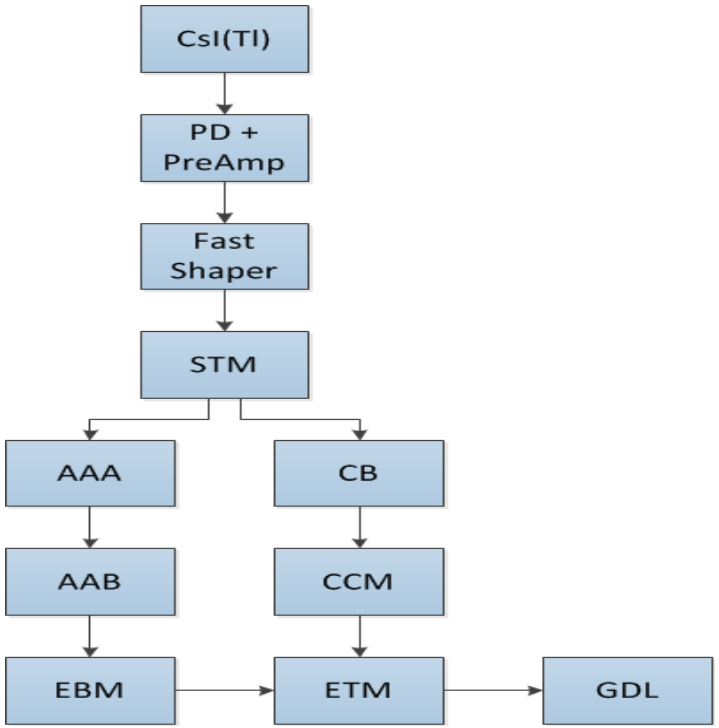


Cosmic based on φ

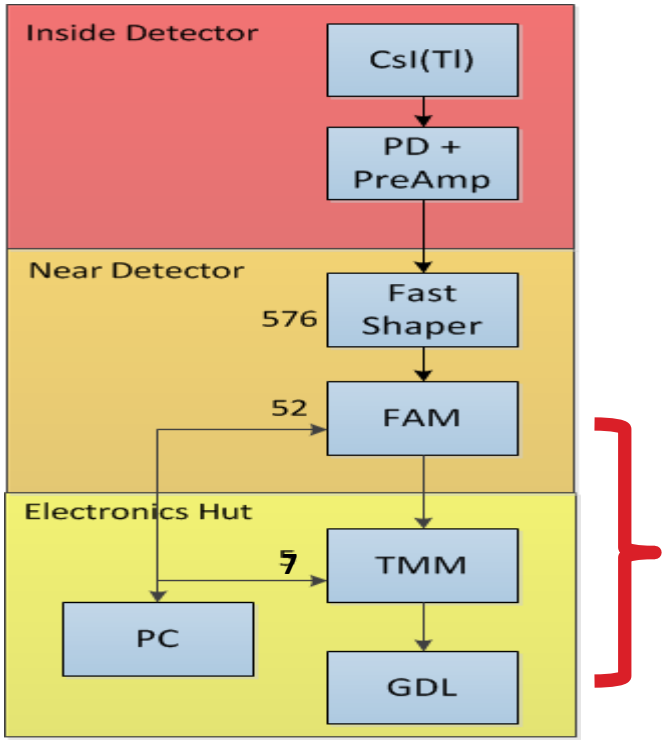
Item	Number of bits	
Trigger timing (Final, Fwd, Barrel, Bwd)	4	←1 @Belle
Total Energy (>0.5, 1.0, 3.0 GeV)	3	
Isolated cluster	4	
Bhabha-type	11	←1 @Belle
OR-ed Bhabha	1	New at Belle2
Barrel Bhabha	1	New at Belle2
Prescale Bhabha	1	
Cosmic veto	1	
TC hit pattern	576	New at Belle2
Total	26+576	

Other trigger bits are supposed to be invented from TSIM study

Hardware configuration

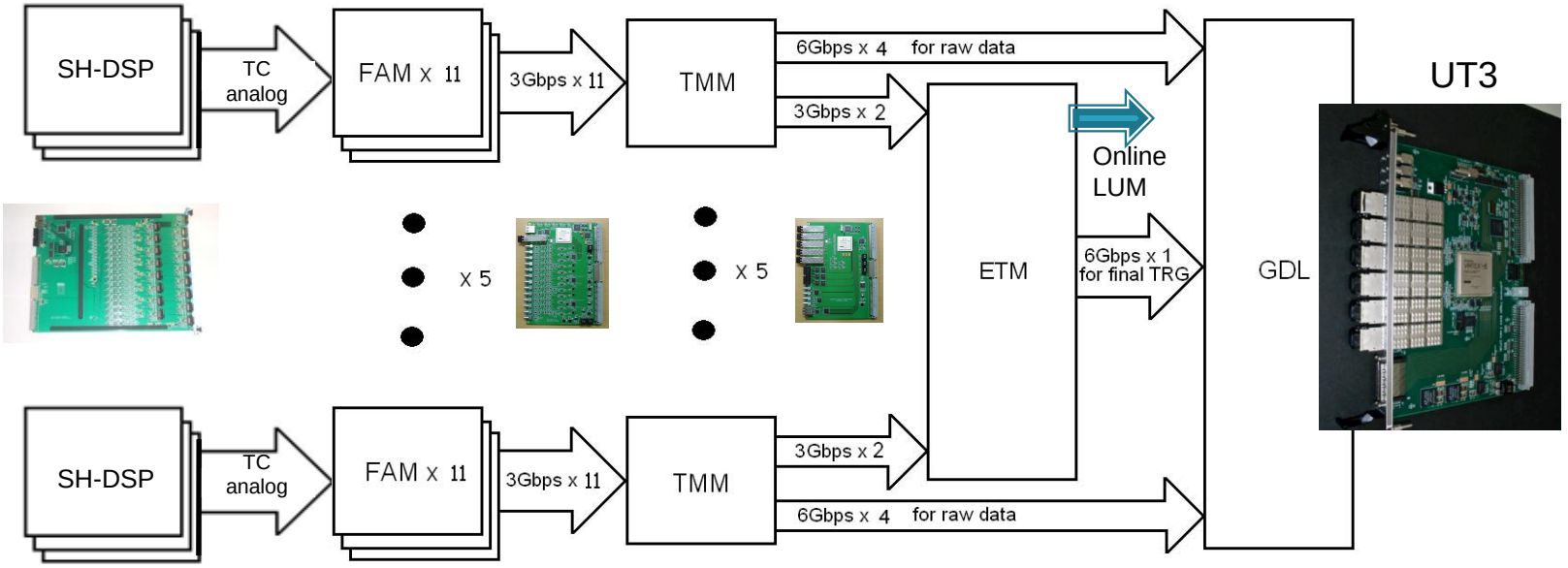


Belle



Belle 2

Hardware configuration



Peaking time of TC	700
ADC pipeline	100
Peak finding process	300~400
Programmable delay	300
Gbit transfer(200bits)	100
Optical cable length	200~300

Bridge delay	200~300
Gbit transfer(~ 1100bits)	400

Input alignment	100
Trigger decision	200~300

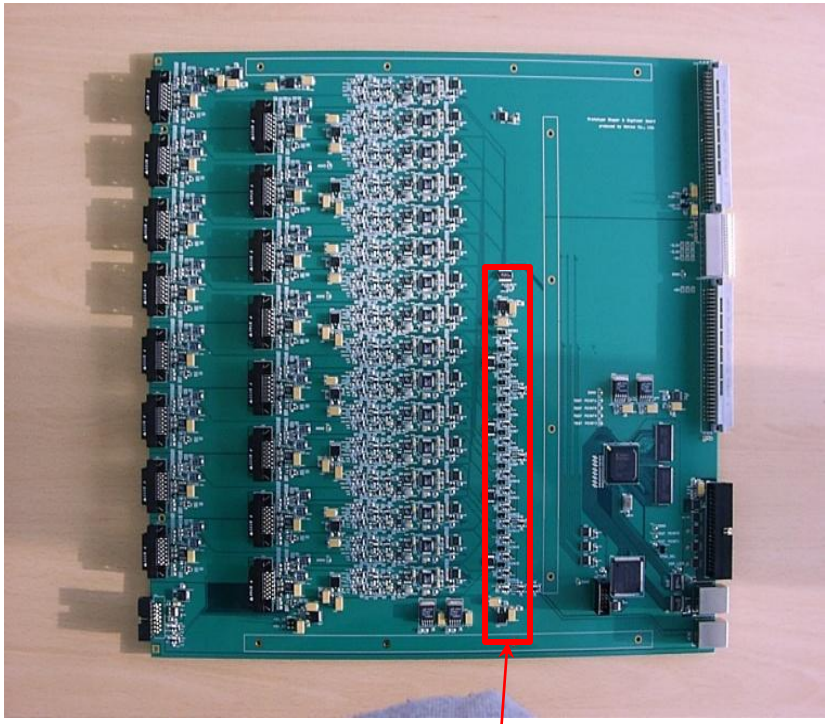
* Total latency = 2600 ~ 3000 ns

** TMM FPGA = XC6VLX130T-1FF1156C

- Flexible trigger configuration is possible by FADC + FPGA architecture.
- For analog LUM monitor, we think about implementing a kind of AAA used in Belle.
- Belle II ECL trigger is easy to accommodate any Endcap option in the future.
  - pulse-height and timing correction @ FAM
  - However, we have to resolve any possible problem from channel number increasing

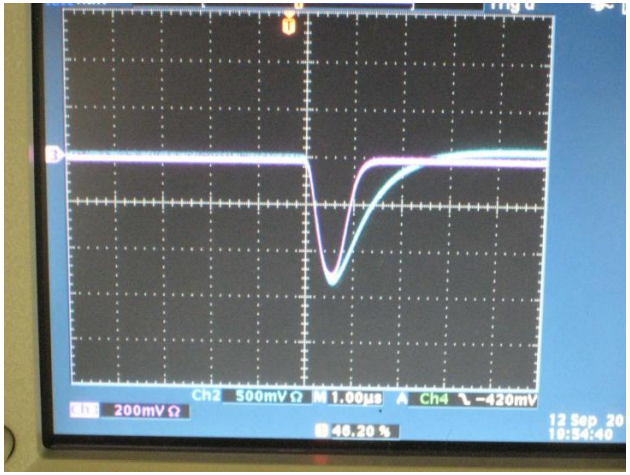
Fast Shaper

New Shaper-DSP Prototype



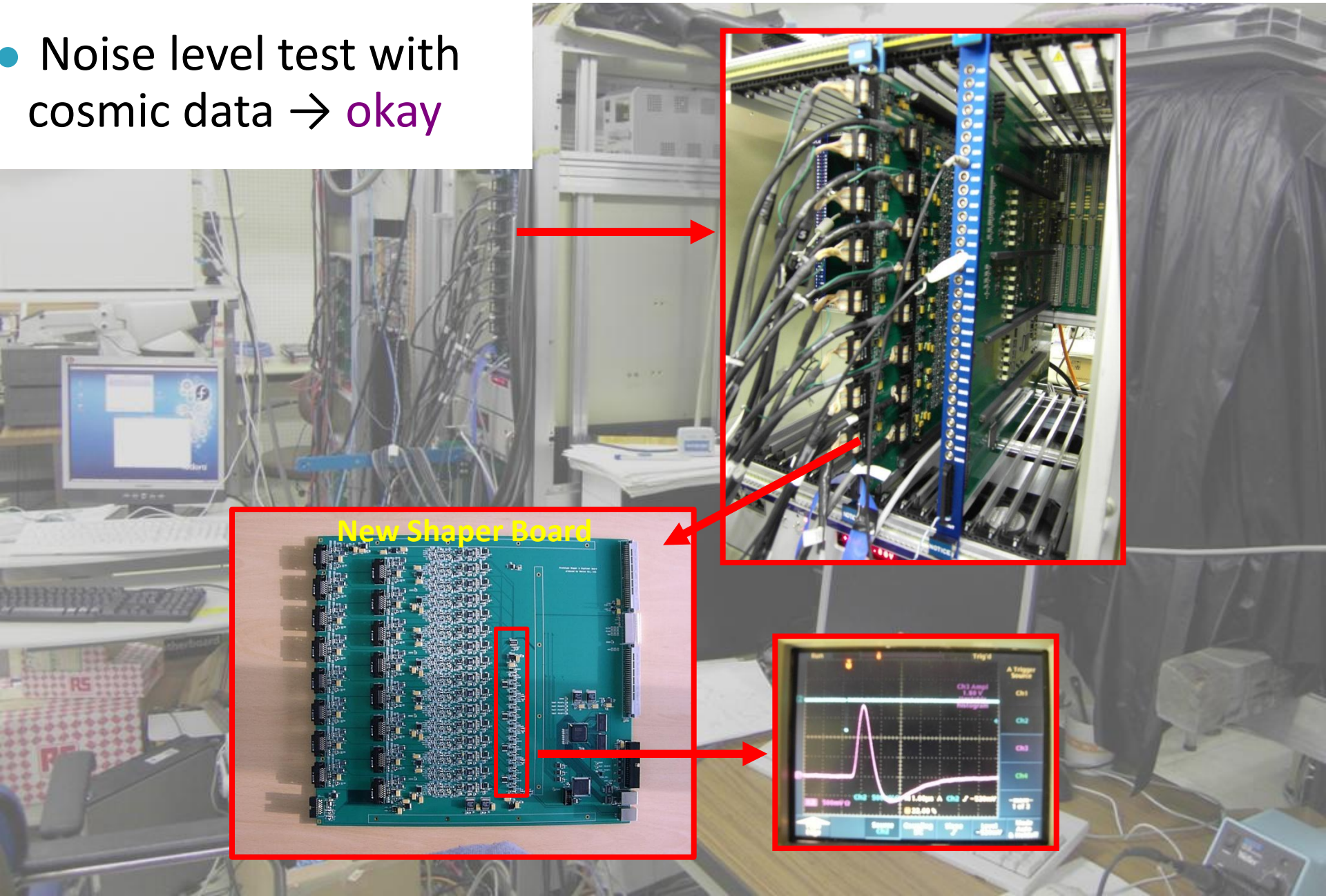
Fast shaper circuits

- Located in Shaper-DSP board
- 576 boards
- Input : 16 counter signals
- Output : 1 TC analog sum
- Fast shaping time = 100ns
- Pulse height correction
- Channel-by-channel calibration



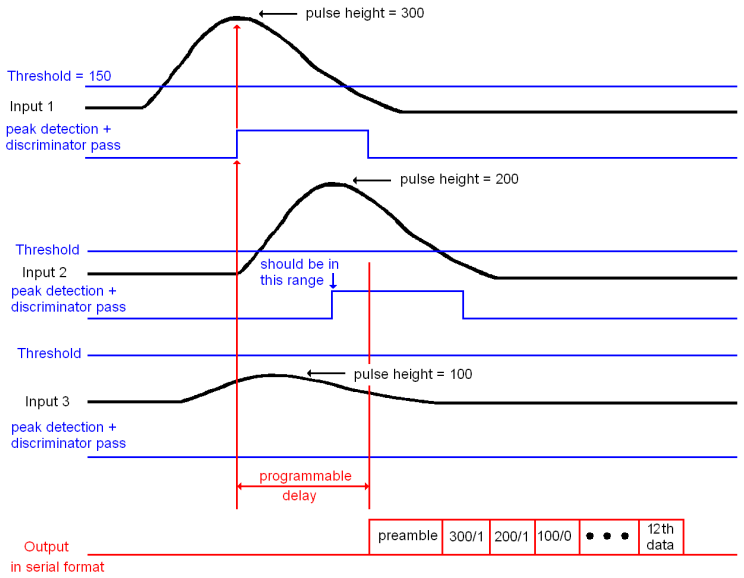
ECL test bench @ Tsukuba-B2

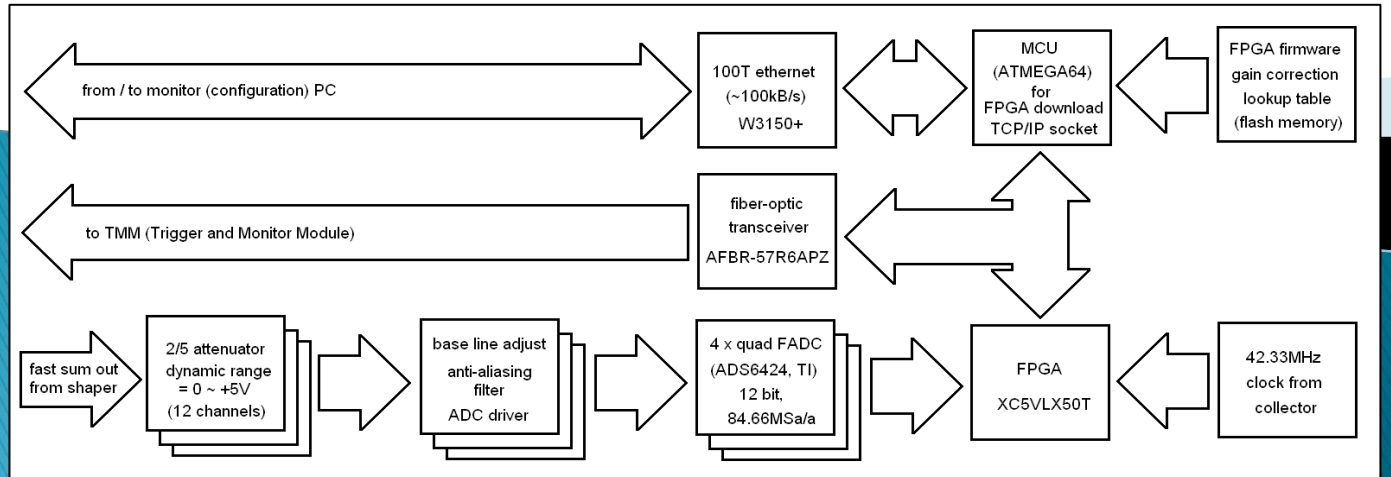
- Noise level test with cosmic data → okay



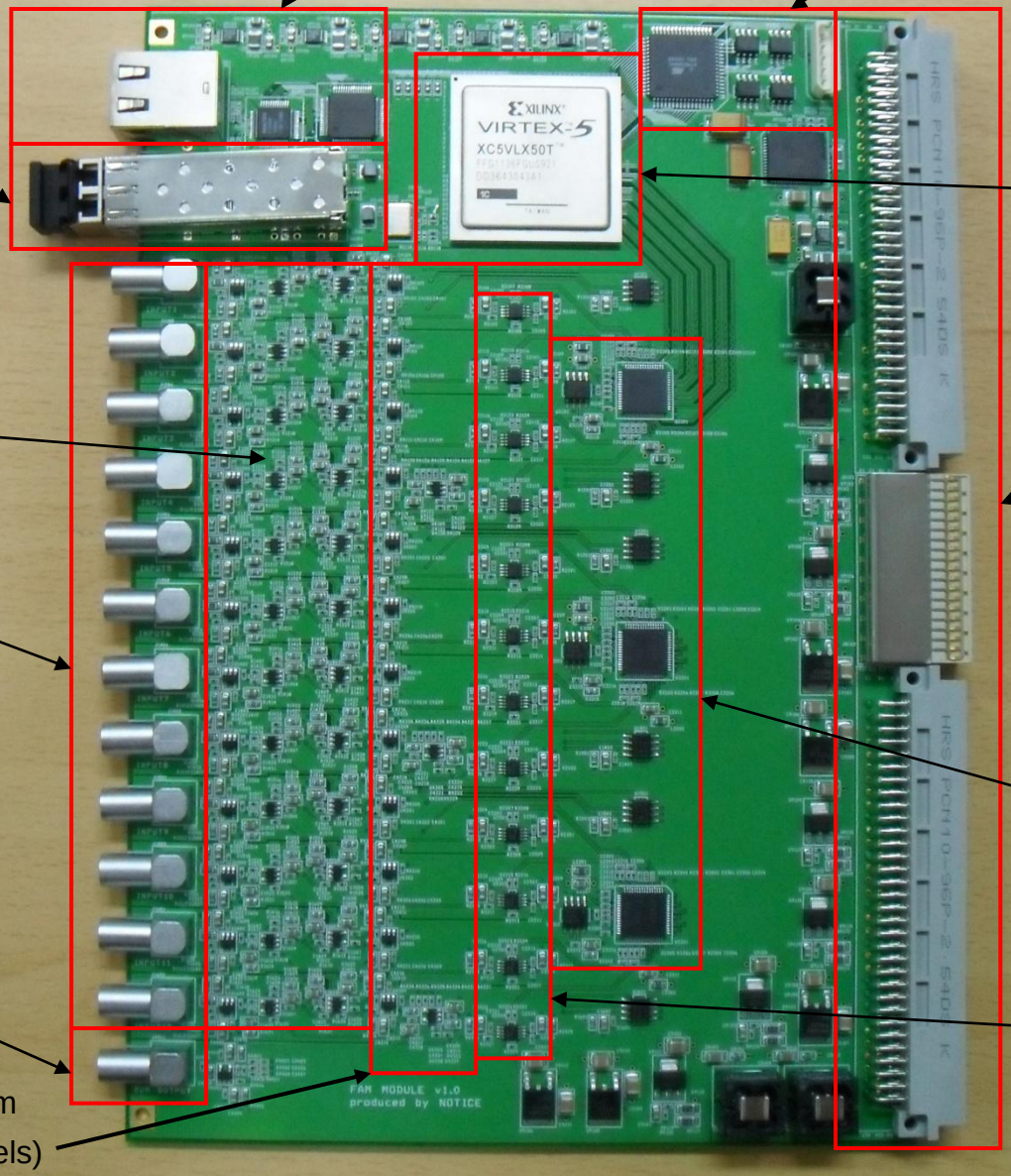
FAM

- 52 boards (one/VME crate)
- Input : 12 x TC analog sum signals
- Output : 1 optical digital signal
  - 12 x TC peaks + discriminator bit
- Operation :
  - Continuous signal digitization @ FADC
  - Find a pulse peak value per each TC @FPGA
  - Compare with threshold (100 MeV) @FPGA
  - Align 12 TC outputs @ FPGA
- Core logic for digitization and peak searching is tested in new-EBM module





FAM



100T TCP/IP
for slow control & monitor

MCU and flash memory
for FPGA downloading
and TCP/IP communication

fiber optic links to TMM
(AFBR-57R6APZ,
up to 4.25Gbps)

FPGA(XC5VLX50T)

12 channel analog
Buffer stage

Power and
FAM clock from
collector module

12 Fast sum input
from shaper module

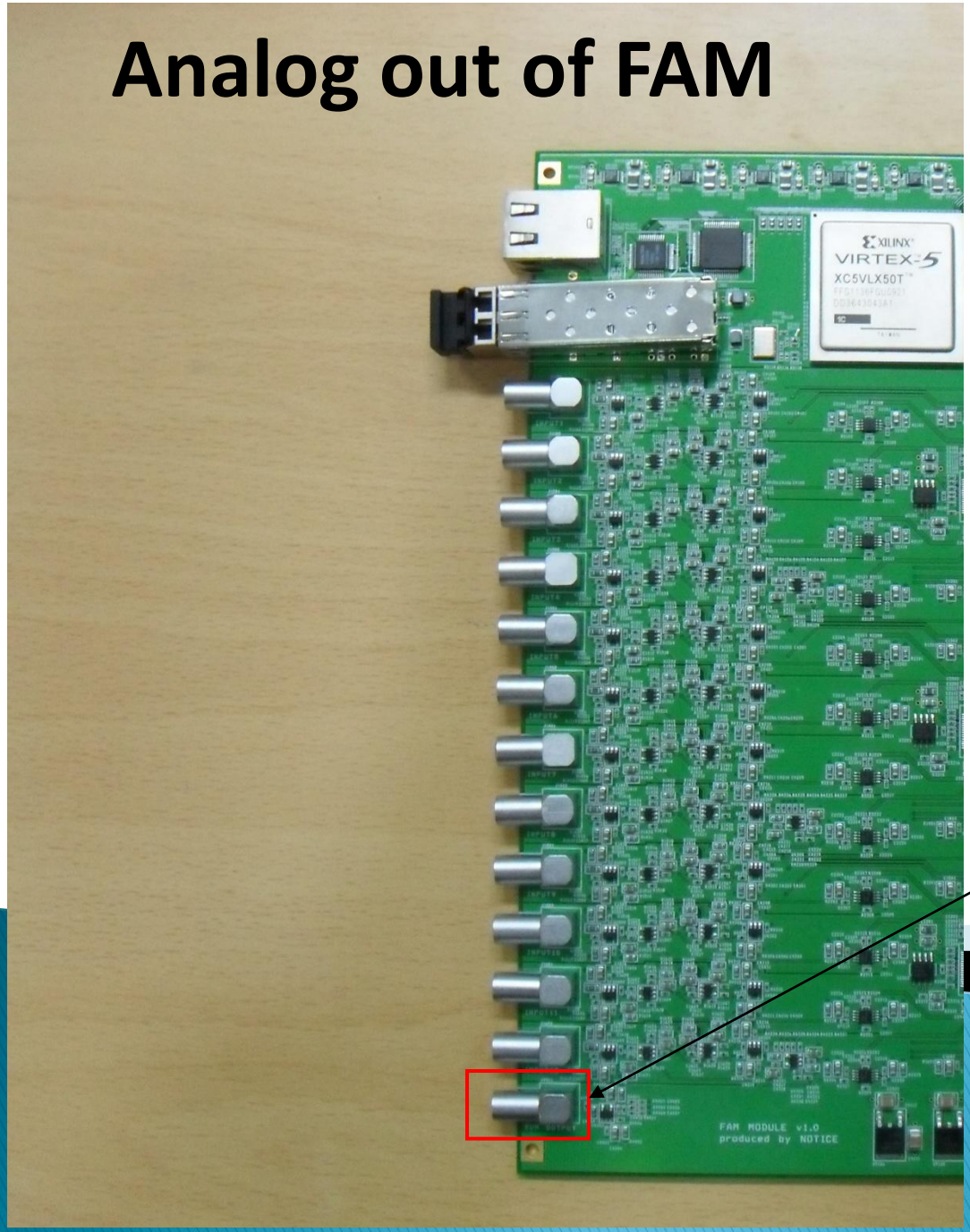
Flash ADC
100MSa/s 12bit
(ADS6424)

Analog sum output
future application

ADC driver
(AD8132)

Analog sum
(12 channels)

Analog out of FAM



Analog sum output

future application

Being studied to use as

Luminosity monitor

independent to DAQ system.

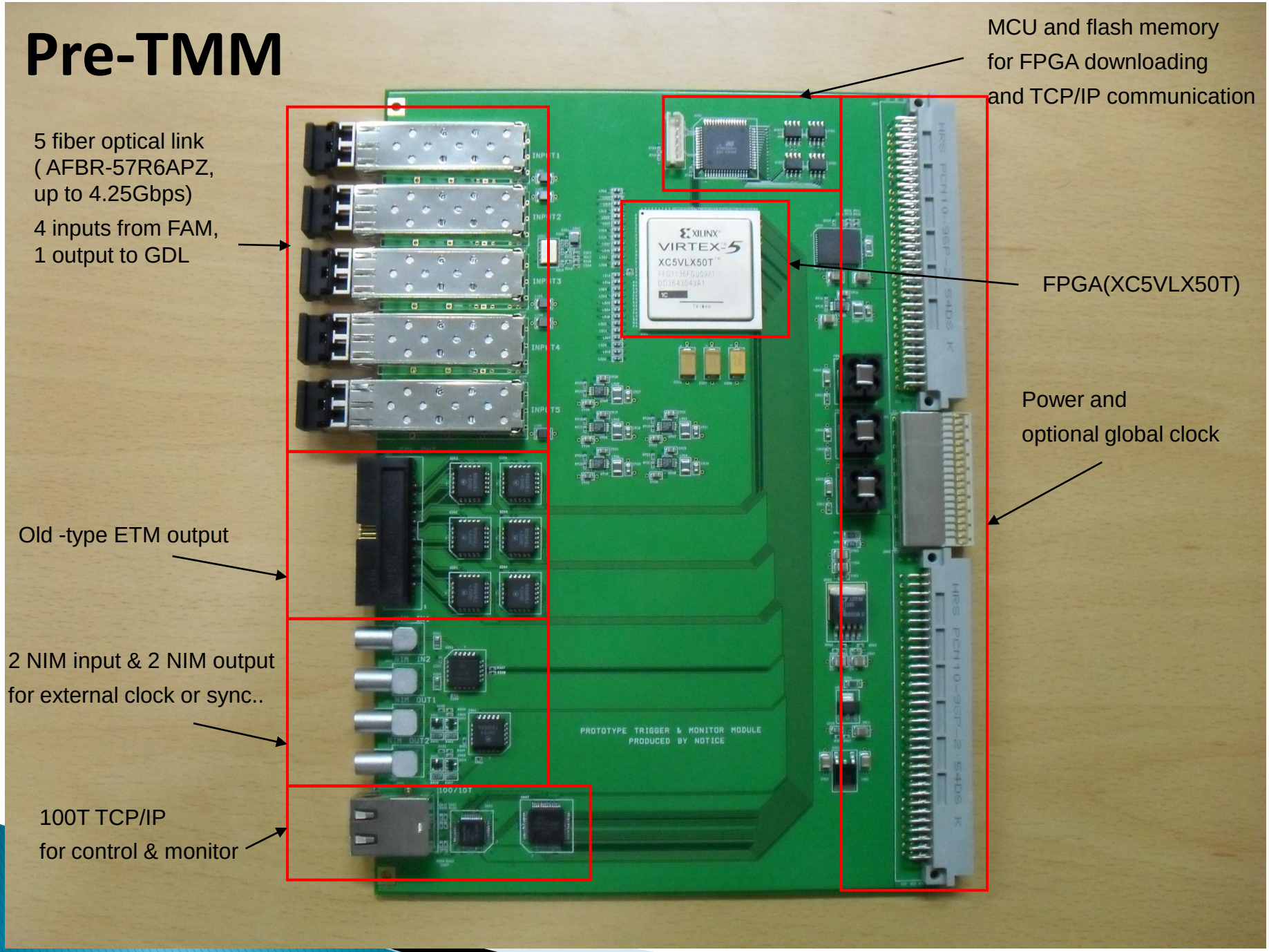
TMM

- 6 (L-1:Merger) + 1(L-2: Master) : same board
- Input : 576 TC signals from 52 FAM modules
- L-1 : 9 inputs from FAM / 2 outputs to L-2 + 4 outputs* to GDL
- L-2 : 2x6 inputs from L-1 / 1 output* to GDL
- Output * : 576 TC raw data to GDL for matching w/ CDC trigger
- Output* : 25 final ECL trigger output to GDL

4	Calorimeter trigger timings (Final, Fwd, Barrel, Bwd)
3	Total Energy (> 0.5, 1.0, 3.0 GeV)
4	Isolated Cluster Number (3 bits + 1 carry-bit)
13	Bhabha triggers / Barrel Bhabha / Prescaled Bhabha
1	Beam-BG veto

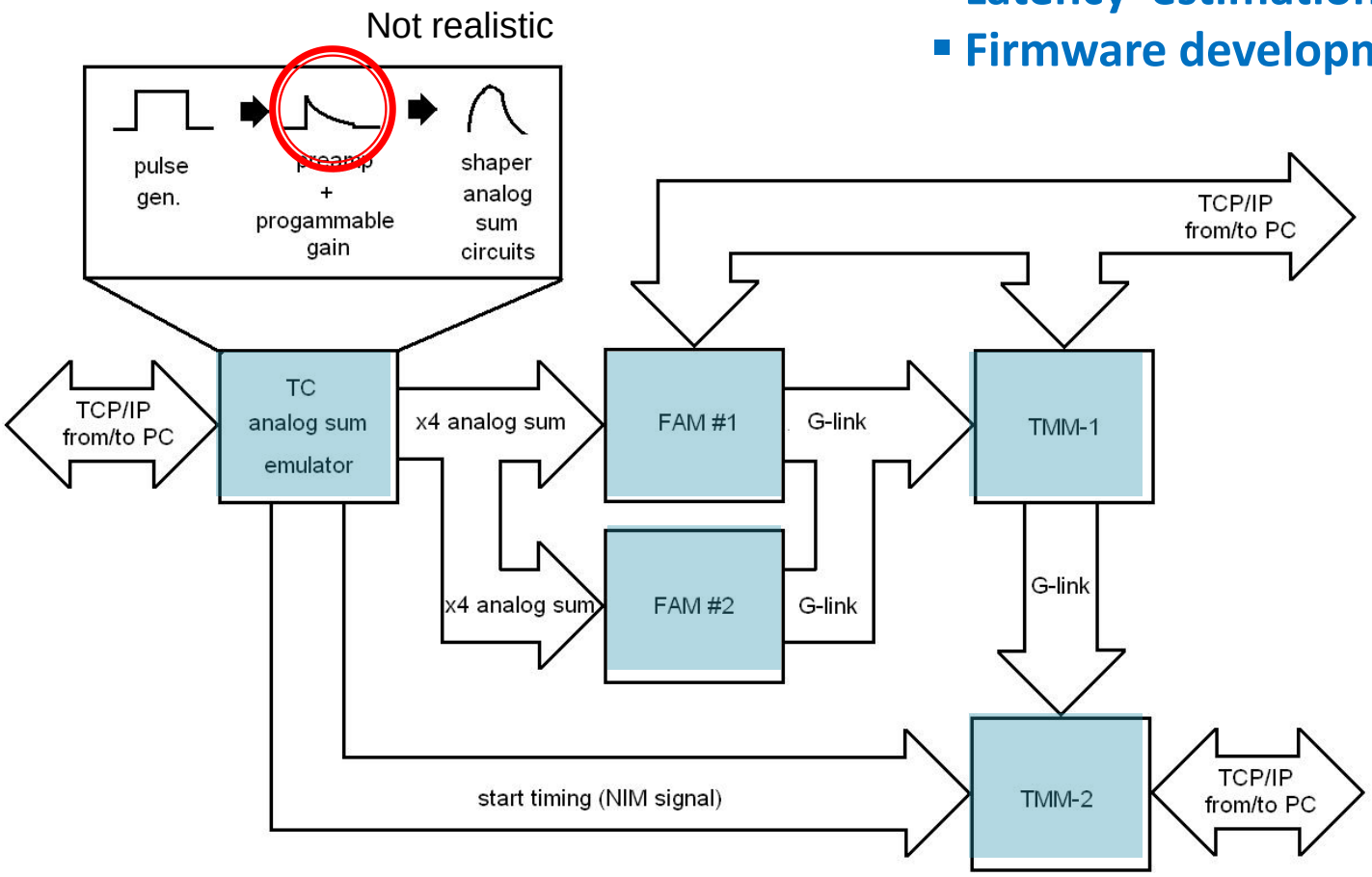
** More useful triggers will be added after TSIM study.

Pre-TMM


MCU and flash memory
for FPGA downloading
and TCP/IP communication
5 fiber optical link
(AFBR-57R6APZ,
up to 4.25Gbps)
4 inputs from FAM,
1 output to GDL
FPGA(XC5VLX50T)
Power and
optional global clock
Old -type ETM output
2 NIM input & 2 NIM output
for external clock or sync..
100T TCP/IP
for control & monitor
XILINX
VIRTEX-5
XC5VLX50T
PROTOTYPE TRIGGER & MONITOR MODULE
PRODUCED BY NOTICE

Toy system for FAM/TMM test

- Latency estimation
- Firmware development



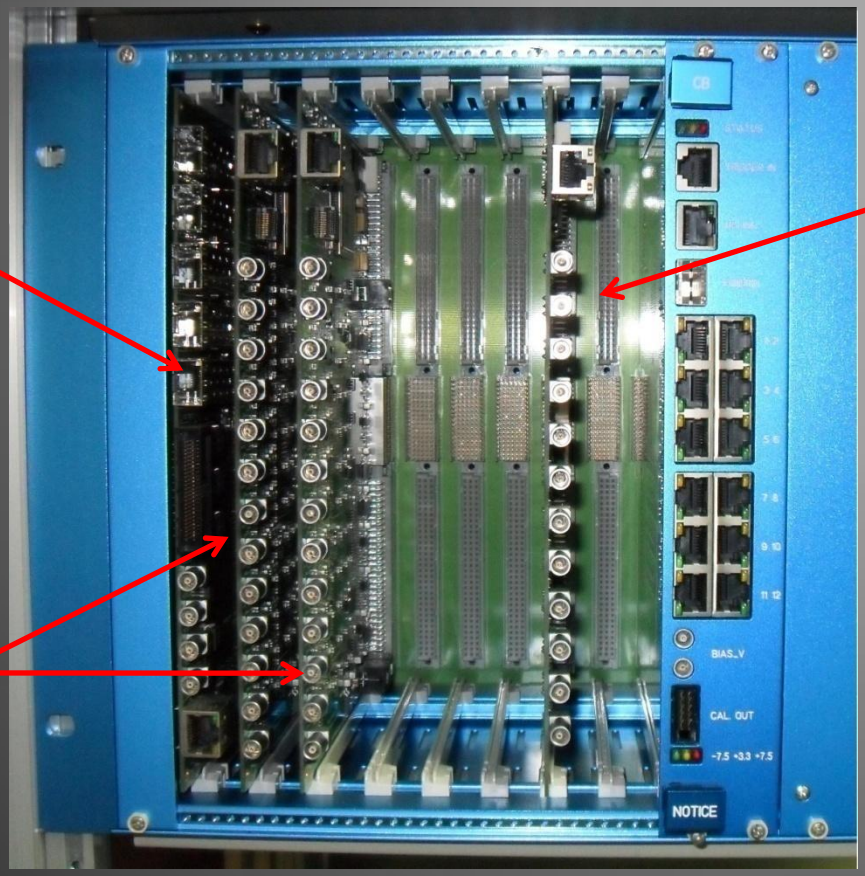
We need a special VME crate with +7.5V power supply.

Toy system for FAM/TMM test

VME crate

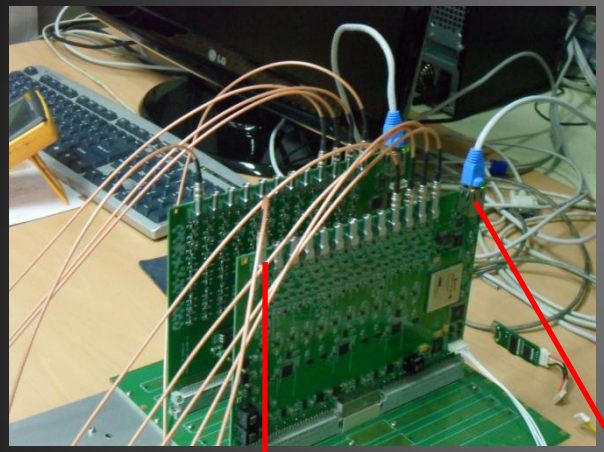
Pre-TMM

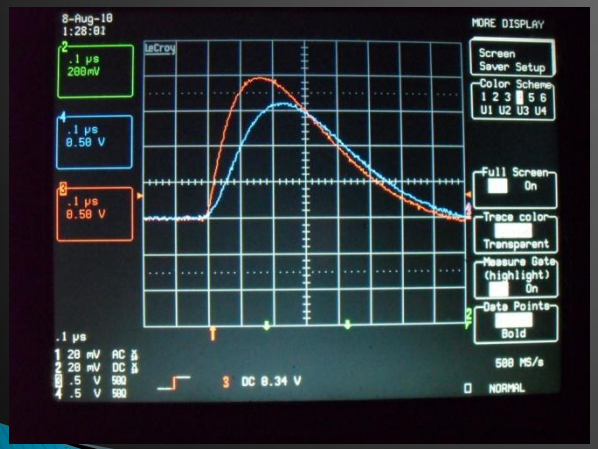
FAM

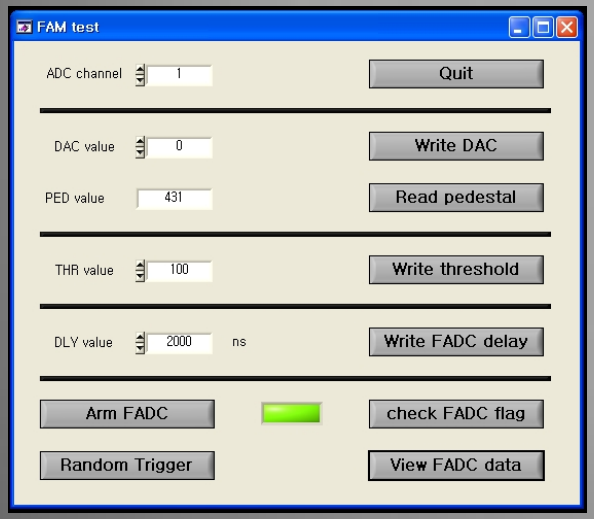


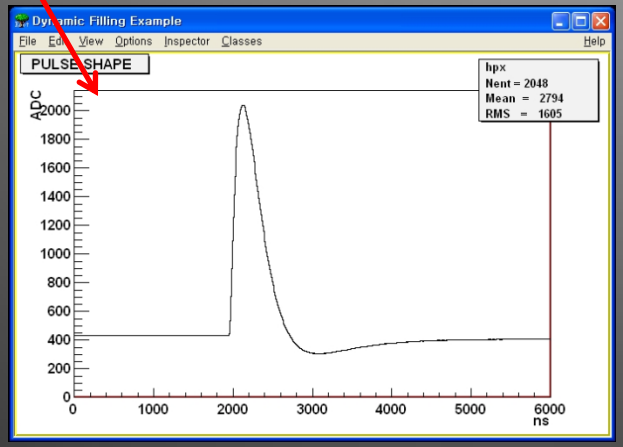
TC Analog sum emulator

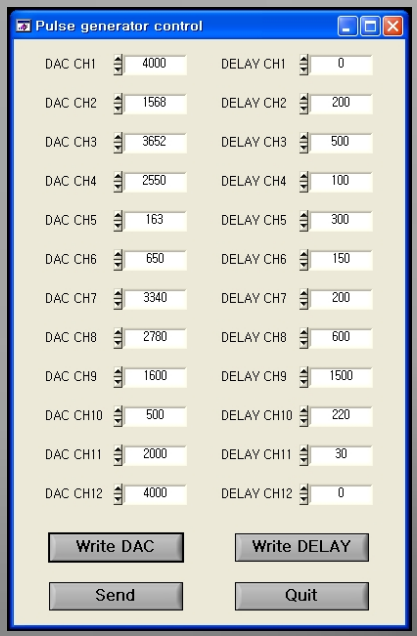
Current status : FAM test and improvement











Online monitoring

- **FAM (52):**
  - Each counter test pulse output @ calibration period
  - 12 TC hit pattern & energy distribution & waveform @ local-online
  - Each input TC peak timing & FAM output timing @ local-online
  - FAM core firmware performance @ local-online
- **TMM (5):**
  - Input /output TC hit pattern @ local-online
- **ETM(1) :**
  - Input TC hit pattern @ local-online, DQM
  - E_tot / 11-Bhabha energy and ICN @ local-online, DQM
  - Output hit pattern @ local-online, DQM
  - ETM core firmware performance @ local-online
- **Anything else ?**

Plan of tsim-ecl (by Unno san, and S.H.Kim)

- **Preparation of tsim-ecl with basf2**
- **Improvement of BhaBha veto logic**
  - **Reproduce Tsim study result for Belle (by H.O. Kim)**
    →introduce ϕ information in addition to θ
  - **try to improve the performance more**
    → higher eff. of τ and ISR by keeping eff. of B
- **Improvement of background veto(cosmic veto)**
  - **try to improve eff. of τ and ISR**
    → introduce θ information in addition to ϕ
    suggested by Hayashii-san.

Schedule

	Oct.10	Jan.11	Apr	Jul	Oct	Jan.12	Apr	Jul	Oct	Jan.13	Apr	Jul	Oct	Jan.14
Hardware														
SH-DSP (576)	2nd prototype			final prototype			mass produciton				installation & debug			ready
FAM (52)	1st prototype				final prototype			mass production			installation & debug			ready
TMM (5)	1st prototype					final prototype			mass prod.		installation & debug			ready
ETM (1)	1st prototype					final prototype			mass prod.		installation & debug			ready
Cable								mass production			installation & debug			ready
Cosmic stand			1st integration test				2nd integ. test							
Firmware														
FAM		simple version			full version			final version				debug		ready
TMM		simple version			full version			final version				debug		ready
ETM		simple version			full version			final version				debug		ready
Online software														
FAM/TMM/ETM						code preparation						debug		ready
GDL/DAQ interface						code preparation						debug		ready
Offline software														
Raw data format						consult w/ DAQ group								
Recon code								preparation				debug		ready
TSIM														
Geant-4	code ready & trigger logic study													

Summary

- **Belle2 ECL trigger : FADC/FPGA–based flexible architecture.**
- **DSP, FAM, TMM prototypes are available.**
- **Fast shaper :**
  - Tested Gain/pulse-shape/noise-level
  - Shaping time : 200ns → 100ns
- **FAM :**
  - Tested core firmware with new EBM at Belle.
  - Analog sum output for online LUM monitor.
- **TMM :**
  - Core firmware development with pre-prototype
- **Under FAM+TMM chain study with Toy system.**
- **Reviewed online monitoring items and global schedule.**
- **Y. Unno works on G4-TSIM to improve trigger logics.**

backup

Comments on cosmic veto trigger

Cosmic ray run (May/20)

Belle Run Summary(v2.6) - Exp 73 Run 119

tsc_timing	--	--
csi_timing	814Hz	813Hz
e_high	33.4Hz	33.3Hz
e_low	188Hz	188Hz
e_lum	2.7Hz	2.7Hz
csi_bb	0.9Hz	0.9Hz
csi_brlbb	0.6Hz	0.6Hz
nicl0	475Hz	474Hz
nicl1	362Hz	361Hz
nicl2	7.6Hz	7.6Hz
nicl3	0.0Hz	0.0Hz
csi_cosmic	661Hz	660Hz
csi_tpbbgg	0.4Hz	0.3Hz
csi_tpbb	--	--
csi_tpgg	0.2Hz	0.2Hz
csi_tpgx	--	--

16 hie	= e_high x !csi_bb x !csi_cosmic	9	5.78Hz	5.75Hz
17 clst4	= nicl>3 x !csi_cosmic	2	1.83Hz	1.81Hz
18 clst5		3	0.46Hz	0.47Hz
19 loe_clst3		74	8.60Hz	8.58Hz
20 e_hi_clst4		43	5.09Hz	5.11Hz
21 e_had		340	1.99Hz	1.98Hz
22 e_had_tp		438	2.57Hz	2.55Hz
23 hie_tp		1018	5.96Hz	5.92Hz
24 hadron_a		.	.	.
25 hadron_b		.	.	.
26 hadron_c		.	.	.
27 loe_fs_o		.	.	.
28 loe_fs_to		.	.	.
29 clst2_o		.	0.00Hz	0.00Hz
30 clst2_to		.	.	.
31 two_photon		.	.	.
32 tau		30	34.46Hz	34.36Hz

Beam BG study run(Jun/7)

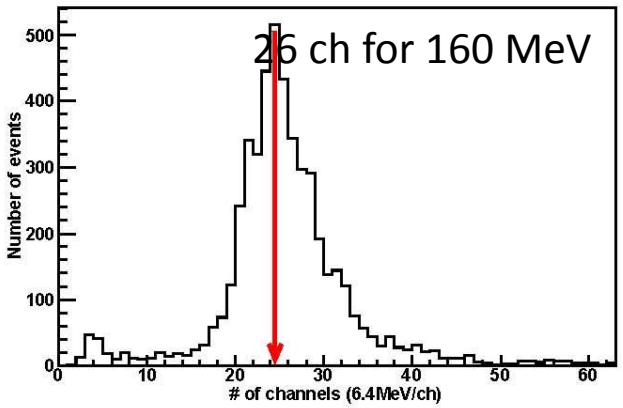
Belle Run Summary(v2.6) - Exp 73 Run 565

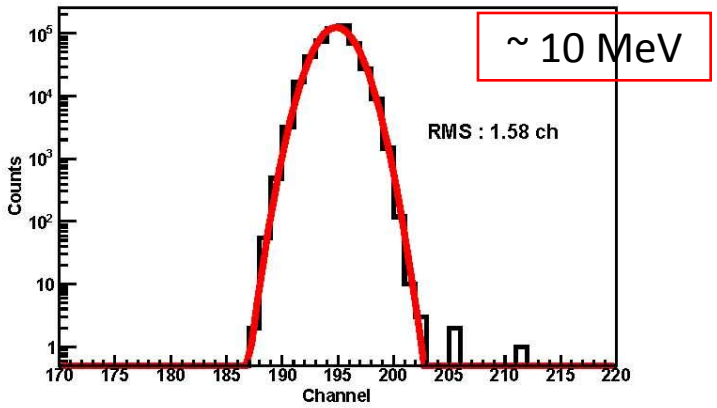
tsc_timing	7.2kHz	6.2kHz
csi_timing	12kHz	12kHz
e_high	323Hz	50.7Hz
e_low	714Hz	437Hz
e_lum	279Hz	4.2Hz
csi_bb	171Hz	1.2Hz
csi_brlbb	142Hz	0.8Hz
nicl0	11kHz	11kHz
nicl1	952Hz	861Hz
nicl2	77.5Hz	9.8Hz
nicl3	103Hz	0.0Hz
csi_cosmic	12kHz	11kHz
csi_tpbbgg	147Hz	23.4Hz
csi_tpbb	0.4Hz	0.3Hz
csi_tpgg	4.0Hz	--
csi_tpgx	0.7Hz	0.0Hz

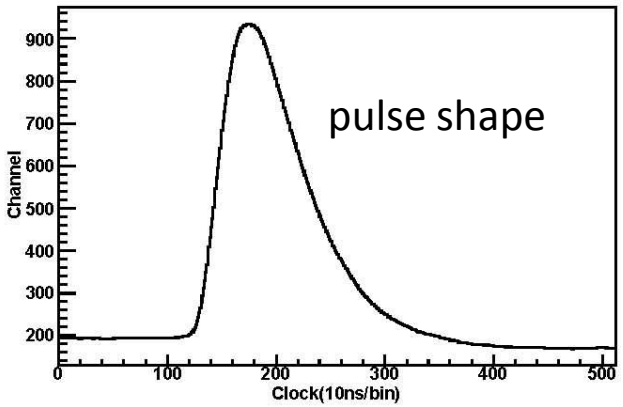
16 hie	. . .	8.86Hz	9.01Hz
17 clst4	. . .	3.36Hz	3.42Hz
18 clst5	. . .	0.50Hz	0.51Hz
19 loe_clst3	. . .	21.65Hz	22.07Hz
20 e_hi_clst4	. . .	5.17Hz	5.29Hz
21 e_had	. . .	3.20Hz	3.26Hz
22 e_had_tp	. . .	3.87Hz	3.94Hz
23 hie_tp	. . .	9.02Hz	9.17Hz
24 hadron_a	. . .	4.96Hz	4.79Hz
25 hadron_b	. . .	4.30Hz	4.20Hz
26 hadron_c	. . .	0.05Hz	0.04Hz
27 loe_fs_o	. . .	8.35Hz	8.26Hz
28 loe_fs_to	. . .	6.13Hz	6.09Hz
29 clst2_o	. . .	33.91Hz	33.56Hz
30 clst2_to	. . .	25.25Hz	25.18Hz
31 two_photon	. . .	298.58Hz	295.96Hz
32 tau	. . .	102.83Hz	103.59Hz

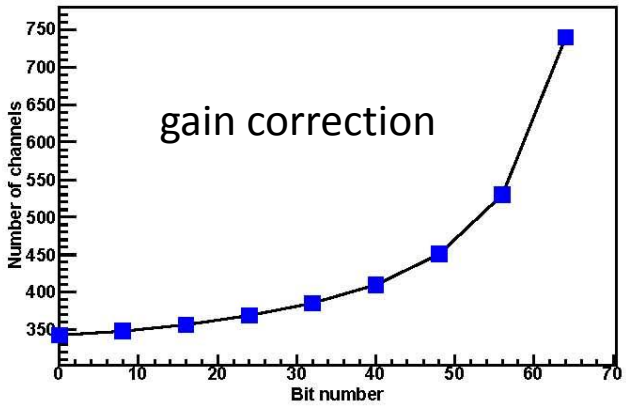
Cosmic veto → Beam BG veto

Test result


26 ch for 160 MeV
Number of events
# of channels (6.4MeV/ch)


~ 10 MeV
RMS : 1.58 ch
Counts
Channel


pulse shape
Channel
Clock(10ns/bin)


gain correction
Number of channels
Bit number

TC occupancy

```
-------------------------------------------
Belle Run Summary(v2.6) - Exp    69  Run  1203
-------------------------------------------

Start Time: 2009 Jun 17, 14:20:17 took   22 sec to start
Stop  Time: 2009 Jun 17, 17:25:39 took 11122 sec
Stop Reason: FATAL from [RUNSUM] LER/HER beam lost (1216.'
```

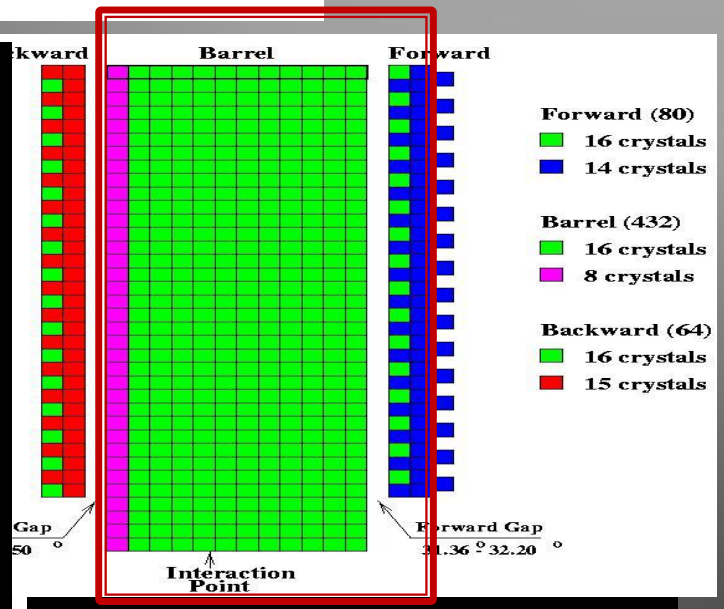
Occupancy/TC < 15KHz/500TCs x 10 x 2 x 40 x 0.5 = 12kHz

Here assumed very conservatively :

- $2x10^{34}$
- er trigger
- rate due to beam BG
- ity x 50% of trigger rate
- e width (2us) would be okay.

```
Luminosity:      ECL          EFC          KEKB
   at start   202.34e32    189.05e32    163.31e32
   at stop    190.86e32    118.29e32     70.91e32
   peak/fill  210.83e32
```

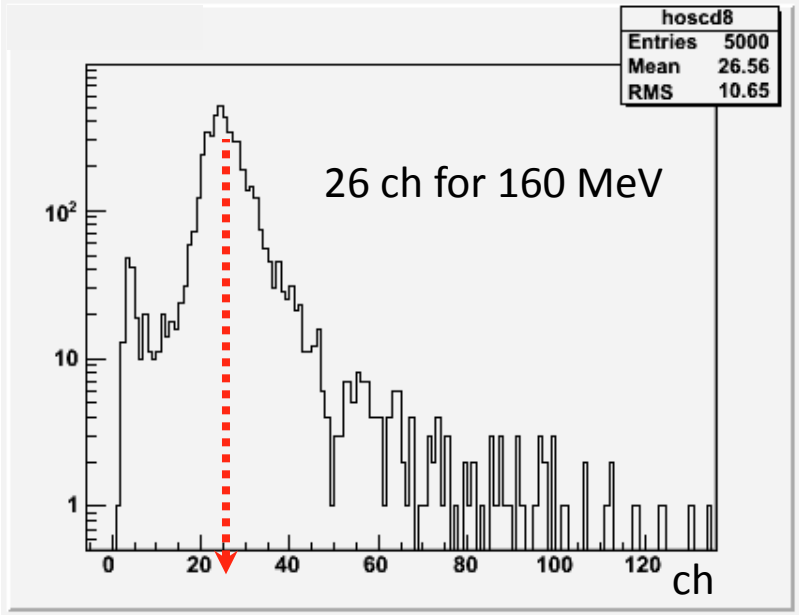
tsc_mult	4.6kHz	3.9kHz
tsc_pat	1.0kHz	552Hz
tsc_ge1	103kHz	102kHz
tsc_ge2	4.6kHz	3.9kHz
tsc_timing	4.6kHz	3.9kHz
csi_timing	13kHz	13kHz
e_high	1.4kHz	1.2kHz
e_low	2.1kHz	1.9kHz
e_lum	964Hz	791Hz
csi_bb	916Hz	809Hz
csi_brlbb	267Hz	202Hz
nicl0	12kHz	12kHz
nicl1	1.5kHz	1.4kHz
nicl2	118Hz	73.2Hz
nicl3	101Hz	41.4Hz
csi_cosmic	12kHz	12kHz
csi_tpbbgg	890Hz	849Hz
csi_tpbb	268Hz	266Hz
csi_tpgg	319Hz	317Hz
csi_tpgx	120Hz	118Hz

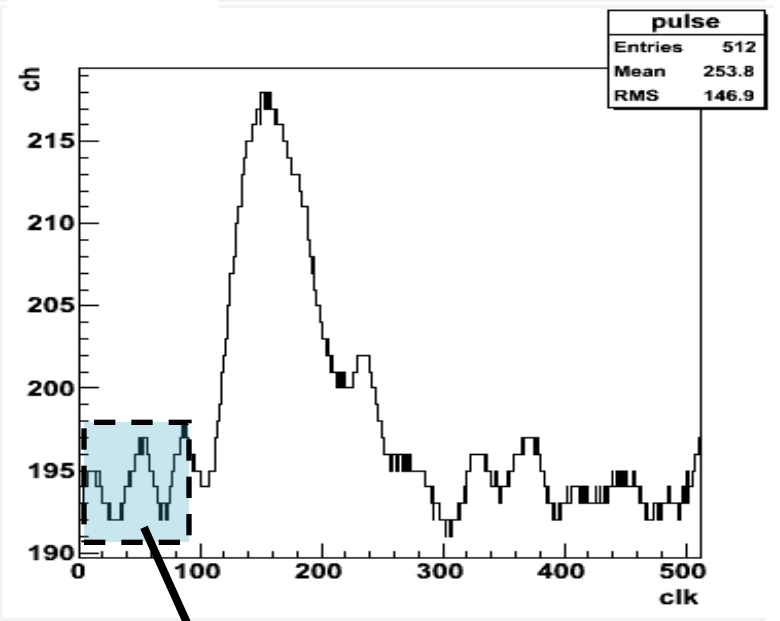


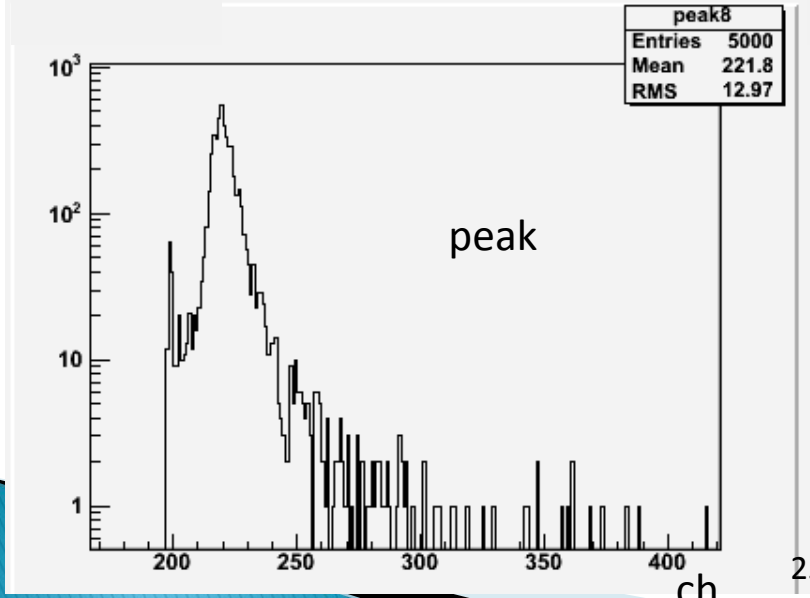
Physics trigger region

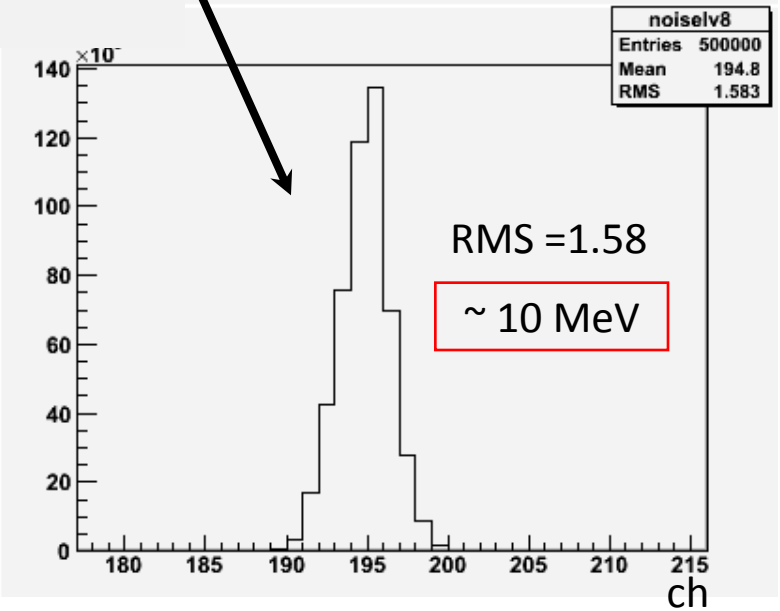
- Noise level test with cosmic data → okay

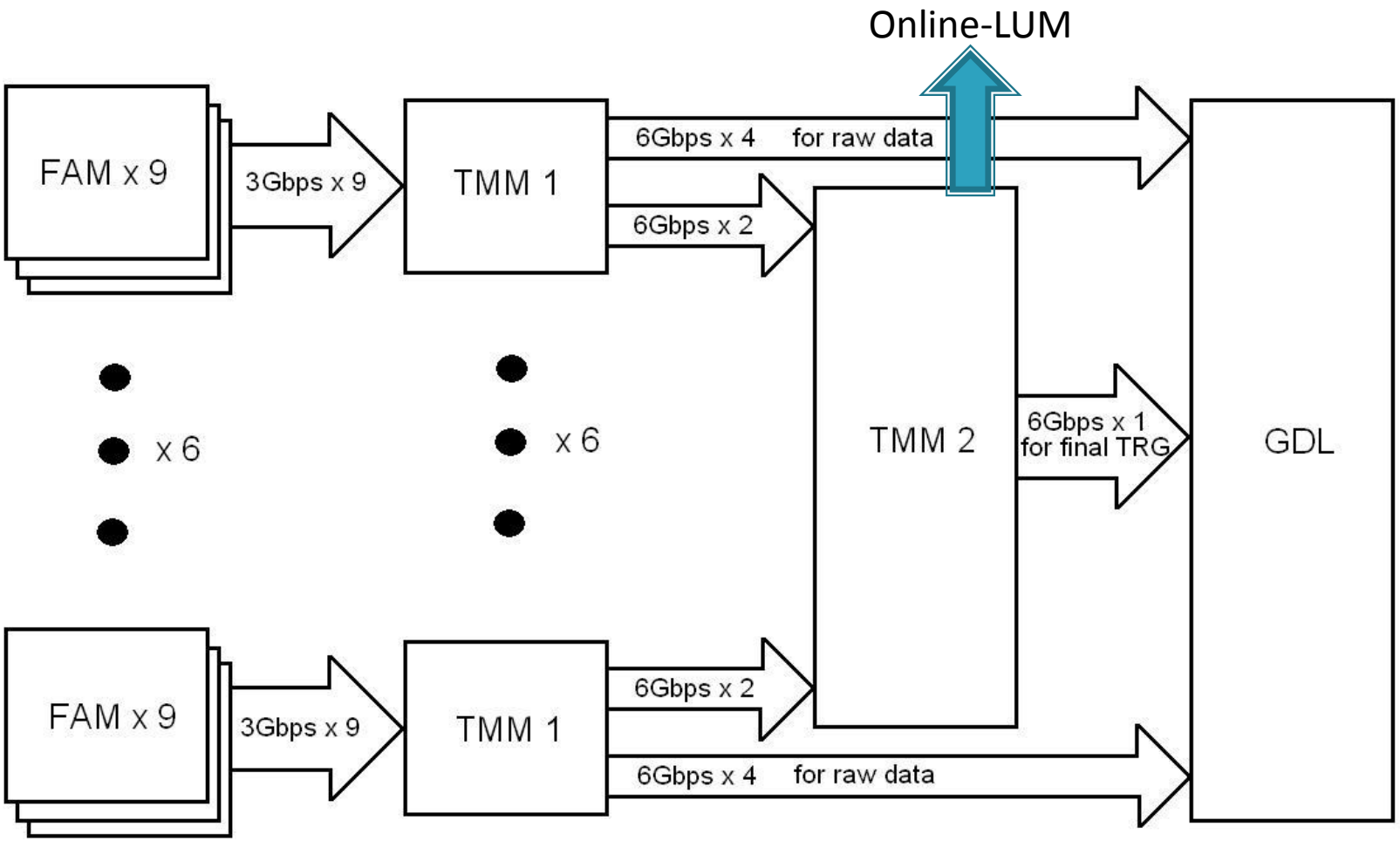
Ryu Soo (SNU)











Peaking time of TC	700
ADC pipeline	100
Peak finding process	300~400
Programmable delay	300
Gbit transfer(200bits)	100
Optical cable length	200~300

Bridge delay	200~300
Gbit transfer(~450bits)	100

Input alignment	100
Trigger decision	200~300

* Total latency = 2300 ~ 2700 ns

** TMM FPGA = XC6VLX75T-1FT784C