# CDC Merger

Alan Teng[1], Liu Shih-Min[1], C.H. Wang[2]

[1] Department of Electrical Engineering,

[2] Department of Electro-Optical Engineering,

National United University, Maoli, Taiwan.

# Outline

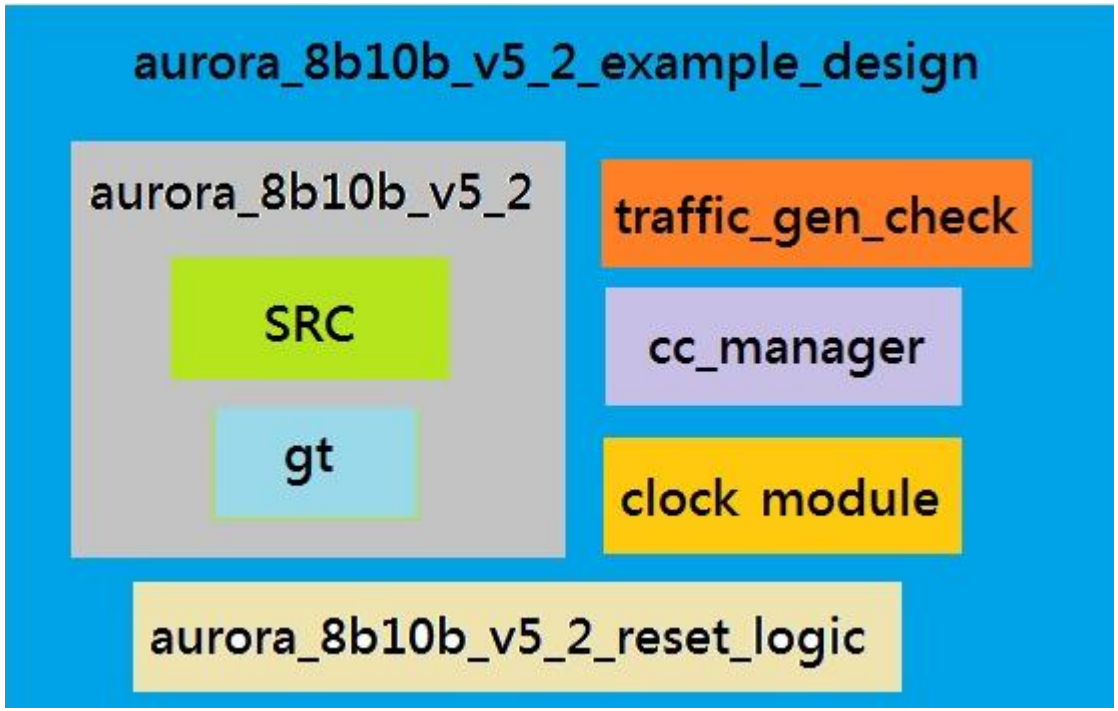
- Aurora IPcore files
- Change Xilinx IPcore to Altera
- Transmit speed
- Transceiver difference
- Test over
- In test
- problem

# Aurora IPcore files (Structure)

- Aurora IPcore files include:
  - ./SRC
    - Aurora protocol core files
  - ./example_design
    - User interface example files
      - ./cc_manager (clock correction files)
      - ./clock_module (PLL files)
      - ./gt (transceiver files)
      - ./traffic_gen_check (read and write files)
      - aurora_8b10b_v5_2_reset_logic.vhd (reset control)
      - aurora_8b10b_v5_2.vhd (Integration core and transceiver)
      - aurora_8b10b_v5_2_example_design.vhd (TOP level)

# Examples:

- File Relations



# Change Xilinx IPcore to Altera

- Need to be removed and replaced components
  - Need removed
    - I/O buffer (Done!)
  - Need replaced
    - FD、FDR、SRL16...etc.
    - Transceiver、PLL (Done!)

# Transmit speed

- Xilinx : linerate
- Altera : effective datarate
  - Transmit how many bit per-second

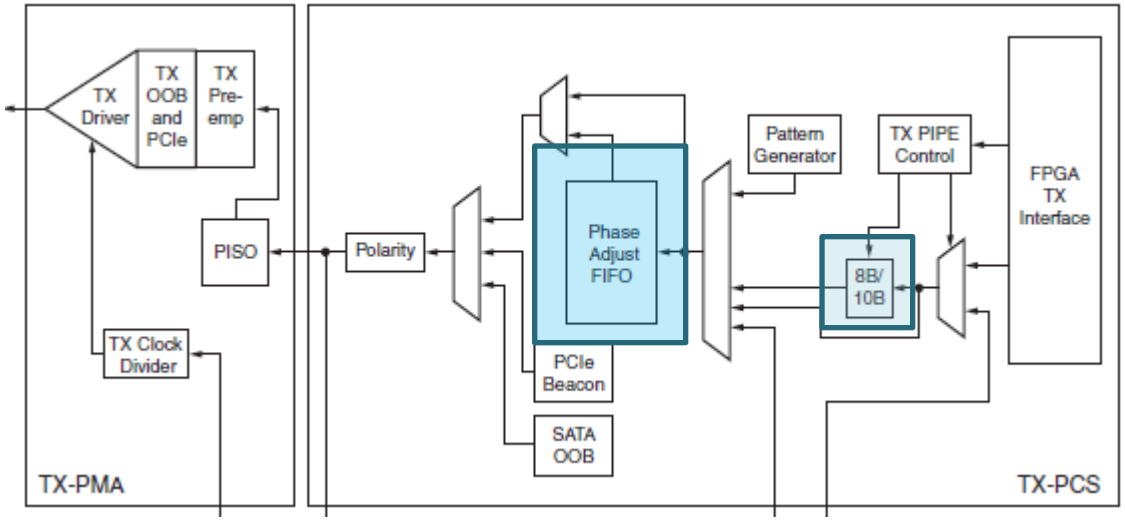
- linerate and datarate
  - Aurora use 8b10b encoder/decoder，so 8 bits data will use 10 bits space, and datarate will be linrate*0.8.
  - For example,linerate is 5Gbps the datarate is 5Gbps*0.8 = 4Gbps

# Transceiver difference

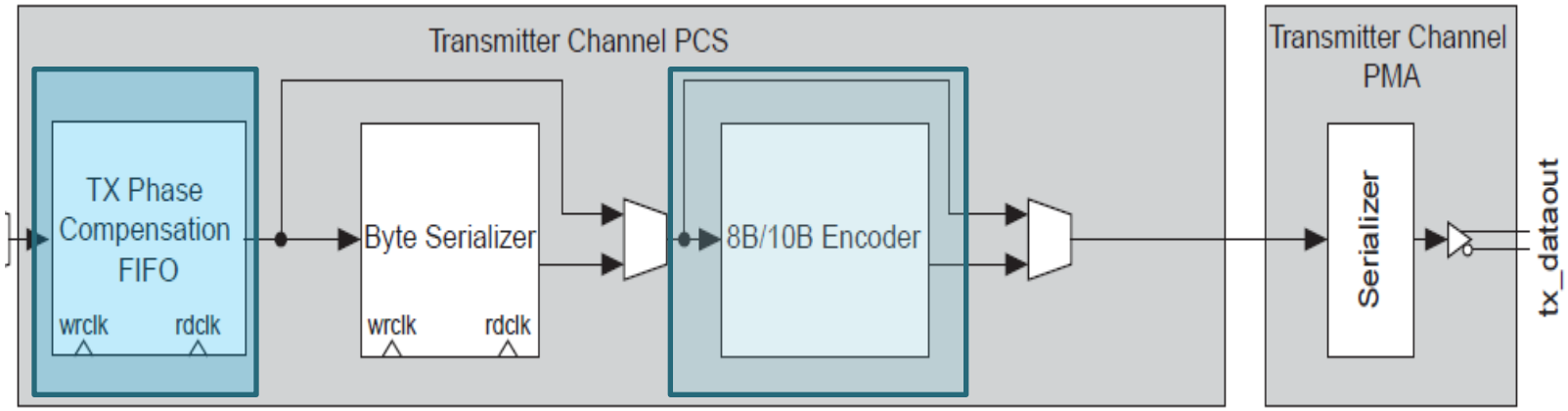
- Xilinx
  - transmit and receive use the same clock
  - support Aurora protocol function
- Altera
  - transmit and receive use different clocks
  - Support part of Aurora protocol function

# Xilinx and Altera transceiver structure: transmitter

**XILINX**

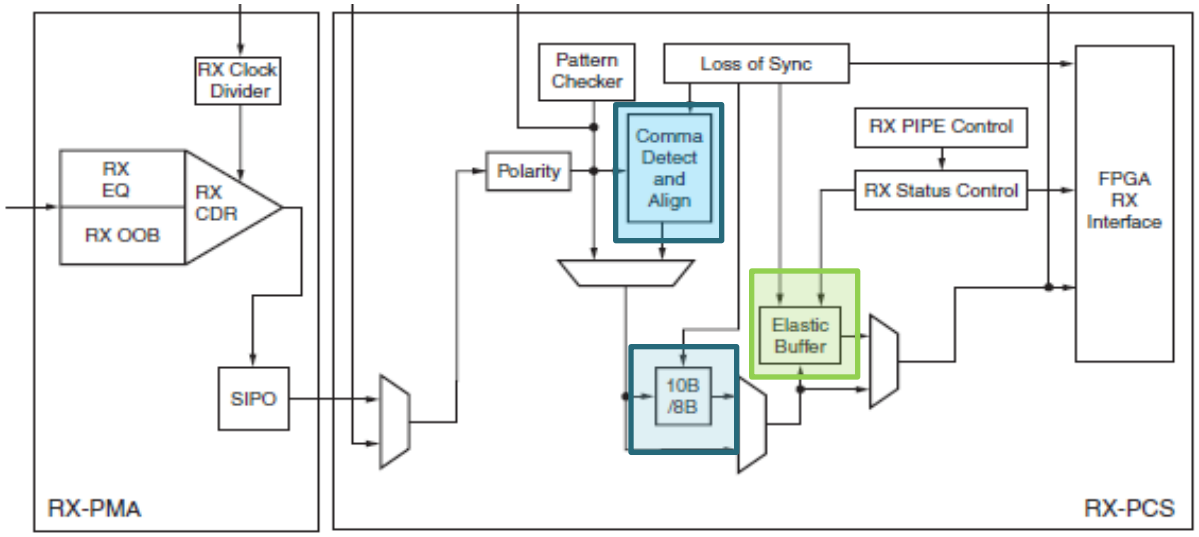



**ALTERA**

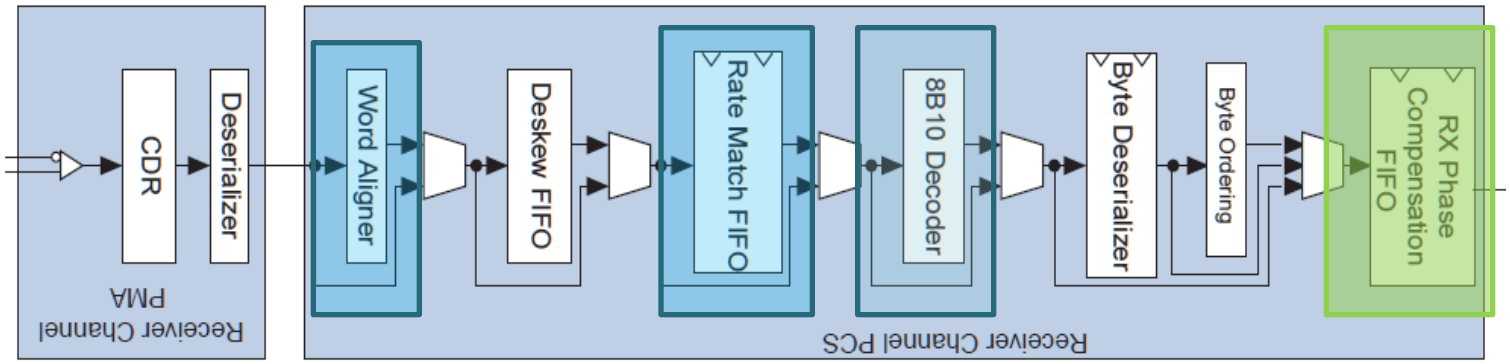


# Xilinx and Altera transceiver structure: receiver

**XILINX**




**ALTERA**



# Tests have been completed !

- SP6 Aurora 3.125G in Altera Stratix4
  - SP6 ⟺ Stratix-4
  - Virtex6 ⟺ Stratix-4

OK

- VT6 Aurora 3.125G in Altera Stratix4
  - VT6 ⟺ Stratix-4

OK

# In progressing…

- VT6 Aurora 5G in Altera Stratix4
  - Change IPcore completed
  - VT6 and Stratix4 transceiver test completed
  - Loopback is in test
  - VT6 ⟺ Stratix4 test is in test

# Problem during the 5G test

- Altera transceiver can't setup 5Gbps and 16bit width directly
  - Solved successfully
- Received data is incorrect
  - Solved successfully

- 5G Core on Stratix4 still can't work
  - When receive the initial sequence, the core gives no response. – expected to be solved soon.

# Summary

- The Aurora protocol has been studied in details.
- The implementation of Aurora on Altera transceiver is successfully completed for speed < 3 Gbps.
- Problem shows for the 5G speed which is under investigation now.
- We will start the board circuit layout soon.