

Belle2 CDC TRG System

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TRG/DAQ Workshop

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Zhongguanyuan Global Village, PKU

CDC

- CDC becomes large
 - #wires : 8400 -> 14000
- Cell structure is same
- # Super Layers is decreased
 - 11 -> 9
- All wires including stereo layers will be used in CDC TRG

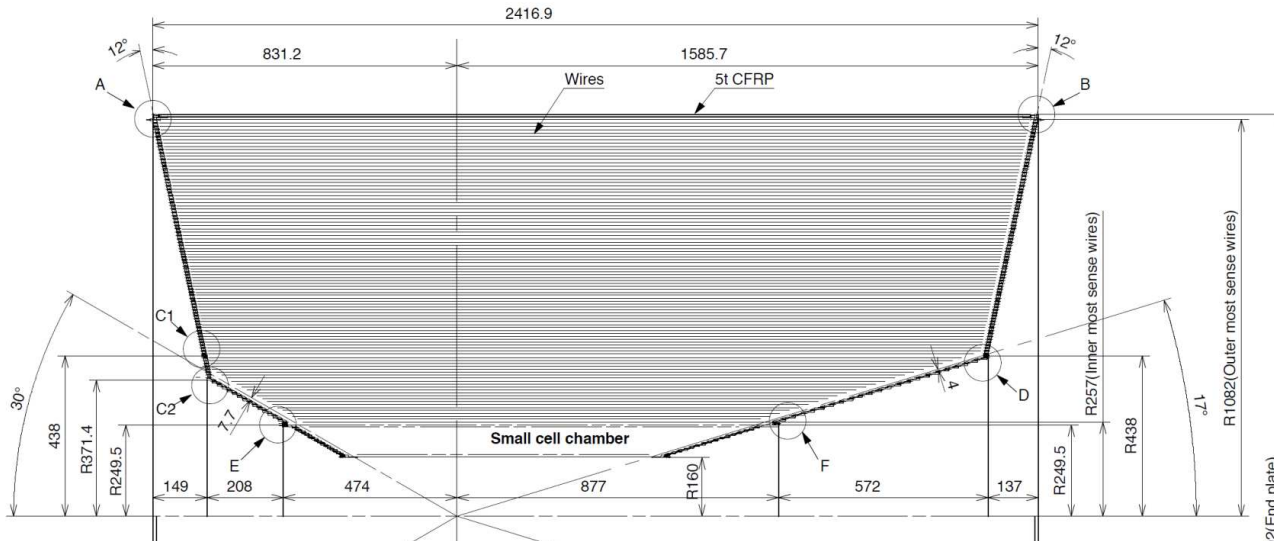
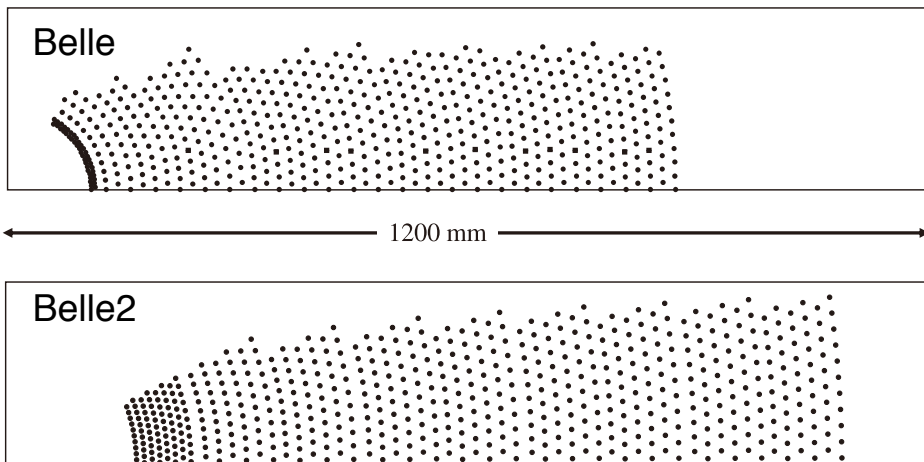
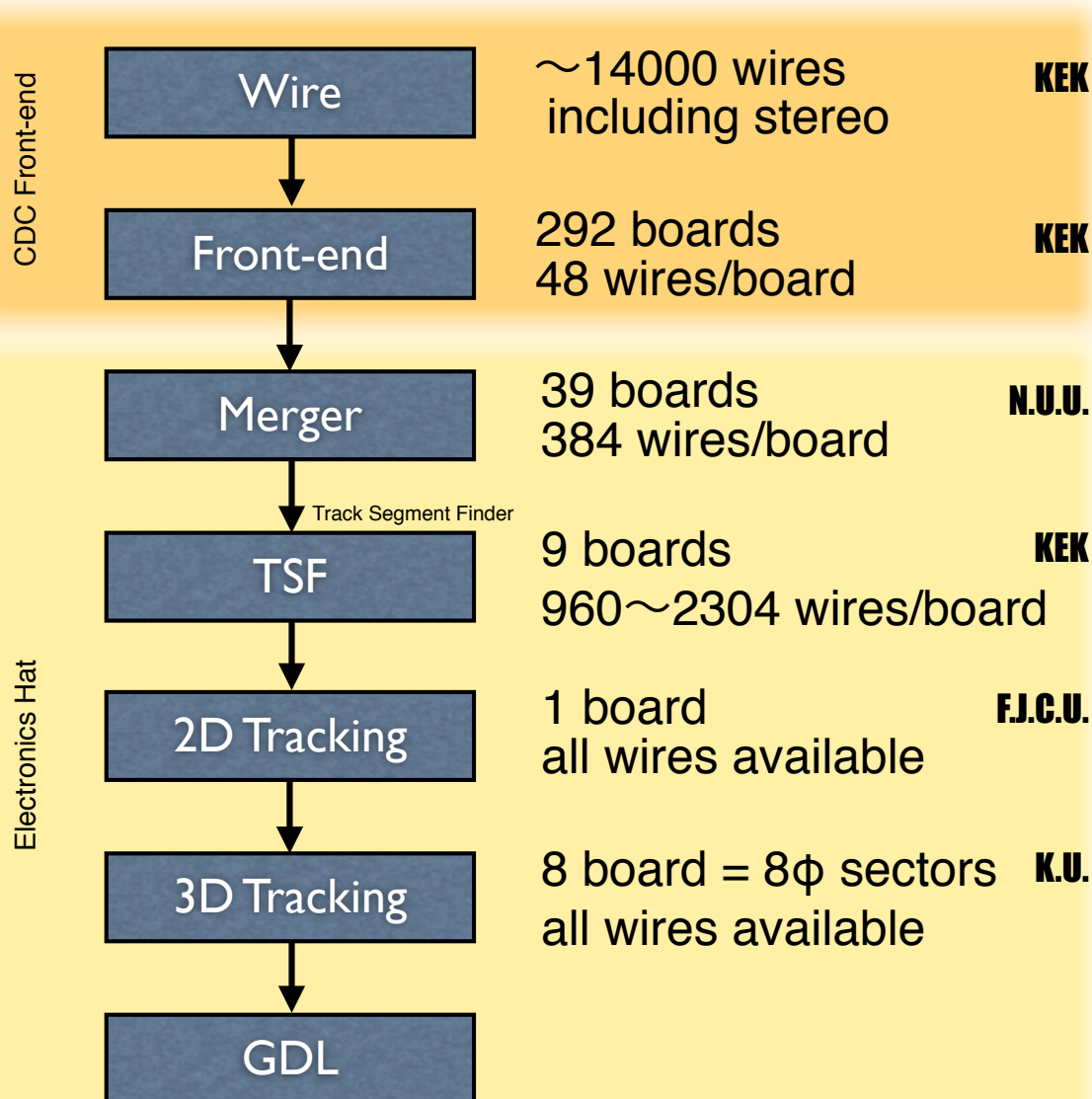


Table 6.2: Configuration of the CDC sense wires.

superlayer type and No.	No. of layers	Signal cells per layer	radius (mm)	Stereo angle (mrad)
Axial 1	8	160	168.0 – 238.0	0.
Stereo U 2	6	160	257.0 – 348.0	45.4 – 45.8
Axial 3	6	192	365.2 – 455.7	0.
Stereo V 4	6	224	476.9 – 566.9	-55.3 – -64.3
Axial 5	6	256	584.1 – 674.1	0.
Stereo U 6	6	288	695.3 – 785.3	63.1 – 70.0
Axial 7	6	320	802.5 – 892.5	0.
Stereo V 8	6	352	913.7 – 1003.7	-68.5 – -74.0
Axial 9	6	384	1020.9 – 1111.4	0.

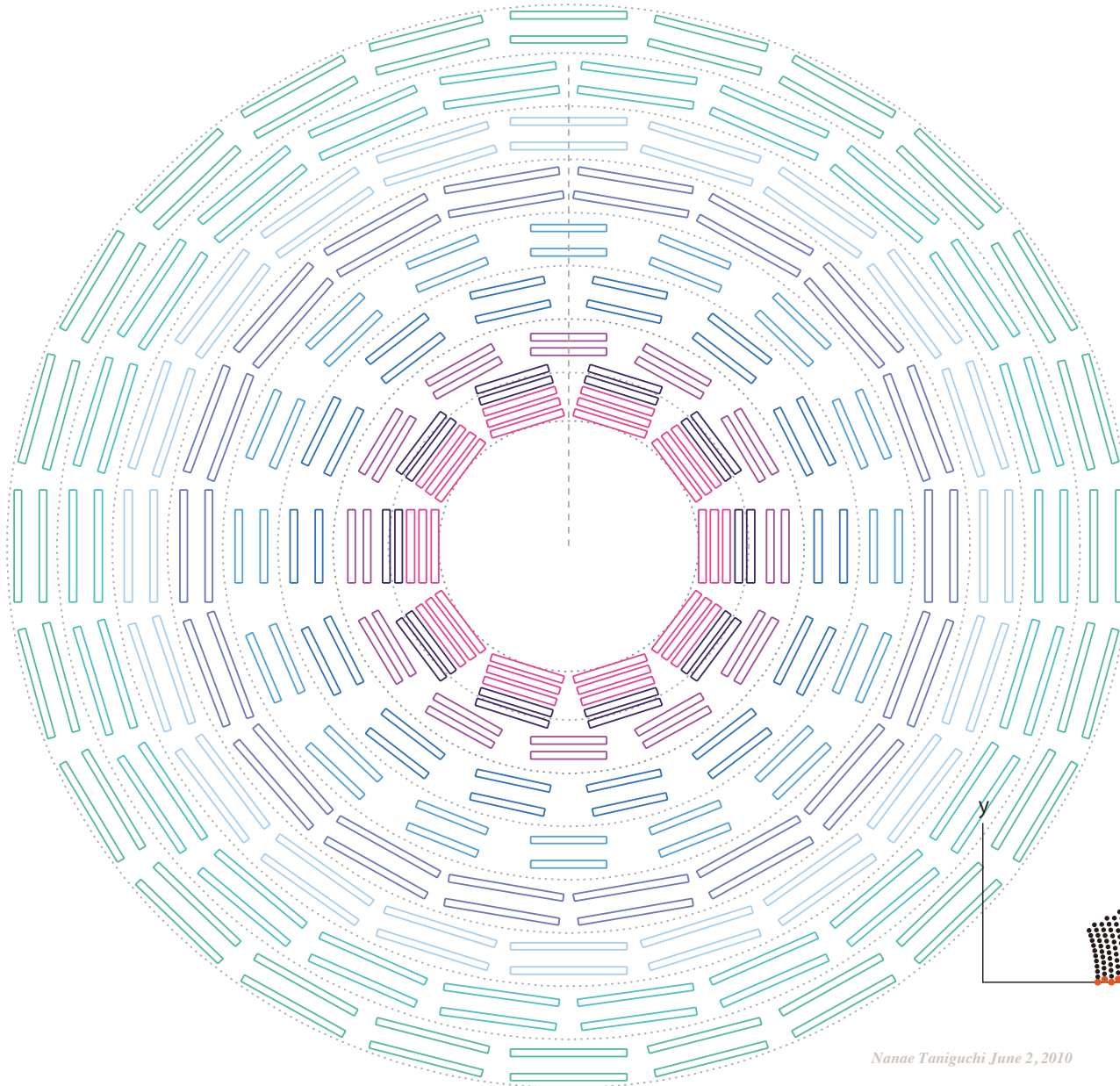


CDC TRG : Logical Flow

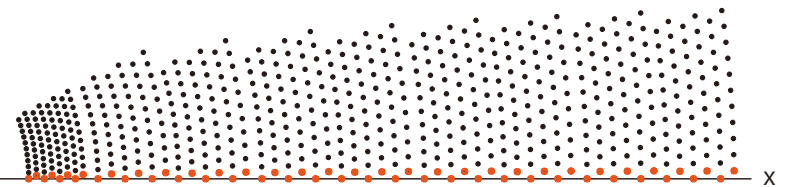


Proto-Type	Production	Firmware	TSIM
n/a	?	n/a	OK
3rd version in progress	2012 ?	2nd version in progress	OK
1st version in progress	2012 ?	2nd version in progress	OK
3rd (final) version in design stage [UT3gamma a]	2011 ?	1st version in progress	2nd version in progress
		1st version in progress	1st version in progress
		1st version in progress	1st version in progress

CDC TRG : Front-End Location

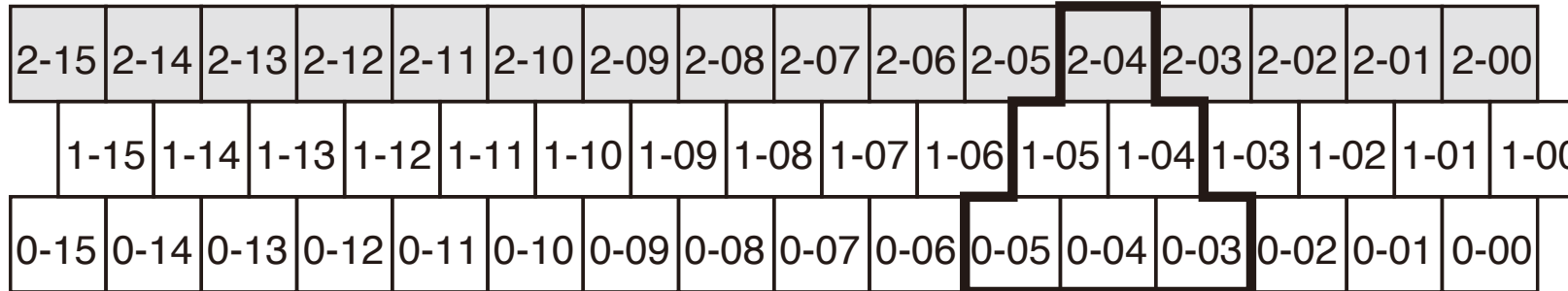


- **Front-End**
 - 48 ch/board
 - 292 boards in total
- **2 front-end layers in a super layer**
- **first wire in each layer (red-wires) should be the edge of phi division**
 - Request to CDC group



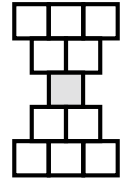
Front-end

CDC Front-End Board



Partial Track Segment (pTS)

Outer TSF



TRG logic system clock : 125 MHz

Data update : 62.5 MHz (every 2 clocks)

Data

1 bit for hit info. for all cells

4 bit for hit timing for the priority wire cells (LSB 2ns)

2 bit for the fastest timing in the pTS (LSB 8ns)

Data size : $1 \times 48 + 4 \times 16 + 2 \times 16 = 144$ (bit)

Data flow : $144 \times 62.5 \text{ M} = 9 \text{ G}$ (bps)



Priority wire cell

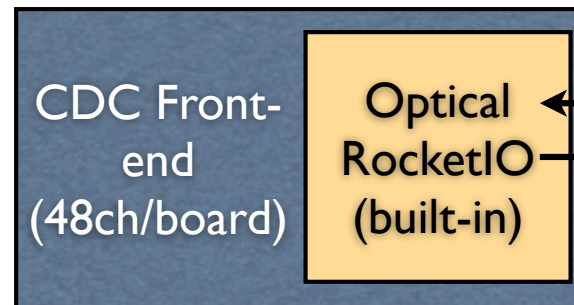


Wire cell

TRG Stream IN

[12.5Gbps = 3.125Gbps x4]

- * control
- * calibration data
- * simulation data



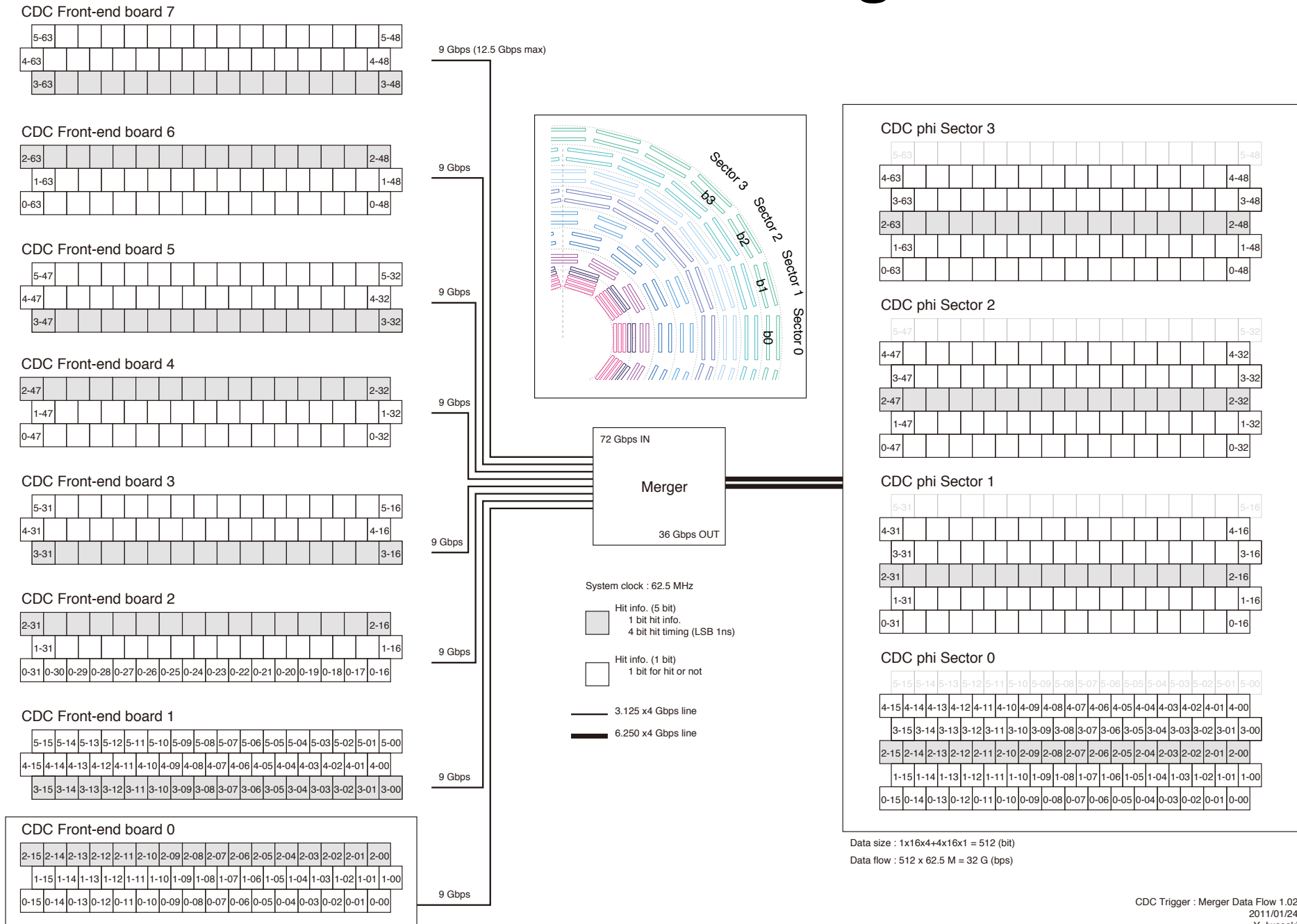
TRG Stream OUT

[12.5Gbps = 3.125Gbps x4]

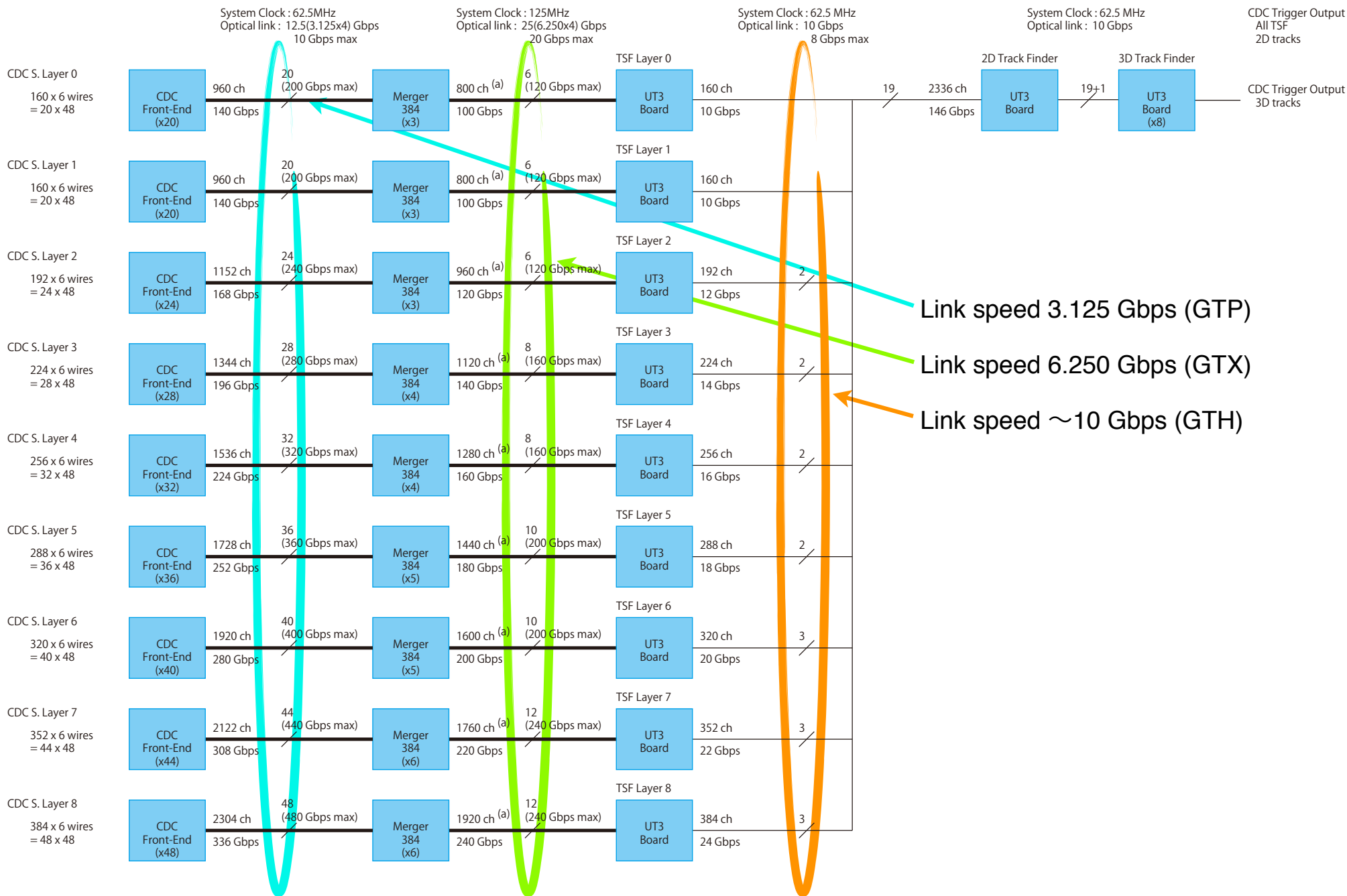
- * hit pattern (48 cells)
- * hit timing (16 cells)
- * fastest timing (16 cells)
- * calibration data

We like to send "TRG local clock" to Front-ends when in development stage

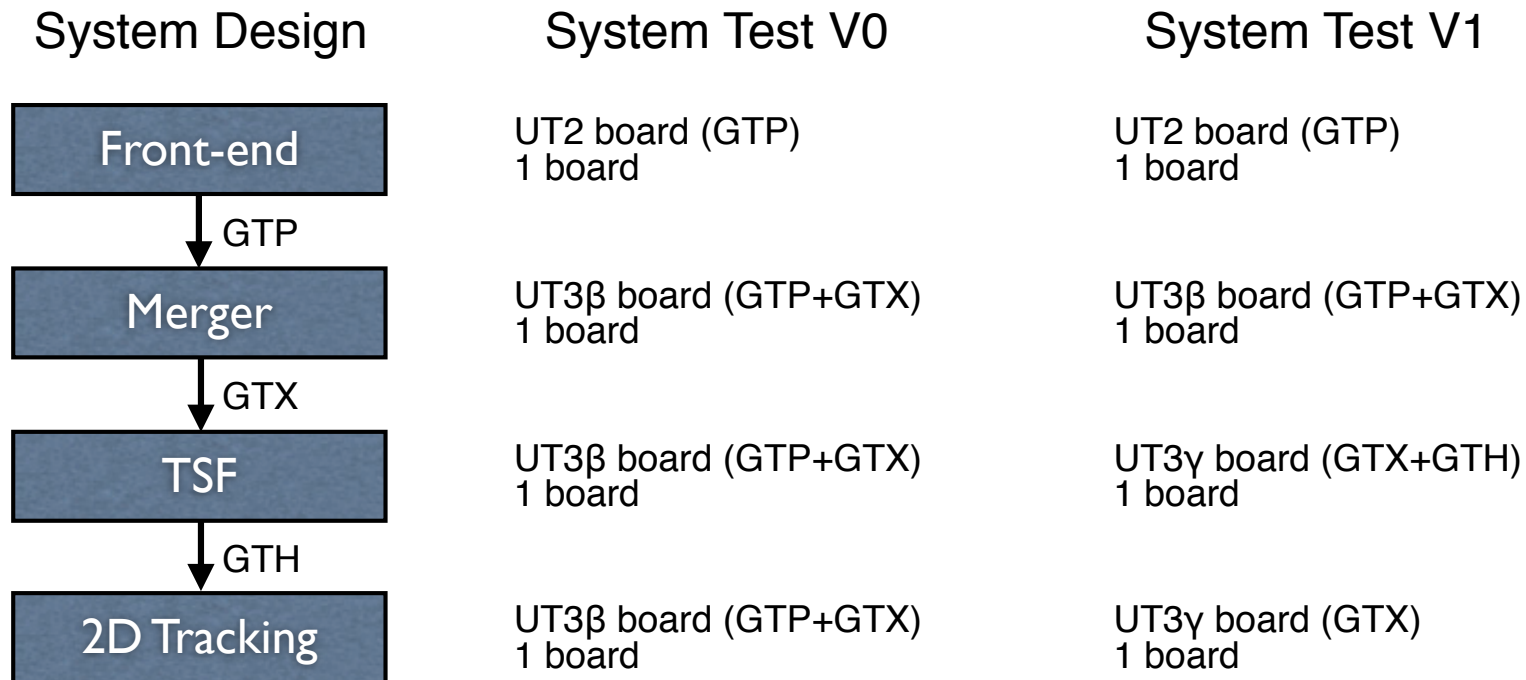
Front-end and Merger



Signal Flow in CDCTRG

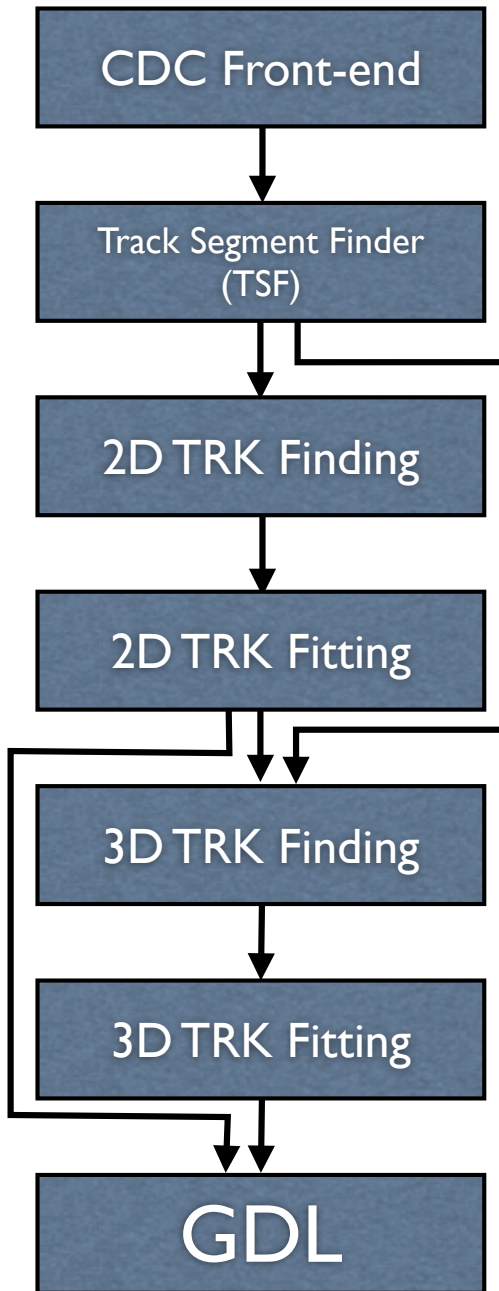


Partial System Test

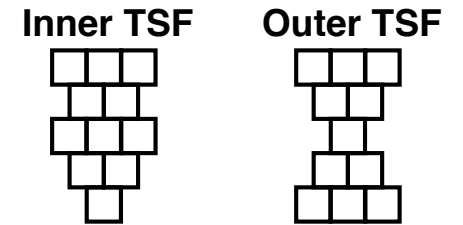


- **Partial System is building in Tsukuba B2F**
 - **Version 0 : test with compatible boards without GTH**
 - **Version 1 : test with compatible boards with design link speed**
 - **Version 2 : test with production boards**
- **We will report performance of V0 at B2GM in spring**

CDC Trigger : Algorithm



Formed in all super layers : ~2000TSFs
Hit decision by Memory Look Up (MLU)

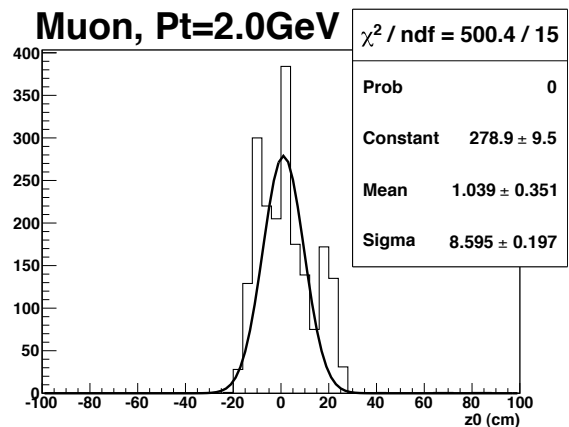


Finding by Hough transformation
→ Pt and ϕ , #tracks, charge sum

Linear fit in Conformal plane
→ improved Pt and ϕ
Pt resolution : 2~15%

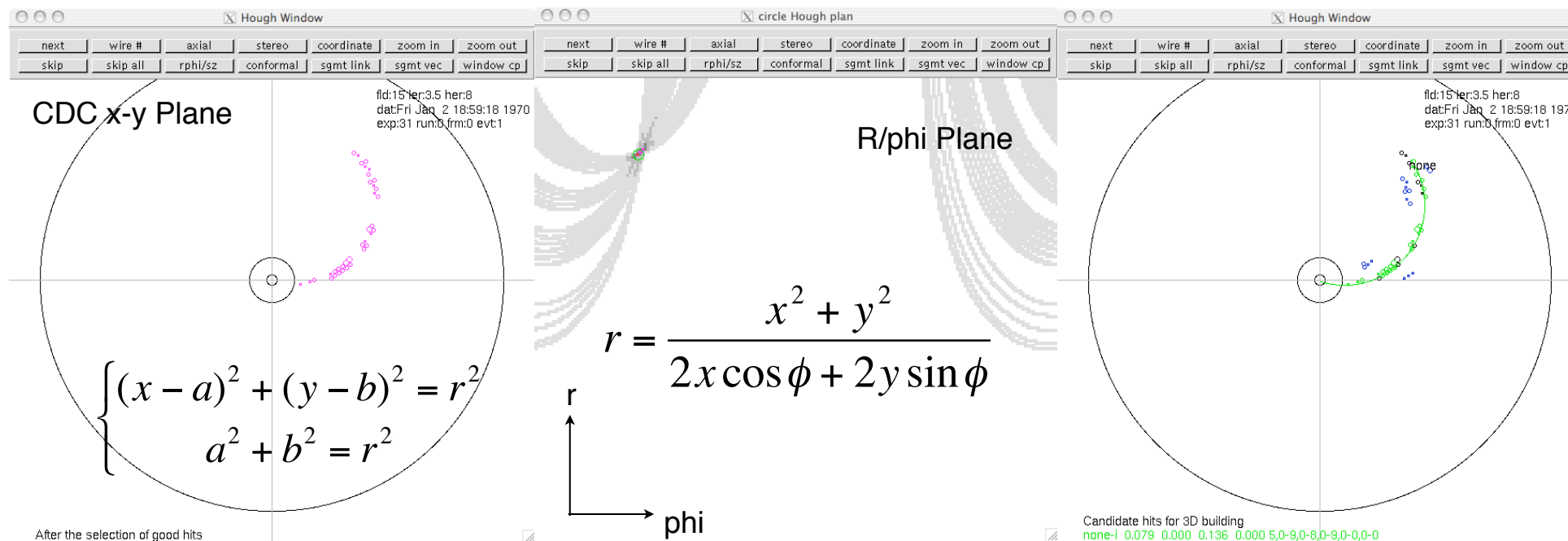
Attach stereo TSFs to 2D tracks
→ 3D track candidates

Fit 3D tracks → z and $\cot\theta$
z resolution : ~ 4cm



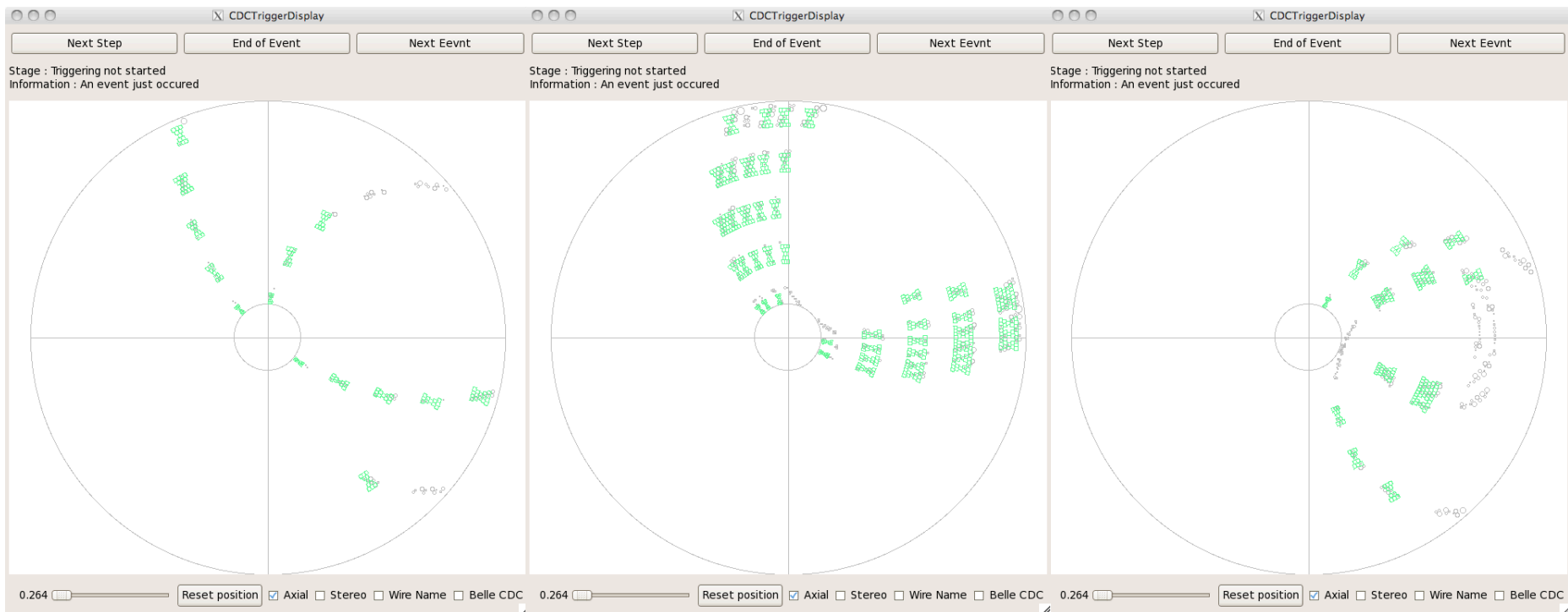
2D Track Finding

- **Hough algorithm**
 - **Circle (on the origin) search -> Peak finding on the parameter plane**
 - **Plan to do similar method like “trasan” (offline track finding module in Belle)**
 - **Input : TS hit**
 - **Peak finding and mesh size are keys to obtain good performance**
 - **F.J.C.U. group will study peak finding using TSIM**

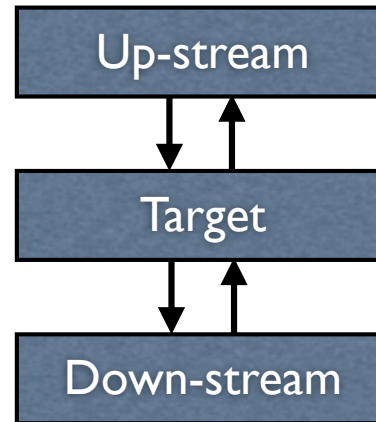


CDC Trigger Simulation

- **Basic components were installed under basf2**
 - **trg/cdc/...**
 - **Present version can simulate up to TSF**
- **Hardware module base simulation is necessary**
 - **Especially for 3D tracking developments**
 - **Input and output of each hardware module will be simulated**
 - **Simulated input can be sent to real hardware**



How to Debug CDC TRG System?



- **To debug a target, we need both input and output**
 - **Input is simulated data sent from Up-stream to Down-stream via Target, then send to Target from Down-stream**
 - **Output is recorded and examined at Up-stream**

Summary

- **Proto-typing of modules are on the way**
 - No big delay in schedule
 - UT will be made fiscal year 2011
- **Partial system tests**
 - To demonstrate stability of our system design
 - To develop monitor tools, maintenance methods, debugging, etc
- **Trigger algorithm development with TSIM is going on**

