



1

Status on the 3D fitter

TRG/DAQ Workshop Jan 26 2011 Jaebak Kim(*), Eunil Won, Byeongrok Ko, Kyungtae Kim Korea University

Last B2GM

- Things to do
 - New basf2 CDC geometry has to be in
 - Move C++ program into integer space
 - Write VHDL
 - Use timing information to reach z0 resolution
 ~O(4cm)
 - Write identical C++ into tsim cdc

Last B2GM

- Things to do
 - New basf2 CDC geometry has to be in-
 - Move C++ program into integer space IN PROGRESS
 - Write VHDL IN PROGRESS
 - Use timing information to reach z0 resolution ~O(4cm) (KKT)
 - Write identical C++ into tsim cdc

IN PROGRESS

<u>(KKT</u>

DONE

New basf2 CDC geometry

- I calculated multiple perfect tracks using the geometry in the basf2 for the CDC given by KKT. (in order to test the 3d-fitter)
- I put the track data into the 3d-fitter to see if the fitter worked correctly with the BELLE2 geometry

 (In doing so, I was able to improve the fitter.)
- Track info
 - $p_T: [0.5 \sim 2.5] \text{GeV}$
 - Track angle: [0~360]deg
 - z/r slope: Gaussian (mean: -0.09359,sig: 0.01)

• Previous fitter (Results using basf2 geometry)



• Improved fitter (Results using basf2 geometry)



• The current code uses this relation

• $(ztostraw - z) * tan\theta_{st} = r * tan(|\phi_{fit} - \phi|)$





• We will do this test again using the data from tsim, and also when the C++ code is changed into integer space.

Move C++ to integer + VHDL

- I am planning to move the C++ code into integer space step by step, while writing VHDL for each step I go.
- In doing so, I can made sure that the C++ code and VHDL will give the same output.
- We have two C++ versions. I will change one of them to VHDL and see which one will be better later.

- I have made some toy components for the 3D fitter firmware at a 130Mhz clock on a Virtex 5 220T chip. (UT2 board)
 - Speed the 42Mhz board clock to 130Mhz using DCM (To match with other trigger logic boards)
 - An LUT(Look up table) using BRAM(Block RAM)
 - An LUT using CLB(Configurable Logic Block) (Distributed RAM)
 - Multiplication using DSP slices in Virtex chip

- The board clock is 42Mhz so I speeded it up to 120Mhz using DCM.
 - From 23.81ns => 42 Mhz,
 - To 8.3ns => 120 Mhz



- LUT using BRAM
- These LUT's will be used for atan, cos, sin functions.

🞯 Waveform - DEV:0	MyDe	vice0 ((XC5VI	. <mark>x</mark> 220t) (UNIT:0 N	MLAO (IL/	A) 🔅												۲ <u>۵</u>	X
Bus/Signal	х	0	381	382	383	384	385	386	387	388	389	390	391	392	393	394	395	396	397	,
夲 /addra	126	126	251)	(252)	253	(254)	(255)			2	X 3	<u>4</u>	5	χ_6	X 7	X 8	9	(<u>10</u>)	(11	
<mark>∽ אסטעד_</mark>	125	125	250)	(251)	252	253	(254)	255		(1	X	<u>3</u>	4	χ 5	X 6	χ_7	8	<u>(</u> 9)	(10	

- LUT using CLB (Distributed RAM)
- These LUT will be used for storing constants that change for each super layer.

🗐 Waveform - DEV:0	MyDe	viceO	(XC5VLX22	OT) UNIT	:0 MyILA	0 (ILA)												õ 🗖 🖉	X
Bus/Signal	х	0	393 	394 	395 	396 	397 	398 	399 	400	401 	402	403 	404	405 	406 	407 	408 	
⊶ <mark>/addr_s</mark>	5	5	14	<u>) 15</u>	<u>(</u> 0	χ_1_	<u>)</u> 2	Х з	X 4	<u> 5</u>	<u>)</u> 6	7	χ 8	<u>)</u> 9	<u>(10</u>	<u>) 11</u>	<u>/ 12</u>	<u> 13</u>	X
∽ <i>ј</i> ооит_	5	5	14	<u>(15</u>	<u>) 0</u>	χ_1_	<u>)</u> 2	Х 3	4	5	<u>)</u> 6	7	χ 8	<u>)</u> 9	<u>(10</u>	<u>) 11</u>	12	<u> 13</u>	X

- Signed integer multiplication using DSP slices in Virtex Chip
- Multiplication can be done in one clock

🕲 Waveform - DEV:0	MyDe	vice0 (XC5VLX220T)	UNIT:0 MyILAO (ILA)					• I	d' 🛛
Bus/Signal	х	0	585	586	587	588 	589 	590 	591	592 	
~/a_s	78	78	5	χ 4) з) <u> </u>	(1	χ	(-1	X -2 →	◪≏
∽/b_s	-78	-78	-5	X -4	X -3	X -2	(-1	X 0	(1	X>	
∽ /dout	-624.	-624.	-36	X -25	X -16	X -9	-4	X -1	0	χ <u>-1</u>	

- I am changing the C++ code into integer space step by step while writing the VHDL for each step.
- I will show how I transformed the phi into integer space.

- I need to change the phi input into integer space.
 To do this I need to know the Max and Min values of the phi input.
 - I need to choose how many integers I will use.

- I round the ϕ_{int} to make them integers.
- I am just quantizing $Ø_{float}$.

- Also, to have better resolution for the integer values, we transform \emptyset_i into $\emptyset_{i rel} = \emptyset_i \emptyset_{A3}$ (\emptyset_{A3} -Third superlayer for axial wires)
- If we do so the $Ø_{float max}$ will be smaller. Then $Ø_{int}$ will have better resolution.
- That is, the space between quantized Ø will be smaller.

Use timing information to reach z0 resolution ~o(4cm)

• To estimate the needed timing information resolution for z0 resolution to be 4cm, I made an input track for the 3d trigger and smeared them 2000 times.



Red: Smeared track Blue: Actual track

Use timing information to reach z0 resolution ~o(4cm) (cont'd)

• Results (when drift speed is $40\mu m/ns$)

Pt = 2 GeV/c

Time_rms(ns)	z0_rms(cm)
22.5	2.310
27.5	2.823
35	3.594
40	4.107

Pt = 0.5 GeV/c

Time_rms(ns)	z0_rms(cm)
22.5	2.349
27.5	2.871
35	3.655
40	4.177

Use timing information to reach z0 resolution ~o(4cm) (cont'd)

- The results show we need ~38ns time information resolution when the drift speed is $40\mu m/ns$
- This was done with float numbers in the fitter code, so we will do it again after the code is changed into integer space.
- Further studies on how to get the time information resolution is being done by KyungTae.

Summary

- Basf2 CDC geometry has been implemented and tested in the 3D fitter.
- We were able to improve the 3D fitter.
- We made toy VHDL modules for the fitter.
- We are changing the code into integer space.
- We were able to calculate the needed time resolution for z0 to be ~O(4cm).



- Basic equations to get axial wire position.
 - $-p_T(\frac{GeV}{c}) = 0.3 * z(e) * B(T) * \rho(m) = 0.3 * 1.5 * \rho$
 - Simple perfect track : $x^2 + (y \rho)^2 = \rho^2$
 - CDC TS position: $x^2 + y^2 = r^2$



Blue: CDC super layers Red: Perfect Track

• Equation to calculate stereo wire position



 θ_{st} is greatly exaggerated

• Equation to calculate stereo wire position



- Equation to get z.
 - Using data from the Belle tsim, we have found the relation between r and z.
 - -z = -0.09358 * r $-z theta = \frac{\pi}{2} tan(\frac{z}{r} slope)$



• Now we can calculate the stereo wire position.

• Results

