

status of R&D for CDC readout

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- introduction
 - reminder of last B2GM
- current status
 - study with modified prototype for submission of new ASIC

introduction

AMP shaper discriminator chip
8ch/chip developed for Belle II CDC

24ch connector

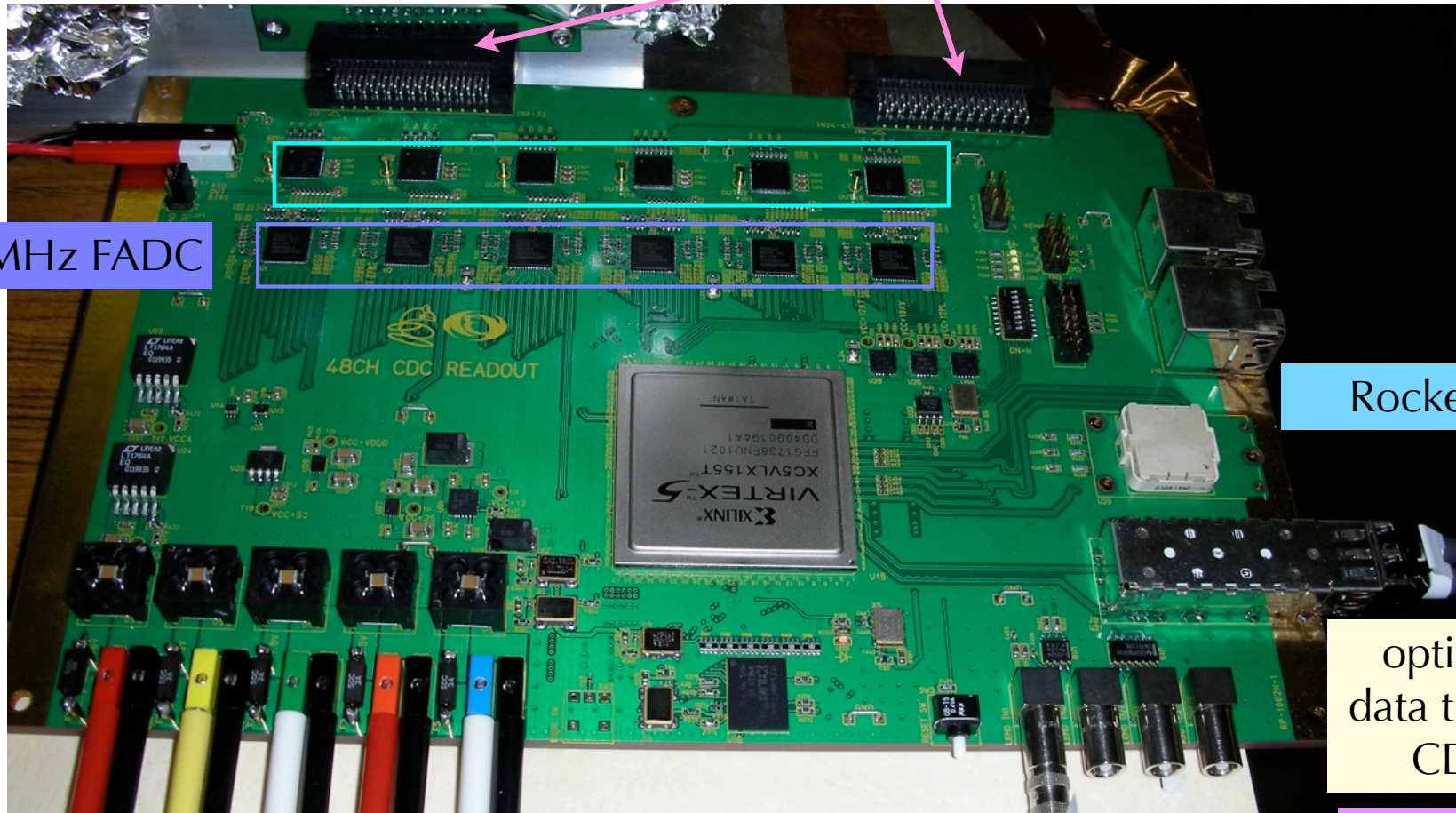
32MHz FADC

Rocket I/O

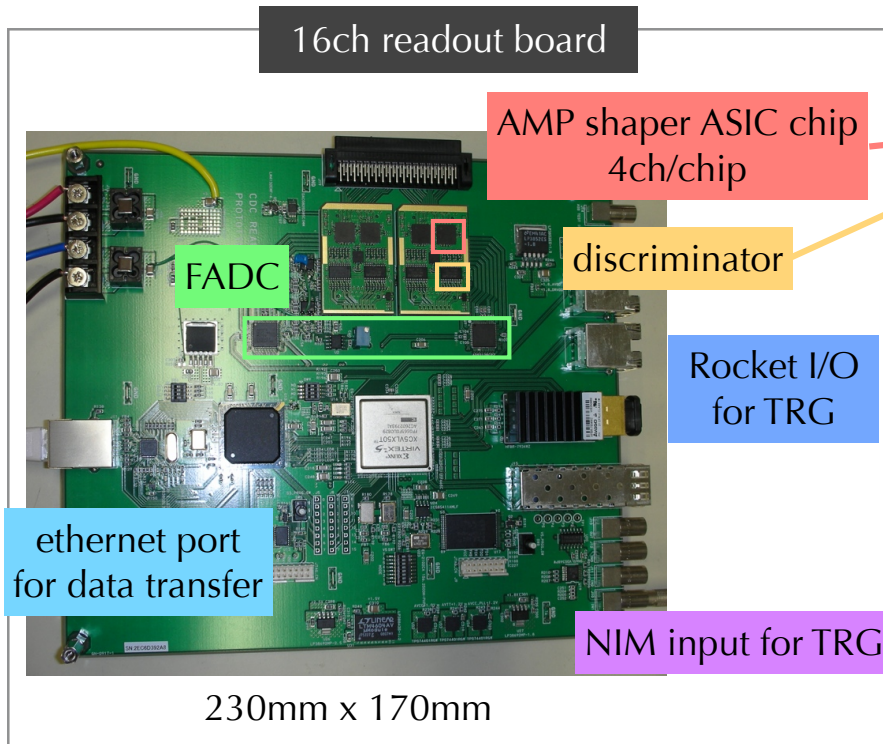
optical fiber
data transfer for
CDC test

NIM input
for test pulse

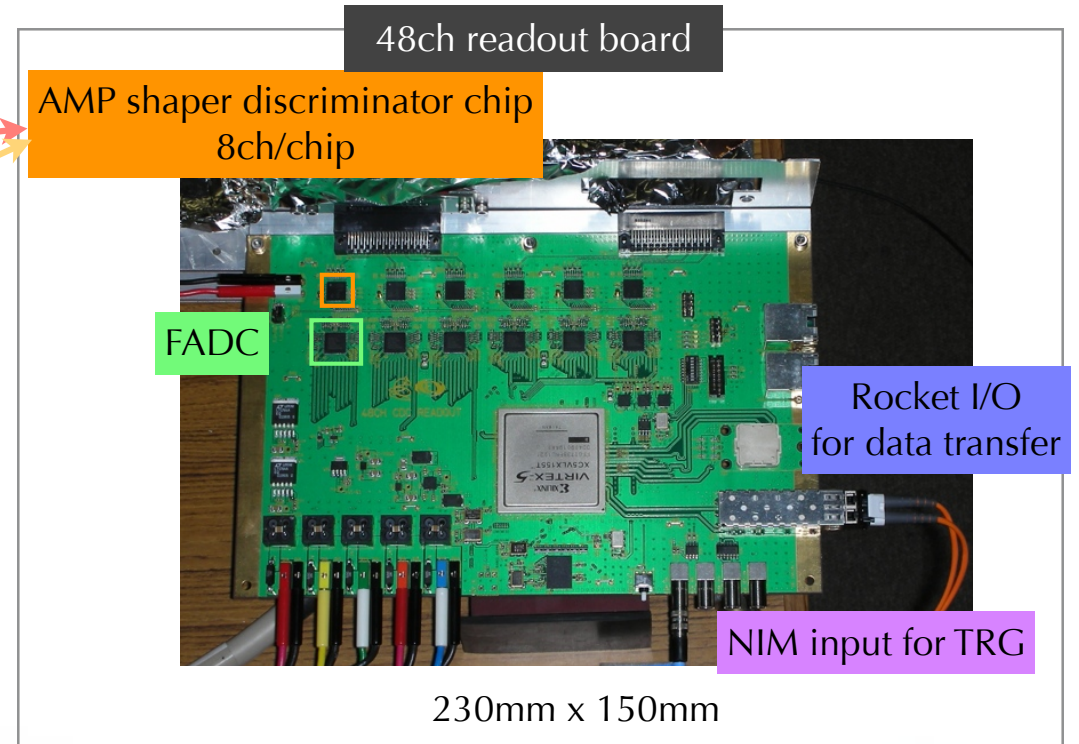
230mm x 150mm NIM input for TRG



comparison



gain 1.4V/pC



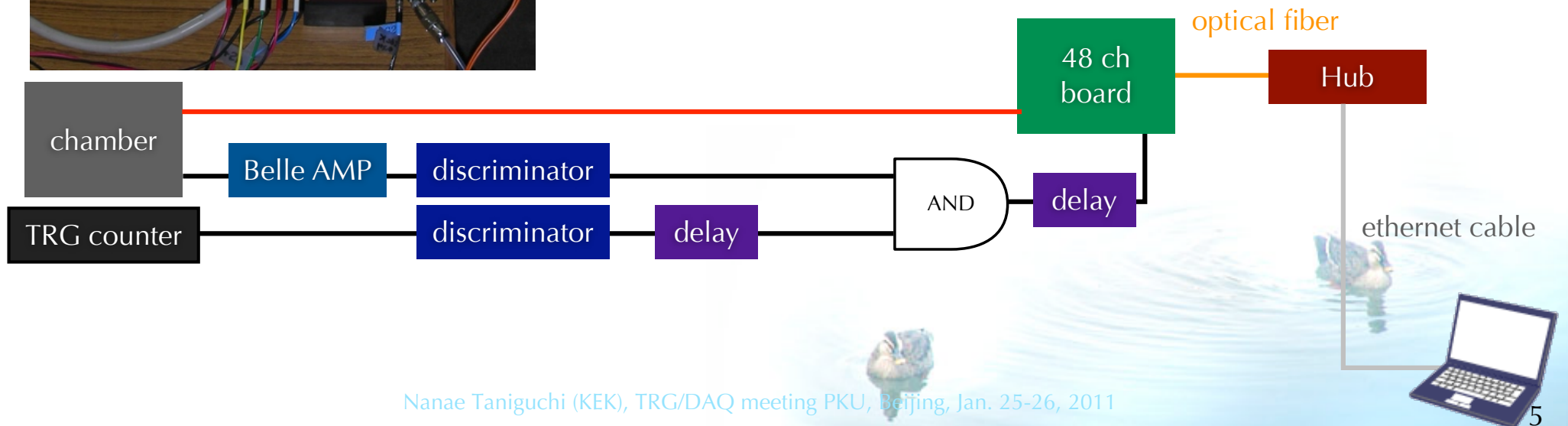
gain 1.1V/pC for analog
19V/pC for digital

Chamber



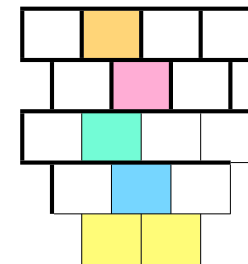
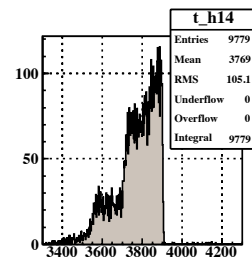
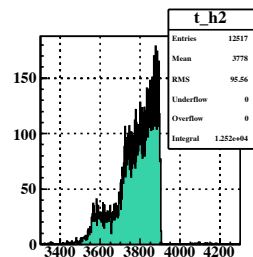
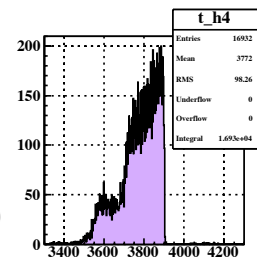
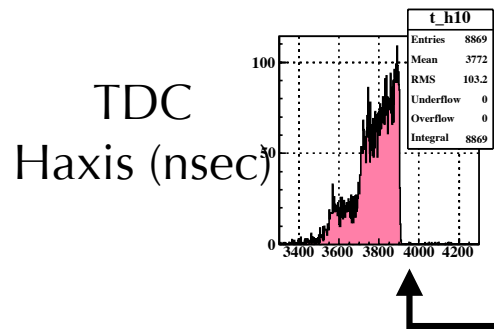
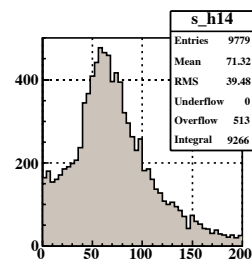
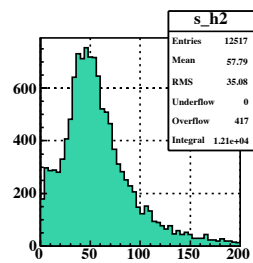
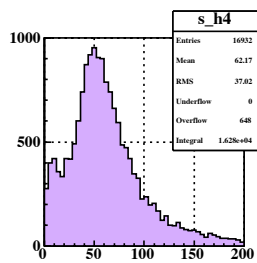
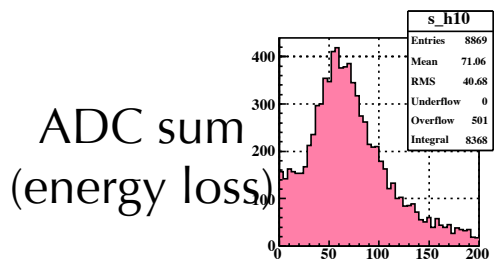
set up

- same way as previous test
 - 5-layer test chamber, 14ch can be used
 - same gas (He(50):C₂H₆(50))
 - same FPGA program (for ch16)
 - same analysis

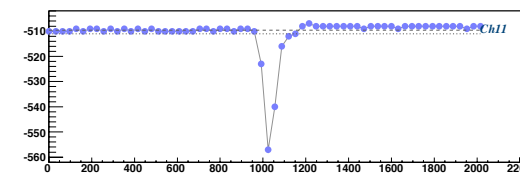
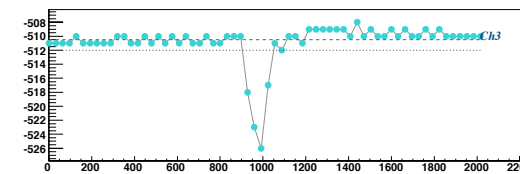
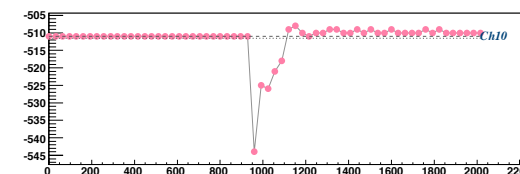
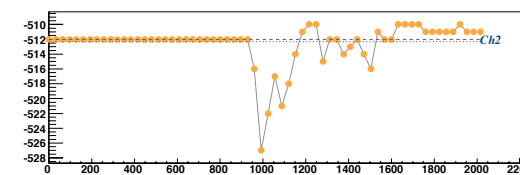


HV=2.3kV
He:C₂H₆
cosmic

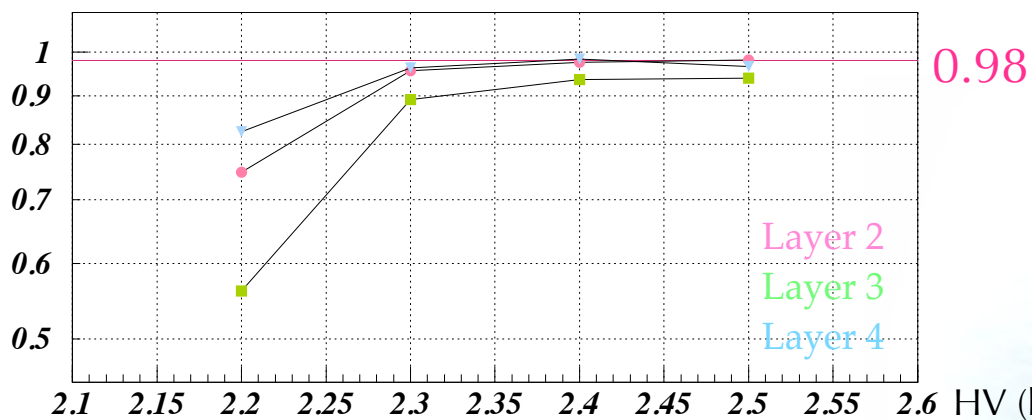
cosmic ray data



waveform sampling



efficiency



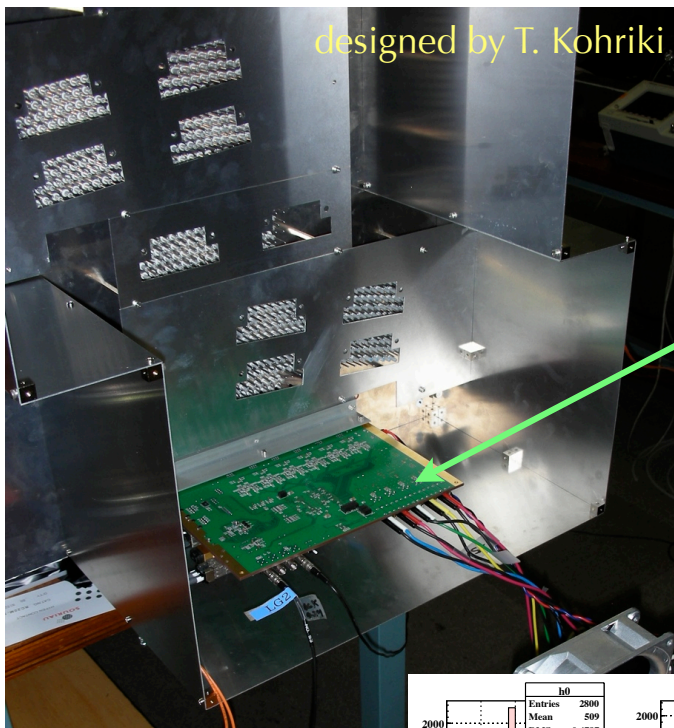
designed by T. Kohriki

test chamber for 3D TRG study
(5 super-layers, AUAVA, 2m long)

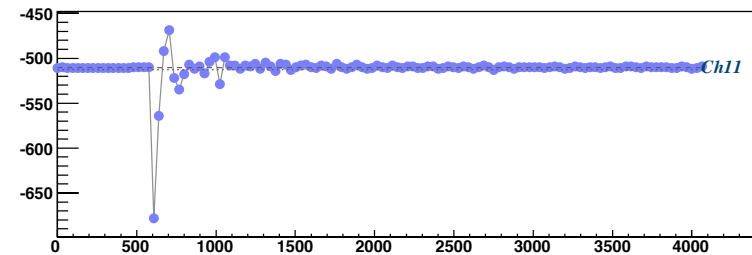
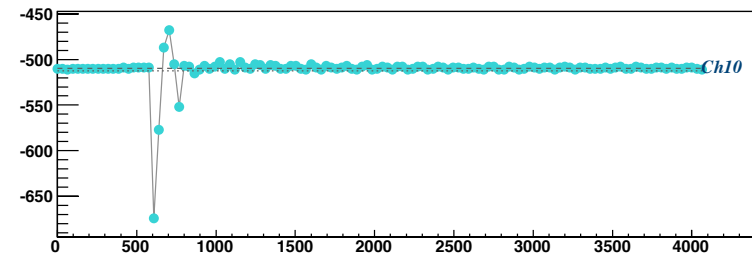
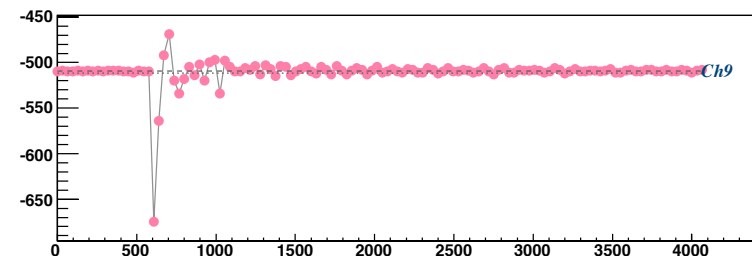
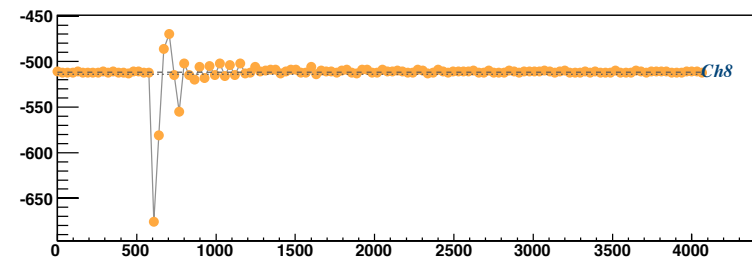
November 12, 2010

48ch board

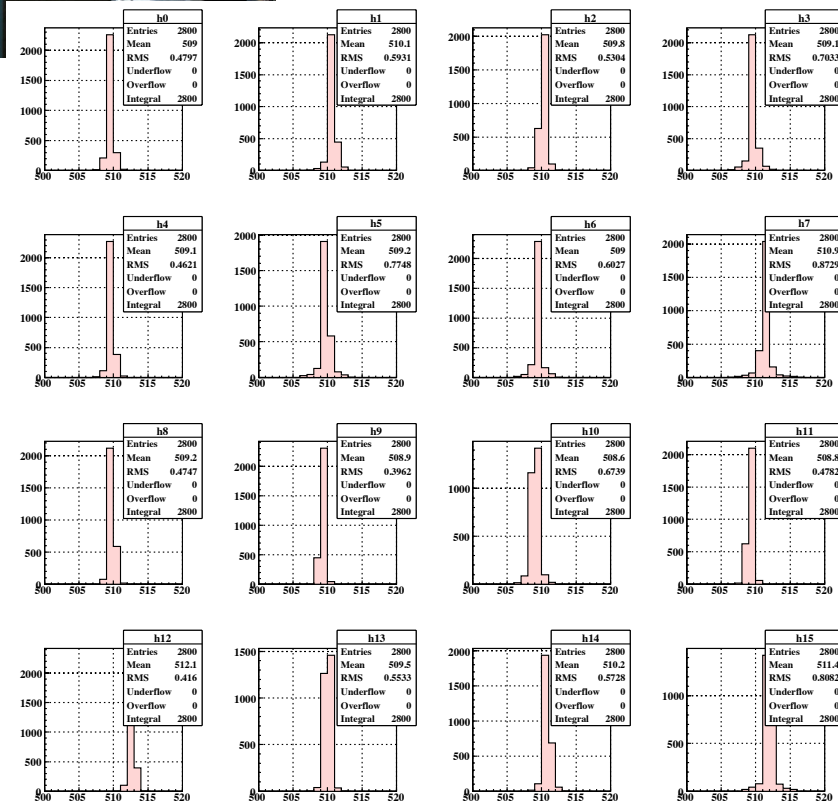
good test for assembling of
real Belle II CDC.



waveform sampling of test pulse



pedestal (ch0-15)



status and problem

	STATUS
pedestal	better
common noise	OK
TDC distribution	looks OK
energy loss distribution	looks OK
signal shape (after pulse)	OK
cross talk	slightly large
efficiency	lower

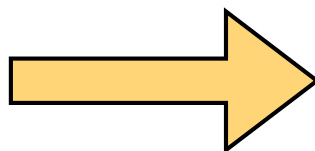
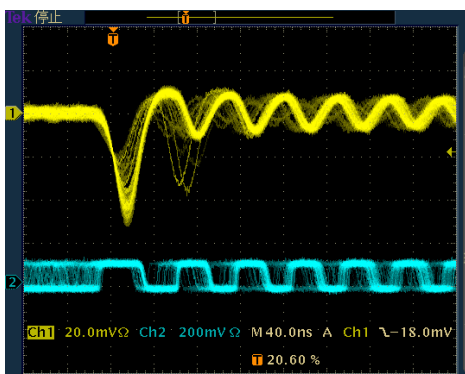
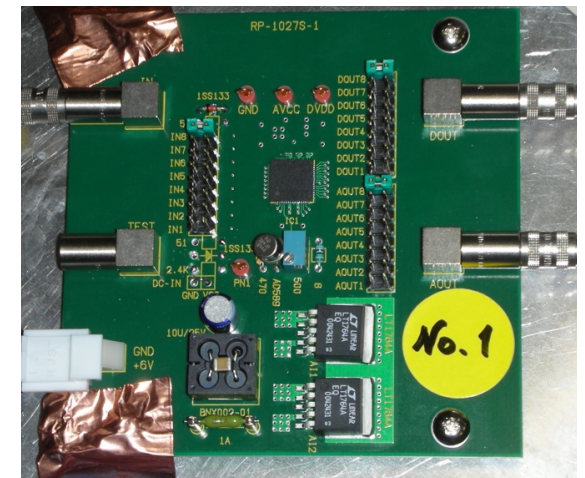
- lower gain
 - gain loss due to temporary circuit for adjustment
- lower efficiency
 - high threshold against low gain
 - not able to decrease threshold because of unstable digital out
- larger cross talk
 - sensitive against noise due to chip layout

current status

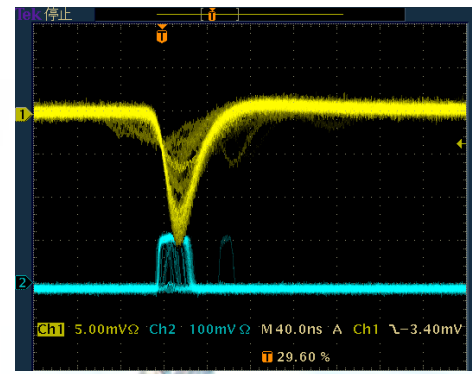
- modification to recover gain
 - try to various input capacitance of 48ch board
 - Finally 0Ω (with more modification)
 - try to adjust supply voltage to ASIC with 1-chip test board
- study and discussion about parameters of new ASIC chip with electronics group
- FPGA firmware for 48ch

reminder

- Study with 1-chip board (spring, 2010)
 - ch0 problem
 - 50pF capacitance on input line
 - decide the layout of 48ch board

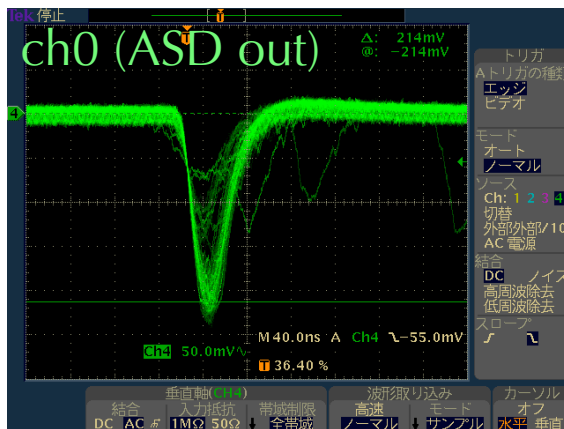


signal shape is good
loss gain

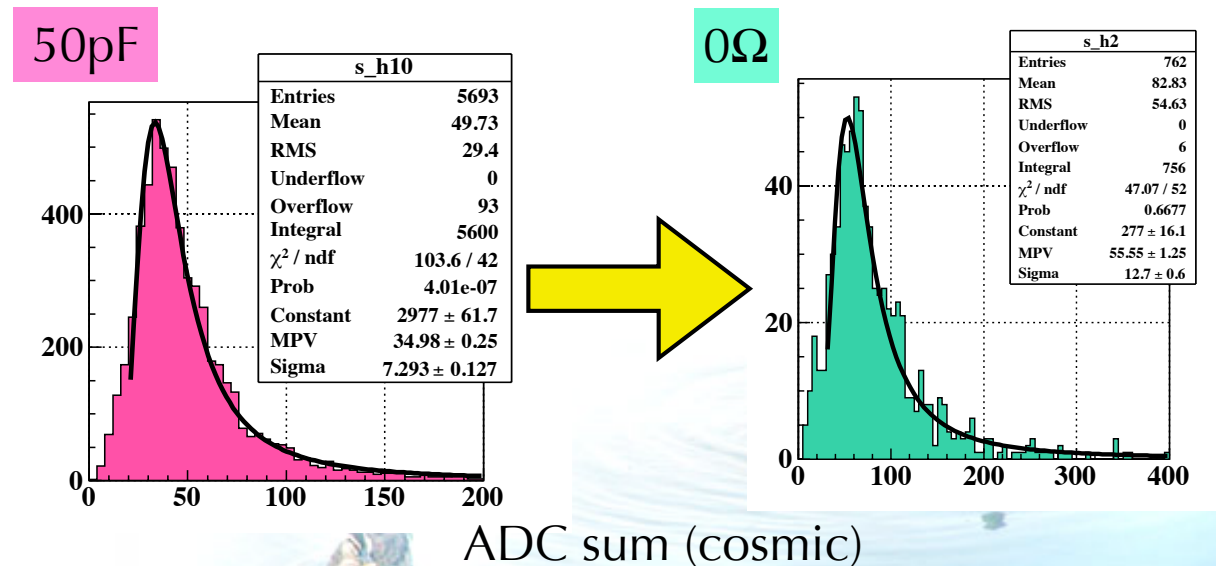


0Ω on input

- Study with 48ch board (Nov.~Dec.,2010)
 - try various capacitance on input line → 0Ω is O.K !
 - gain recover ~ x1.5



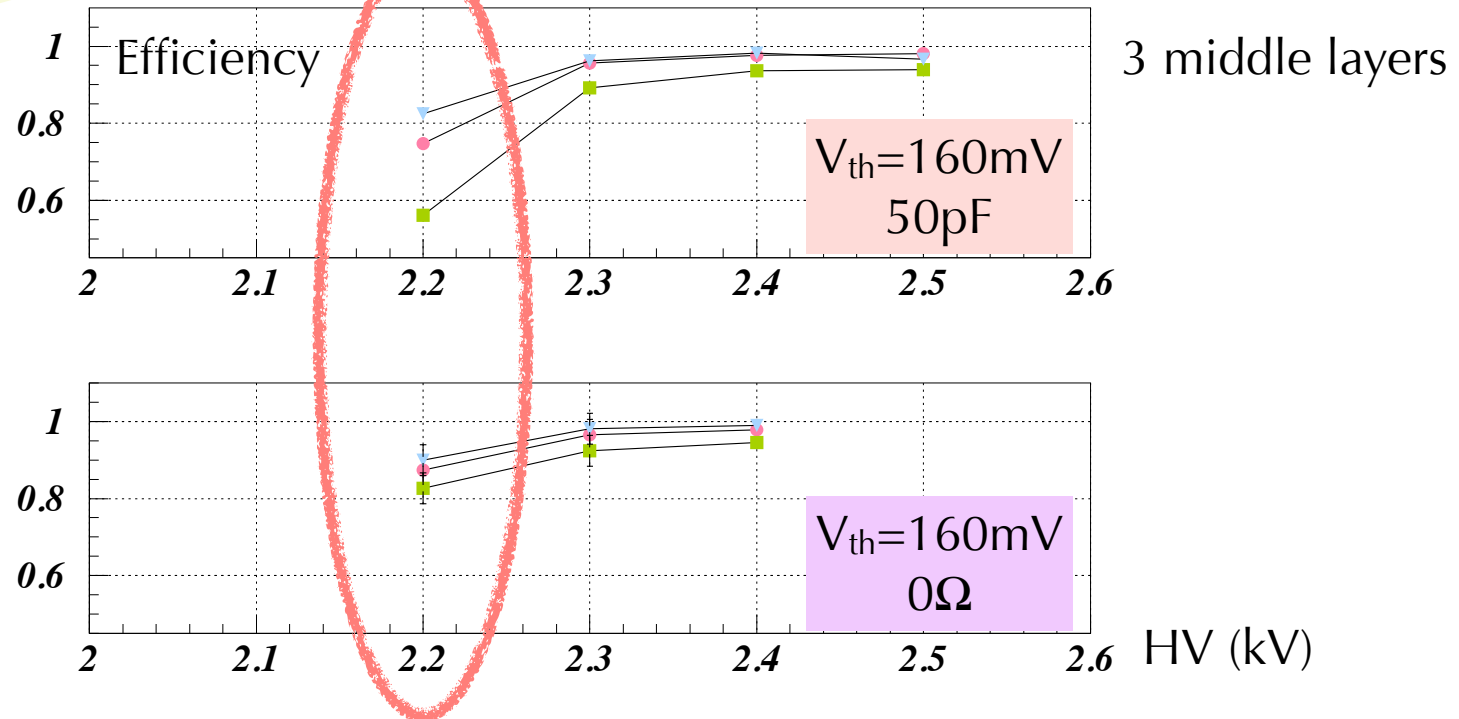
chamber signal (X-ray)



ADC sum (cosmic)

0Ω on input

cosmic ray data



- target chamber HV is 2.2kV
 - lower than Belle, for safe operation under high rate
- proper operation voltage for ASIC(ver.FY2011)
 - 1.3~1.5 gain recovery from study using 1-chip board
 - expect to improve efficiency

conclusion

- 48ch board works
- parameters are almost determined
 - simulation for ASIC (and surrounding circuit) under progress
 - some problem will be solved in next version
 - modify all input line with 0Ω
- New ASIC chip will be delivered before summer
 - also modify 1-chip test board for better study



FPGA firmware

- same program as 16ch board (~Nov.2010)
- quick test of 48ch firmware (Dec.2010~)
 - debug mode under progress
 - suppressed mode (Feb.~ March, 2011)

readout mode

5th B2GM, Apr. 2010

cosmic ray data

Readout mode

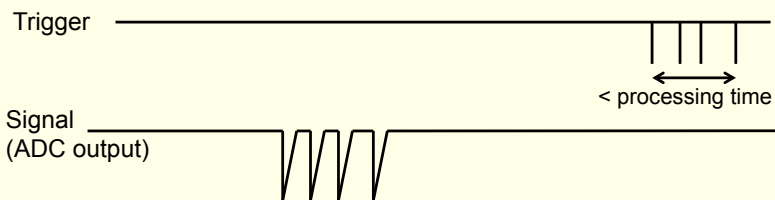
- Raw data mode
 - Useful for debugging or an initial test
 - All ADC and TDC data are transferred
 - Large data size ~ several hundreds of bytes
- Suppressed data mode
 - Normal mode
 - Summed ADC and TDC data are transferred
 - Small data size ~ several tens of bytes

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Multi-hit

Max. 4 events can be received during data processing

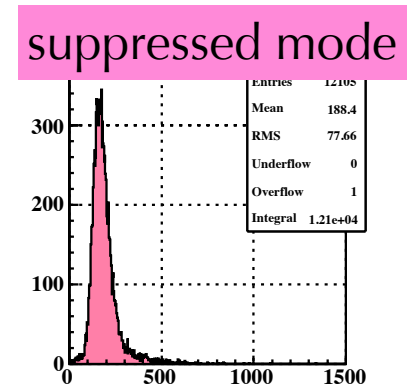
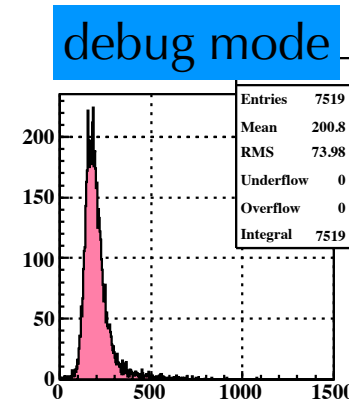
Processing time depend on the number of hit channels, ~ few usec



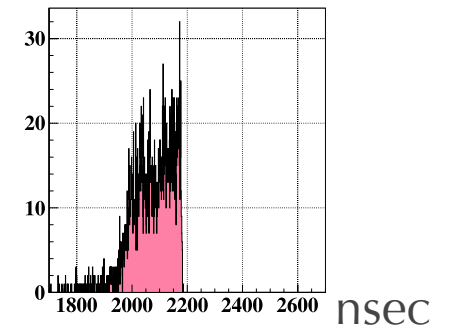
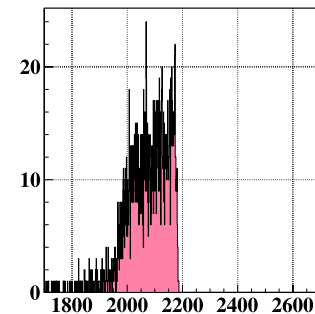
Only the suppressed data mode

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ADC sum

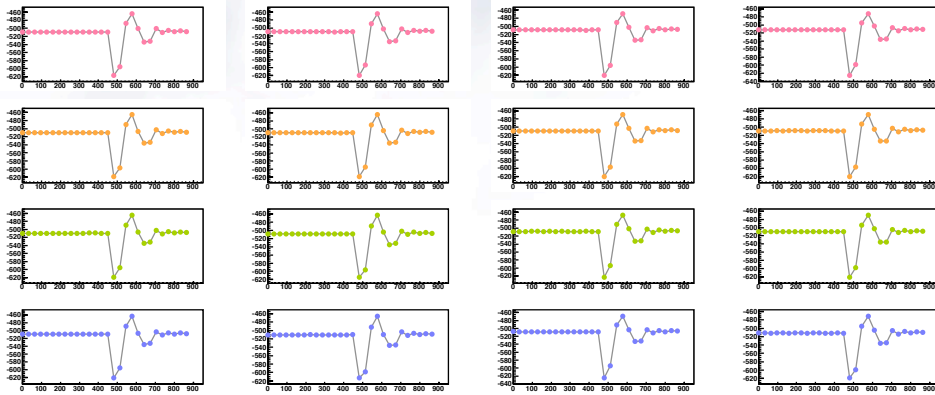


TDC



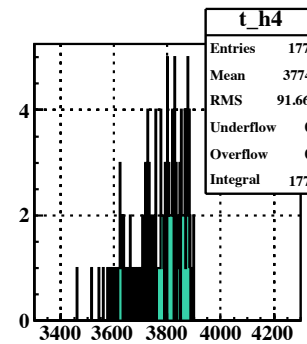
- debug mode (no buffer)
 - $30/10^4$ (0.3%) events are lost at the event rate of 20 Hz
- suppressed mode
 - all event are received at the same condition

quick test of 48ch firmware

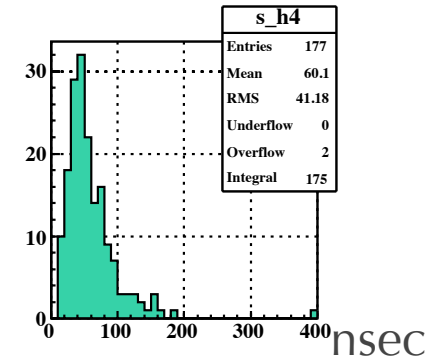


confirm test pulse for all 48 ch

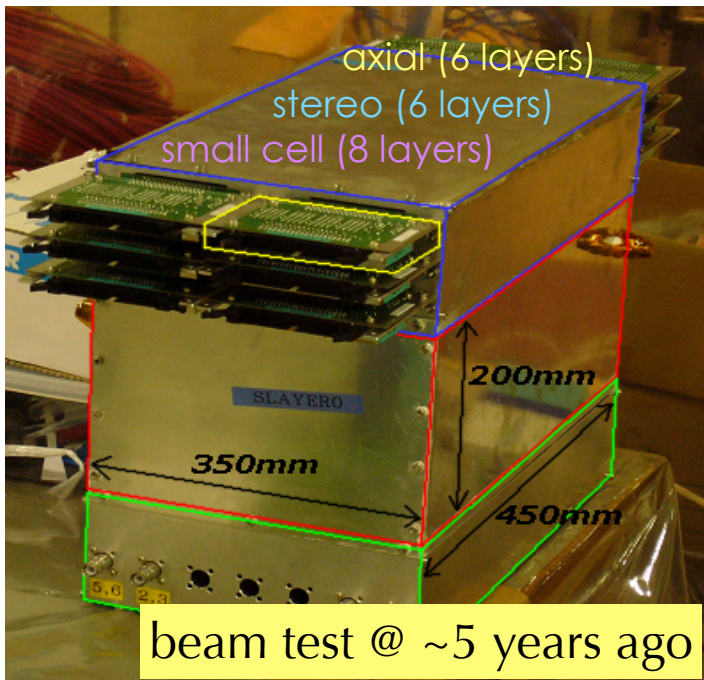
TDC



ADC sum



cosmic ray data for 14ch



beam test @ ~5 years ago (KEK), TRG/DAQ r

plan to repair 20-layers test chamber with 192ch

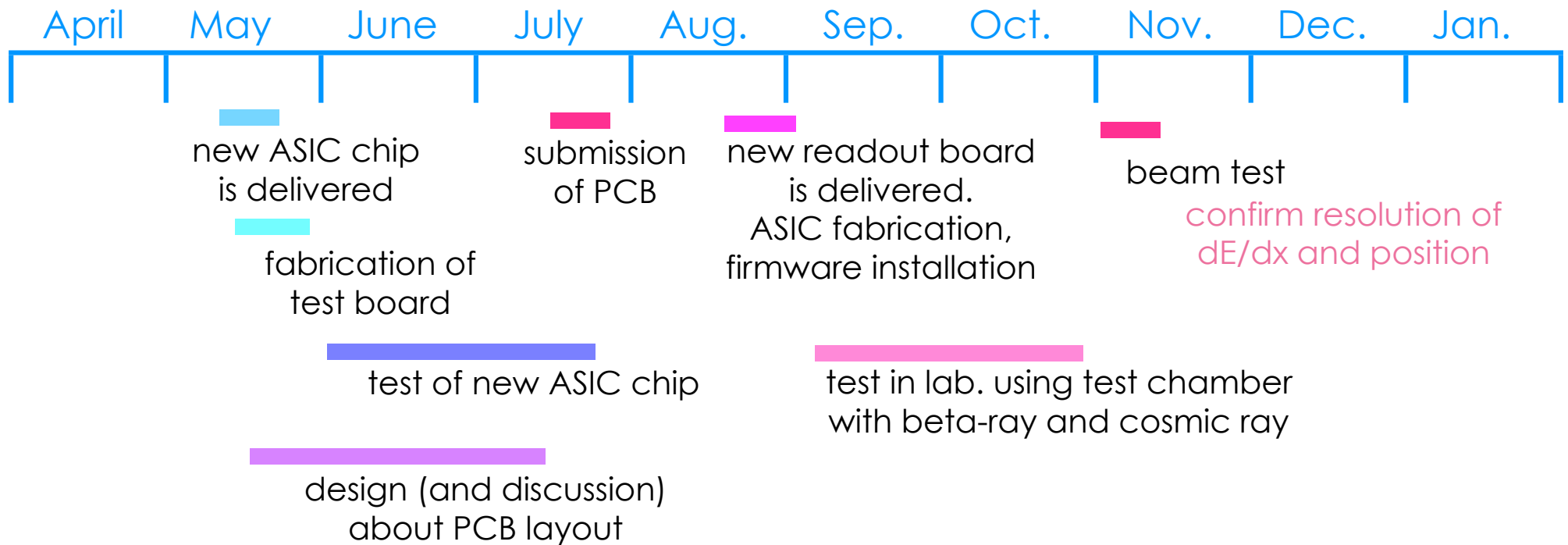
- HV check
- replace signal cables
- ↓
- test with debug mode
- ↓
- test with suppressed mode

Feb. ~
March



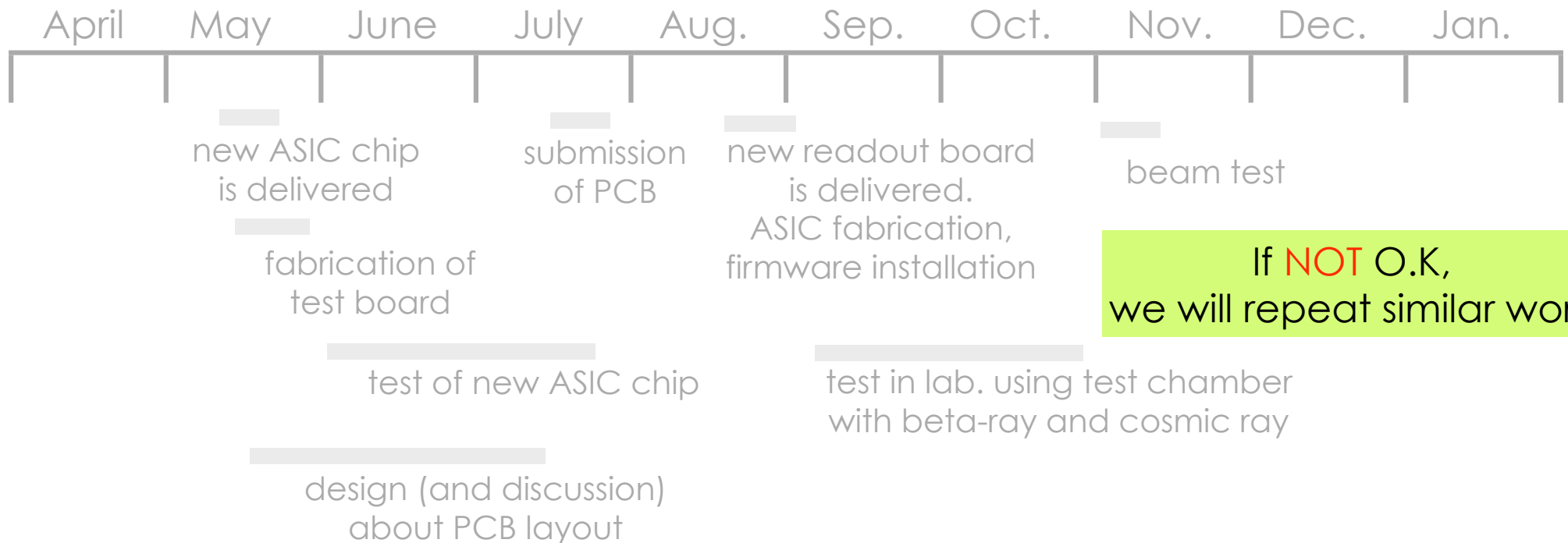
beam test for new 48ch board (FY2011)

R&D schedule on 2011



R&D schedule on 2011

If performance is O.K,
ver. 2011 become final version

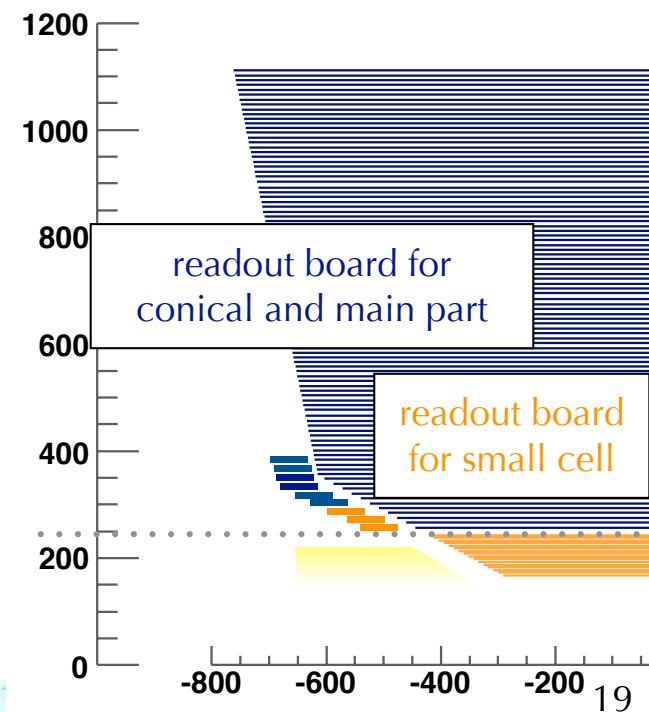
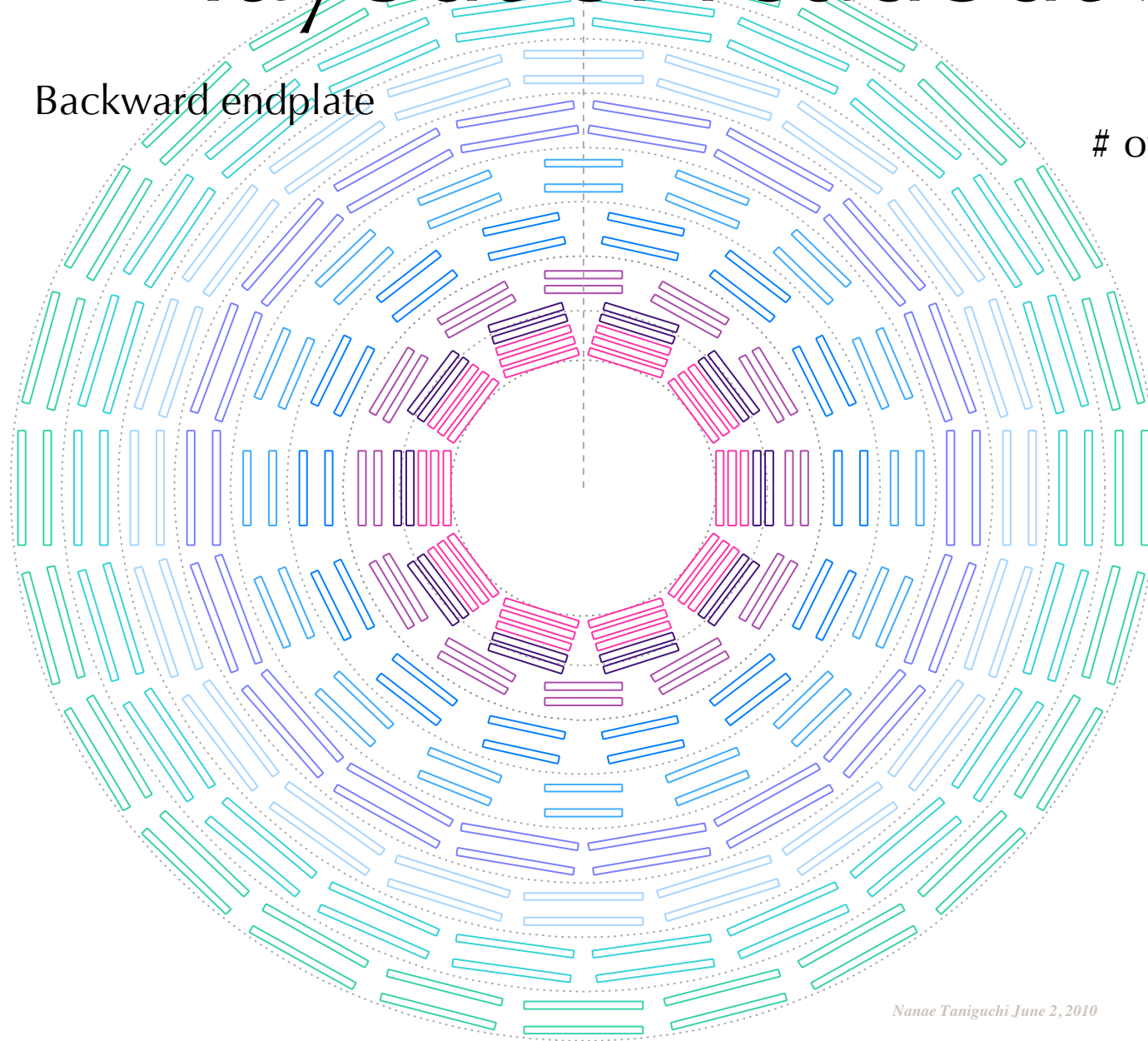


If **NOT** O.K,
we will repeat similar work

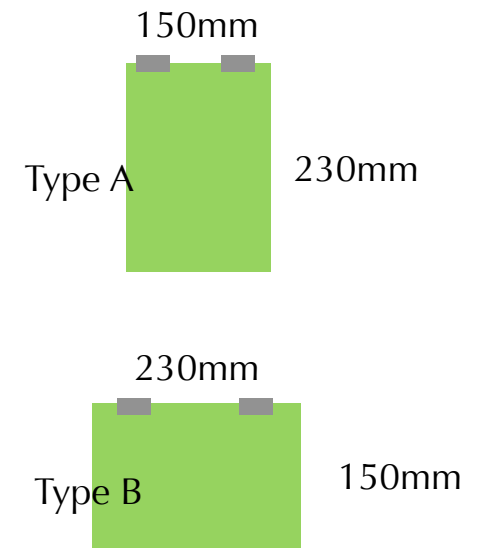
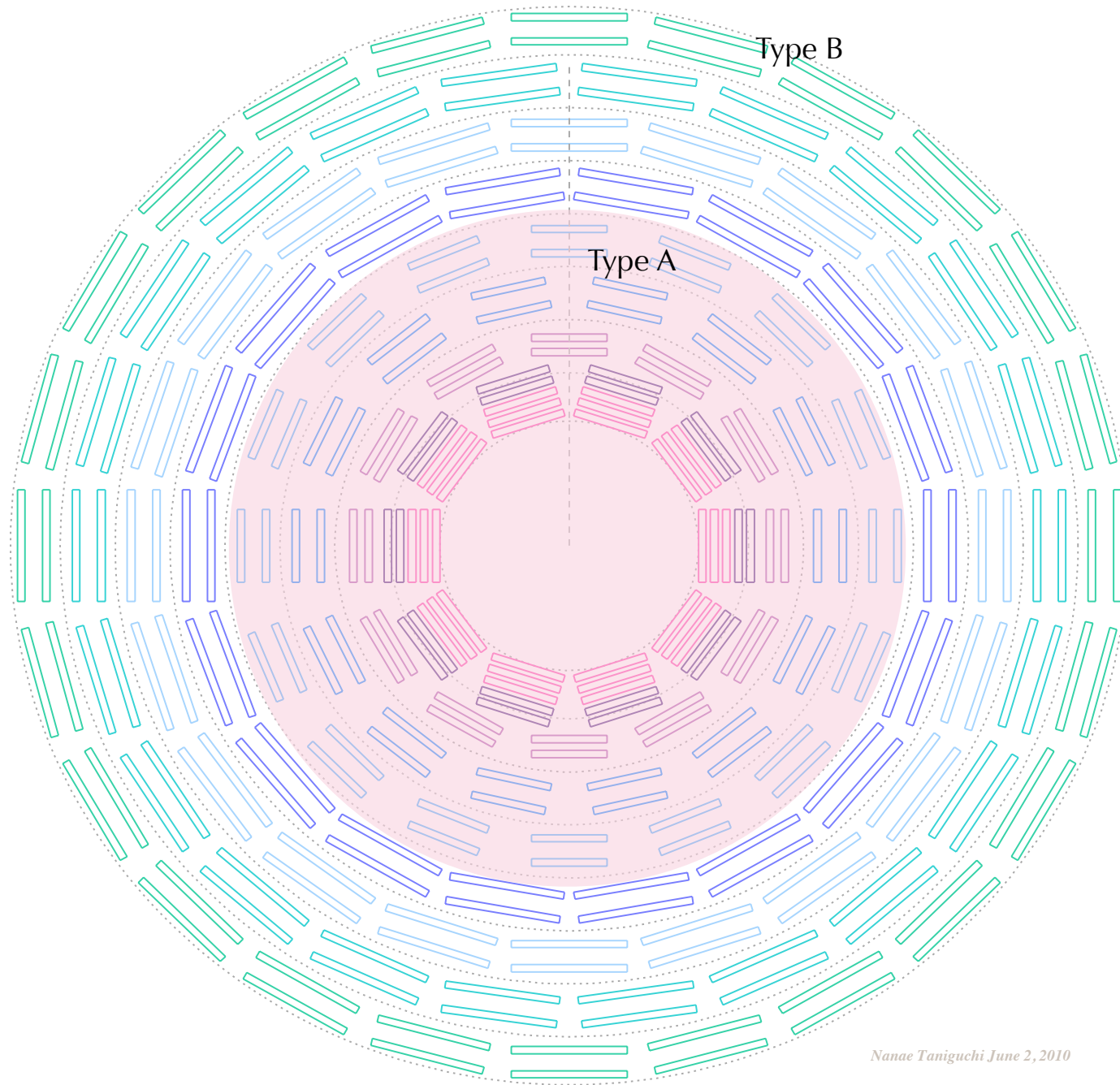
layout of readout board

Backward endplate

of readout board = 302 (Bwd.)



Nanae Taniguchi June 2, 2010



Nanae Taniguchi June 2, 2010



power supply

	Voltage[V]	current[A] (48ch)	x300 [A]	x350 [A]
digital	+1.0	1.74	522	609
	+1.8	2.25	675	787.5
	+3.3	1.0	300	350
NIM	-5.0	0.03	9	10.5
ASIC	+4.0(5.0)	0.23	69	80.5
		5.25	1575	1837.5

~10W/board

power supply



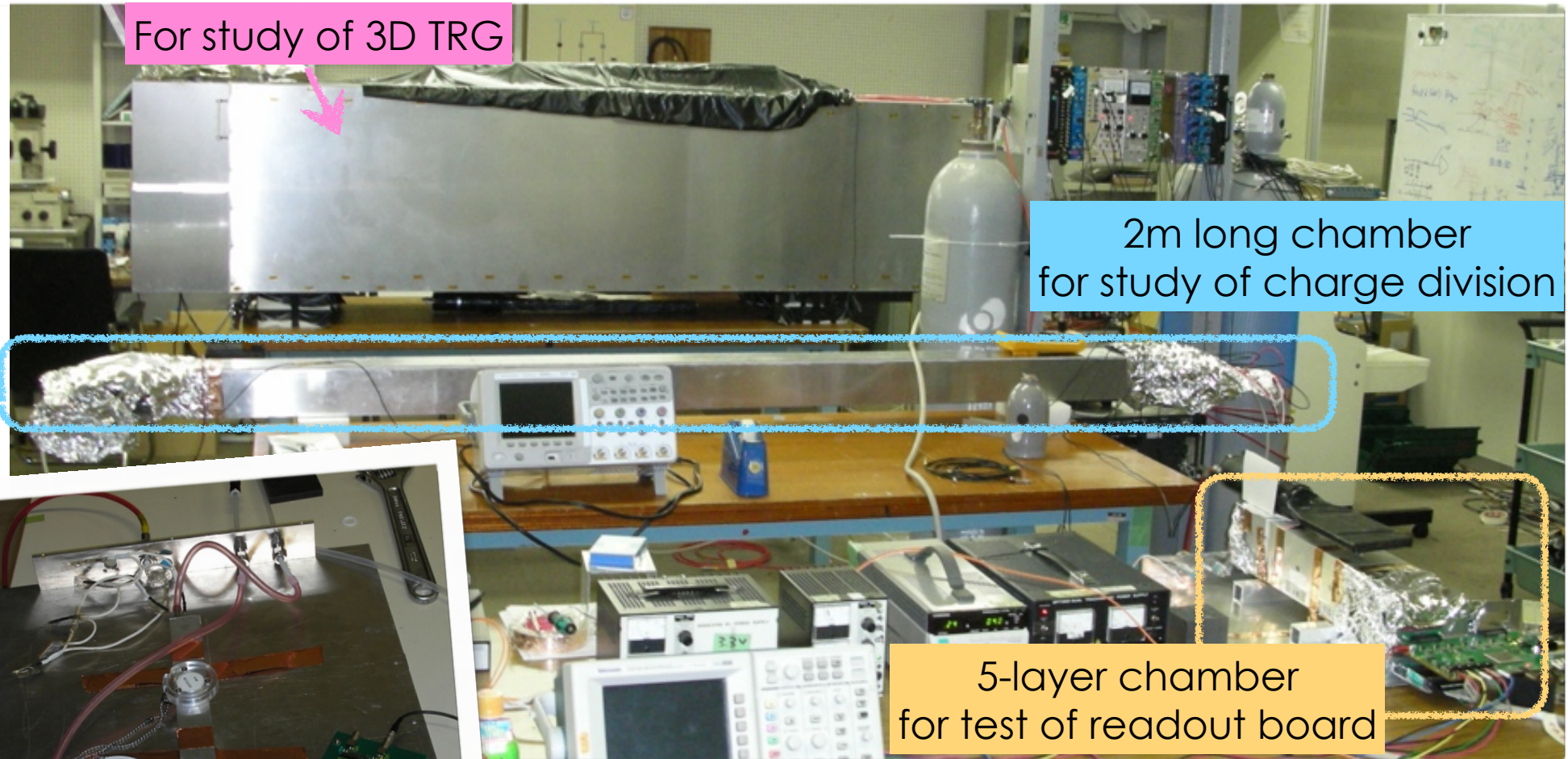
5V - 100A ~67 module

- reuse power supply module of Belle shaper-QT
 - after overhaul and modification
- checking in detail
 - company people have brought a module

summary

- 48ch readout board works (although several problem)
 - learned a lot of things and found solution
 - problem will be solved in next prototype
 - new ASIC (Spring, 2011), new board (Summer ~ Autumn)
- FPGA firmware in progress
 - further study with 20-layers test chamber
- layout and power supply for readout board under progress

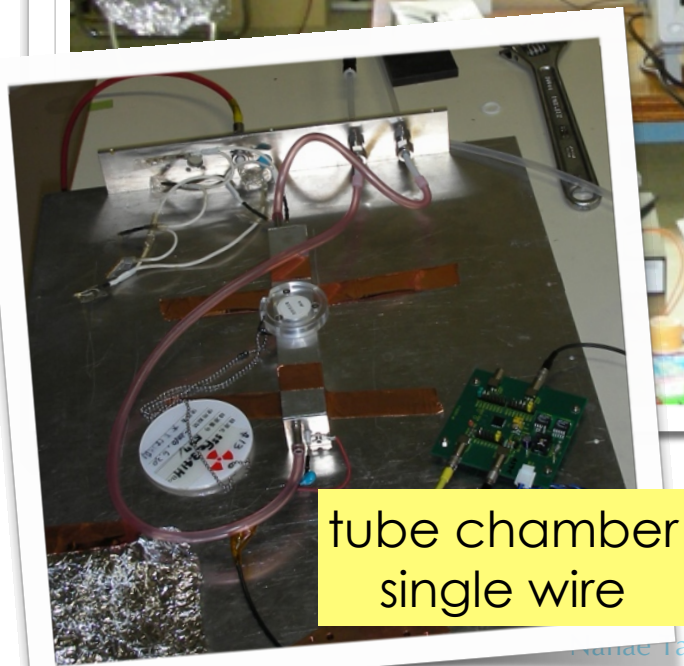
chamber family



For study of 3D TRG

2m long chamber
for study of charge division

5-layer chamber
for test of readout board



tube chamber
single wire

backup slides



cabling

NOT decided yet

