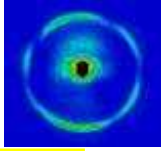


Status of the Aerogel RICH Readout

S. Nishida

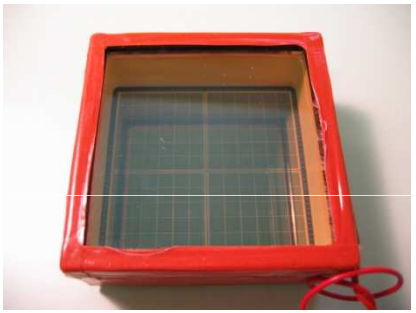
KEK

Belle II Trigger DAQ Workshop in Beijing

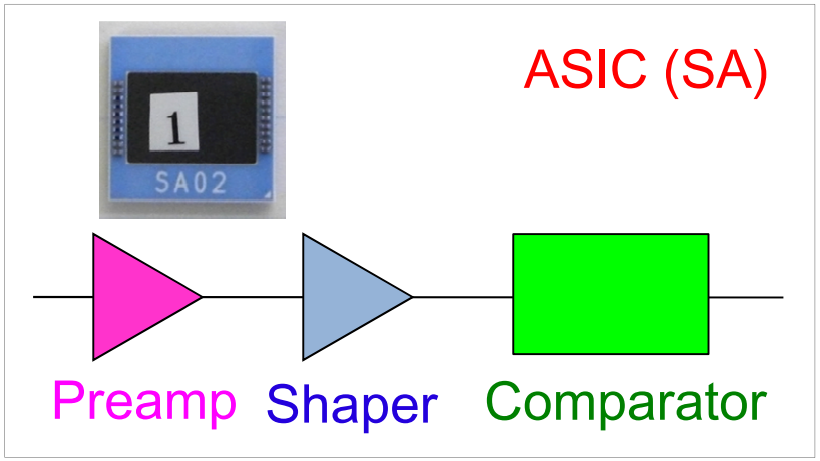
Jan 25, 2011

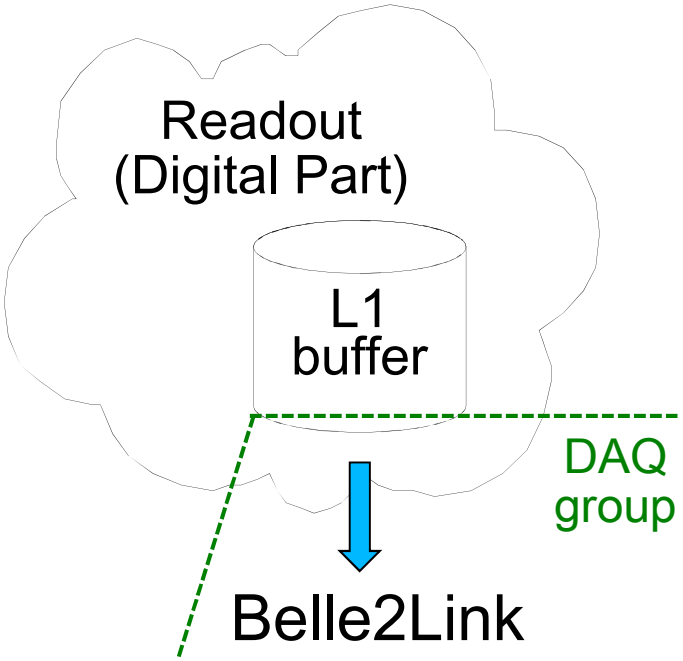
Introduction

Aerogel RICH Readout (Front end electronics)

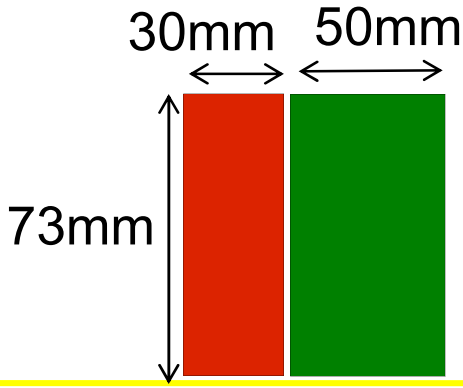


HAPD (144ch)





- Total ~ 500 HAPDs.
- ASIC: 36ch per chip (i.e. 4 chip / HAPD).
- Quite limited space (~5cm) behind HAPD.
- ~500 Belle2Link is too many : need Merger.



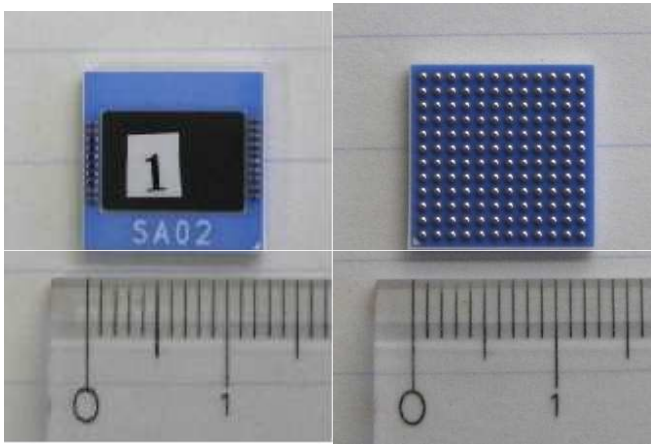
ASIC History

- 4 series of test productions for evaluation (S01-S04) at VDEC (2002-2005).
- New series of ASIC for the real application at Belle2: SA01-SA03.

SA01 (2007)

- 12 ch / chip; QFP package.
- Good performance. Succeeded to detect Cherenkov ring at the beam test.
- Minor problem: gain too high.

SA02 (2009)



- 36 ch / chip; LTCC package.
- Good performance (at the test bench).
- Gain = 1/4 of SA01.

SA03 (2011)

SA03

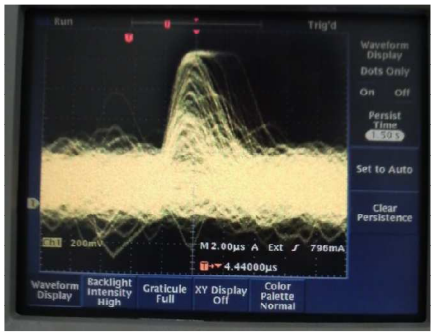
SA03 (2011) : (hopefully) the final version, pins compatible with SA02.

Modification from SA02:

- Shorter shaping time : 250-1000ns (SA02) → 100-250ns (SA03)
- Radiation (Single Event Effect) torellance.
  - ✓ SEE tolerant control register by DICE (Dual interlocked cell).
  - ✓ Parameter (non-destructive) readout.

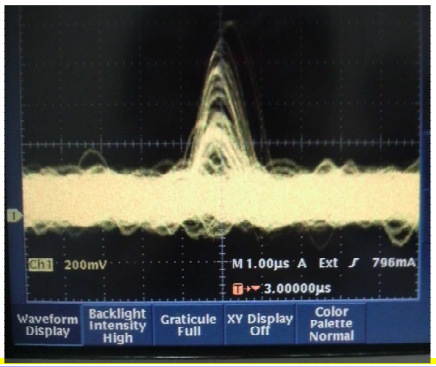
One concern in HAPD is radiation.

- Leakage current → ~10 μA.
- 250ns shaping time is necessary for HAPD after 10^{12} n/cm^2 (~10year) neutron irradiation.
- Target ~100ns.



shaping time 1000ns

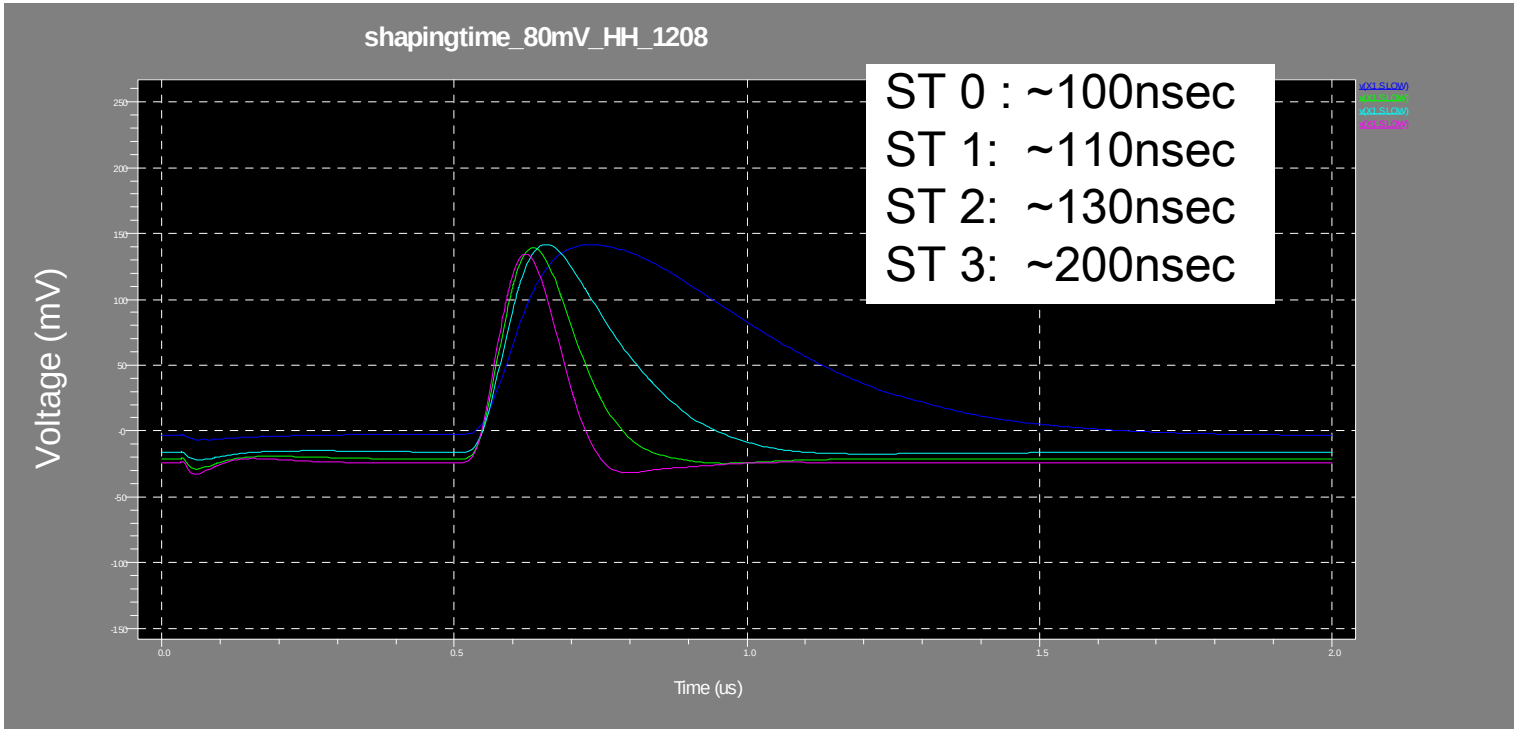
after 5×10^{11} neutron/cm^2 (~ 5 years) irradiation



shaping time 250ns

SA03

Simulation
O.K.

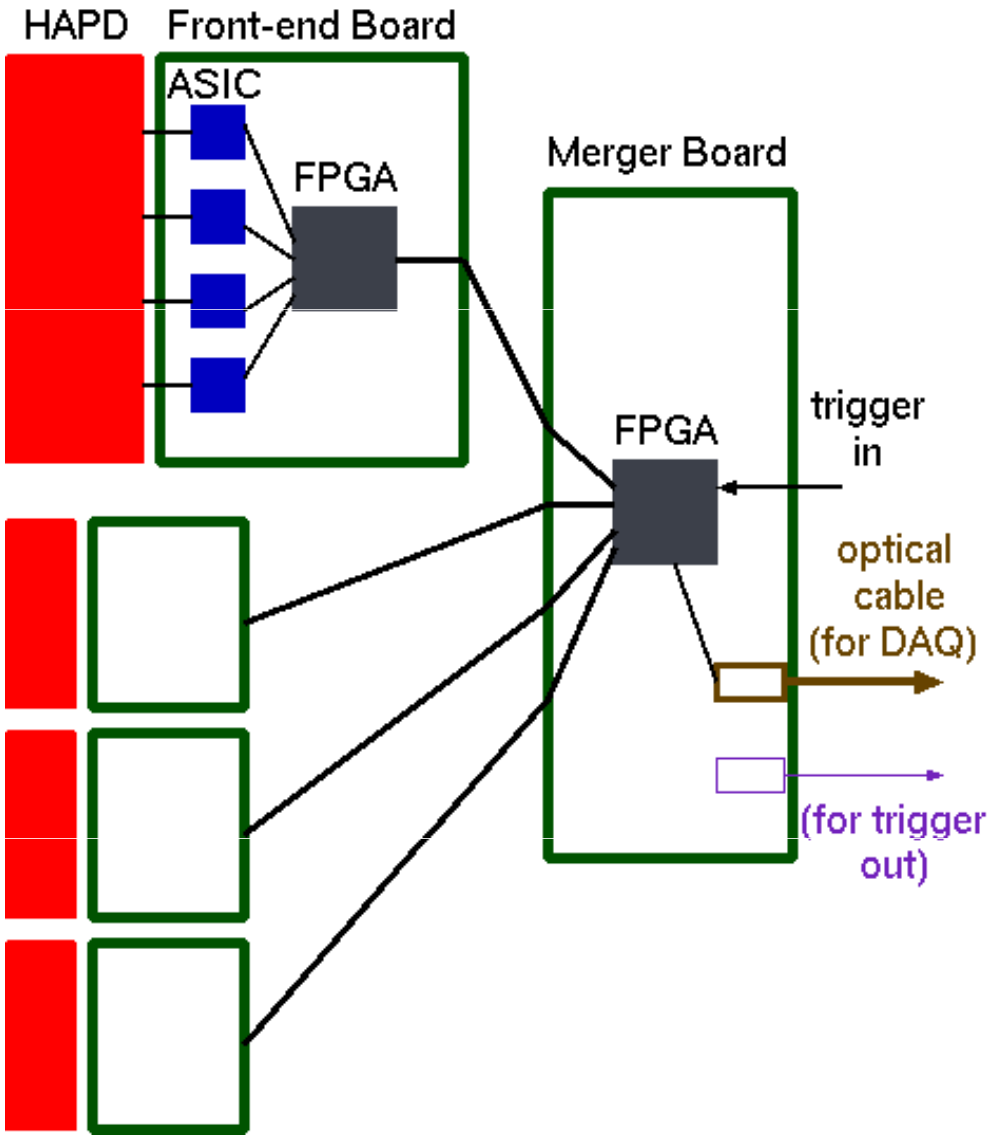


[Takagaki (TMU)]

Plan

- Layout (@ Digian-technology) : Feb / Mar.
- Test production @ TSMC : next fiscal year.
- Mass production (bare chip) ~2000 chips.
  - ✓ At TSMC or X-FAB: depends on the cost.
  - ✓ Rough estimation 6M yen.
- LTCC Packaging.

Aerogel RICH Electronics

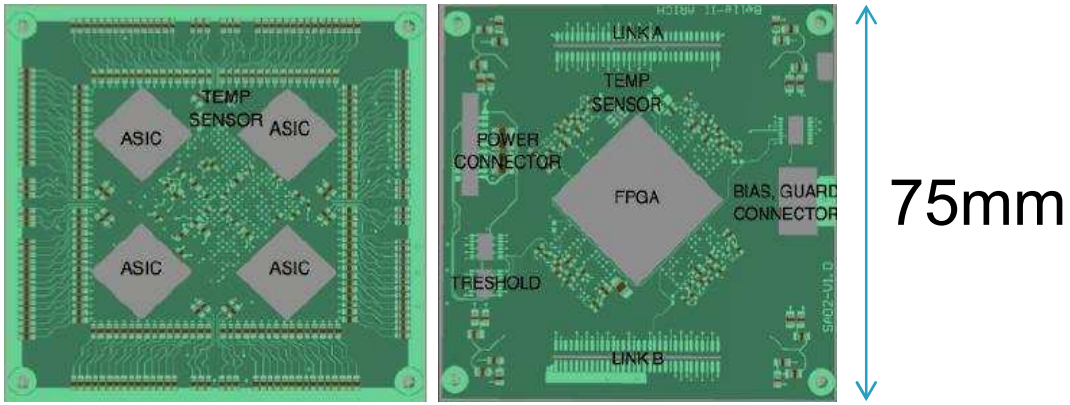


- Front-end (FE) board : 4 ASICs and 1 FPGA to read out 1 HAPD.
- Merger board collects hit data from ~ 4 HAPDs (FE boards).
- Merger board has the interface to Belle2Link (i.e. Merger board is the "front-end" board in terms of unified DAQ).
- Conservative raw data rate = 100 Mb/HAPD.
  - ✓ 16 b/ch is assumed.
  - ✓ Zero-suppression is requested at merger board (or FE board).

Front-end Board

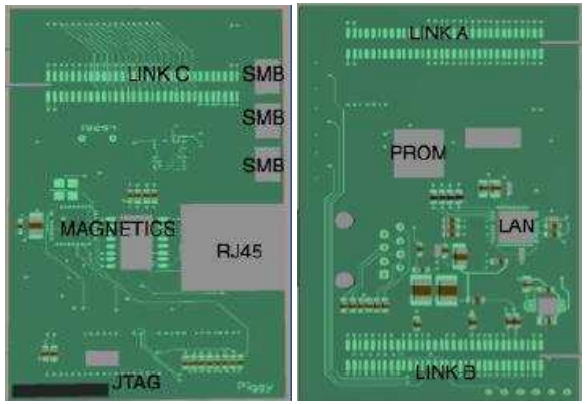
- Prototype FE board is developed at Ljubljana (by A. Seljak).
  - ✓ Main board with 4 SA02 ASICs and 1 FPGA (Spartan6).
    - ➢ 12 layer board.
  - ✓ Piggy board for SiTCP (for standalone readout).
  - ✓ Production at Elgoline (Slovenia).

main board



top bottom

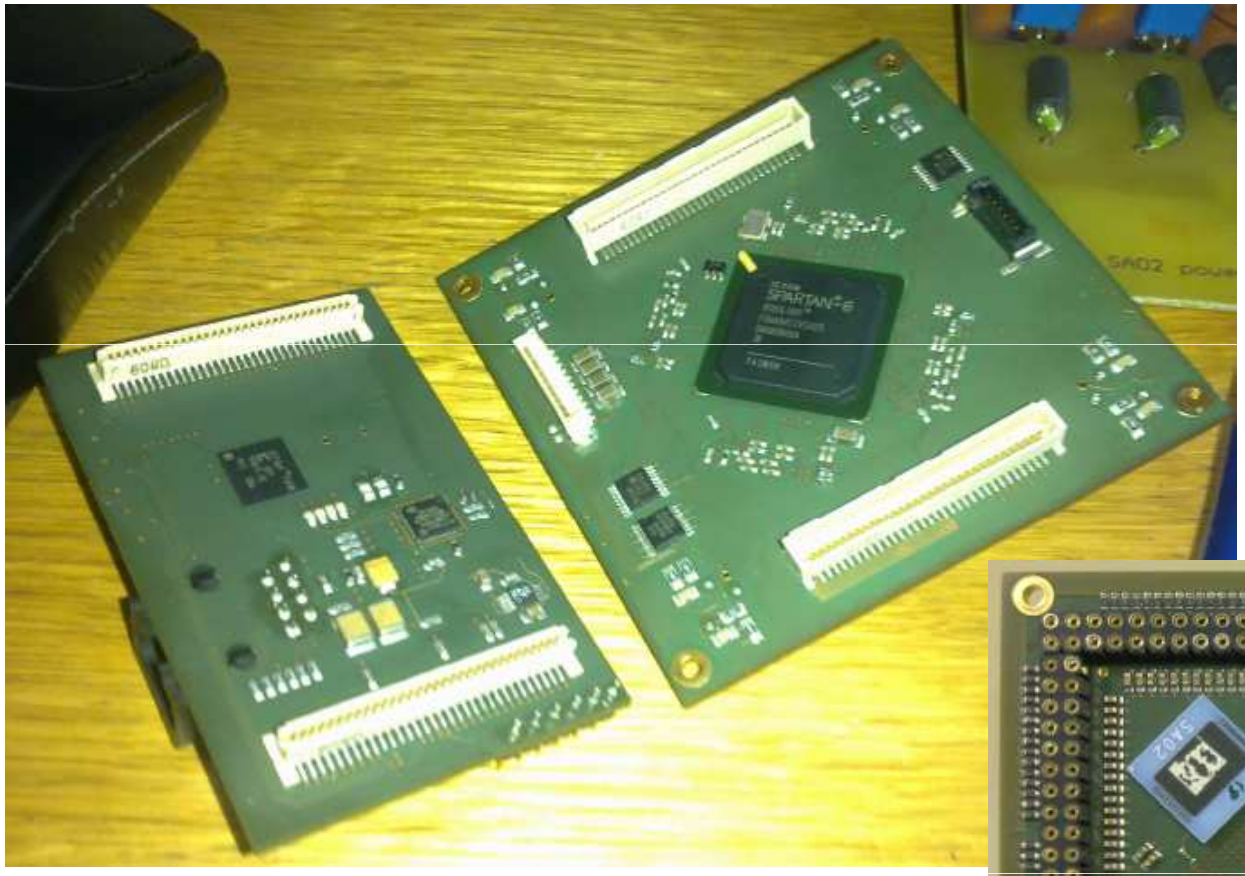
piggy board



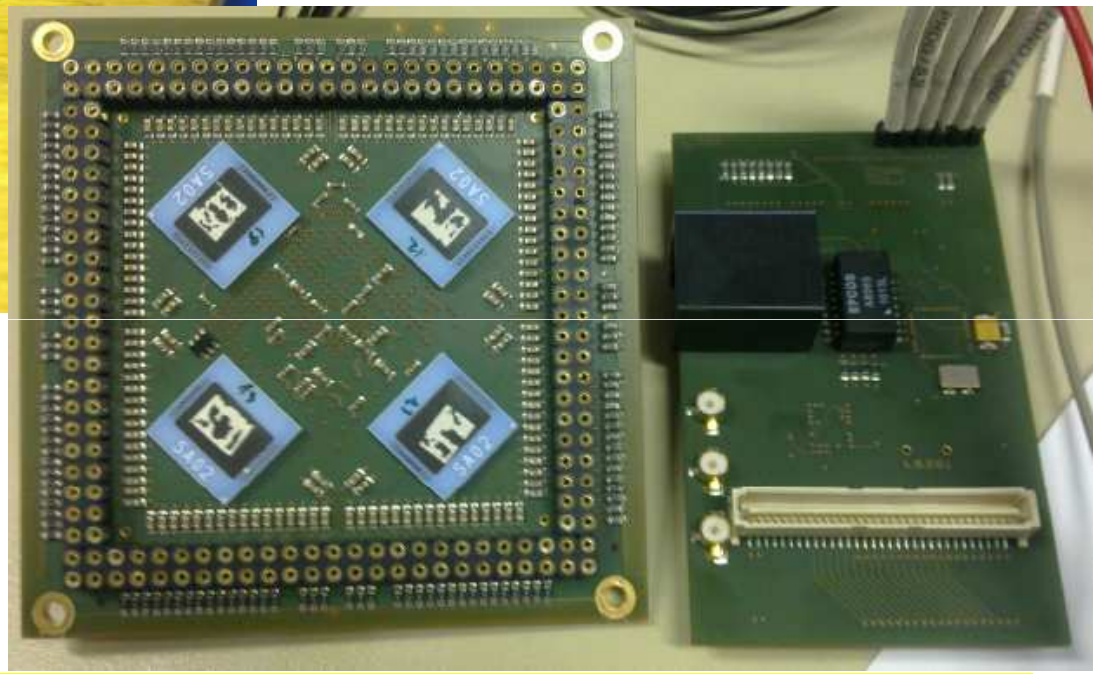
top bottom

Originally, planned to produce last year, but delayed.

Front-end Board



Finally produced!!

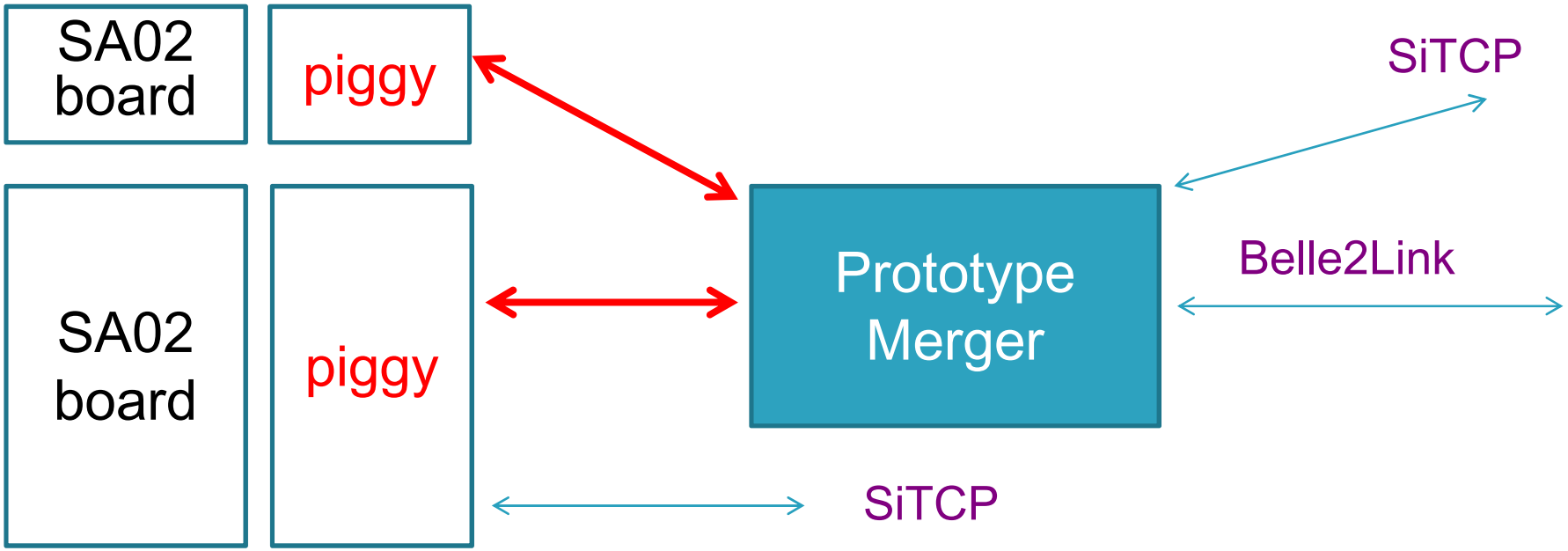


Front-end Board

Status (by A. Seljak)

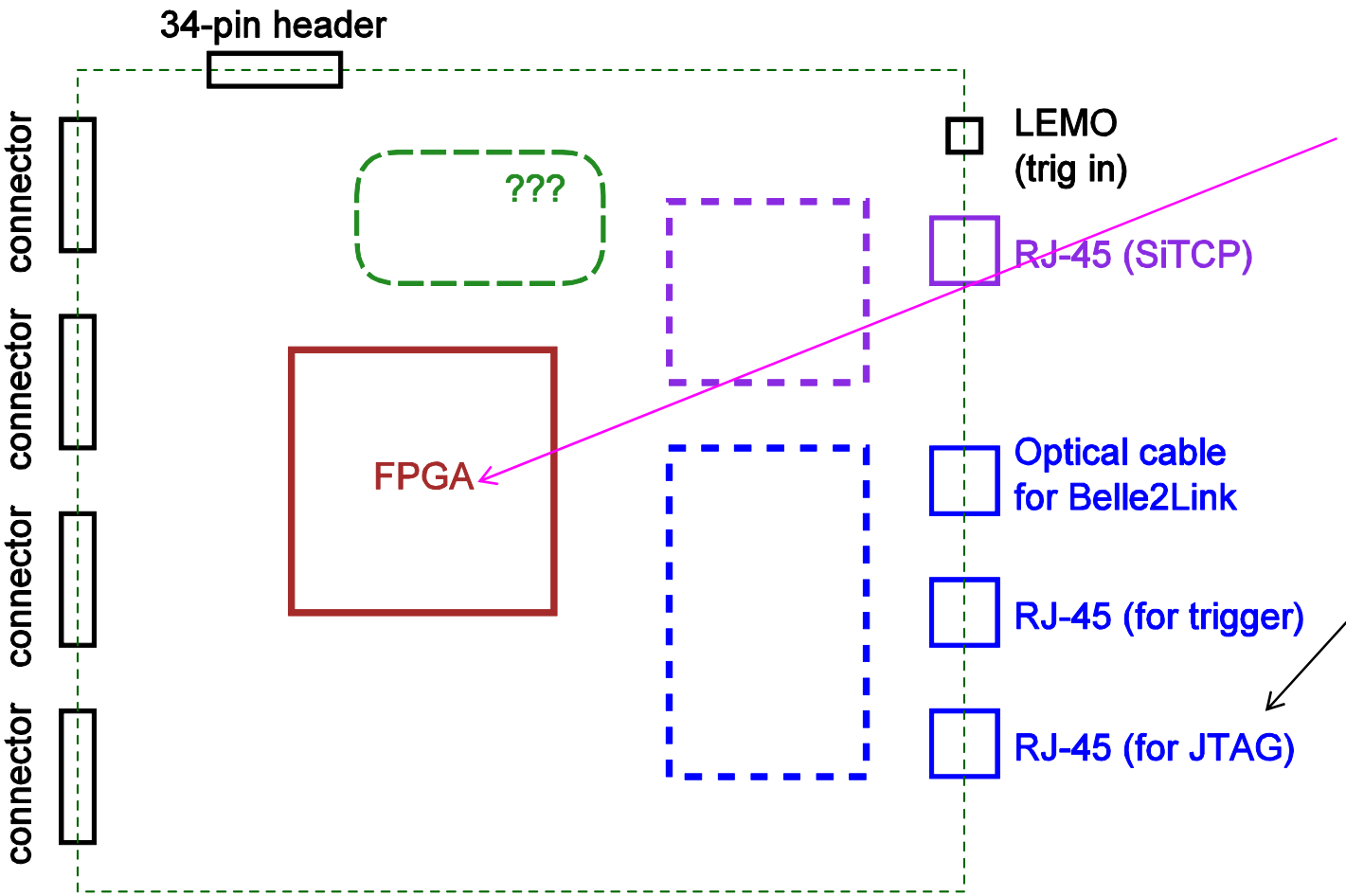
- Analog currents were high, but the problem is fixed.
- FPGA download successful; however PROM cannot be loaded.
  - ✓ Xilinx support confirmed the correctness of the schematics.
  - ✓ Maybe due to the use of virtual machine?
- Functionality of peripherals (multiplexer, digital resistors) is being tested.
- SiTCP part will be tested in February. Without SiTCP, it is hard to test the front end. Iwata-san (TMU) and S.N. will visit Ljubljana for debugging.

Merger Prototype



- First prototype board is to establish the scheme.
  - Big board; do not try to fit the small space.
- Connection to SA02board+piggy.
  - In the final version, piggy will be replaced by the merger.
- Merger 4 HAPDs.
- Target: March 2011.

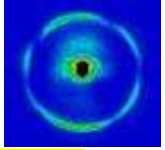
Merger Prototype



Xilinx Virtex5
(XC5VLX50T-FF665)

Only for the FPGA in merger (In the final design, FPGAs in the FE board is also configured by this line)

Merger Prototype

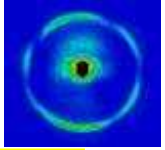


- FPGA XC5VLX50T is probably O.K. from simple estimation of the logic size. Larger one will be used in the next version if necessary.
- Still designing the board.
- Discussing interface between the SA02 board and the merger.
  - ✓ SA02 board: 64 pin molex, but no good cable.
  - ✓ Probably 34 pin (2.54mm pitch) headers for merger.
- The prototype is connected to more HAPDs, but considering the possibility to connect with more HAPDs.
- Specification on the interface between FE and Belle2Link is necessary
  - ✓ List of signals, writing clock speed, ….
  - ✓ Slow control.

Summary and Plan

- ASIC SA03: design started.
- Front-end board: debugging
- Merger prototype board: still in design.

- ASIC mass production.
  - ✓ How to test ? Cost ?
- HAPD readout using front-end board.
- System test with protytpe ARICH + FE board + prototype merger.
- Next round: design of the entire readout system.
  - ✓ Modification of the front-end boards.
  - ✓ Merger board to fit in the small space.



Backup

Description of Noise

$$\sigma^2_{noise} = (AC_{\det}\frac{1}{\sqrt{\tau}})^2 + (\sqrt{\frac{I_{leak}\tau}{eG}}FG)^2$$

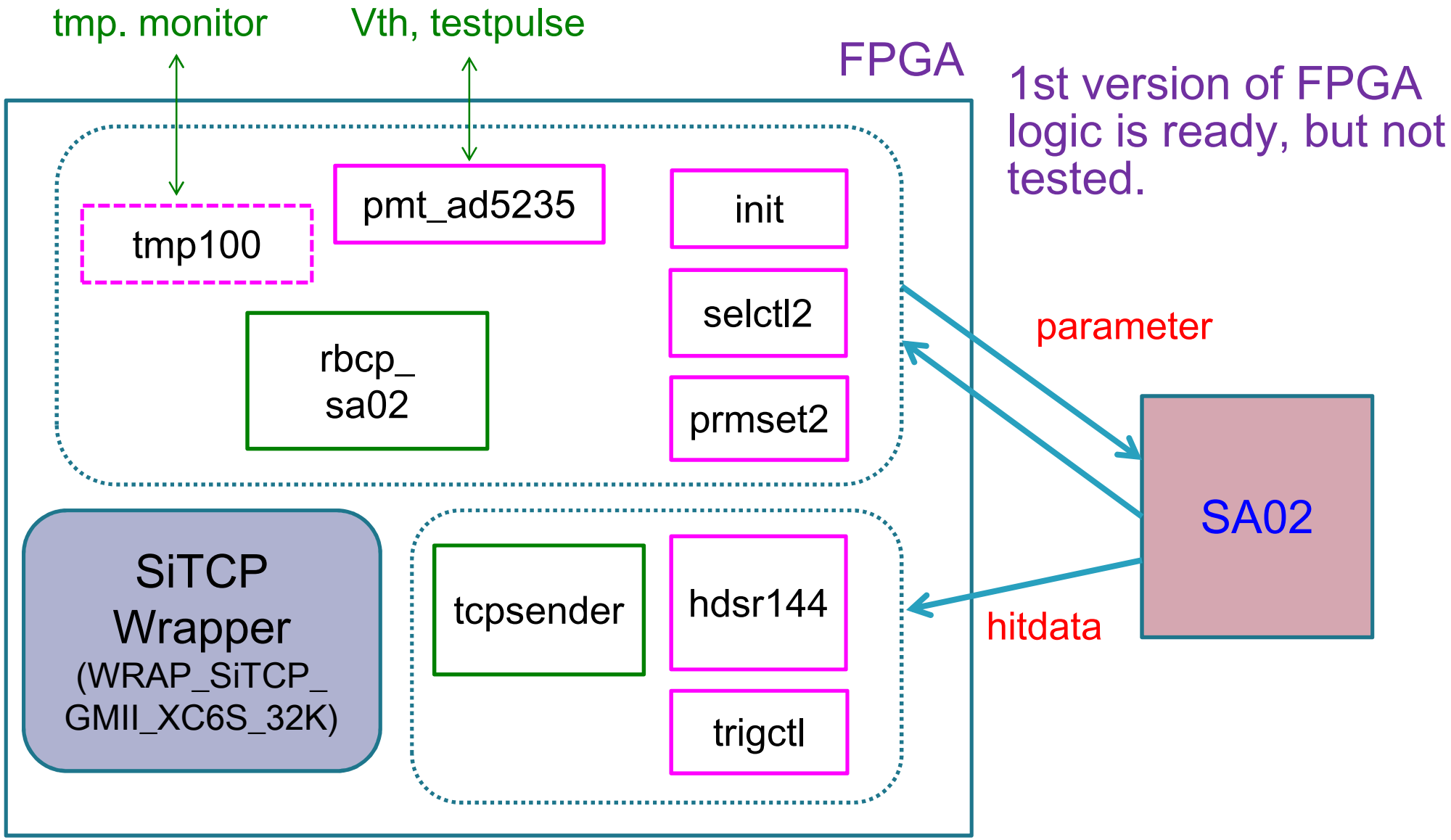
Amplifier noise

Shot noise due to leakage current in APD

C_{det} :	APD capacitance /ch
A :	constants depends on amplifier design
I_{leak} :	Leakage current in APD
τ :	Peaking time of shaping amplifier
G :	avalanche gain
F :	excess noise factor (~2)
e :	electron charge

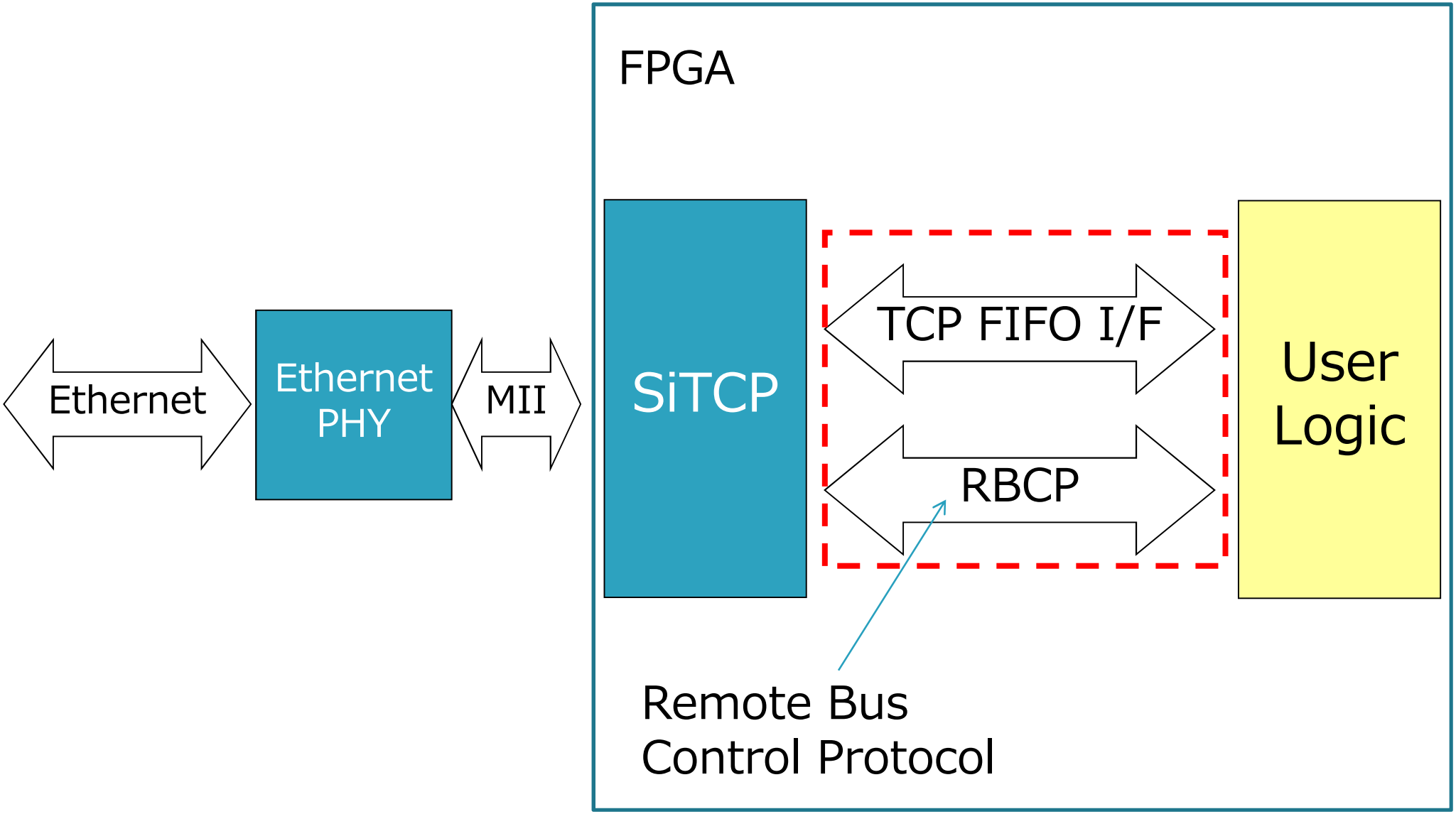
Neutron damage affects I_{leak}
Other APD properties are expected to be unchanged [ex.) NIM A447, 437 (2000)]

Front-end Board



1st version of FPGA logic is ready, but not tested.

SiTCP


FPGA
Ethernet
Ethernet PHY
MII
SiTCP
TCP FIFO I/F
RBCP
User Logic
Remote Bus Control Protocol

Merger Prototype

- IHEP (China) people will prepare the specification on interface btw FE and Belle2Link (list of signals, writing clocks etc.).
  - ✓ In principle, no flow control exists btw FE and Belle2Link. From detector side, we can just continue writing data.
  - ✓ L1 buffer is in the detector side.
- Slow control (parameter setting / read back) need to be considered. It seems there is no concrete scheme yet.
- Belle2Link probably requires one on-board clock. The clock frequency will be determined this year.