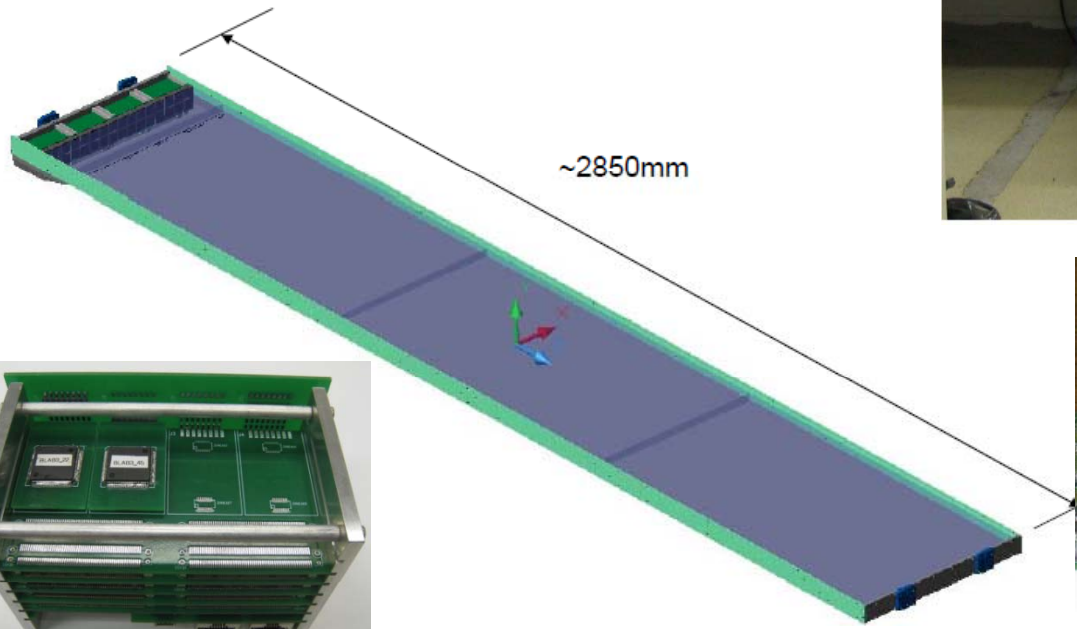
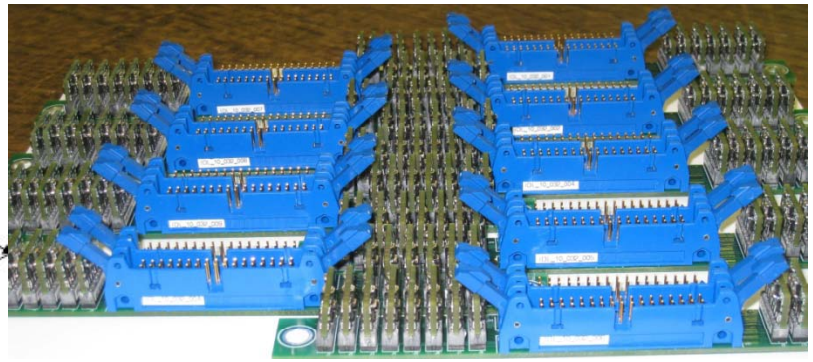
iTOP (barrel PID) and endcap KLM DAQ Summary



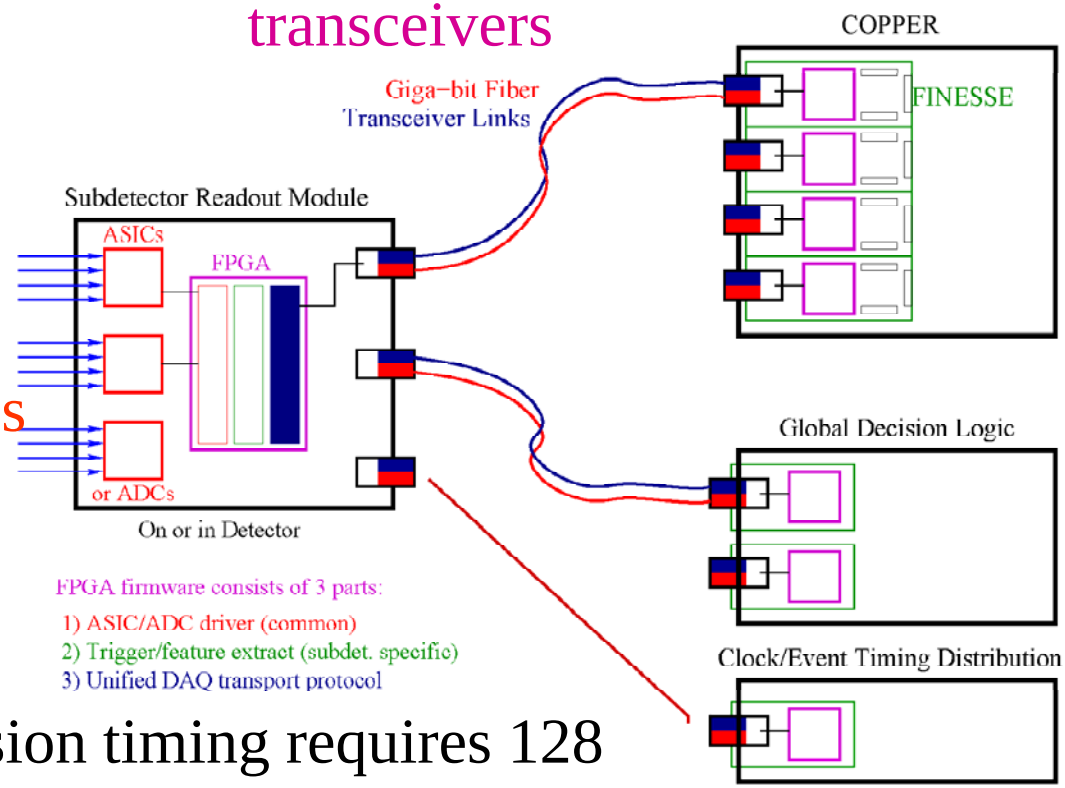


Overview

- Update on B-PID (iTOP) DAQ
  - Big issue is SCROD
- eKLM prototyping:
  - Prototyping status
  - Use Belle2link directly?
- bKLM presented separately (Sumisawa-san)
- Schedule for incorporating Belle2link items

iTOP Readout Overview

128 DAQ fiber transceivers



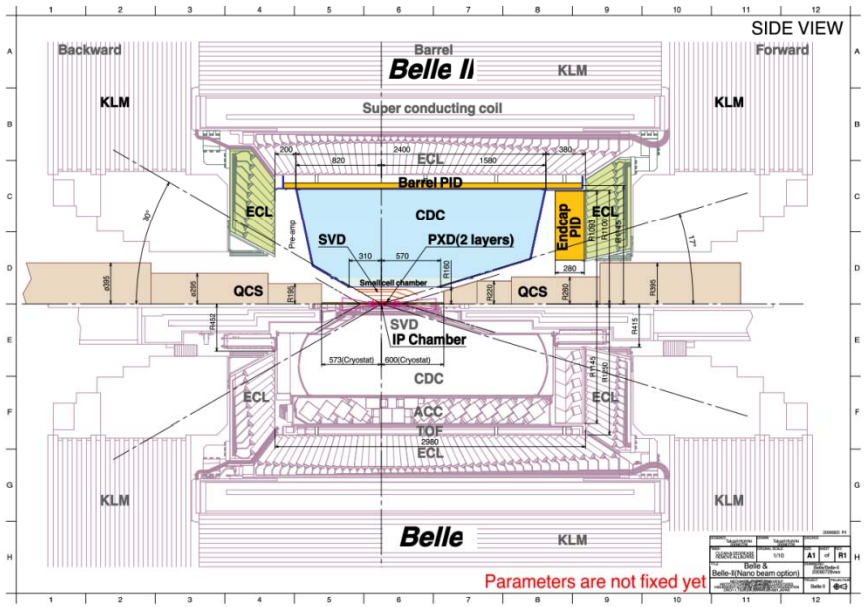
32 FINESSE
8 COPPER

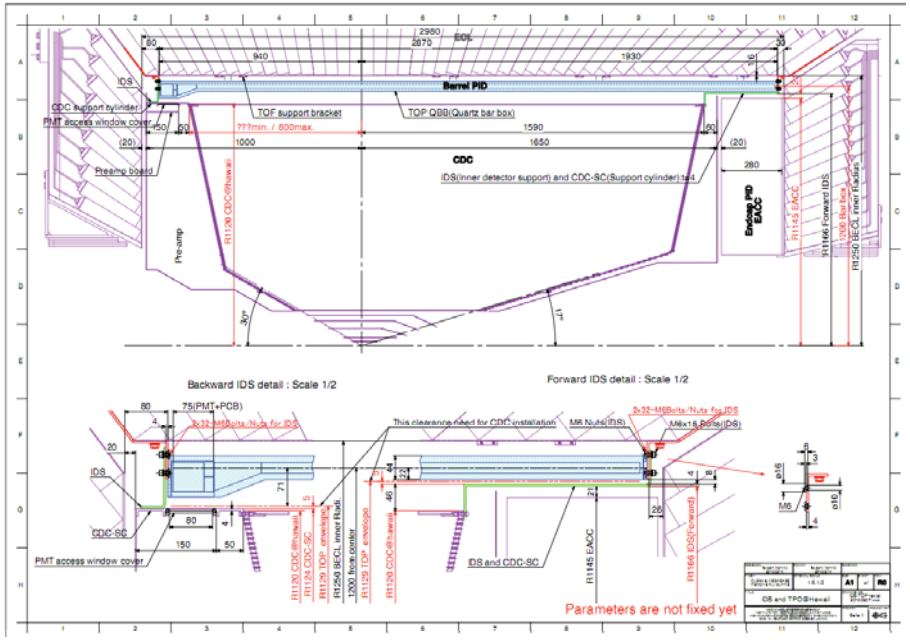
8k channels
1k 8-channel waveform ASICs
128 SRM

Precision timing requires 128 channels high-precision clock distribution (<~ 10ps)

Approximately 30m runs

Belle2 barrel PID upgrade: iTOP





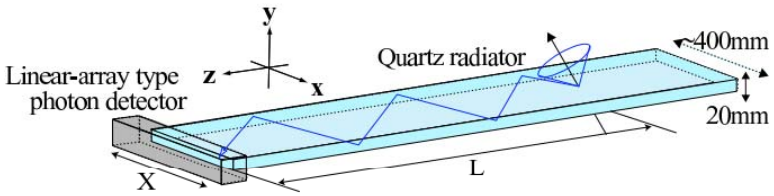
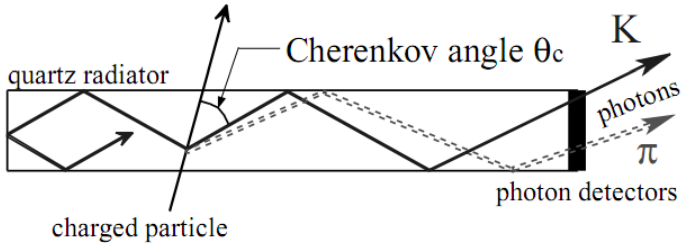
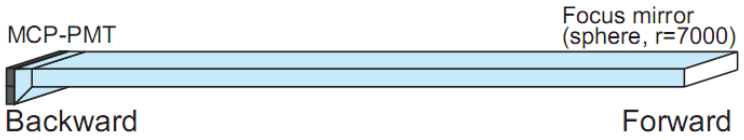
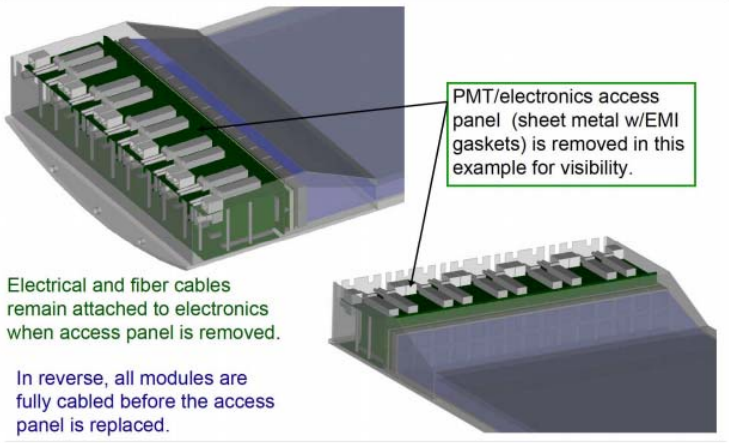


Figure 7.1: Conceptual overview of TOP counter.

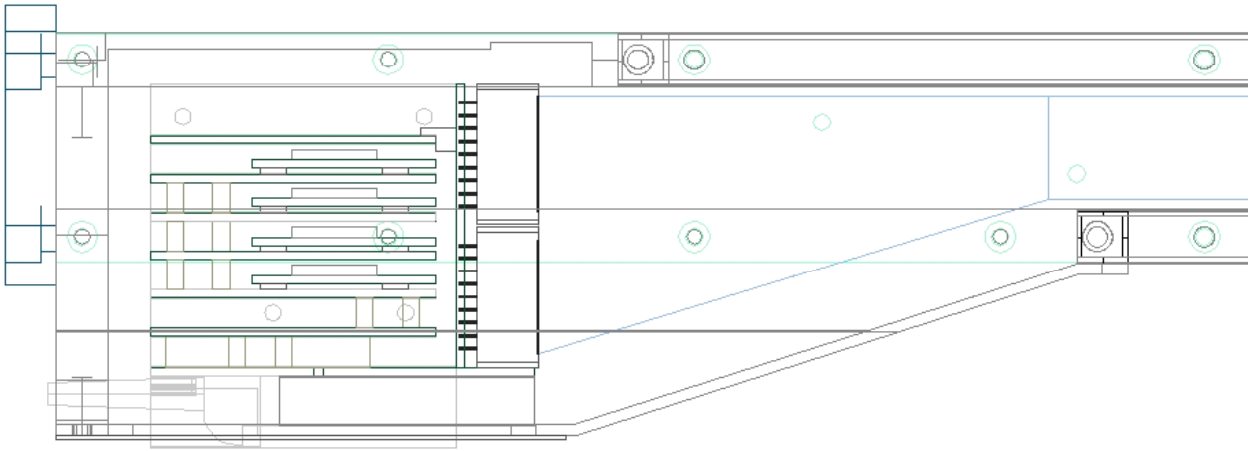


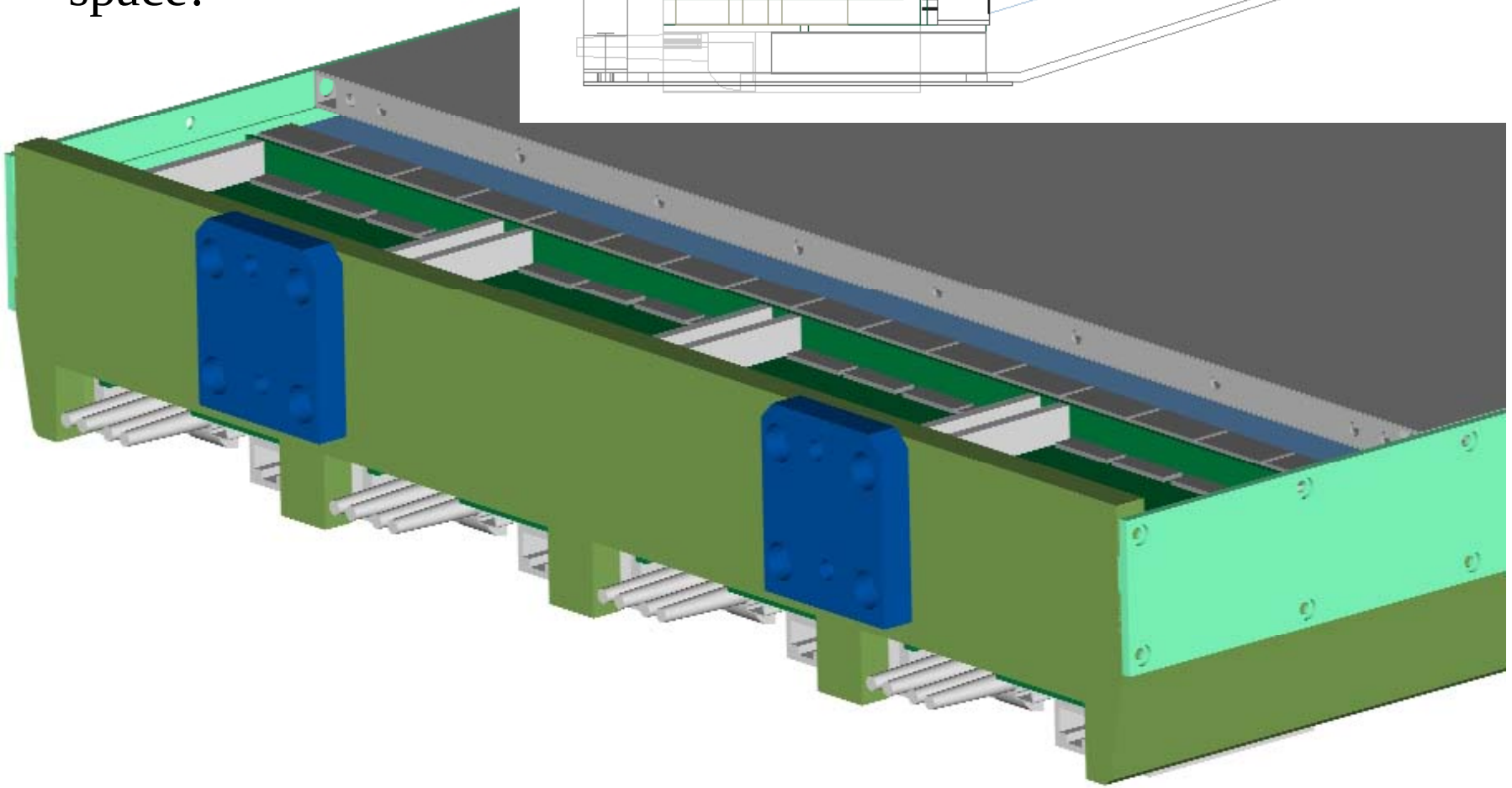




A very crowded location!

8k vs. 14k
(CDC channels)
<< 10% of
space!

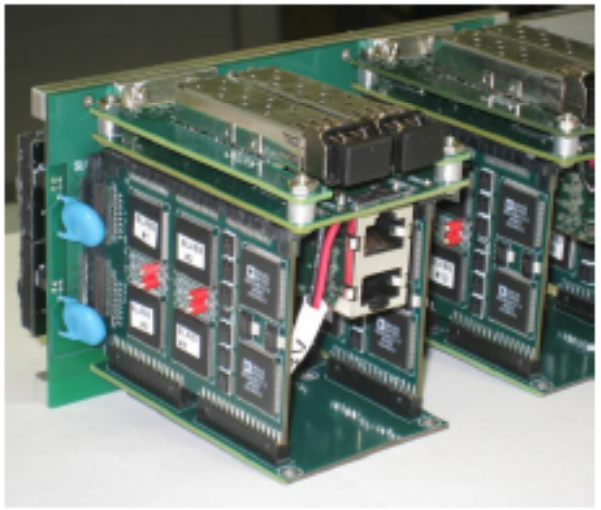


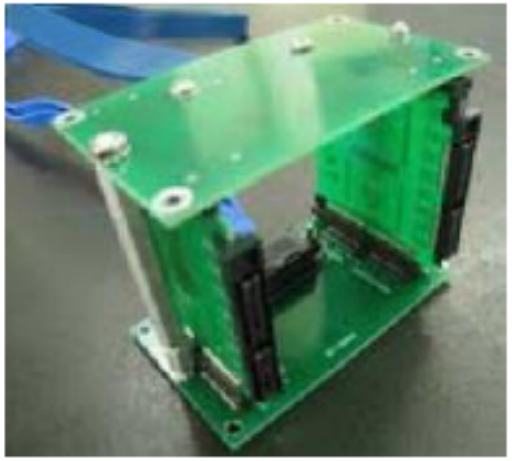


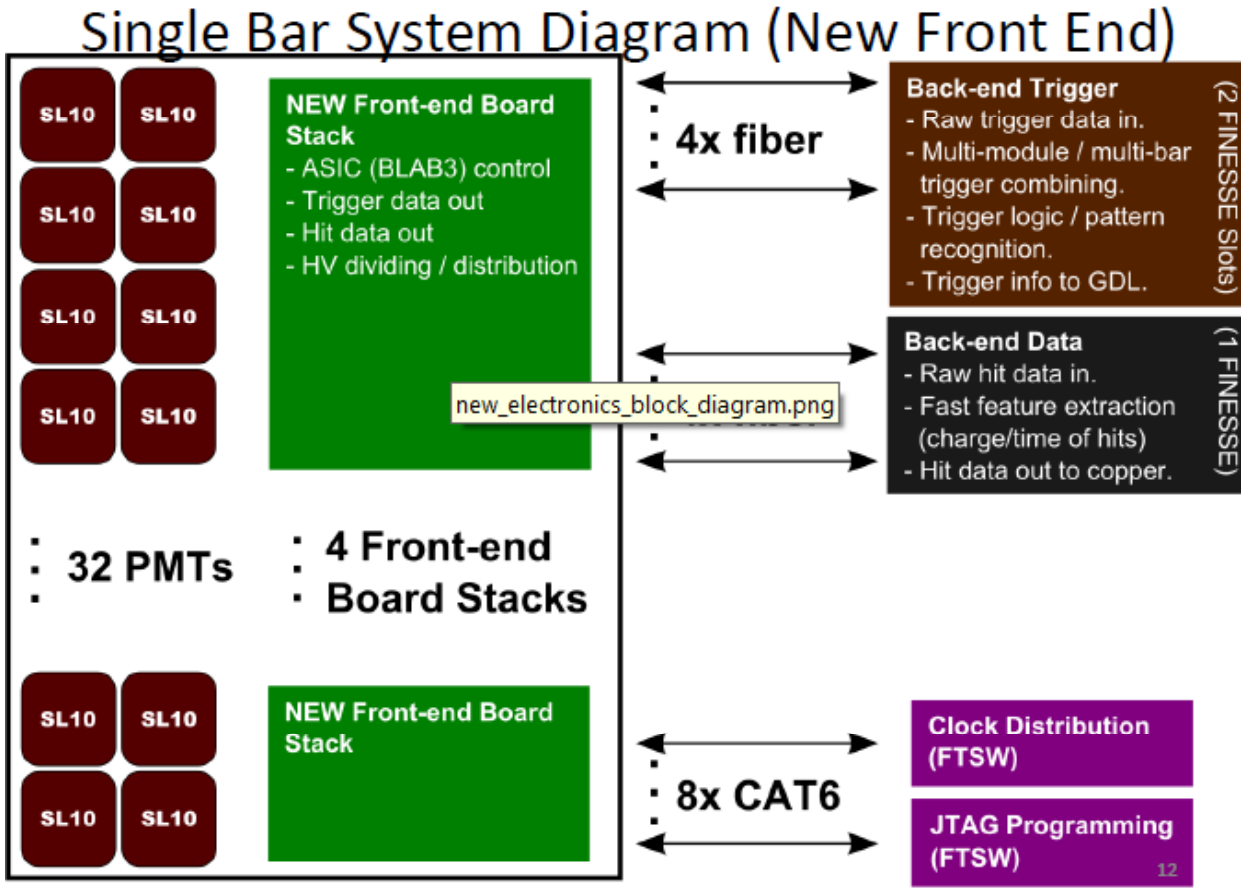
First prototype iteration results

Disadvantages of Existing Board Stack

- BLAB3 issues:
  - Replacement requires re-soldering.
  - Calibration requires a front board adapter to inject test signals.
- Firmware issues:
  - No on-board clock: need clock distribution to test any firmware.
  - Fiberoptic readout only: need back-end working to verify any data out.
- Size issues:
  - Significant amount of wasted space.
  - Existing modules (top right) are too big for Belle II.
  - Split module (lower right) where transceivers are separated from digitizers might meet size restrictions, but this is untested and may not preserve signal fidelity.







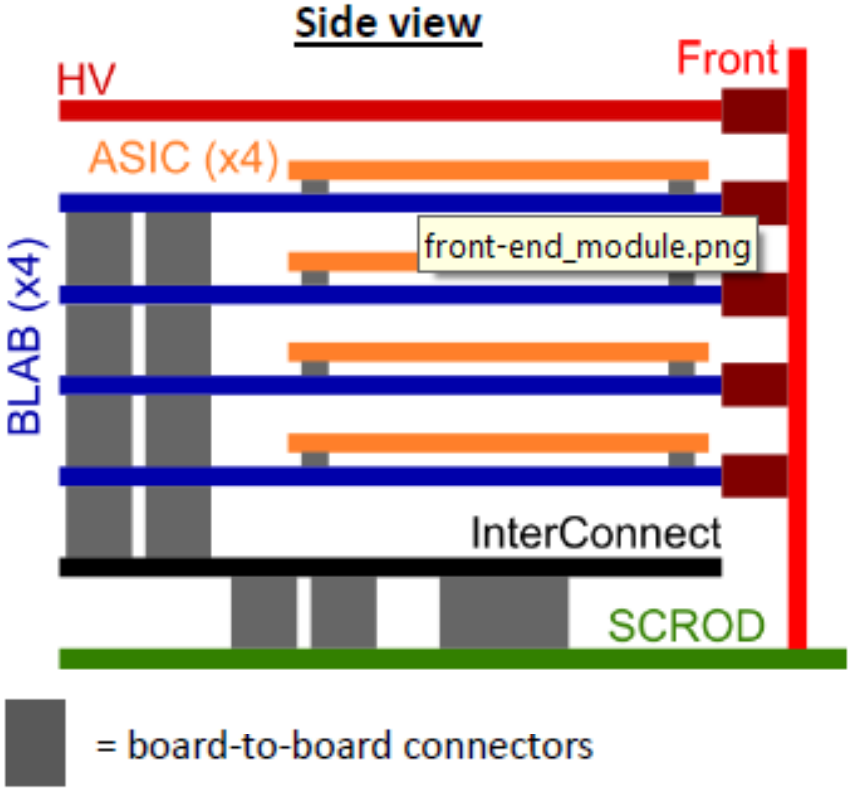
•Remaining system pieces are being developed/tested.

–Changes to front-end don't significantly impact other elements

•Calibration studies in Hawaii are ongoing …

Proposed modular solution

New Front-end Board Stack



Front
- Connects HV board to PMTs
- Connects PMT output to ASIC input

HV
- High voltage components for PMTs
- Cooling for high voltage components

Standard Control, Read-Out, Data (SCROD)
- FPGA (ASIC control)
  - Virtex4, Spartan6
- 2 Fiber transceivers
- 2 RJ45
  - Clock Distribution
  - LVDS (JTAG)
- Mini USB – for easy bench testing

Digitizer Boards (BLAB)
- Carrier card for ASICs
  - 4 ASIC daughter cards per carrier
- ASIC in-situ testing components
  - e.g., pulser for channel checks

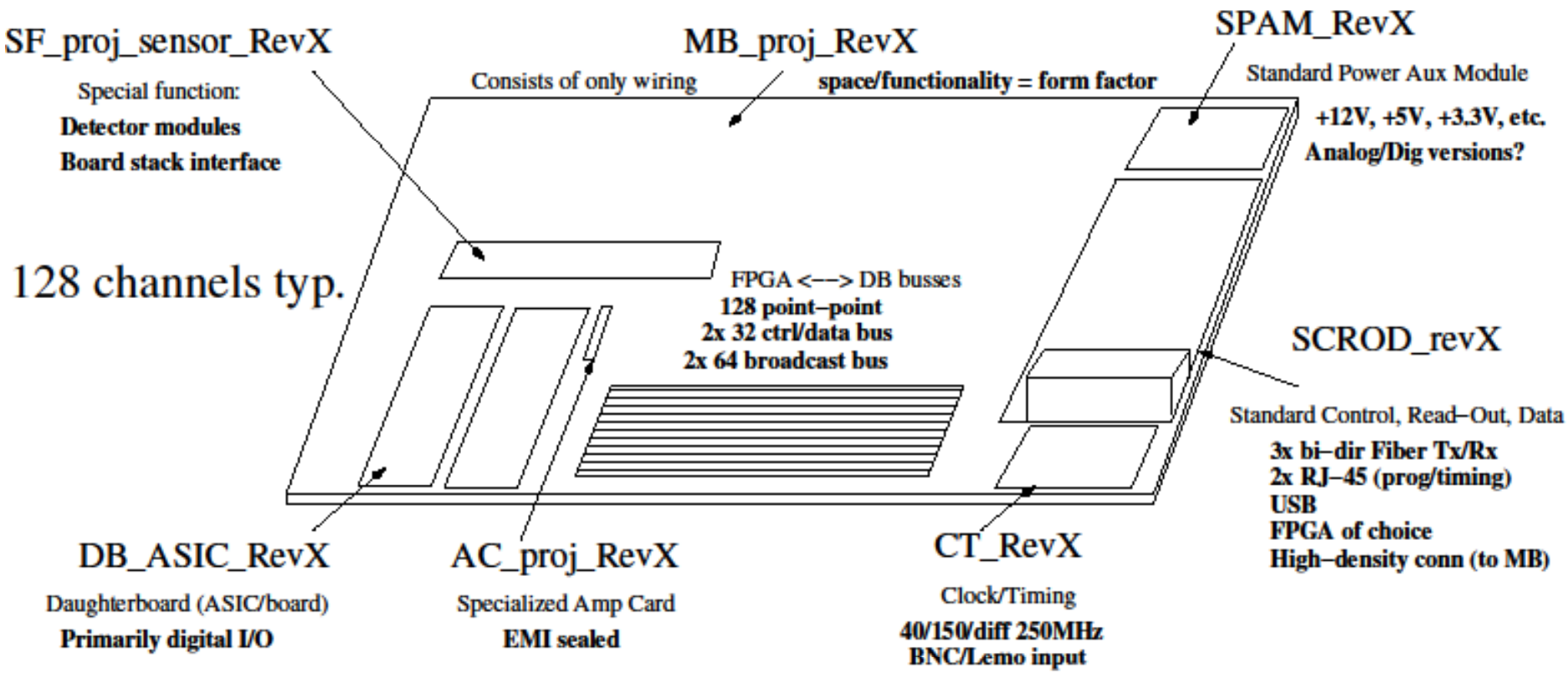
ASIC
- 1 BLAB3 per card
- DACs

Interconnect Board
- Connects SCROD & BLAB
  -Layout of connectors are forced to be unique because of size constraints
- Power regulation/distribution

IDL Consolidated Board Management System (ICBMS)

(a proposal — suggestions how to improve welcome)

This time, the front–end board stacks. Next time, the back–end.



BS_proj_RevX

Board, Special (DB)

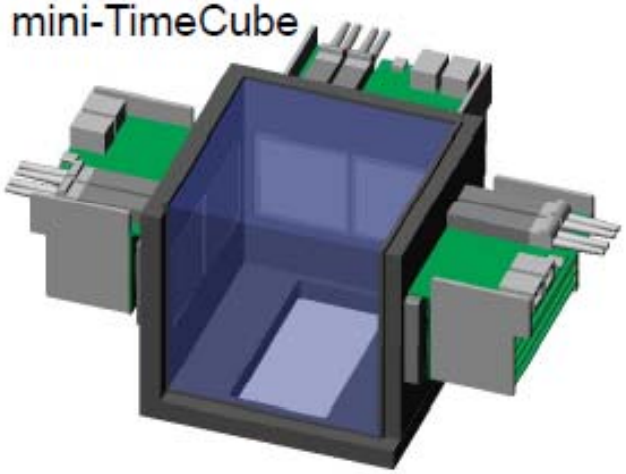
Standard ADCs
Multi–DB functionality (e.g. MUX)

Relevant Projects

1) **xFEL Readout (formerly ROE+...) [128 channels]**
2) **eKLM prototype Readout [150 channels]**
3) **mTimeCube Readout [6x 128 channels]**
4) **iTOP proto Readout [7x 16? channels]**
5) **ATF2 xRay Readout [128 channels]**
6) **fDIRC CTA Readout [7x 128 channels]**

all the rest...

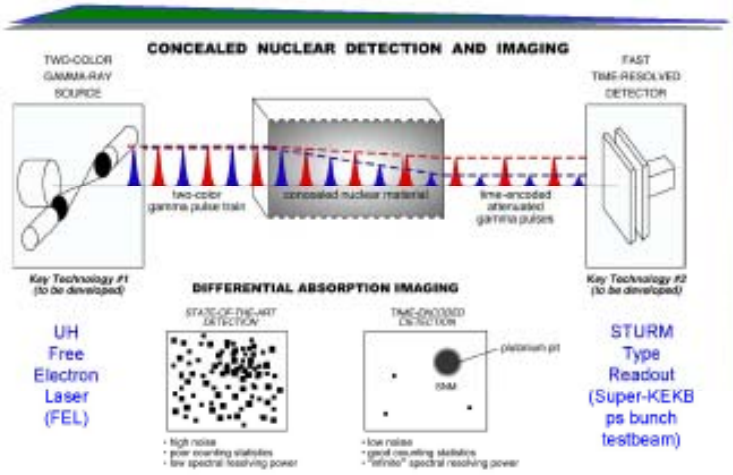
mini-TimeCube



endcap KLM upgrade

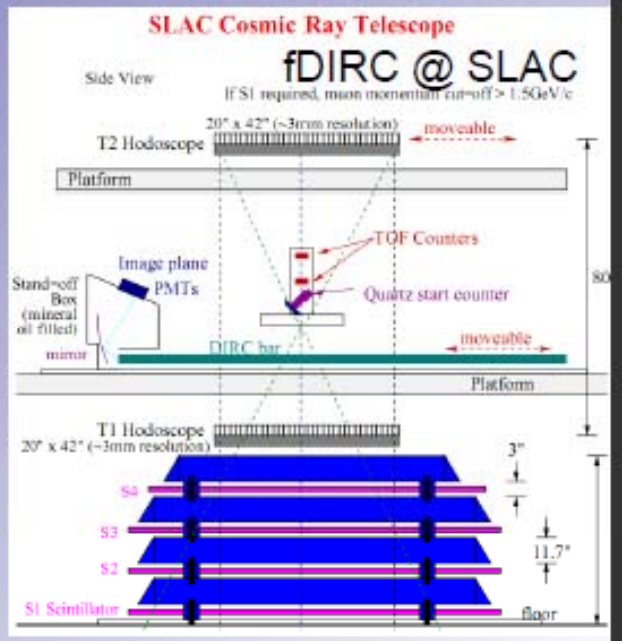
ATF2 X-Ray beamline

Time-Encoded Differential Absorption



UH Free Electron Laser (FEL)

STURM Type Readout (Super-KEKB ps bunch testbeam)

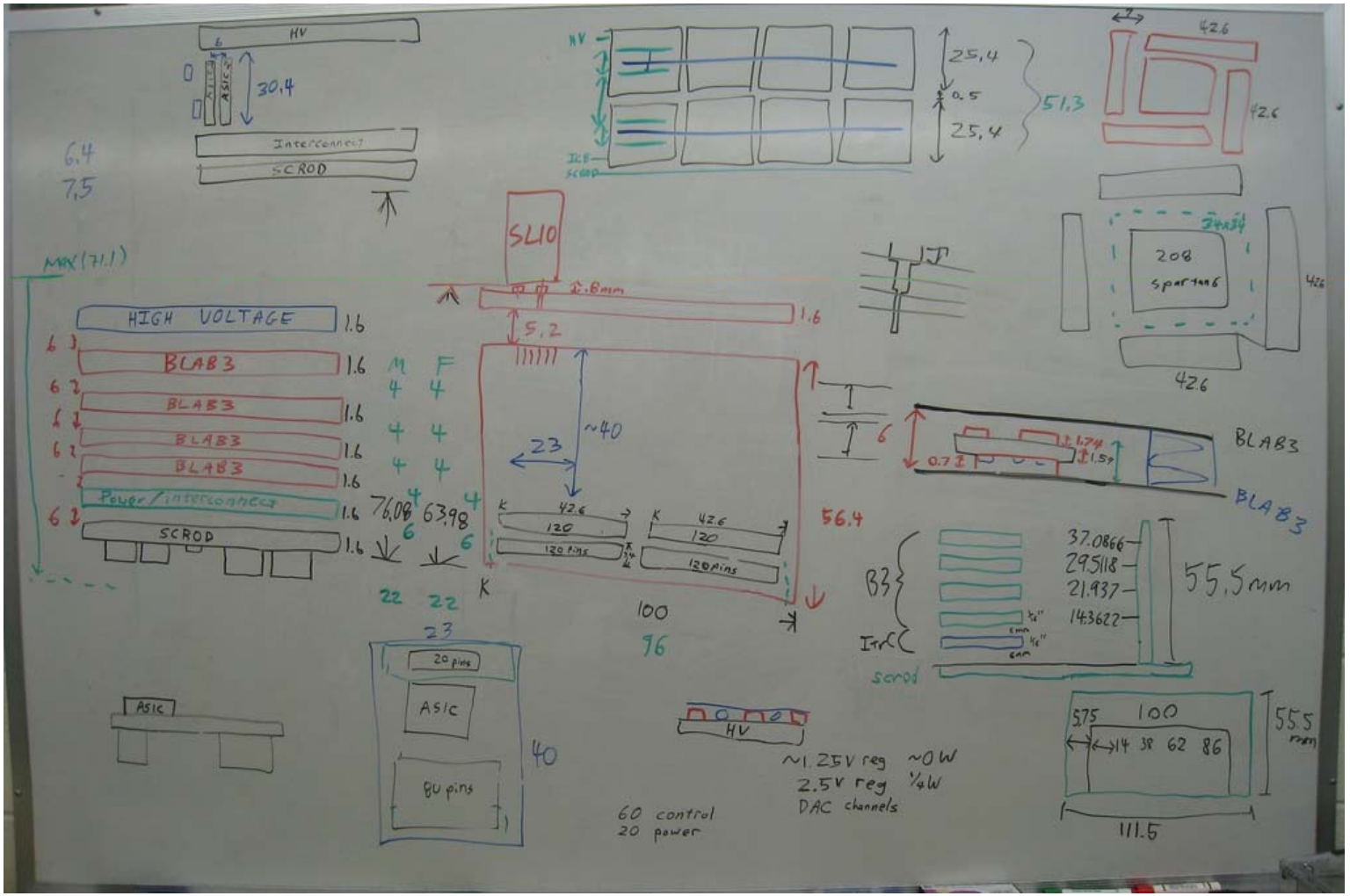


relevant projects and SCROD count

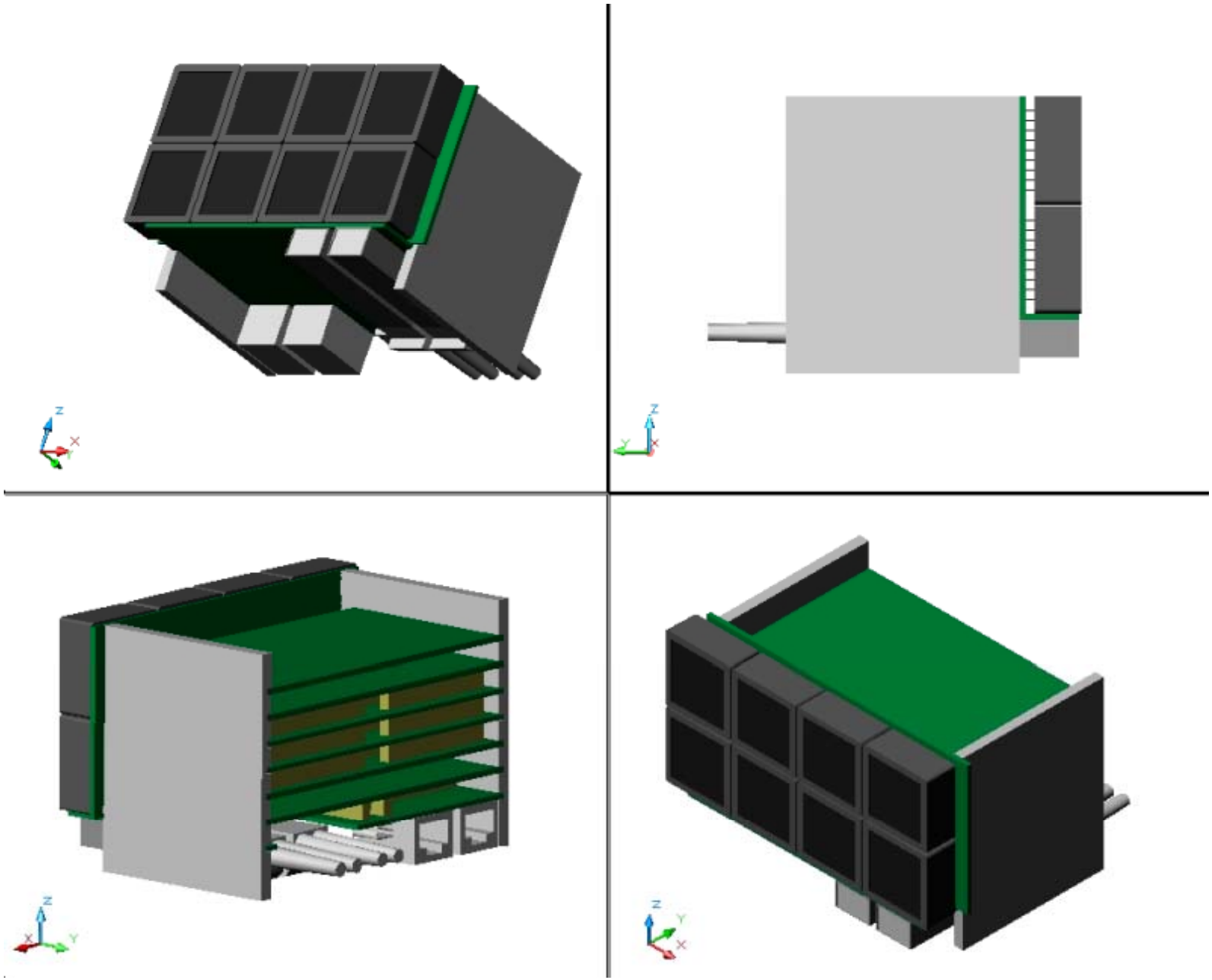
- iTOP readout
  - [16*8*4*16 = 8192 channels = 64 SCRODs]
- eKLM prototype readout
  - [150 channels = 1 SCROD] (128 in final system?)
- ATF2 xRay readout
  - [128 channels = 1 SCROD]   (n stations in final system)
- fDIRC CTA readout
  - [7*128 = 896 channels = 7 SCRODs]
- xFEL readout
  - [128 channels = 1 SCROD]
- mTimeCube readout
  - [6*128 = 768 channels = 6 SCRODs]
- total 80 SCRODs needed; take advantage of economies of scale

SCROD feasible? (mid-October)

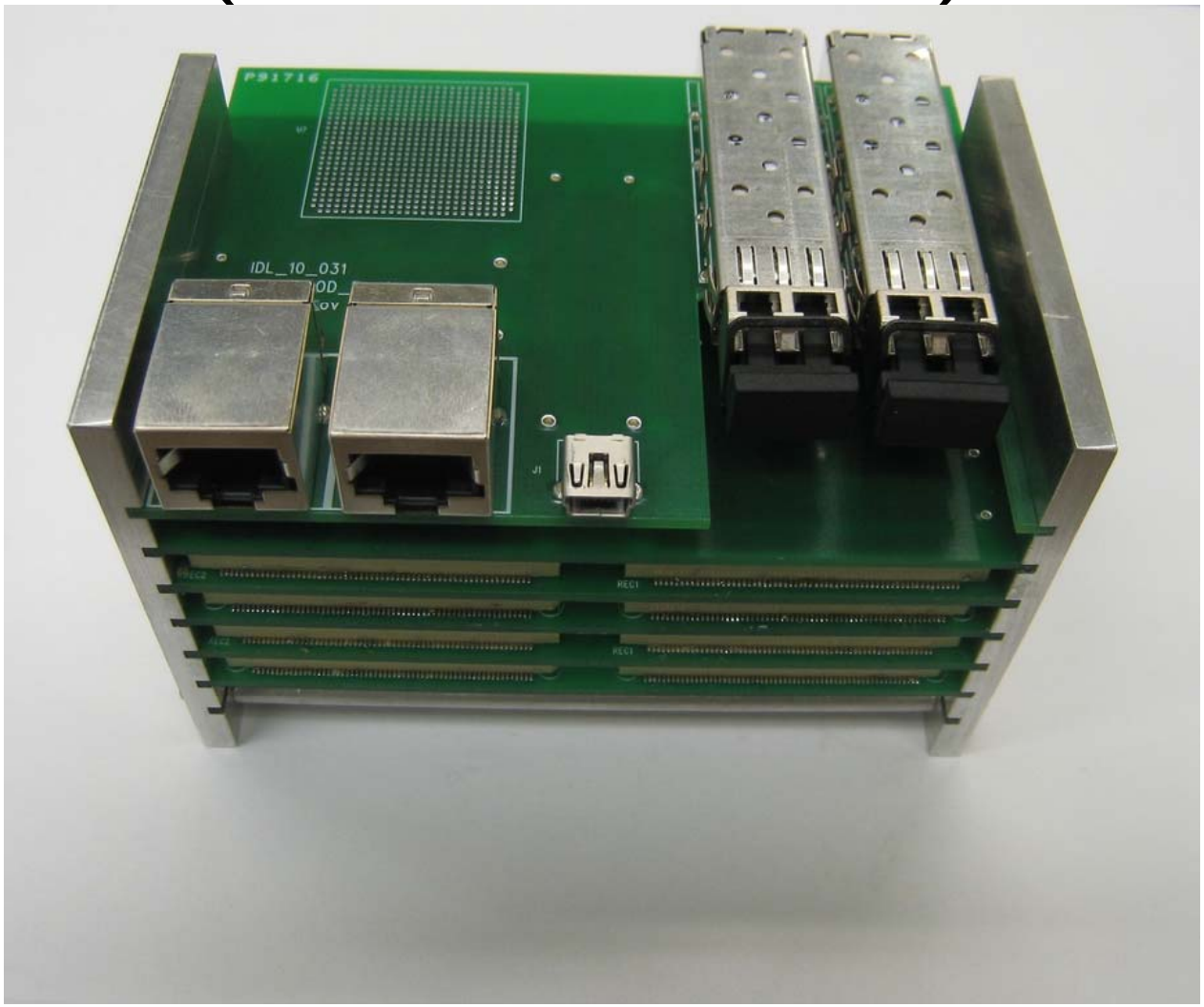
brainstorming the mechanical mockup (mid-November)



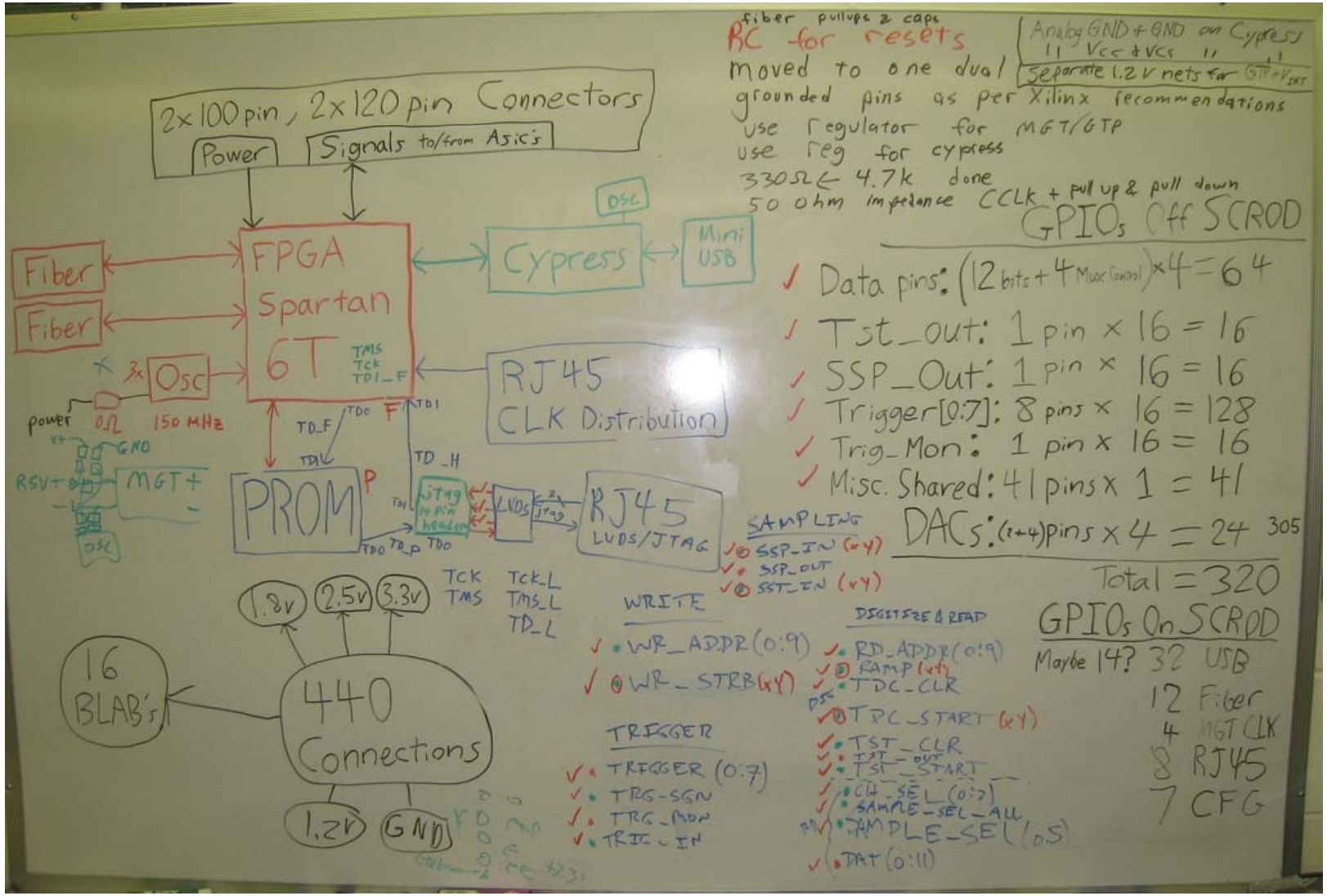
Might work mechanically, if can really fit components…



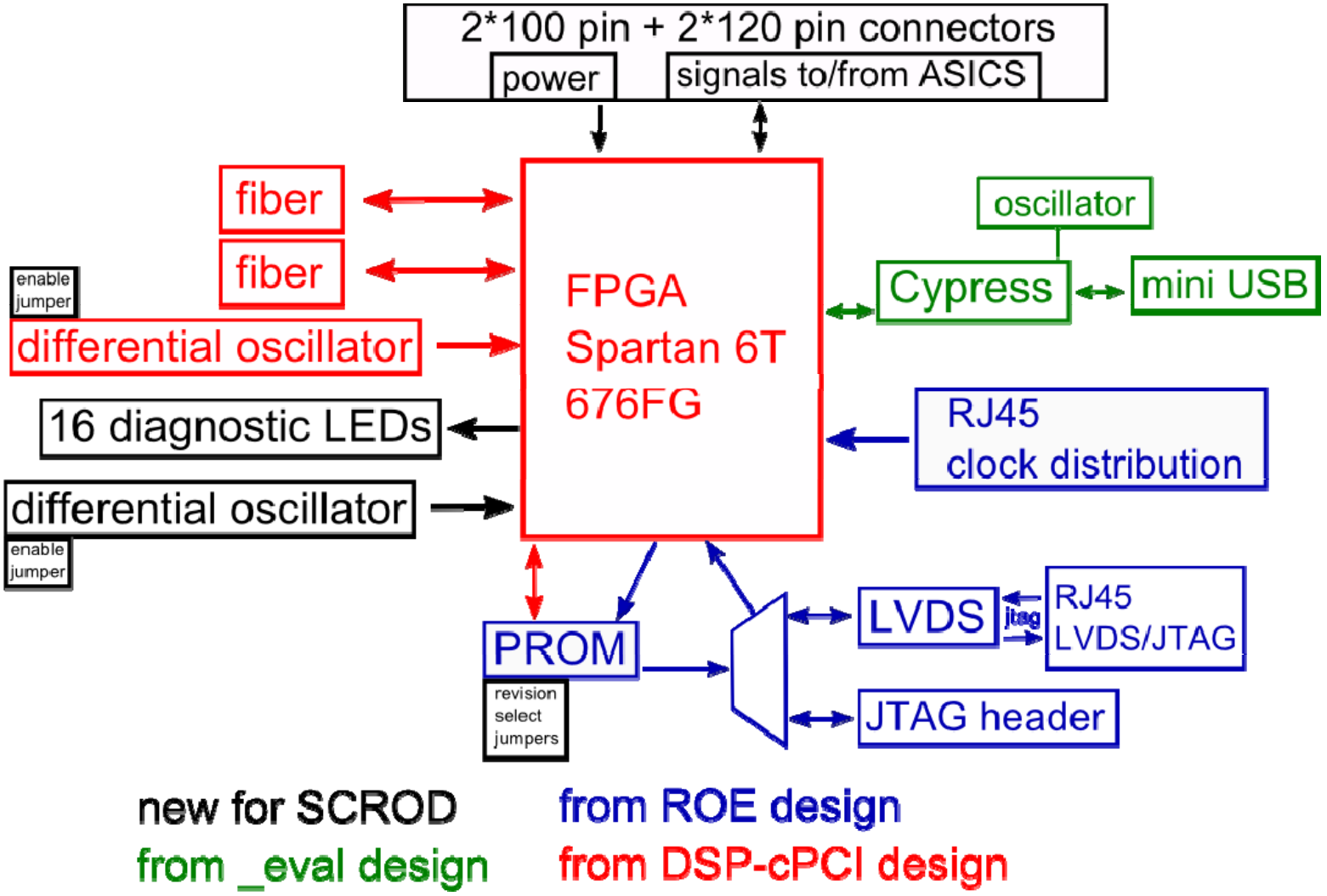
mechanical mockup (mid-November)



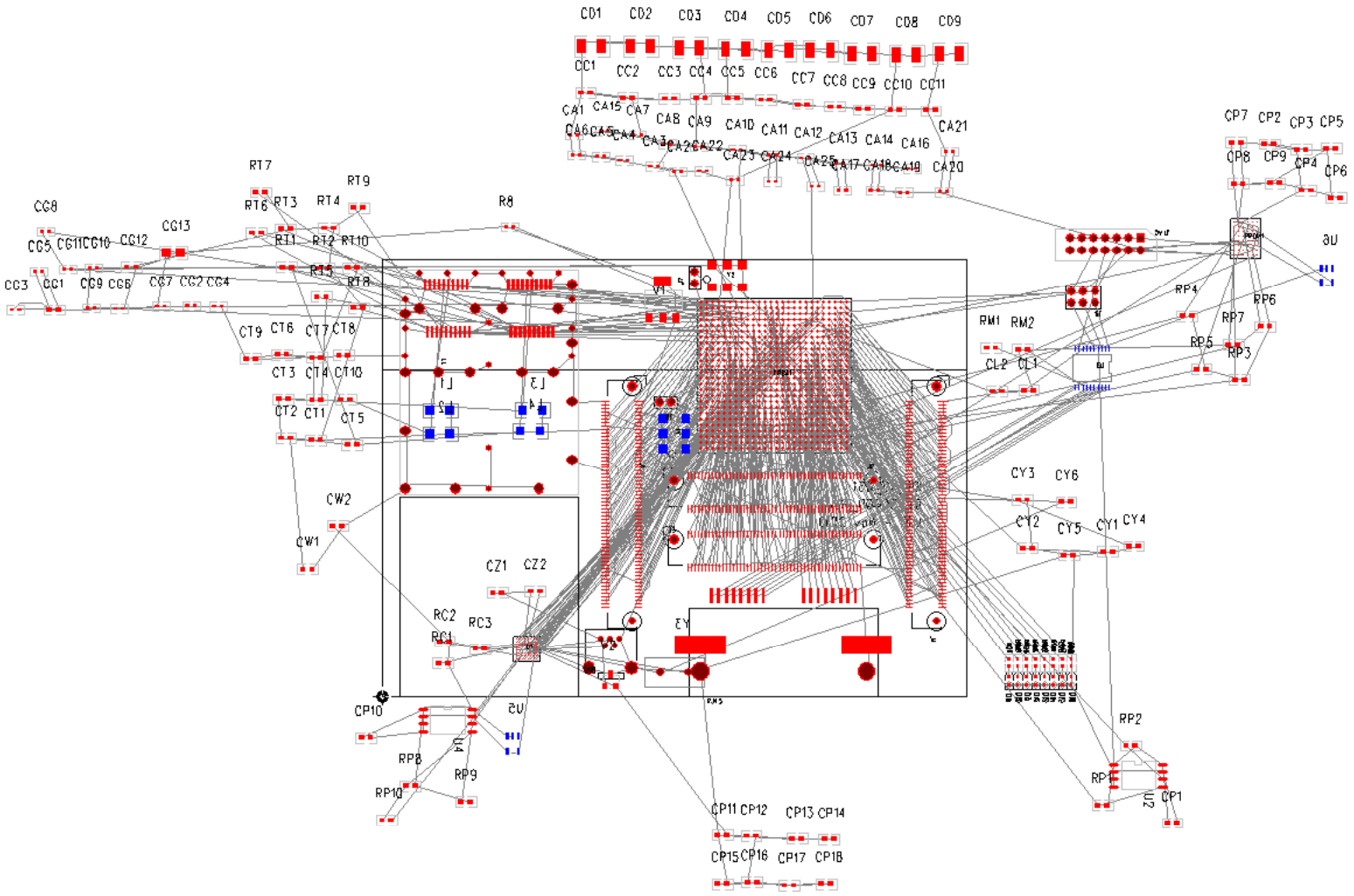
brainstorming SCROD



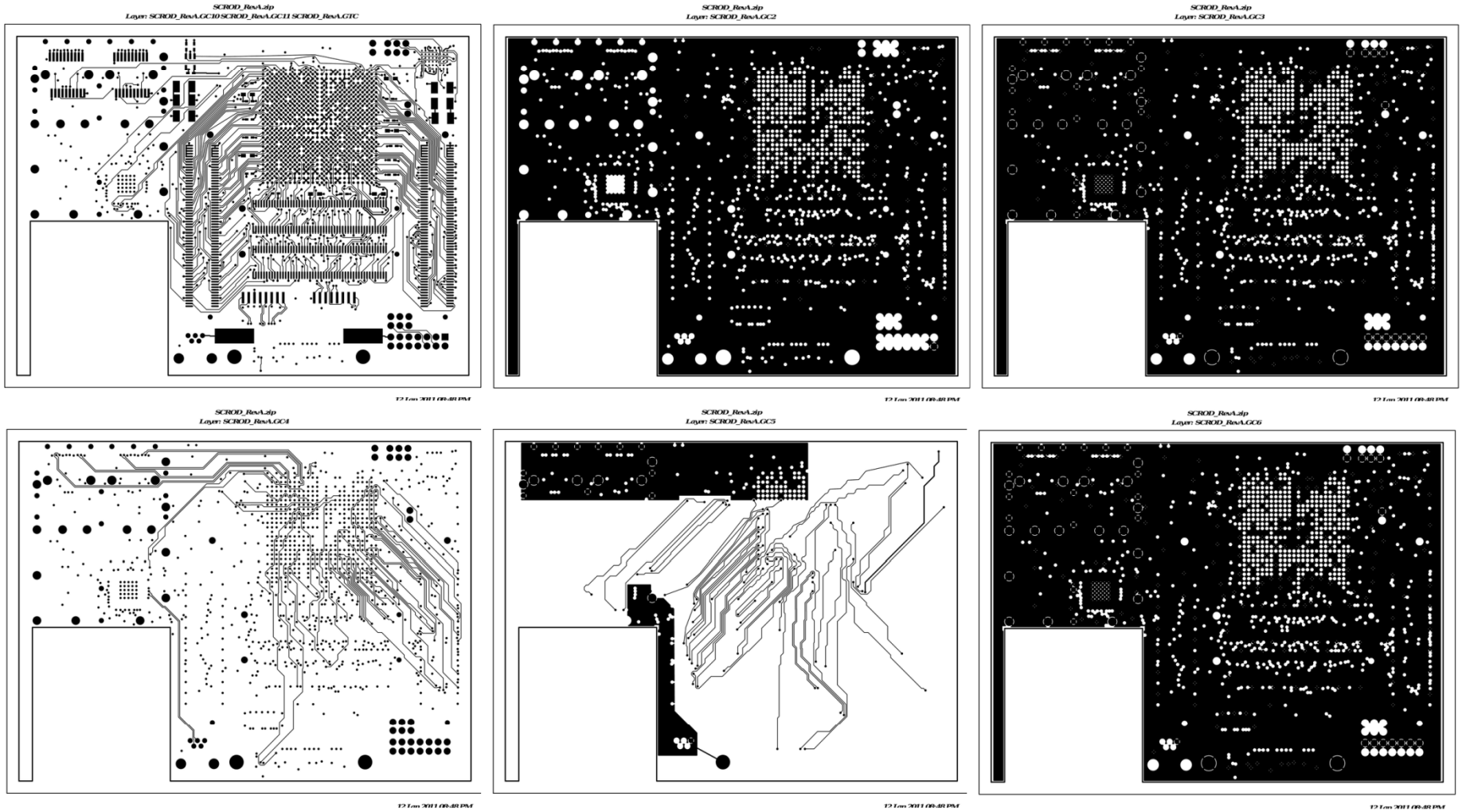
SCROD block diagram



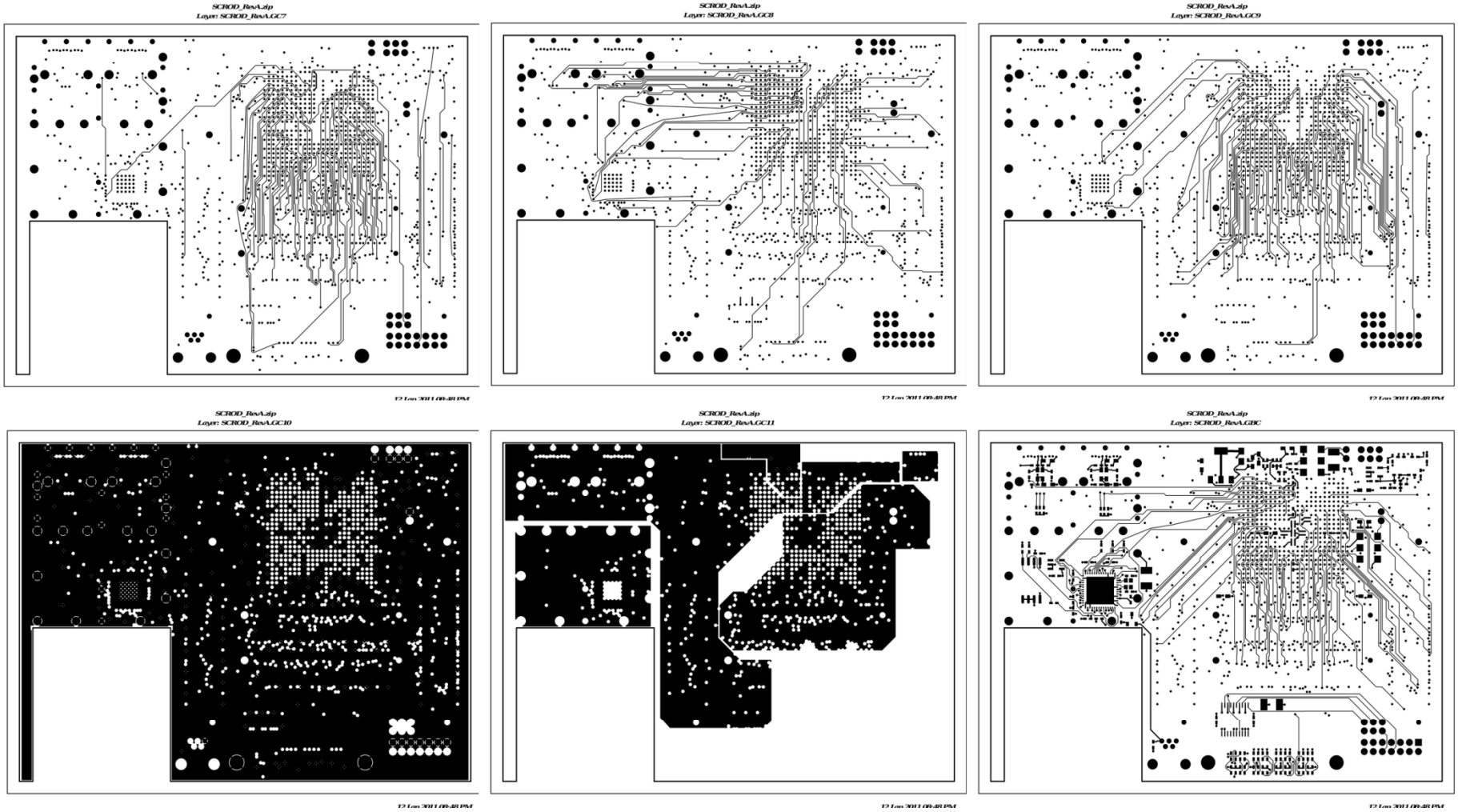
status of SCROD layout on Dec 23rd



status of layout as of Jan 13th: top six layers



status of layout as of Jan 13th: bottom six layers



references and further info

- references:
  - http://b2comp.kek.jp/~twiki/pub/Organization/B2TDR/B2TDR.pdf
  - http://www.phys.hawaii.edu/~idlab/taskAndSchedule/ICBMS.pdf
- latest info:
  - http://idlab.phys.hawaii.edu/pcb-designs/scrod

Expected rates: FDIRC vs TOP counter

J. Va'vra, Scaling from Belle-I Aerogel data (I. Idachi provided update on 11/18/2010)

SL-10 MCP-PMT predicted rates in TOP counter:

Lumi	Polar angle Theta [deg]	Number of PMTs per one quartz block	Bar box volume [cm^3]	Bckg scaling with L	Rate in one SL-10 [MHz]	Pixel rate [kHz]	Total dose [C/cm^2 per 10 years]
10^{36}	35-130°	30	~2.4×10^4	25 x	~1.0	~63	~8

(numbers worked out for a 1-bar solution)

H-8500 MaPMT predicted rates in FDIRC:

Lumi	Polar angle Theta [deg]	Number of PMTs per one FBLOCK	Bar box volume [cm^3]	Bckg scaling with L	Rate in one H-8500 MaPMT [MHz]	Double-pixel rate [kHz]	Total dose [C/cm^2 per 10 years]
10^{36}	35-130°	48	~2.6×10^4	25 x	~0.94	~29	~1

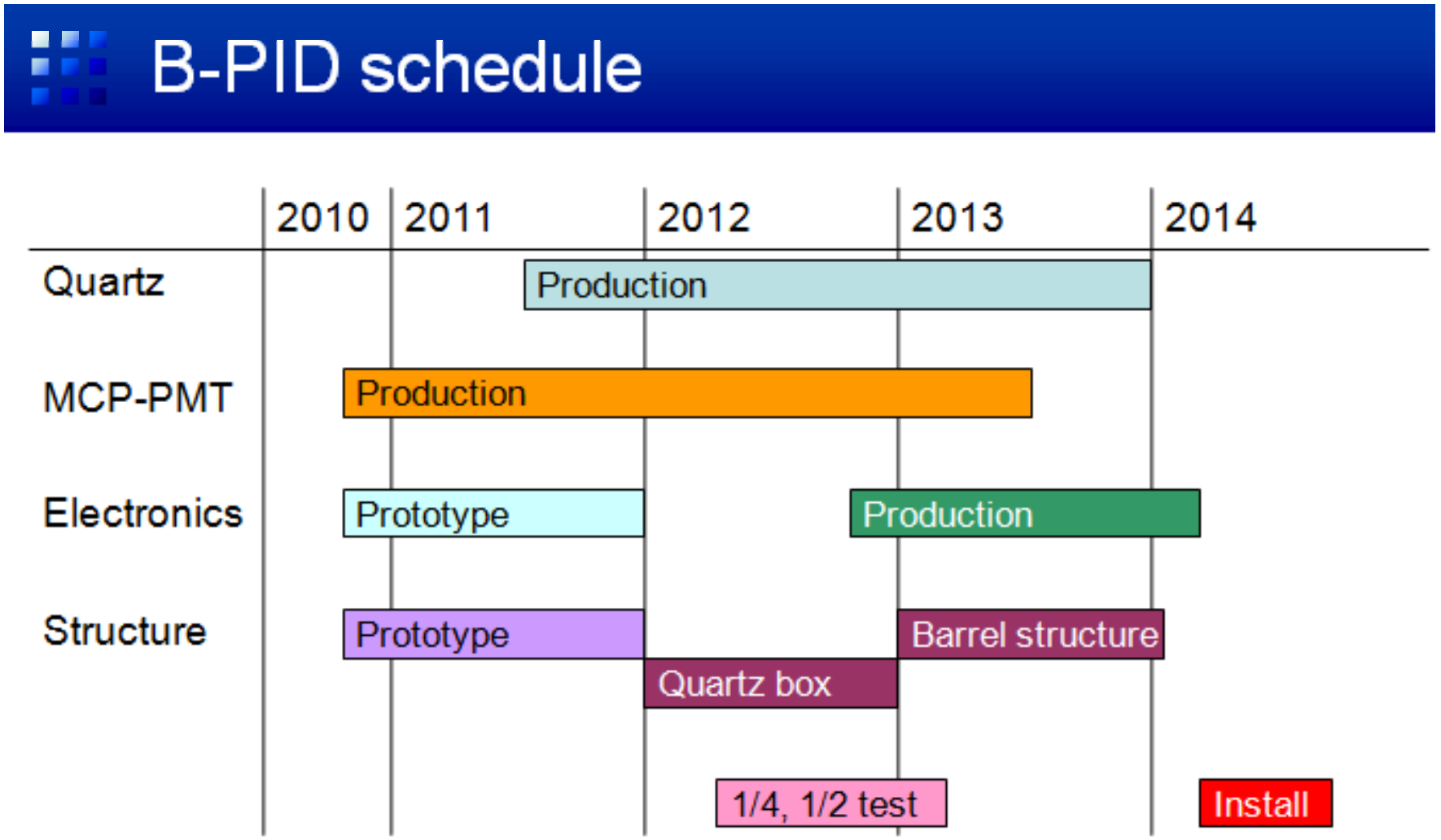
- Still many factors uncertain: (a) collection efficiency of background photons, (c) calculated for a total integrated luminosity of 200 ab^{-1}, need only 50 (Peter Krizan's comment), etc.
- However, starting from the same assumtions, FDIRC detectors have ~ 2-3x smaller pixel rate, and 8-10x smaller total charge dose/cm^2 compared to the TOP counter's detectors.

Data link margin (re-visited)

- Can work problem from other direction:
  - 2.4Gbps (on 3Gbaud link)
  - At 30kHz L2 (100ns window, 0.3% RealTime)
- 24kbits/event for 512 bits/hit = 48 hits/link
  - ~200 hits/event/iTOP counter
  - Expect ~4 background p.e./event

- Maintain > 10x link margin

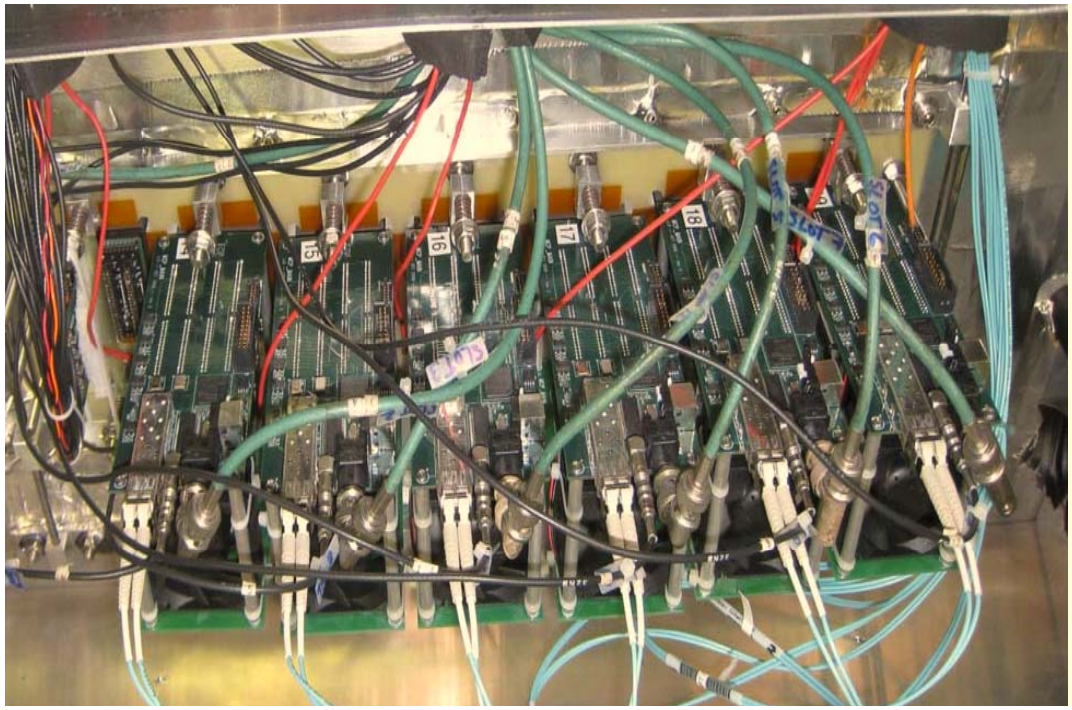
Schedule update



Important iTOP Milestones

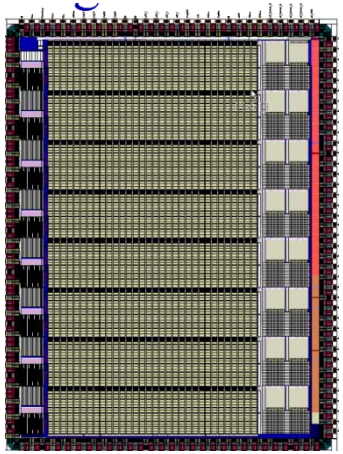
- Experience with chromatic correction in fDIRC prototype (upgrade to Belle II prototype waveform ASIC + DSP feature extraction) [this year]

Cosmic test stand @ SLAC
~400 channels

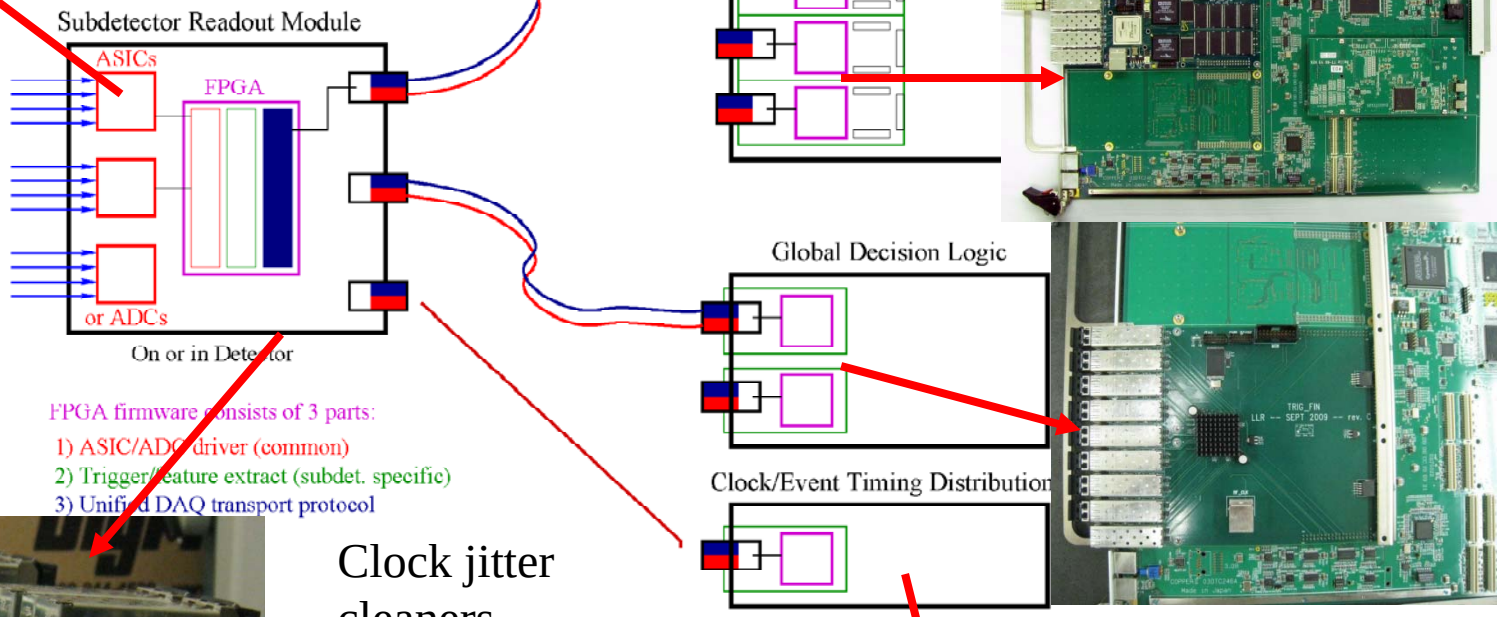


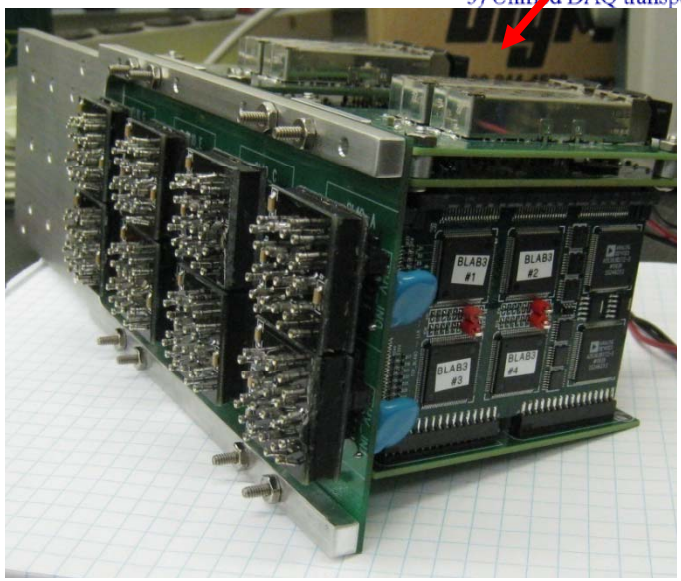
- 1/16th test system (25ps system timing)
- Beam test (cosmic test) of full iTOP module

Major milestone:1/16 system test

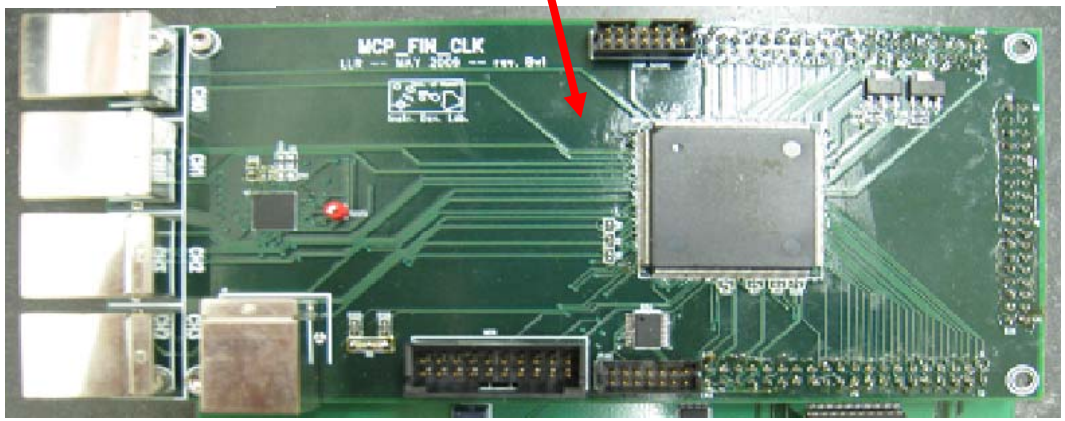


Third generation waveform sampling ASIC



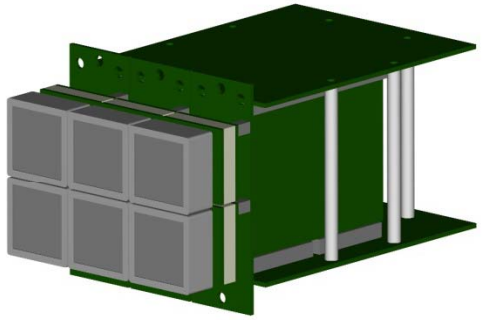


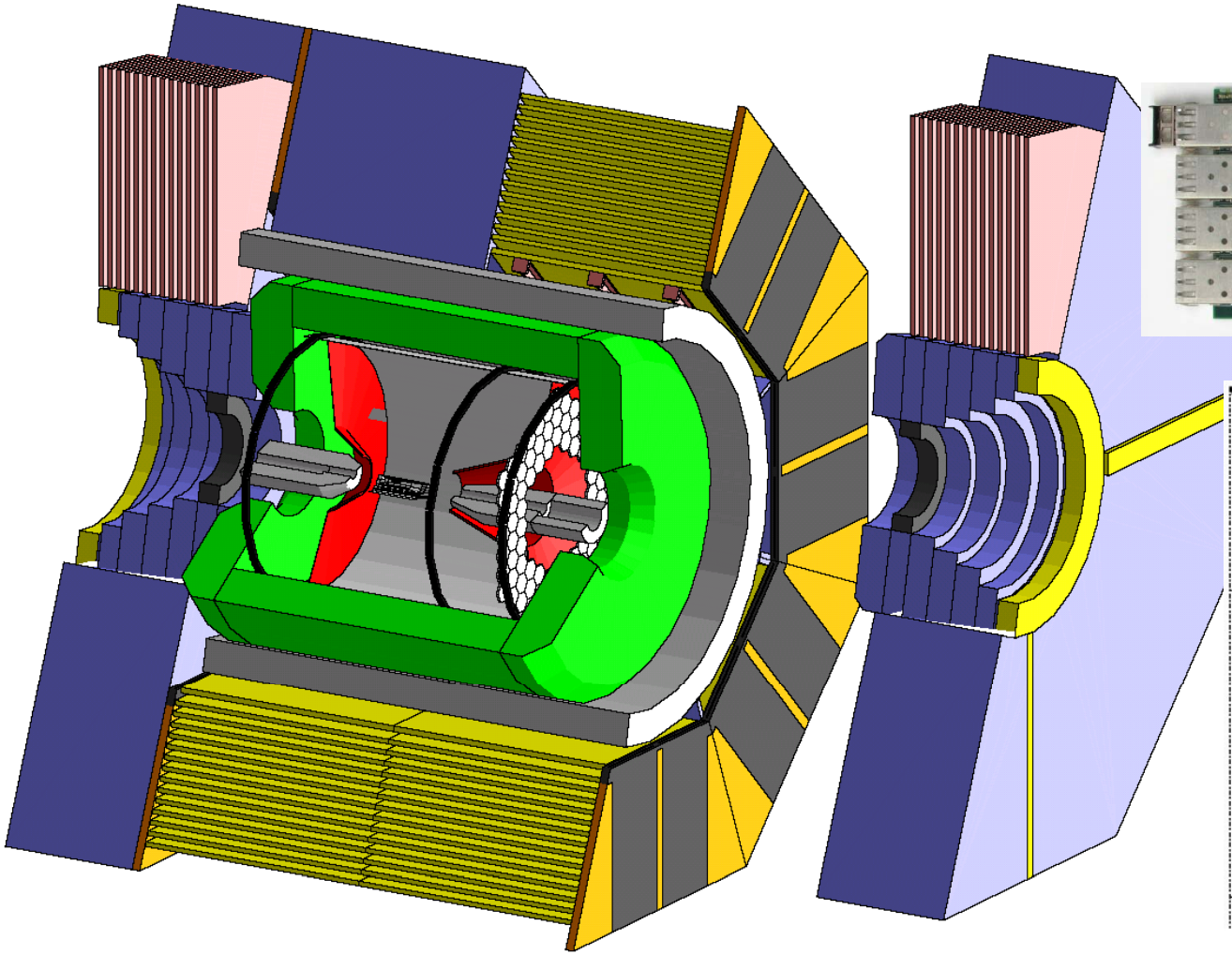
Clock jitter cleaners

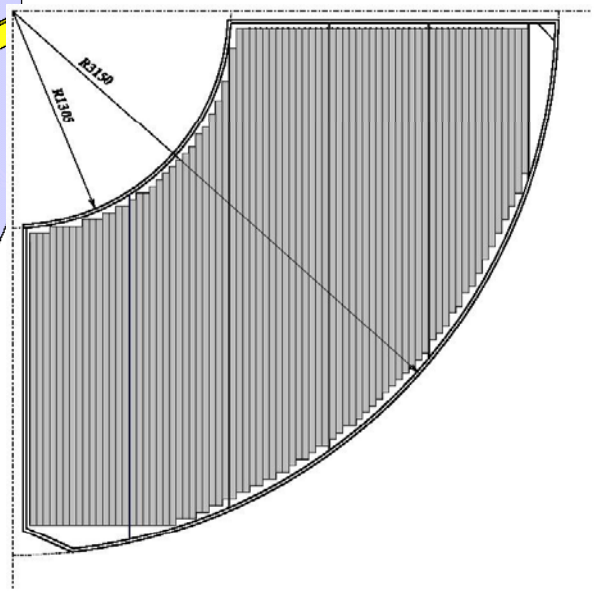


iTOP & KLM Electronics

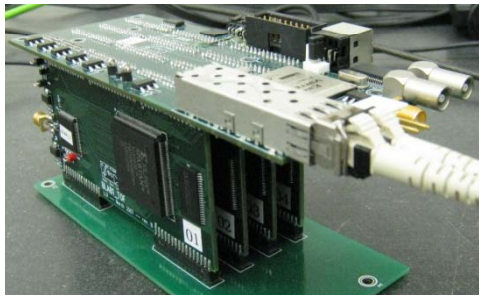
- US Role in Electronics and Trigger/DAQ





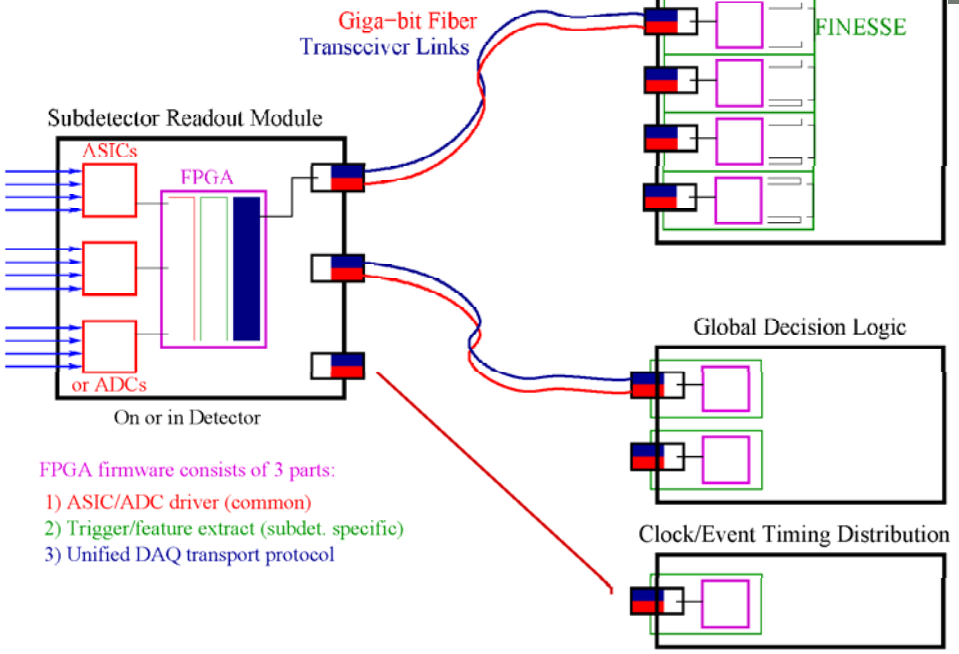


Endcap KLM Readout – very similar

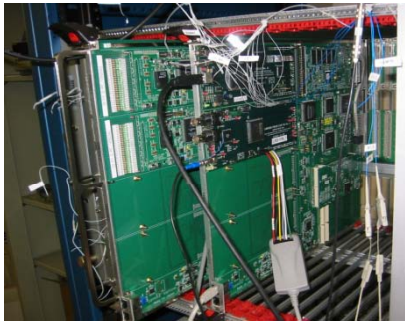


16.8k channels
1.1k 16-channel
Waveform sampling
ASICs
112 SRM

112 DAQ fiber
transceivers

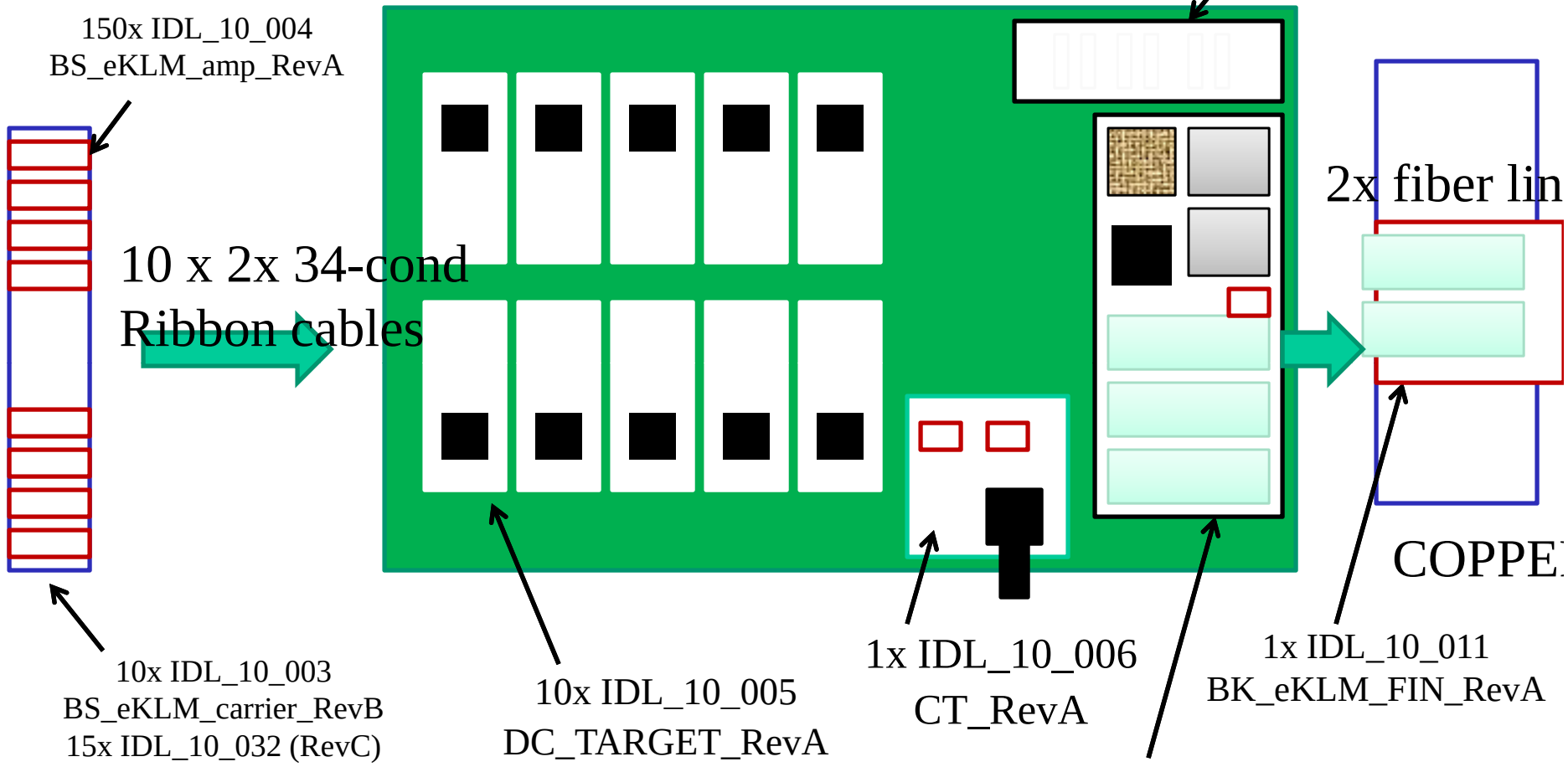


28 FINESSE
7 COPPER



Barrel KLM Readout
– No ASIC – FPGA as digitizer

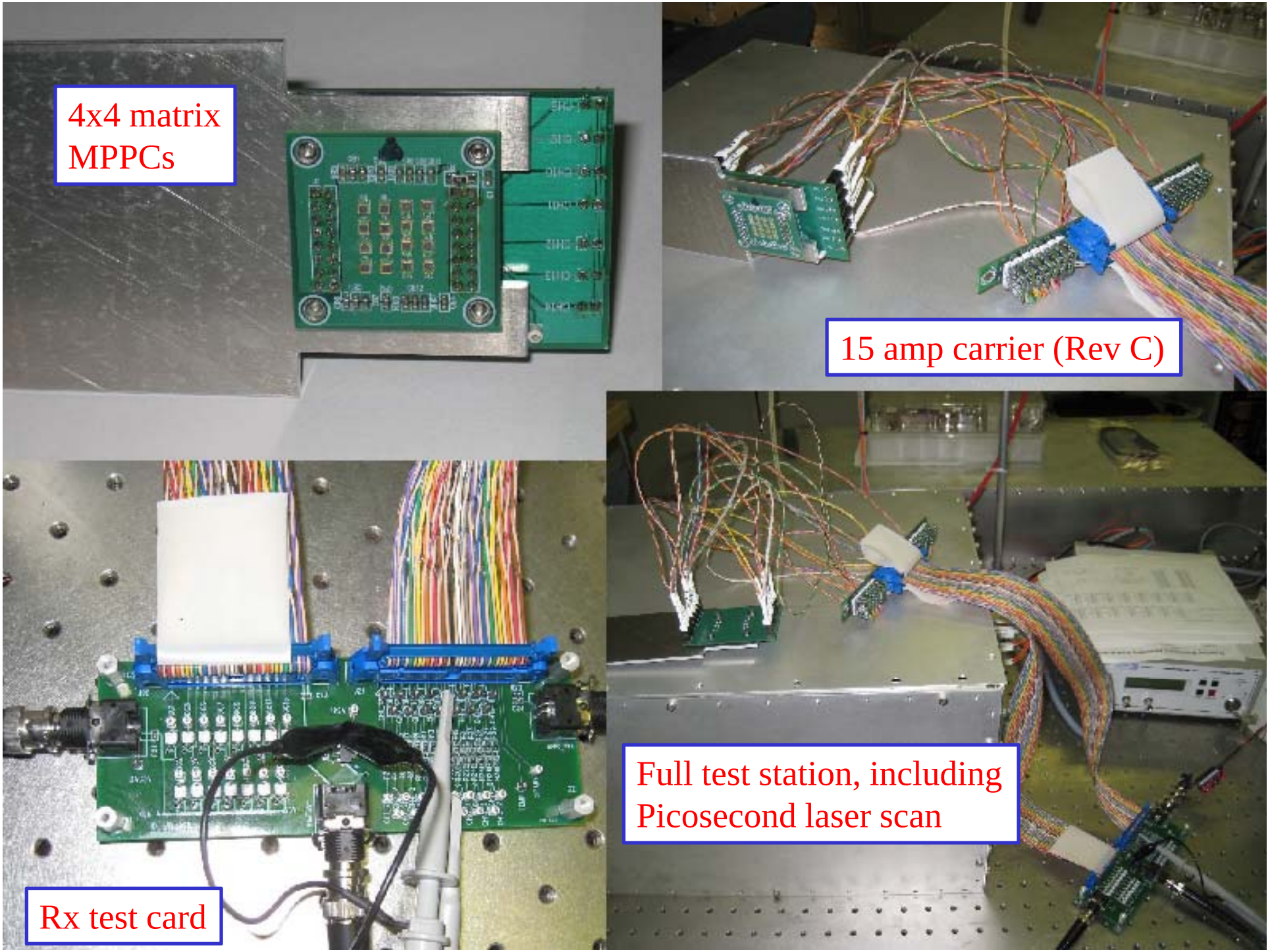
KLM Readout (150 channels)



Purely test cards:

2x IDL_10_002
BS_eKLM_test_RevA

2x IDL_10_010
BS_eKLM_MPPC_RevA

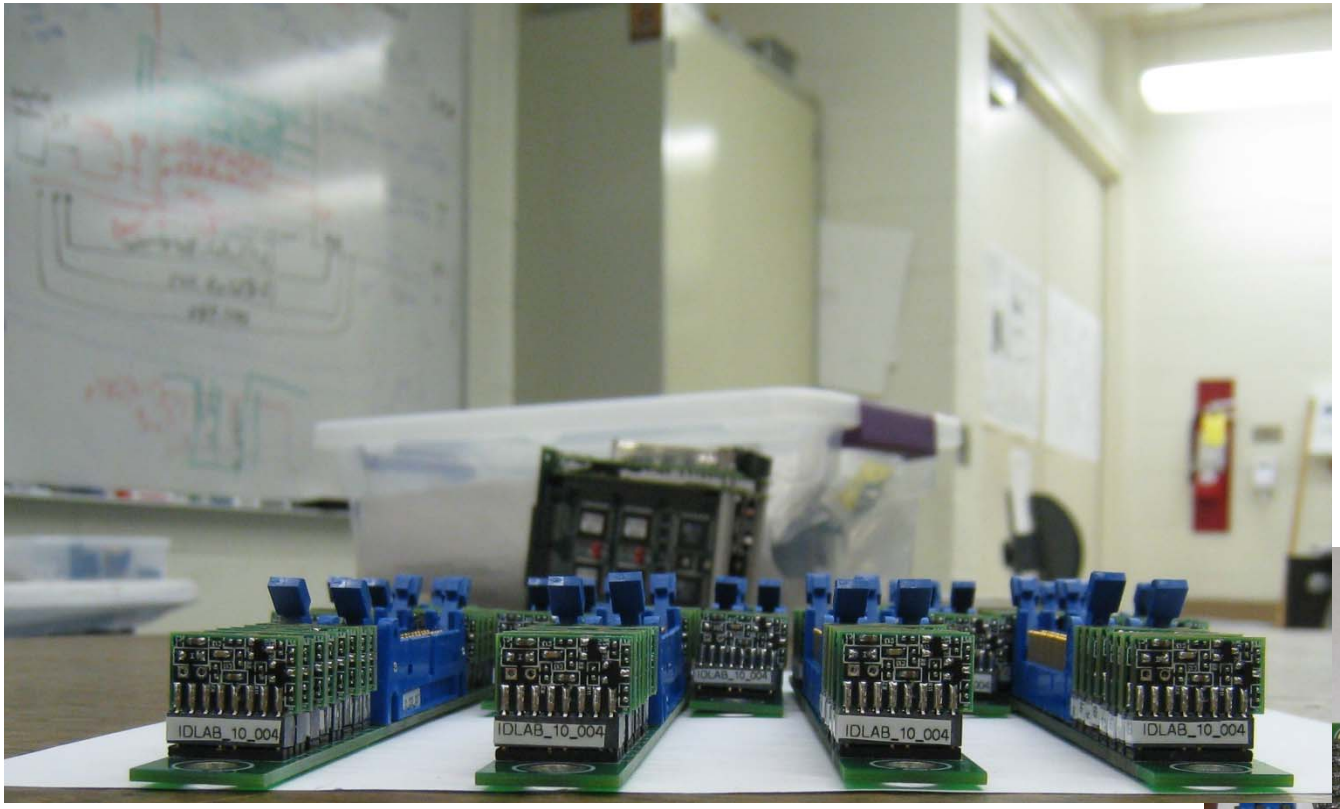

4x4 matrix
MPPCs
15 amp carrier (Rev C)
Full test station, including
Picosecond laser scan
Rx test card

Sample (zoomed out) waveform

PiLas Laser (1MHz rep rate)
All 15 channels OK

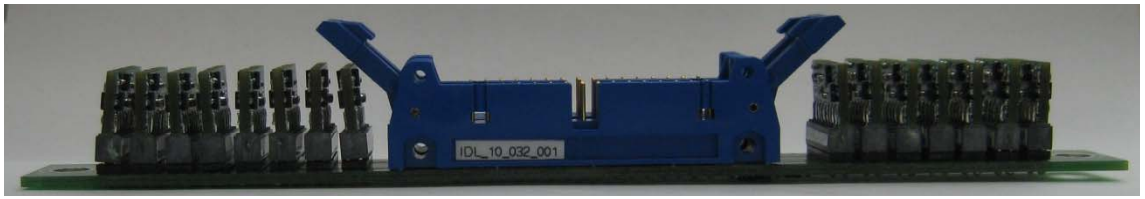
Delivered IHEP Nov 2010

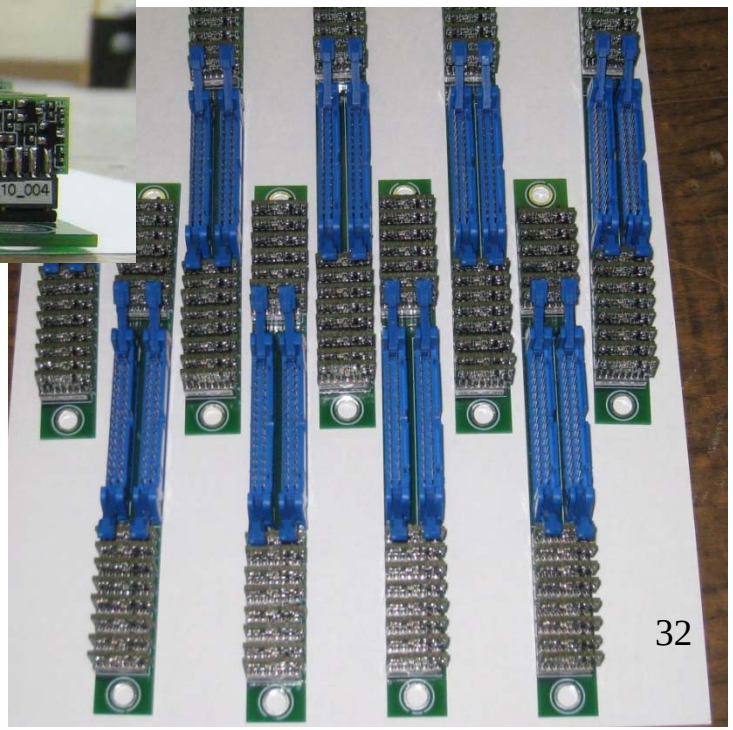
eKLM Production Amps



Production Batch complete

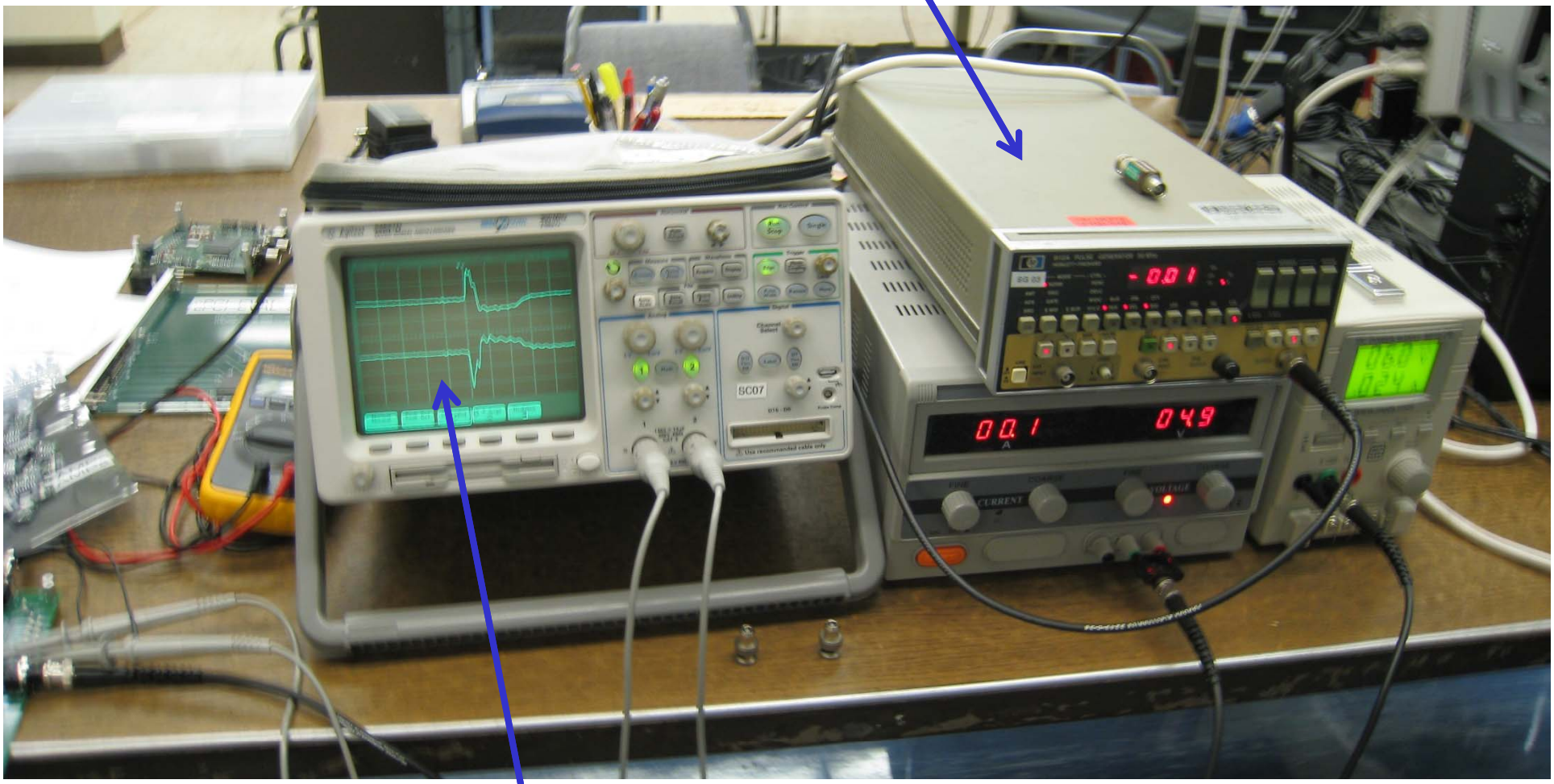
All channels tested OK





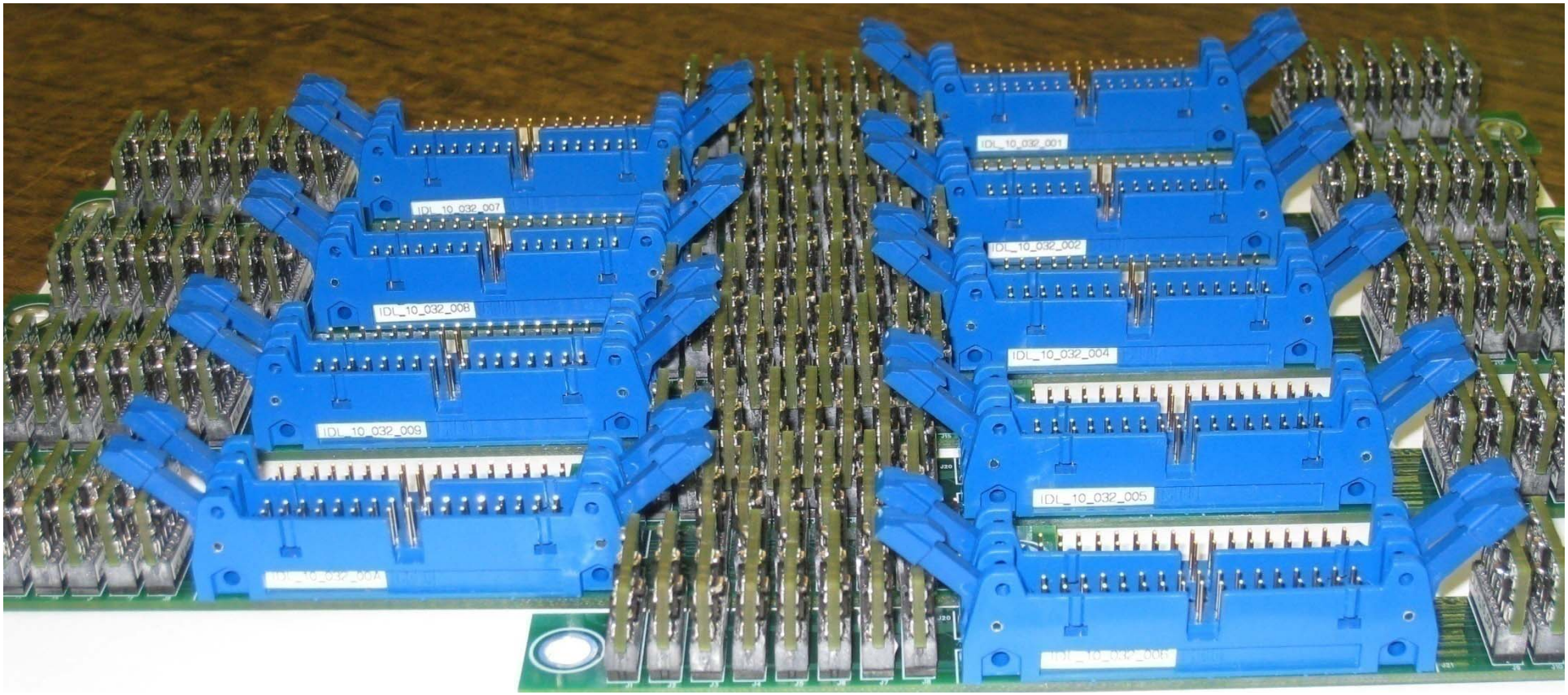
Amplifier test stand

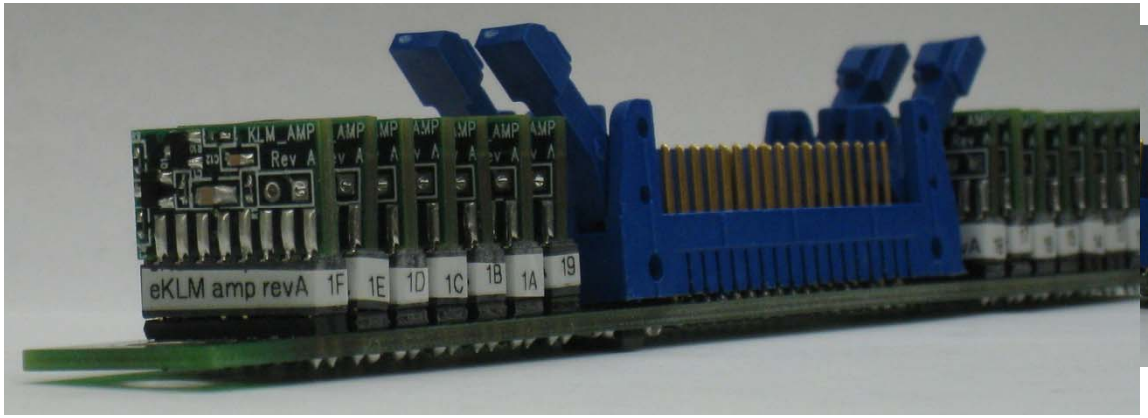
Signal generator (10ns pulse)

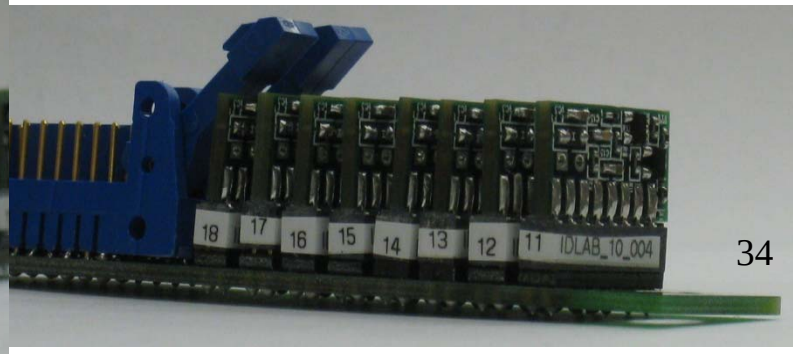


Amplifier output

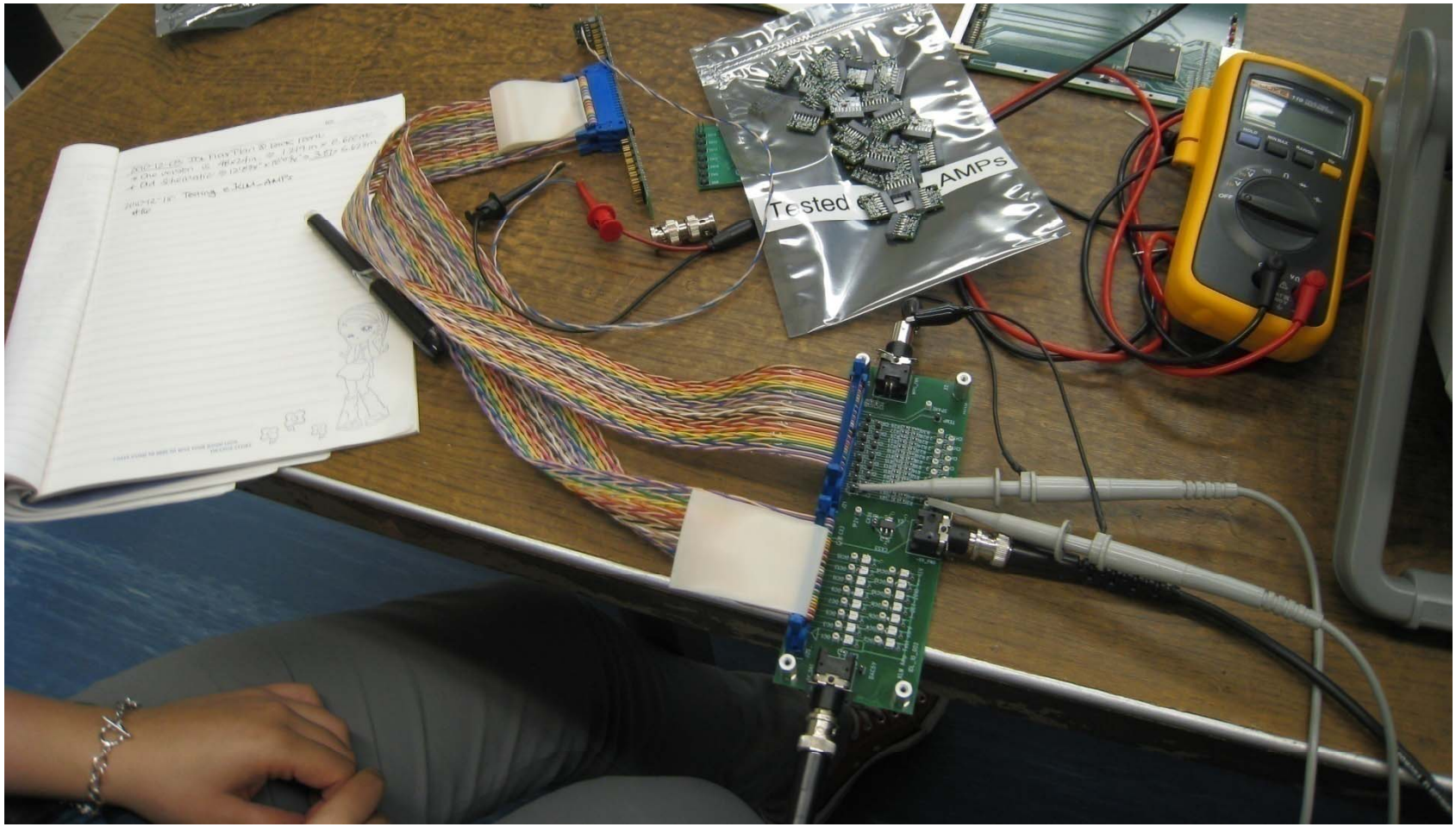
eKLM Production Amps





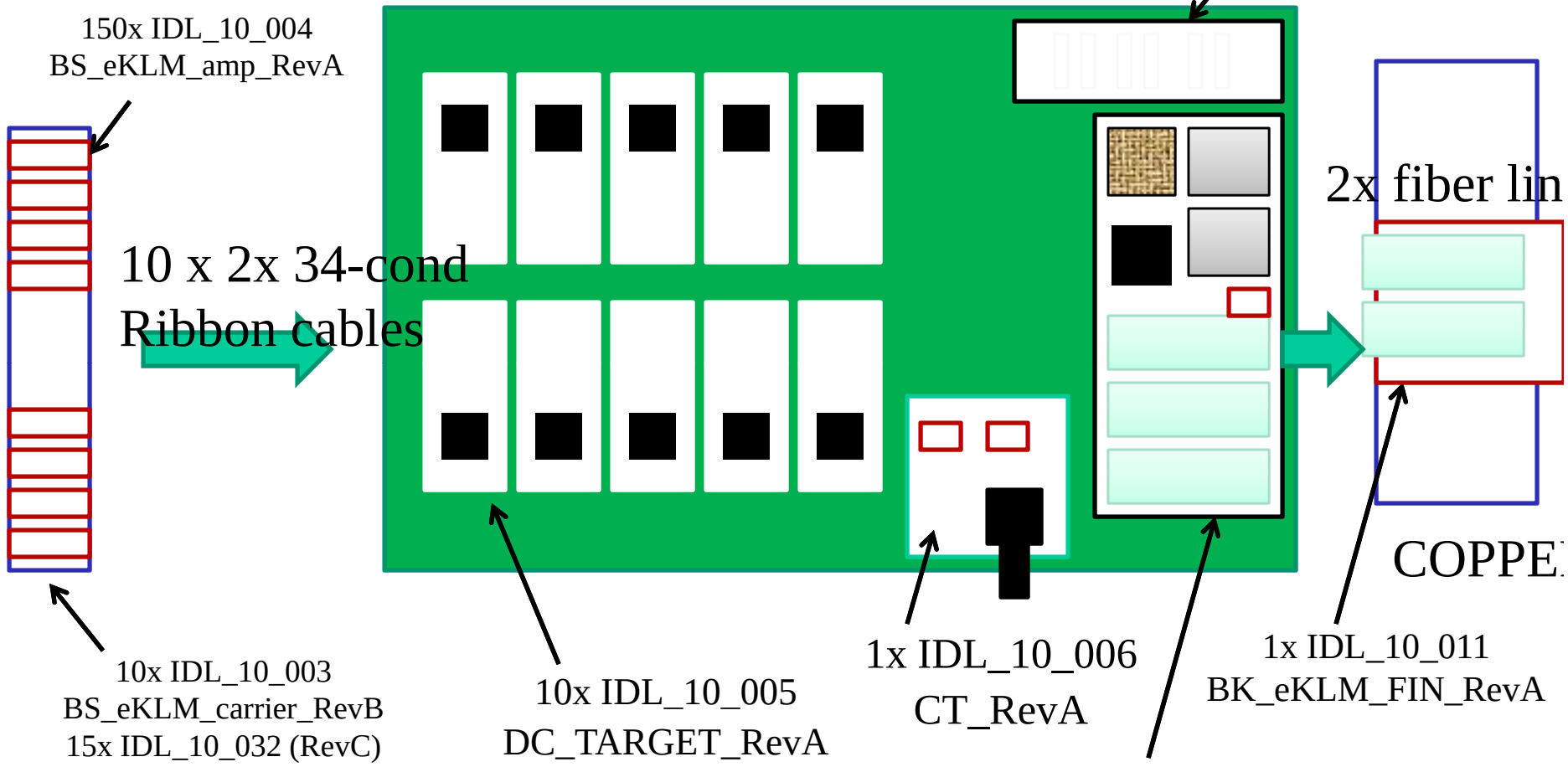


Test card zoom



Production batch of 150 amps tested. 5 needed rework.

KLM Readout (150 channels)

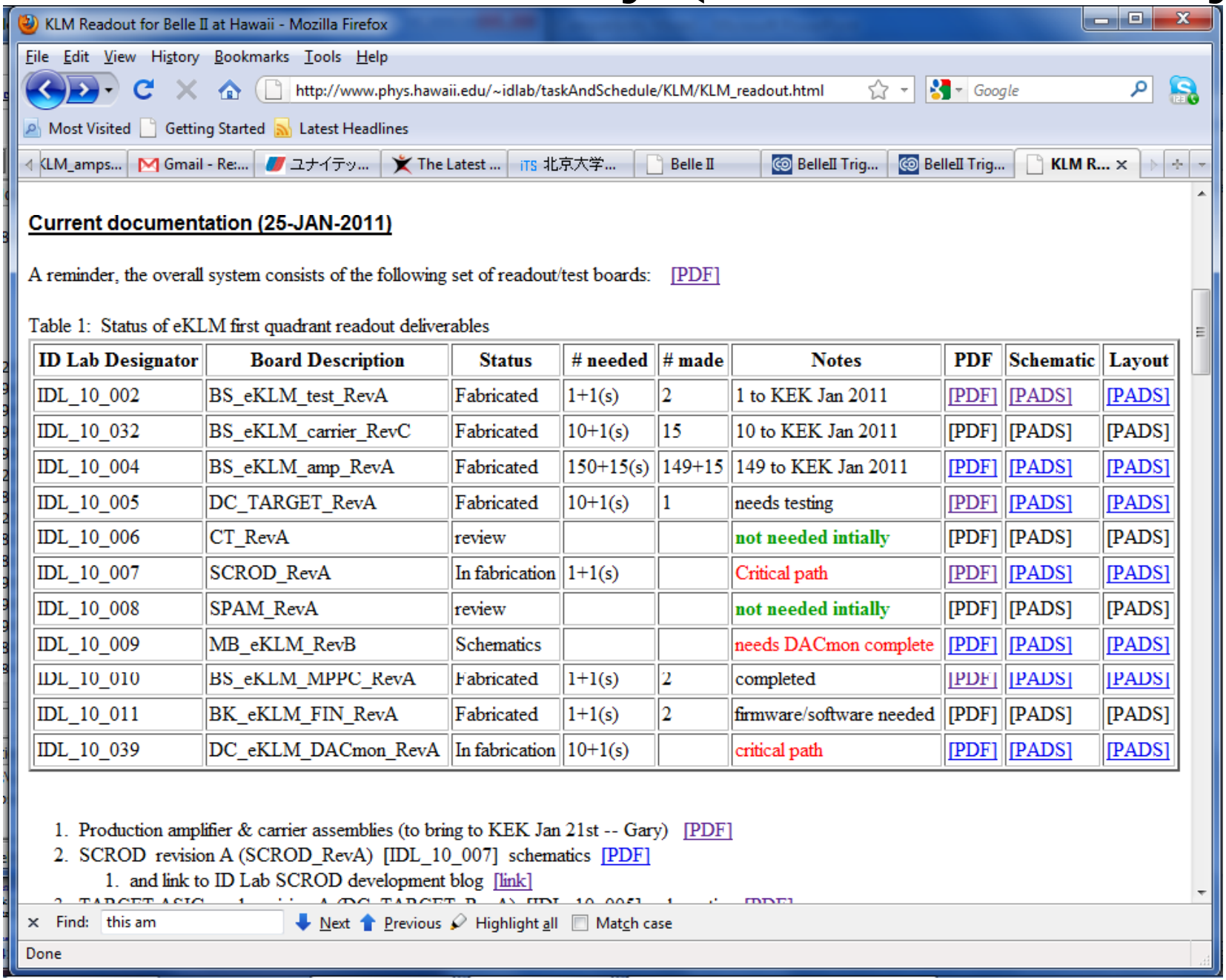


Purely test cards:

2x IDL_10_002
BS_eKLM_test_RevA

2x IDL_10_010
BS_eKLM_MPPC_RevA

Current Board summary (mid Feb delivery)



Current documentation (25-JAN-2011)

A reminder, the overall system consists of the following set of readout/test boards: [PDF]

Table 1: Status of eKLM first quadrant readout deliverables

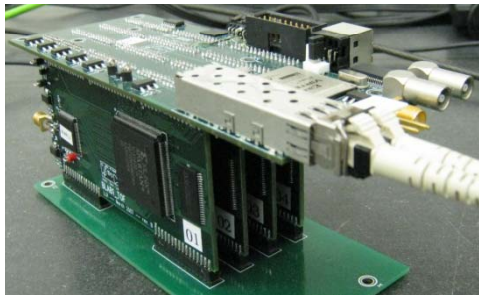
ID Lab Designator	Board Description	Status	# needed	# made	Notes	PDF	Schematic	Layout
IDL_10_002	BS_eKLM_test_RevA	Fabricated	1+1(s)	2	1 to KEK Jan 2011	[PDF]	[PADS]	[PADS]
IDL_10_032	BS_eKLM_carrier_RevC	Fabricated	10+1(s)	15	10 to KEK Jan 2011	[PDF]	[PADS]	[PADS]
IDL_10_004	BS_eKLM_amp_RevA	Fabricated	150+15(s)	149+15	149 to KEK Jan 2011	[PDF]	[PADS]	[PADS]
IDL_10_005	DC_TARGET_RevA	Fabricated	10+1(s)	1	needs testing	[PDF]	[PADS]	[PADS]
IDL_10_006	CT_RevA	review			not needed intially	[PDF]	[PADS]	[PADS]
IDL_10_007	SCROD_RevA	In fabrication	1+1(s)		Critical path	[PDF]	[PADS]	[PADS]
IDL_10_008	SPAM_RevA	review			not needed intially	[PDF]	[PADS]	[PADS]
IDL_10_009	MB_eKLM_RevB	Schematics			needs DACmon complete	[PDF]	[PADS]	[PADS]
IDL_10_010	BS_eKLM_MPPC_RevA	Fabricated	1+1(s)	2	completed	[PDF]	[PADS]	[PADS]
IDL_10_011	BK_eKLM_FIN_RevA	Fabricated	1+1(s)	2	firmware/software needed	[PDF]	[PADS]	[PADS]
IDL_10_039	DC_eKLM_DACmon_RevA	In fabrication	10+1(s)		critical path	[PDF]	[PADS]	[PADS]

1. Production amplifier & carrier assemblies (to bring to KEK Jan 21st -- Gary) [PDF]
2. SCROD revision A (SCROD_RevA) [IDL_10_007] schematics [PDF]
    1. and link to ID Lab SCROD development blog [link]

Open issues

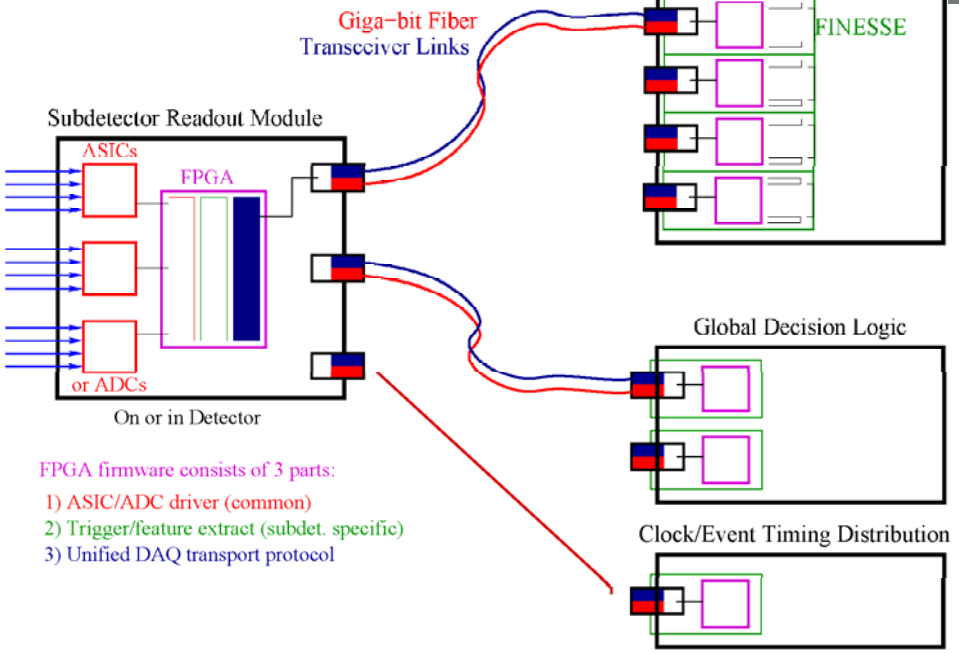
- Much firmware work needed
- Full-time firmware engineer hired
  - Implement Belle2link
  - Make “transparent” to rest of Trg/DAQ
- Full time DSP engineer hired (DSP_FIN)
- Use Belle2link FINESSE for eKLM?

Endcap KLM Readout – status

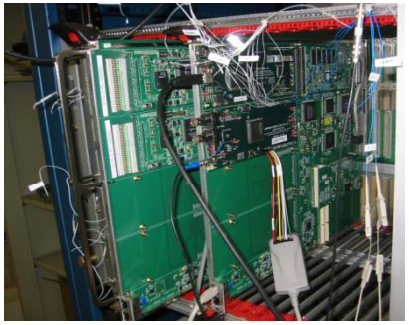


16.8k channels
1.1k 16-channel
Waveform sampling
ASICs
112 SRM

112 DAQ fiber
transceivers



28 FINESSE
7 COPPER



- First quadrant test this spring (firmware?)
- next version: TARGET2, Belle2link

Summary

- Good progress, much to be done
- Next generation “production prototypes”:
  - Evaluate functionality/capability
  - Experience with Belle2link protocol
  - Specifications? (→ Hawaii)
- New manpower, need to train
- Schedule resource driven

Back-up slides

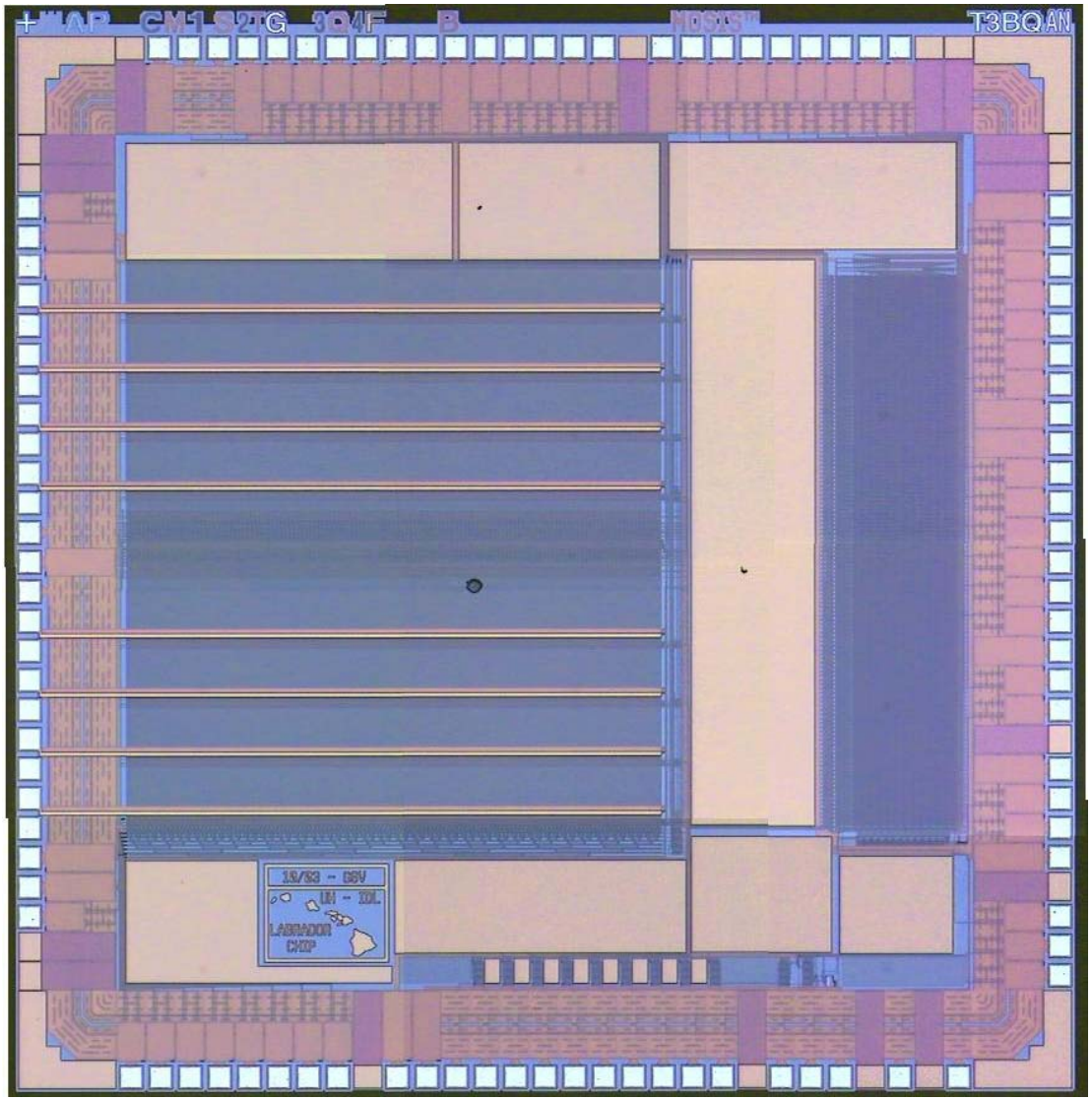
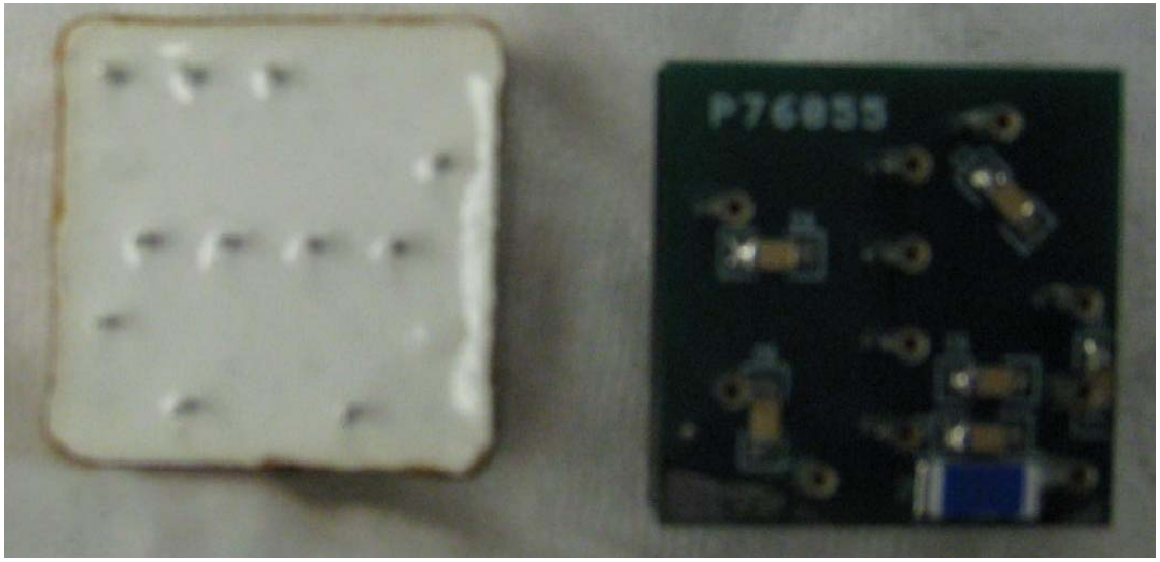
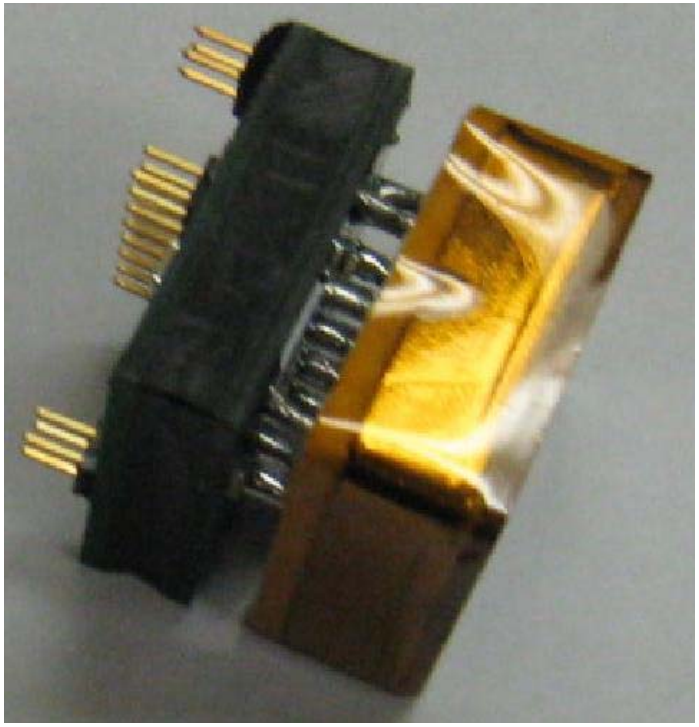


Photo-detector: Hamamatsu SL-10

- Micro-channel Plate:
  - Operates in 1.5T B-field
  - <50ps single photon timing
- Multi-pixel (4x4 anode pads)
- Enhanced Lifetime (Al protection layer)
- Interesting mechanical challenges (PMT case at HV)

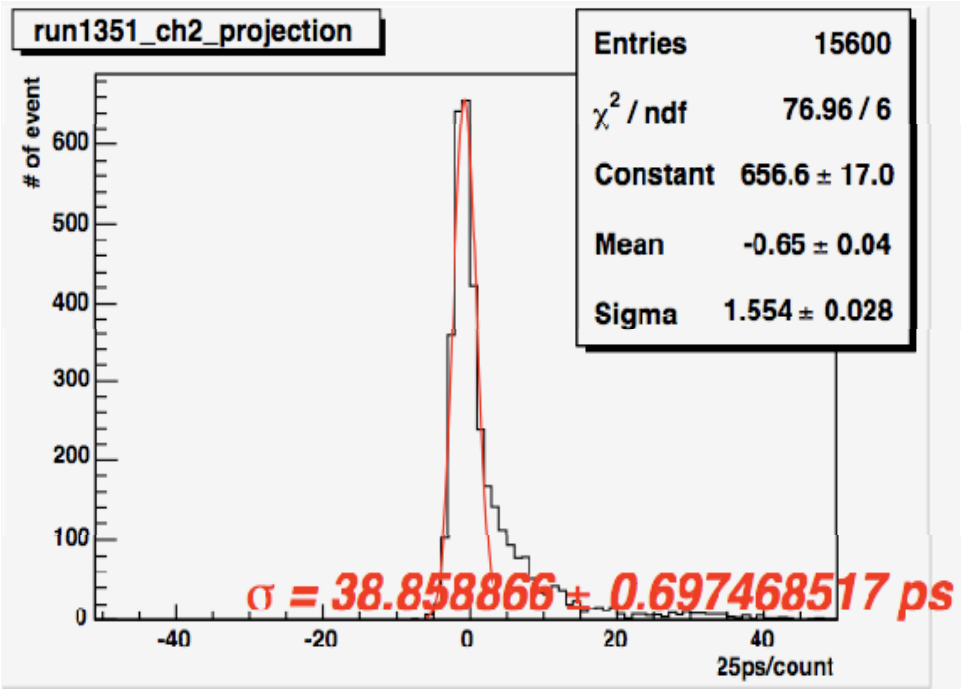


Approximately 1” x 1”

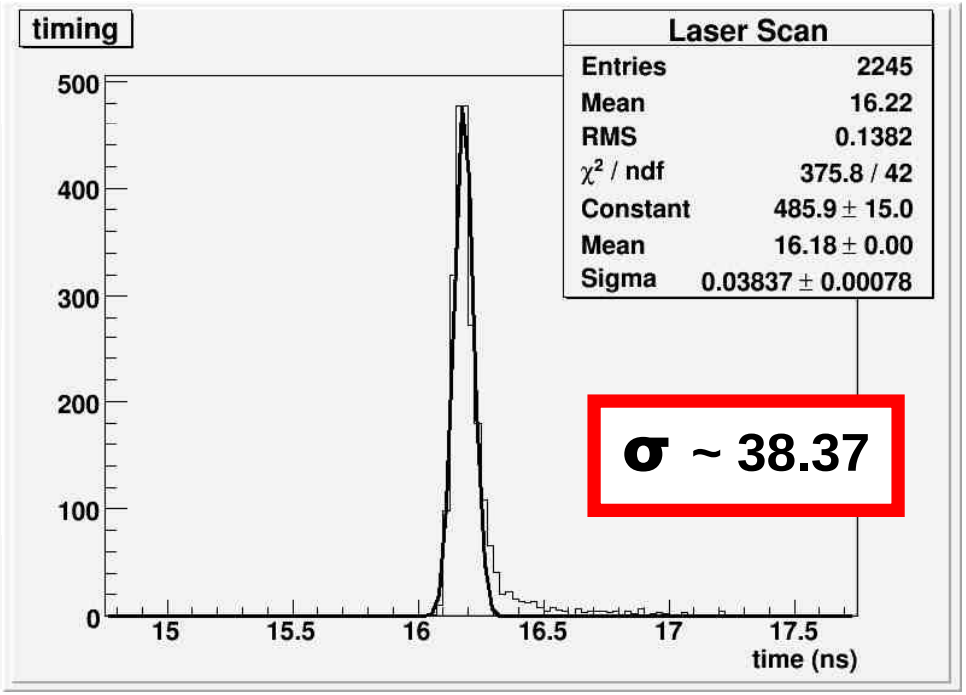


SL-10 Timing Performance

Nagoya



Hawai'i



- Nagoya = constant fraction discriminator + CAMAC ADC/TDC
- Hawai'i = waveform sampling + feature extraction

KLM 15 Ch. Amp test card = IDL_10_002

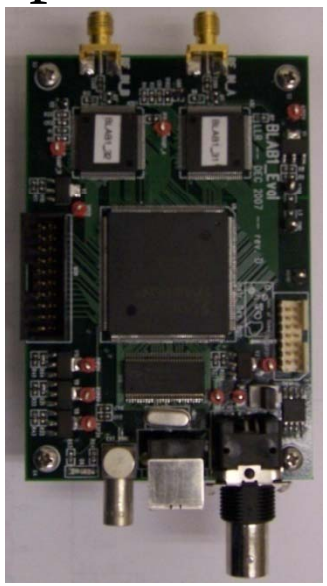
Enumeration	Designator	Descriptor
IDL_10_002_00	HRD	Human Readable Document (describe descendant design, revision info)
IDL_10_002_01	ICD	Interface Control Document (all a designer needs to know if treat board as black box – typically spreadsheet of pins with their function defined)
IDL_10_002_02	Schematics (source)	Typically PADS
IDL_10_002_03	Schematics (PDF)	Easily viewable rendering
IDL_10_002_04	Layout (PADS)	Current edited version
IDL_10_002_05	Gerbers	As submitted for fabrication
IDL_10_002_06	BOM	Bill of Materials (complete)
IDL_10_002_07	DXF	Board outline/mounting holes (opt.)
IDL_10_002_08	Firmware descriptor	Human readable: revisions, etc.
IDL_10_002_09	Firmware (source)	Current source or SVN/CVS link
IDL_10_002_10	Software (source)	Current source or SVN/CVS link With human readable descriptor

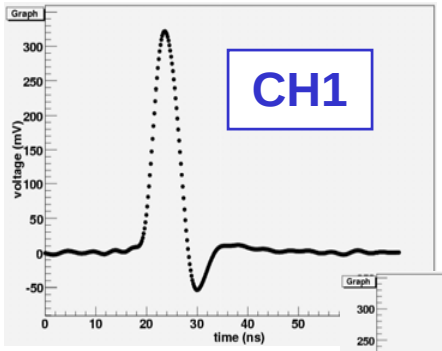
And more as needed

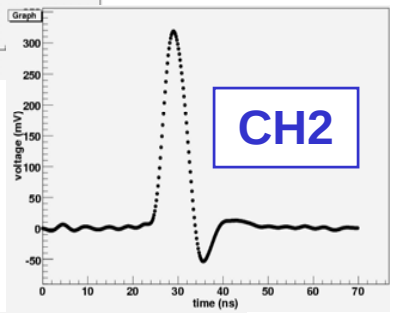
High speed Waveform sampling

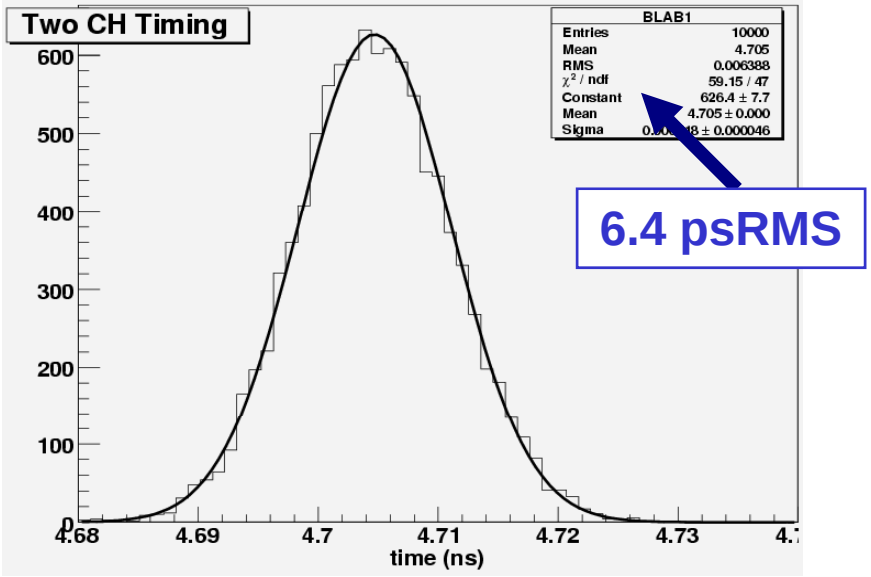
"oscilloscope on a chip"

- Comparable performance to best CFD + HPTDC
- MUCH lower power, no need for huge cable plant!
- Using full samples reduces the impact of noise
- Photodetector limited









NIM **A602** (2009) 438

→Advanced Detector Research award