Belle II DAQ Requirements Summary

Mikihiko Nakao (KEK-IPNS)

mikihiko.nakao@kek.jp

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Outline

- **Dataflow numbers** (Belle2link, COPPER, event-builder, datasize)
- **Timing constraints** (to synchronize and to minimize deadtime)
- **Frontend interface** (Belle2link, timing link, JTAG)
- **Cabling** (dataflow, timing, power, ground)
- **Slow control** (CPU, localrun, database)

Assumptions

- 20 times background, occupancy from detector groups
- 30 kHz L1 trigger rate at 8×10^{35} cm^{-2}s^{-1}
  - 20 kHz is expected by scaling Belle I, 0.5 kHz at 2×10^{34}
    (too simplified? but these are the numbers from Y.Iwasaki)
- Factor 3+ reduction at HLT
  - Factor 6 reduction is difficult without sacrificing efficiency, at least 5 kHz for physics+calib triggers (B:1.0, udsc:2.2, τ:0.6, μ:0.6, e^+e^-:0.4, two-photon:~0)
  - PXD data reduction according to the HLT physics type?

Dataflow numbers

Dataflow numbers are the baseline information to design the Belle II DAQ system, namely, to determine:

- Number of modules to be produced
- COPPER and event-builder layout design
- Dataflow balancing (bandwidth and latency)
- Cabling and electronics near the detector
- Datasize and offline computing

But there are several questions due to simplification:

- Background level is not precisely known
- Non-uniformity of the occupancy
- Expected / Nominal / Maximum?
- Special operation (e.g., local run)

The Table

	#ch	occ [%]	#link	/link [B/s]	FNS	#CPR	ch sz [B]	ev sz [B]	total [B/s]	/CPR [B/s]
PXD	8M	2	40	364M	—	—	4	320k	14.4G	—
SVD	243456	1.9	40	13.8M	HSLB	40	4	18.5k	555M	13.8M
CDC	15104	10	302	0.6M	HSLB	75	4	6k	175M	2.3M
BPID	8192	2.5	128	7.5M	DSP	16	16	4k	120M	8M
EPID	77760	1.3	138	0.87M	HSLB	35	0.5	4k	120M	15M
ECL	8736	33	52	7.7M	HSLB	26	4	12k	360M	15M
BKLM	21696	1	86	9.7M	DSP	6	8	2K	60M	10M
EKLM	16800	2	66	19.5M	DSP	5	4	1.4k	42M	5.3M
TRG					HSLB	60				

- Occupancy: nominal values
- Margins: B2link bandwidth, COPPER throughput
- Maintained in Belle II Twiki — any updates?

Occupancy Non-uniformity

- **The closer to the beampipe, the higher the occupancy**
- **Frontend electronics layout driven by detector configuration and cabling, not by occupancy**
  - **PXD**
  - **SVD**
  - **CDC**
  - **ECL**
- **Design the system according to the maximum?**
- **Is there anything else that can be done?**

Number of modules and crates

- **Timing distribution and JTAG link**
  - **FTSW: 1-to-8 (cat7/opt) / 1-to-12 (opt/cat7) / 1-to-20 (cat7/cat7)**
  - **One cat7/opt module in E-hut per detector**
    Several opt/cat7 module near the detector
  - **CDC — 1-to-4 × 1-to-4 × 1-to-20 (timing)**
    1-to-4 × 1-to-4 × 1-to-20 (JTAG)
    (10-module 6U crate × 4 near the detector, total=40)
  - **ECL — 1-to-6 × 1-to-12, opt/cat7 in the collector crate**
  - **To be decided for other detectors**
- **COPPER modules and crates**
  - **263 COPPER modules according to The Table**
  - **SVD:3 CDC:5 BPID:1 EPID:3 ECL:2 BKLM:1 EKLM:1**
    TRG:4 crates, total=20 crates (Belle I used 15)
  - **20 FTSW modules are needed**

Backend configuration

- **15MB/s/COPPER $\times$ 16 /crate $\sim$ 2 $\times$ GbE**
  - **2 readout PC per COPPER crate?**
  - **Or is the readout PC fast enough to handle 2 GbE / PC?**
- **40 $\times$ GbE is expected**

Clock

- **Source: RF clock (508.877 MHz) and revolution (99.390 kHz)**
- **TTD clock — RF/4 127.219 MHz, how to generate is not decided yet (also referred to as system clock)**
- **TTD local clock — when RF is not available**
  Frequency close to the RF (127.2 MHz) from on-board Xtal
  Should be available at a remote test bench, too
- **Derived clock — easily done by DCM/PLL in FPGA**
  Available in the timing receiver core at the frontend board
- **Distributed to frontend boards and COPPER**
  Should be distributed to trigger boards, too
- **Jitter requirement: BPID (<10ps), others to meet RocketIO**
- **Phase drift — not compensated, to be offline corrected**

Pipeline constraints

Based on SVD and COPPER
Need to be revised for ECL by next B2GM

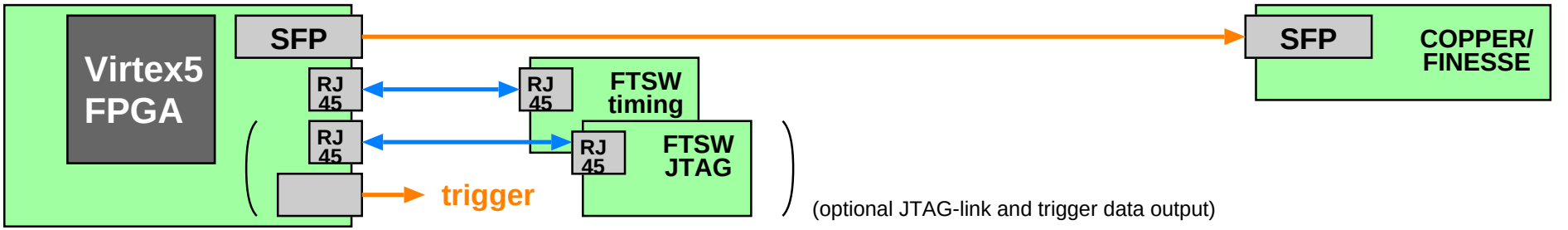
- **Trigger interval: 6 $\times$ 32-MHz-clock (190 ns)**
  - **More than one triggers for same timing window at PXD/ECL**
- **To avoid flow control: 5 triggers simultaneously processed**
  - **6th trigger is not issued (blocked at master TTD)**
- **Readout latency: 840 $\times$ 32-MHz-clock (26.6 μs)**
  - **Maximum time to get ready for the 6th trigger**
  - **If it takes twice more time, one more trigger has to be in pipeline**
  - **Relaxed with deeper buffer (ECL, EPID, . . .)**
- **Maximum event fragment size: 16 kB per datalink**
- **No event reordering**

Event fragment size

- **Cannot allow arbitrary large event fragment**
  - **latency in the data transmission**
  - **number of buffers to allocate**
- **16 kB/link would be a good candidate**
  - **Based on the COPPER buffer size**
  - **ECL requested to read out all channel at low frequency**
  - **Need to specify average event fragment size and absolute maximum**

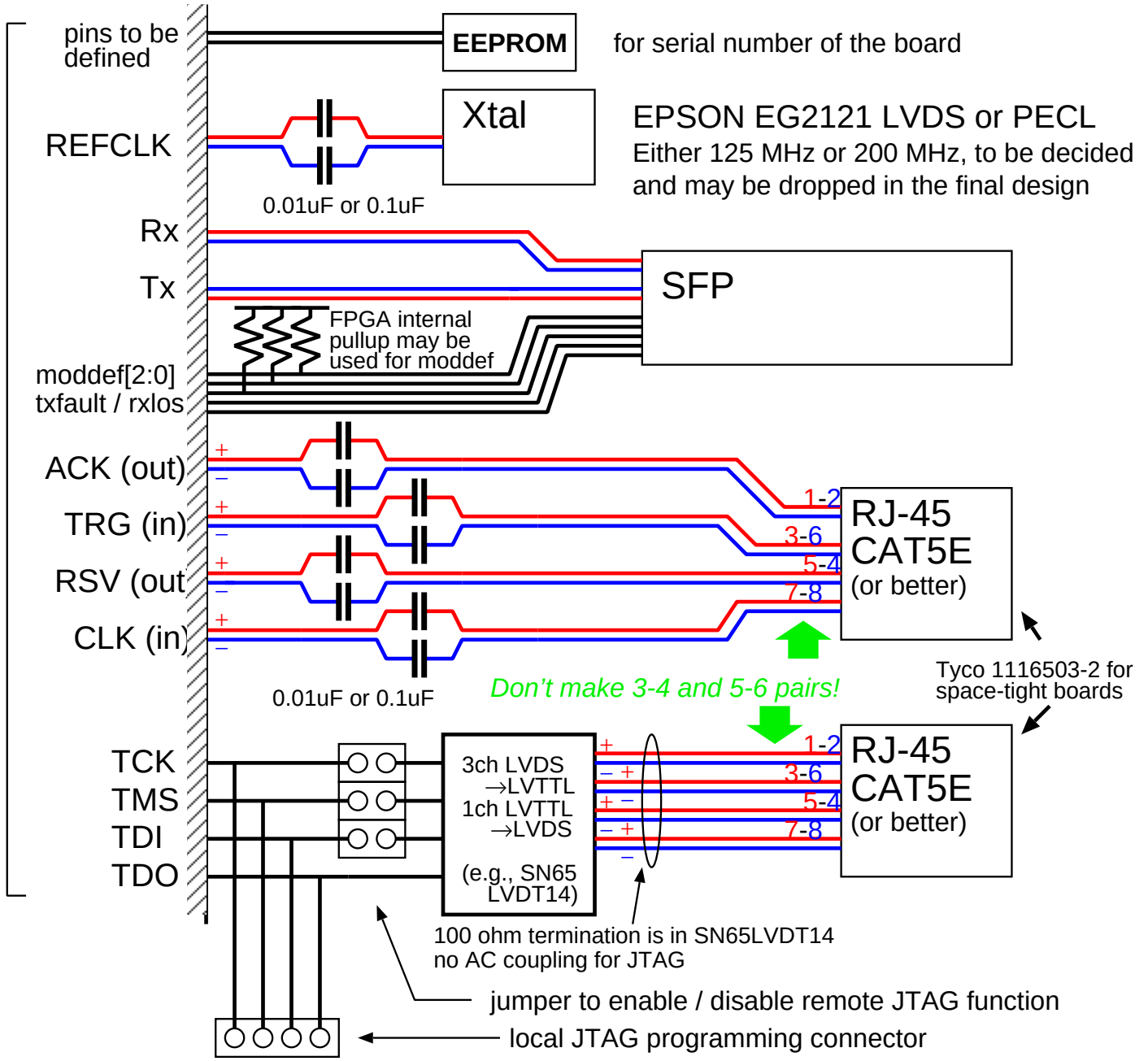
Frontend interface

- **FPGA — Virtex 5 (GTP-RocketIO, ISERDES, SEU recovery)**
  Spartan 6? (GTP-RocketIO, ISERDES2, cost)
- **Connectors — SFP, RJ-45 for timing (+ RJ-45 for JTAG)**
- **Xtal — 125 MHz? (close to 127 MHz, widely available)**
- **AC coupling — REFCLK and RJ-45 timing signal**
  (no AC coupling for the JTAG link, no signal during the run)
- **EEPROM for serial-id of the board**
  (ATMEL AT24C01B, 2-wire protocol proposed by SVD)
- **Power and ground**



Belle2link / timing signal physical interface at the frontend readout board

20101216 version



GTP capable FPGA
Virtex5 LXT is recommended for SEU sensitive area

Pin assignment is partially compatible with Timing Distribution modules of Belle

Power / Ground

- Ground loop must be avoided
- For signals (Belle2link/timing/JTAG-link) no ground connection between E-hut and detector
- Slow control devices and trigger boards should not make the ground loop, too
- For power supplies, ground are from power supplies
  - CDC power supplies (HV and LV) are in E-hut
  - CDC end-plate as the ground plane for frontend boards
  - Power/ground for timing boards to be common to the CDC frontend
  - What is the plan for other detectors?
- If there is a station on the detector, timing module would like to share the location for power/ground
- Ground connection between forward & backward?
  Ground connection between top & bottom?

Fast/slow control path

- A 6U VME crate in E-hut for every subdetector
  - VME CPU (Linux)
  - FTSW to control frontend boards and COPPERs
  - JTAG programming controller
  - Trigger control for the local run
- One sub-detector master PC (readout PC)
  - Server for COPPERs
  - Slow control manager through Belle2link
- Many other VME CPU and PC are foreseen
  - Propose to form a “CPU” group with interested people
    (those who do not care should follow the suggestion)

Summary

- **The dataflow table is stable and useful to design DAQ**
  (no good info / tool yet to update our assumptions)
- **Timing requirement has to be revised based on numbers given by ECL**
- **Hardware spec of the frontend boards is ready**
  (firmware spec is urgently needed)
- **Getting ready to think about module allocation and cabling**
- **Numbers are maintained at TWiki, any feedback is welcome**