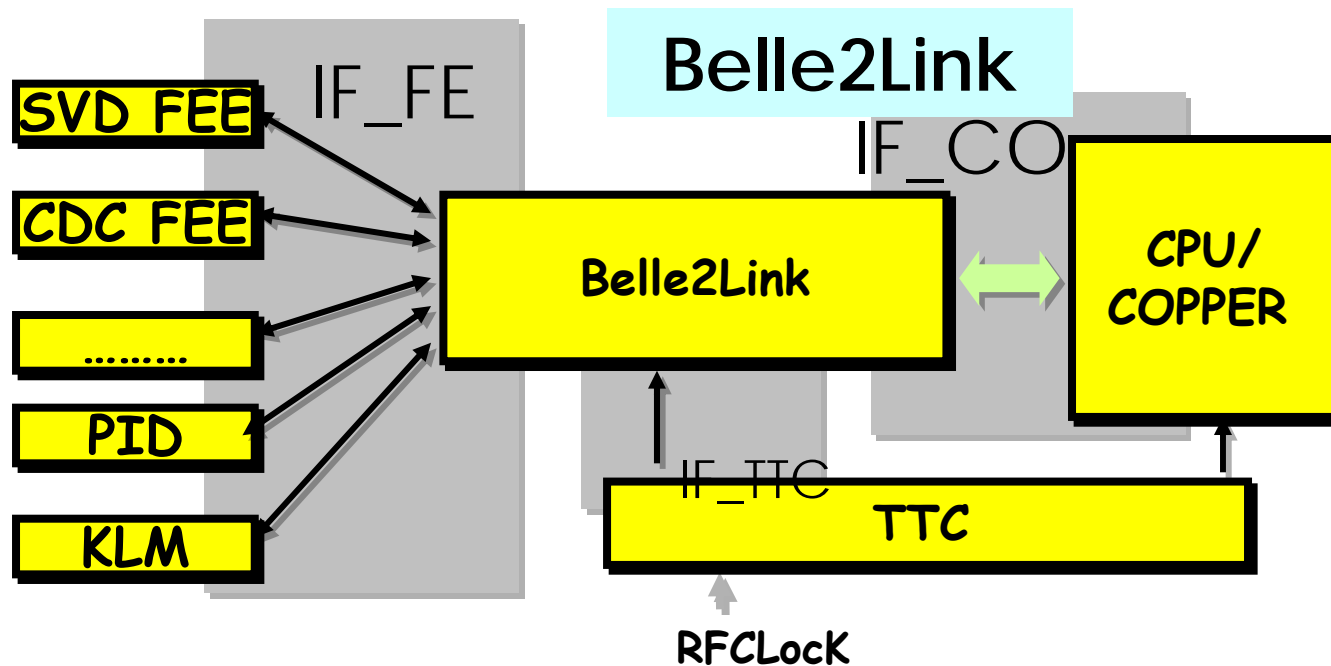# HSLB development in Belle2Link

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HSLB introduction
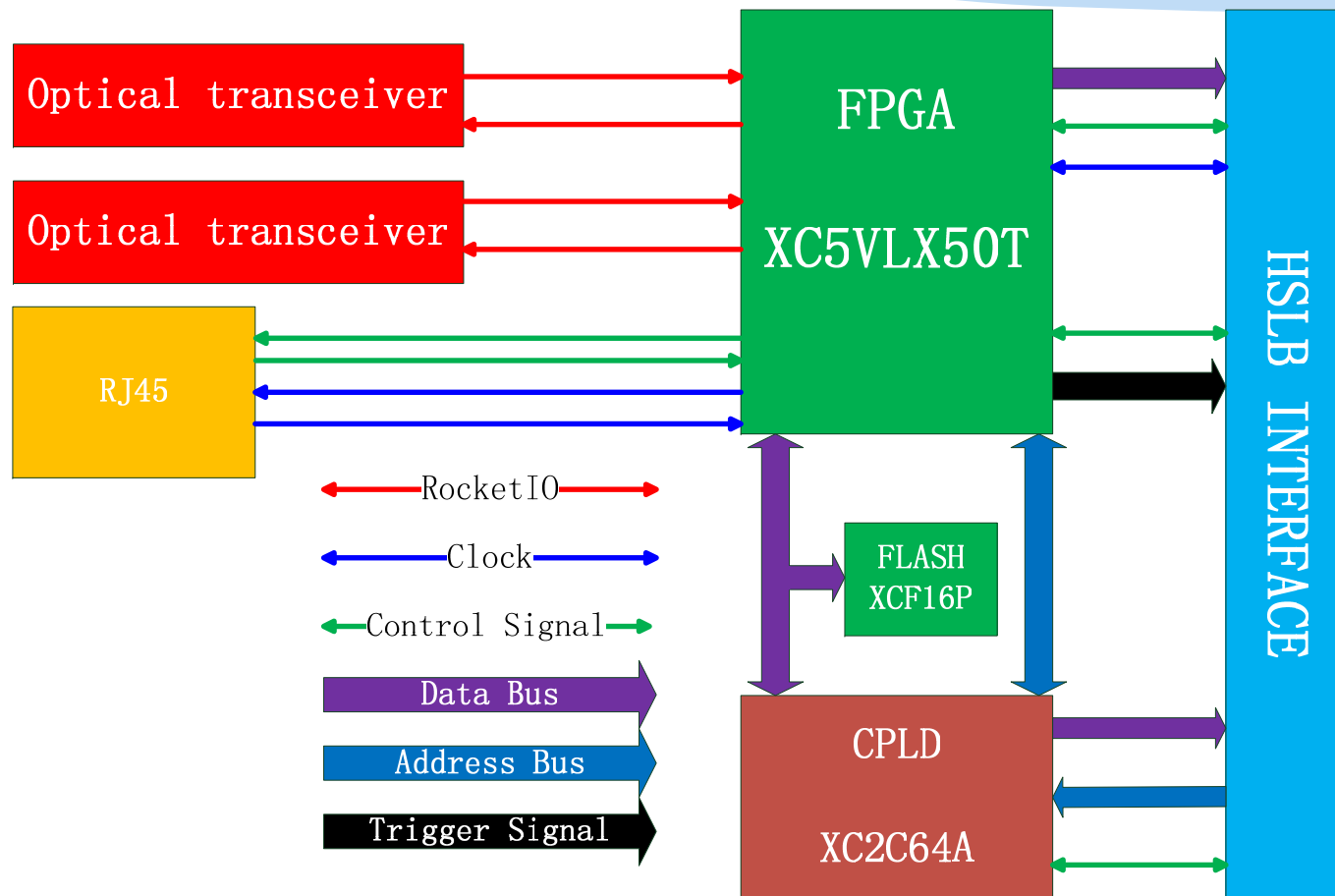
❖ The HSLB(high speed link baord) is the uniform tansmission and receiving board for BelleII2Link. It uses GTP module and optical fiber to realize the gigabit line rate transmission.
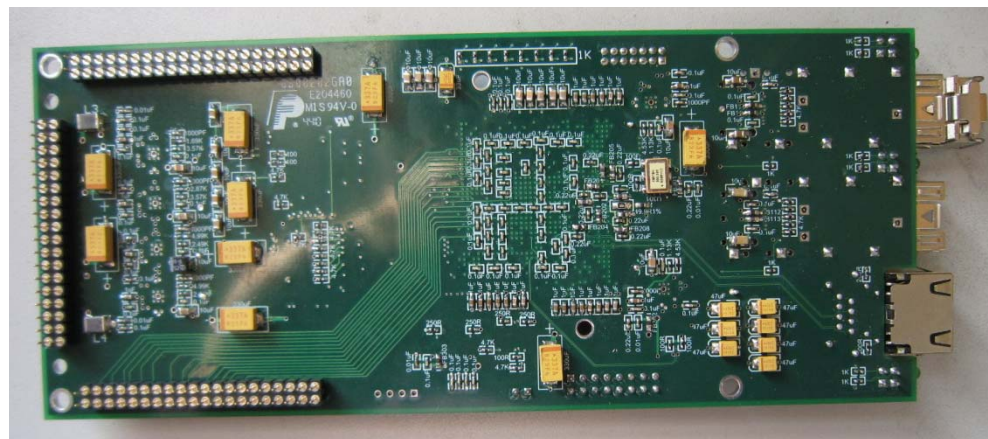
The upgrade of the HSLB

❖ HSLB was upgraded in August. 2010.

❖ Modified the wire order of the RJ45,four pairs （1-2，3-6，4-5，7-8）.All the four pairs are connected to FPGA directly.

❖ Modified the size of the RJ45. Thinner than old one.

❖ Changed the power regulater, use TPS74401.

❖ All clock signals are connected to FPGA directly. Select clock by software.

❖ Modified the CPLD configuration.

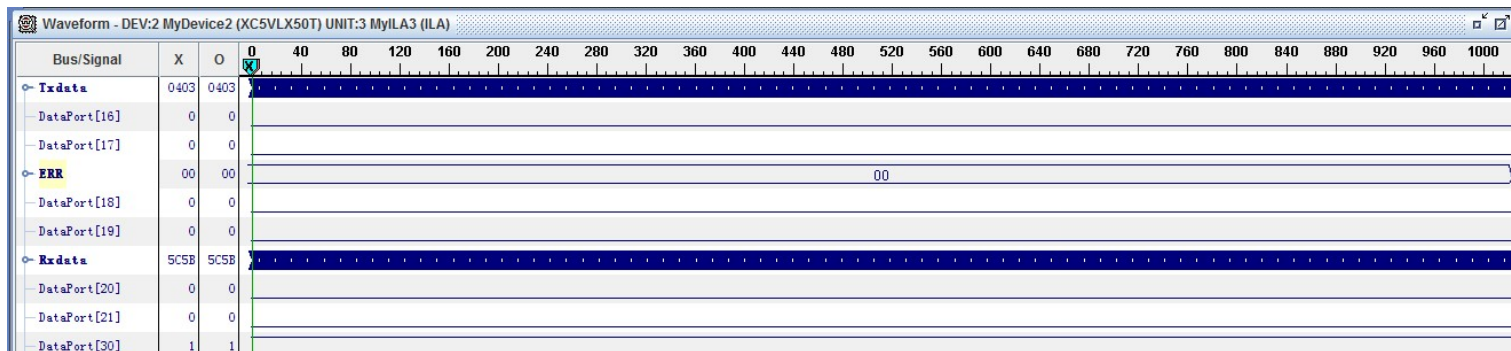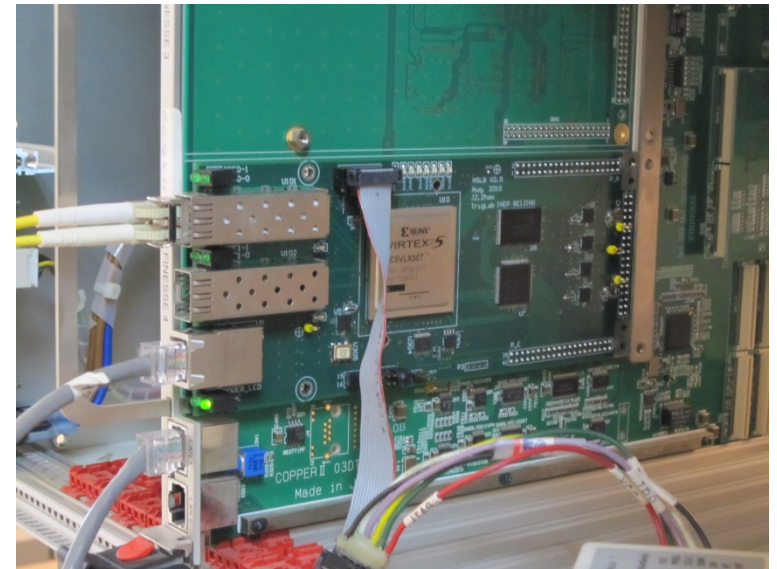# The block diagram of the HSLB

The PCB of the HSLB V2.0

The status of the HSLB

❖ Version 2.0 is working fine.
❖ The line rate of the GTP can reached 3Gbps.
  ❖ test linerate 3Gbps
  ❖ test time:10 hours
  ❖ err count: 0
  ❖ err rate: <10e-14
❖ CPLD online configuration has identified. Fine CPU->CPLD->FPGA
❖ Flash configuration has identified.
❖ Ready for small mass production

The user guide of HSLB

HSLB board User Guide

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Two version of the HSLB

❖ The HSLB board has finished two versions, version1.0 and version 2.0.

❖ Version 1.0 4 boards
❖ Version 2.0 2 boards

version 1.0

version 2.0

Trigger/DAQ workshop for BelleII Experiment
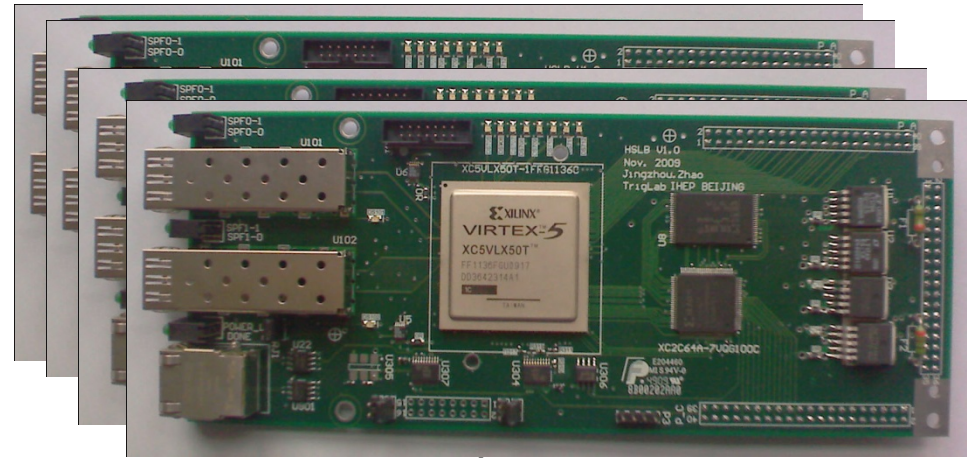
Summary

❖ The HSLB have been designed two version.

❖ Max line rate :3.2Gb/s/ch.

❖ Online configuration works well on version 2.0.

❖ Version 2.0 is satisfactory.

❖ Version 2.0 is ready for small mass production.

❖ The first draft of HSLB User guide has been finished.

IHEP

Thanks for your attention!