PXD DAQ
Status in Giessen

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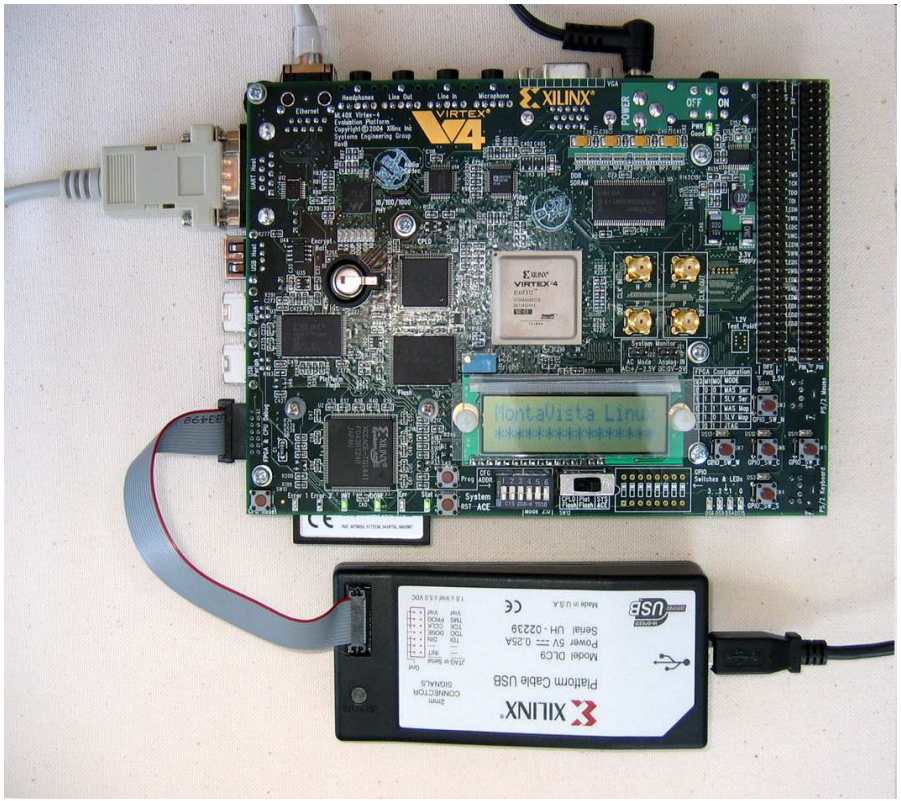
Belle-II TDAQ Workshop, Beijing, Jan 2011

Outline

Main issue today: Status of ROI algorithm on ML403 board (XC4VFX12-FF668-10C) **David Münchow**

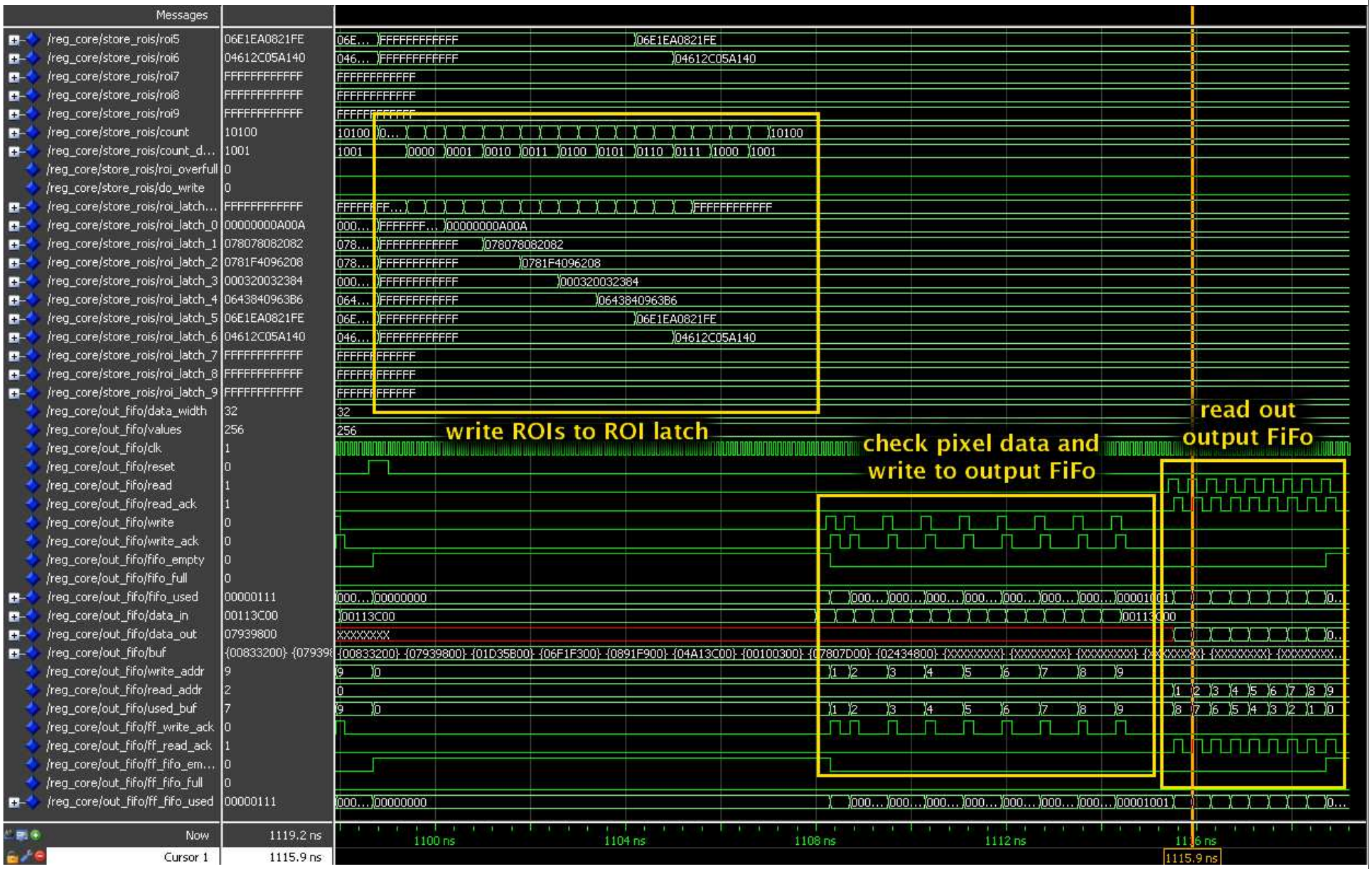


What works?

- PowerPC (100 MHz) writes ROIs and pixel data into registers
  PowerPC can get data drom anywhere (from network, from file)
- VHDL code:
  - Receive ROI data by registers (written from PowerPC)
  - ROI data are received serial -> then latched
  - Receive pixel data by registers (written from PowerPC)

Details:

- Only 1 FIFO (output)
  (FIFO config: write/read enable with full clock speed)
  no input FIFO, not needed (just consumes FPGA resources)
- Code for ROI checker is NOT clocked
- Data Tx/Rx not by PLB anymore
  bus is not used (avoids arbitration)
- n (n<=10) ROIs -> code is parallel x n
  n is variable event-by-event

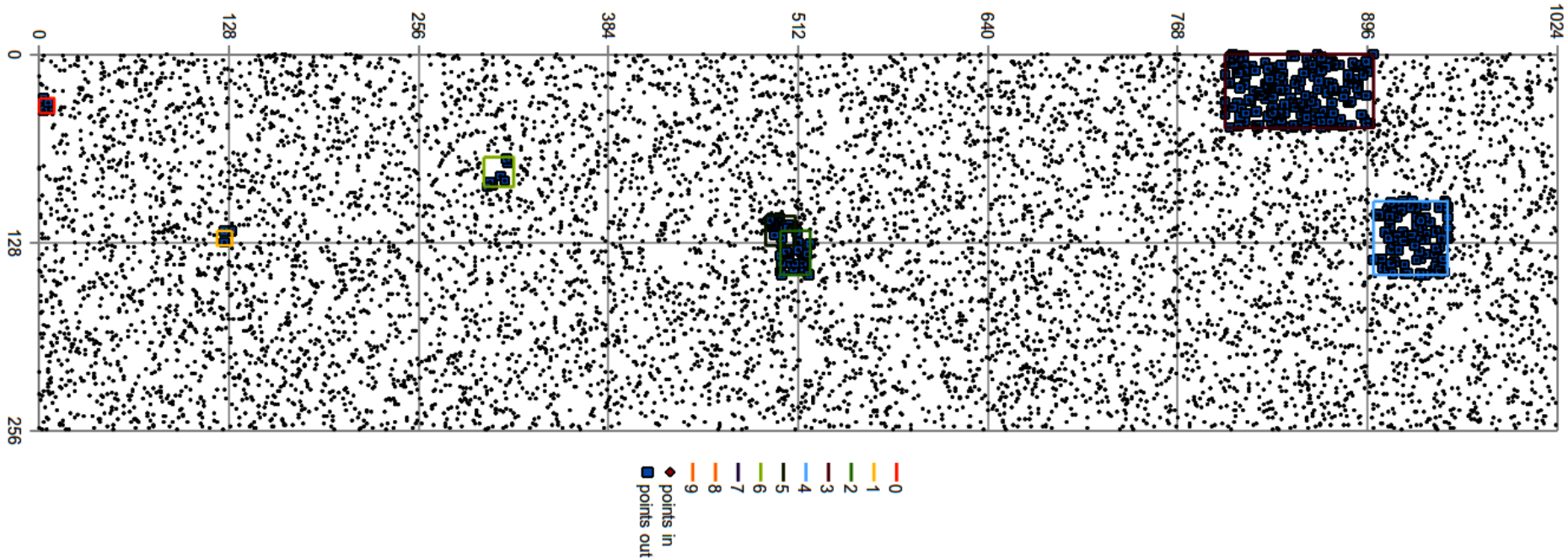

write ROIs to ROI latch
check pixel data and
write to output FiFo
read out
output FiFo

Example

1024 x 256 space
(reality: 800 x 250, but address space needs to be bit aligned anyway, -> 10 bit x 8 bit)

3% occupancy

9 ROIs



Results

- Sythesizing of algorithm takes >30 min
  (i.e. a large fraction of development and debugging is waiting)

- Resources of FX12 are at limit with the algorithm
  (e.g. 10 ROI + 2 FIFOs 1024x32 bit do not fit anymore)
  but not an issue, because FX60 on CN has ~4x more logic cells

- Stability test
  >1.7 x 10^6 events (preliminary result)
  <=10 random ROIs,
  variable number of ROI,
  variable ROI size,
  random data,
  3% occupancy

  -> o.k.

Stability Test after ~20 hours

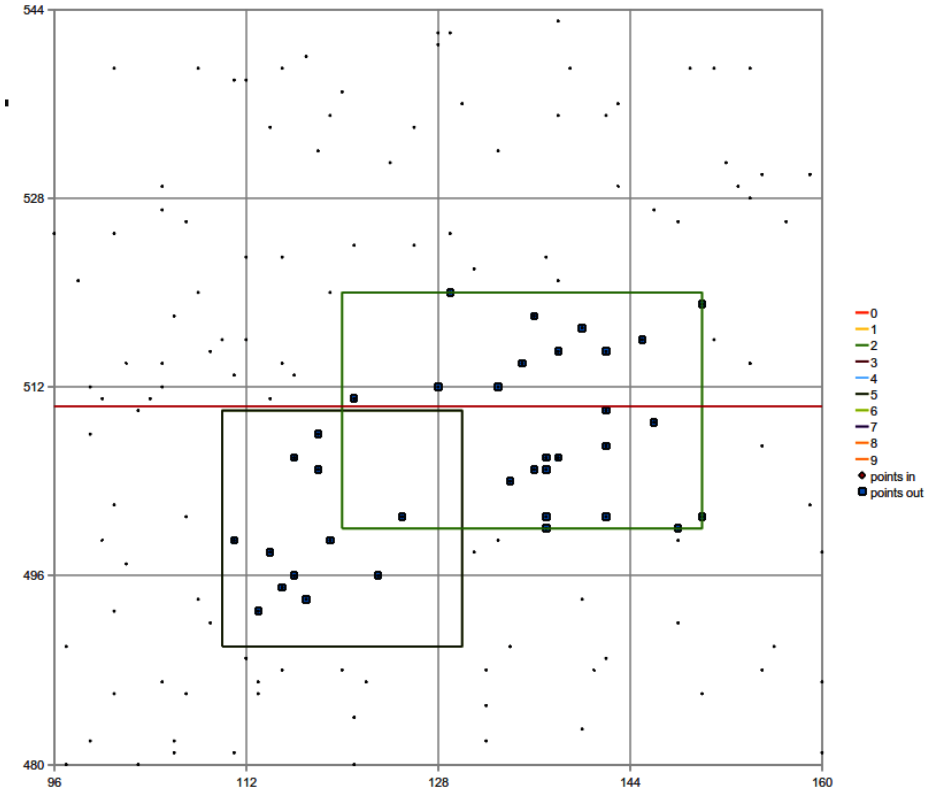
```
count events:   1758620 correct        0 with error  (rate 0.000000  ROIs(8):  195010 195780 194950 195468 194624 195459 196079 195484 195766
count events:   1758630 correct        0 with error  (rate 0.000000  ROIs(4):  195012 195781 194952 195469 194625 195459 196080 195485 195767
count events:   1758640 correct        0 with error  (rate 0.000000  ROIs(6):  195014 195781 194953 195471 194626 195461 196080 195485 195769
count events:   1758650 correct        0 with error  (rate 0.000000  ROIs(1):  195016 195784 194953 195472 194626 195463 196081 195486 195769
count events:   1758660 correct        0 with error  (rate 0.000000  ROIs(6):  195017 195785 194954 195474 194626 195466 196082 195486 195770
count events:   1758670 correct        0 with error  (rate 0.000000  ROIs(6):  195017 195787 194955 195475 194629 195469 196082 195486 195770
count events:   1758680 correct        0 with error  (rate 0.000000  ROIs(1):  195018 195788 194956 195476 194629 195470 196085 195488 195770
count events:   1758690 correct        0 with error  (rate 0.000000  ROIs(3):  195019 195789 194957 195478 194629 195471 196085 195490 195772
count events:   1758700 correct        0 with error  (rate 0.000000  ROIs(4):  195020 195792 194957 195479 194630 195471 196085 195492 195774
count events:   1758710 correct        0 with error  (rate 0.000000  ROIs(6):  195020 195793 194957 195480 194632 195473 196086 195494 195775
count events:   1758720 correct        0 with error  (rate 0.000000  ROIs(1):  195022 195795 194960 195482 194632 195473 196086 195494 195776
count events:   1758730 correct        0 with error  (rate 0.000000  ROIs(7):  195023 195797 194960 195482 194635 195474 196088 195495 195776
count events:   1758740 correct        0 with error  (rate 0.000000  ROIs(5):  195026 195799 194960 195482 194636 195475 196088 195498 195776
count events:   1758750 correct        0 with error  (rate 0.000000  ROIs(8):  195026 195799 194960 195487 194636 195477 196089 195499 195777
count events:   1758760 correct        0 with error  (rate 0.000000  ROIs(7):  195027 195800 194960 195489 194637 195477 196090 195500 195780
count events:   1758770 correct        0 with error  (rate 0.000000  ROIs(8):  195028 195800 194961 195489 194639 195479 196091 195503 195780
count events:   1758780 correct        0 with error  (rate 0.000000  ROIs(7):  195029 195801 194962 195491 194640 195480 196093 195504 195780
count events:   1758790 correct        0 with error  (rate 0.000000  ROIs(5):  195030 195802 194964 195492 194643 195481 196093 195505 195780
count events:   1758800 correct        0 with error  (rate 0.000000  ROIs(9):  195031 195803 194965 195493 194645 195482 196093 195505 195783
count events:   1758810 correct        0 with error  (rate 0.000000  ROIs(7):  195032 195806 194965 195493 194645 195483 196096 195506 195784
count events:   1758820 correct        0 with error  (rate 0.000000  ROIs(7):  195034 195807 194965 195494 194645 195485 196097 195508 195785
count events:   1758830 correct        0 with error  (rate 0.000000  ROIs(6):  195035 195807 194967 195496 194646 195487 196097 195509 195786
count events:   1758840 correct        0 with error  (rate 0.000000  ROIs(6):  195037 195809 194968 195496 194647 195490 196097 195510 195786
count events:   1758850 correct        0 with error  (rate 0.000000  ROIs(4):  195037 195810 194968 195499 194648 195490 196099 195512 195787
count events:   1758860 correct        0 with error  (rate 0.000000  ROIs(8):  195037 195811 194970 195500 194649 195490 196101 195513 195789
count events:   1758870 correct        0 with error  (rate 0.000000  ROIs(9):  195038 195811 194971 195501 194650 195492 196101 195514 195792
count events:   1758880 correct        0 with error  (rate 0.000000  ROIs(4):  195040 195811 194971 195502 194650 195494 196104 195515 195793
count events:   1758890 correct        0 with error  (rate 0.000000  ROIs(8):  195041 195811 194971 195502 194651 195496 196105 195518 195795
count events:   1758900 correct        0 with error  (rate 0.000000  ROIs(5):  195042 195813 194972 195503 194653 195496 196107 195519 195795
count events:   1758910 correct        0 with error  (rate 0.000000  ROIs(7):  195042 195816 194972 195503 194653 195497 196109 195520 195798
```

BUT: yesterday evening David found a problem in the checking routine!!
he would like to check again
i.e. „stable" is a preliminary result

Overlapping ROIs

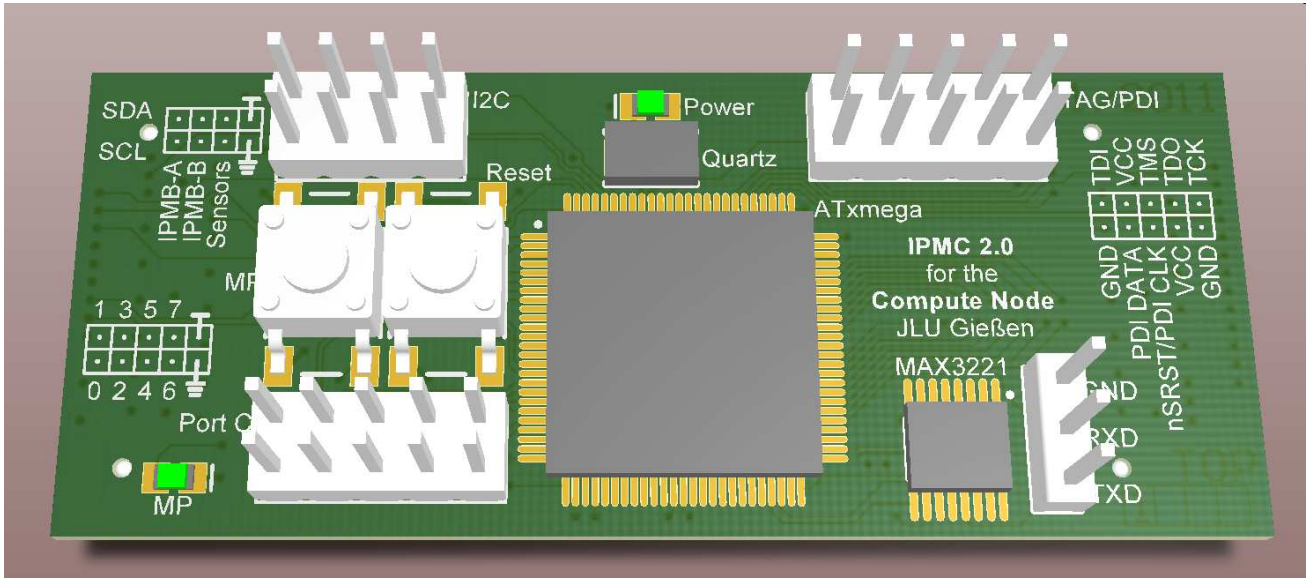
ROI selection => OR

i.e. if ROI overlap, these output data are only written 1x



New IPMI PCB

- Reminder: when ATCA crate is switched on, then:
  a.) fan speed is maximum (noise) and b.) power to boards is minimum
  -> needs negociation to ATCA „shelf manager"
- New CN addon card: Microcontroller ATMEGA1280 -> XMEGA A1
  - 4 internal I2C (-> 2 external I2C chips can be skipped)
  - I/O ports to external I2C not needed anymore
    (-> 2 external switch chips can be skipped)
  - PCBs are ordered, delivery announced for 28.01.
    chip placement and soldering of 1st 2 boards probably next week



Some more progress

- - AURORA core (finally) generated in ISE 10
  - Test programs are O.K. in ModelSim
  - at some point, we have to try, if the different AURORA versions (Virtex-4, Virtex-5, 8B/10B, ISE 8, ISE 10, ISE 11) can be unified.
- After ~200 bitstream files, problem was solved with PowerPC
  -> with some configurations of BRAM etc.,
  PLB address of serial port is generated wrong
  Linux is booting (unpacking), then wrong address, then output to Nirvana
  -> booting PowerPC core with our own Linux can be generated within 6-7 min

Next steps

- All developers will move from development (XC4VFX12, XC4VFX20) boards to CN (XC4VFX60)
  - 10 new CN will come soon from IHEP
    (2 CN for Belle-2 from german ministry funding)
  - 1 large (14-slot) + 4 mini-ATCA shelfs (2-slot) are ordered

  everybody will have a mini-system in the office which he can reboot as often as needed

Next steps

- Move algorithm to CN
  (almost trivial, everything is prepared)
- Connect ROI algorithm to optical link
  (hopefully not too much problems, as pixel data Tx/Rx is already moved to registers instead of PLB)

- Feb 02 - Meeting of Bonn and Gießen Groups
  (Bonn Group of Jochen Dingfelder)
  - data concentrator, interfaces to ATCA, possible test systems etc.
- Feb 21,22 - Meeting in Munich
  (organized by Andreas Moll)
  - 1. HLT interface
  - 2. MC PXD hits as FPGA input
    (also in contact to Prague group, Zbynek Drasal)

Timeline

- Proposed schedule until decision ATCA vs. PC based system

- April 6-10
  Presentation of status of both systems at B2GM
  -> identify open issues
- May 9-11
  Ringberg Workshop
  -> short update of important issues
- June 9 (THU) and 10 (FRI)
  PXD DAQ Workshop in Germany (location not fixed yet)
  -> decision
- July 6-9
  B2GM
  -> announcement of decision