CEPC Silicon Strip Outer Tracker

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On behalf of the Tracker Team

2024.01.29

Outline

- Baseline Design from CDR
- Major components
  - Silicon Strip Sensor
  - Readout electronics
  - Mechanics and Integration
- Existing Technical Experience
- Roadmap towards TDR

Physics requirements from CDR

- Tracking performance
  - reconstruction efficiency > 99% for 1GeV tracks
  - momentum resolution ~ per mille
- Lepton ID
  - ID efficiency > 99%
  - mis-ID rate < 2% for >5GeV isolated leptons
- Charged kaon ID: efficiency and purity > 90%
- Jet and missing energy: BMR < 4%
- Flavor tagging:
  - b-jet tagging efficiency and purity > 80%
  - c-jet tagging efficiency and purity > 60%

Silicon Tracker Requirement

- Silicon tracker provides additional high-precision hit points
  - Improving tracking efficiency and precision
- Monitoring possible field distortion in TPC (DCH)
- Contributing detector alignment
- Seperating bunch crossing events with relative time-stamping
- Potentially dE/dx measurement

$$\sigma_{1/p_{\mathrm{T}}} = a \oplus \frac{b}{p \sin^{3/2}\theta} \quad [\,\mathrm{GeV}^{-1}] \qquad a \sim 2 \times 10^{-5}\,\mathrm{GeV}^{-1} \qquad b \sim 1 \times 10^{-3}$$

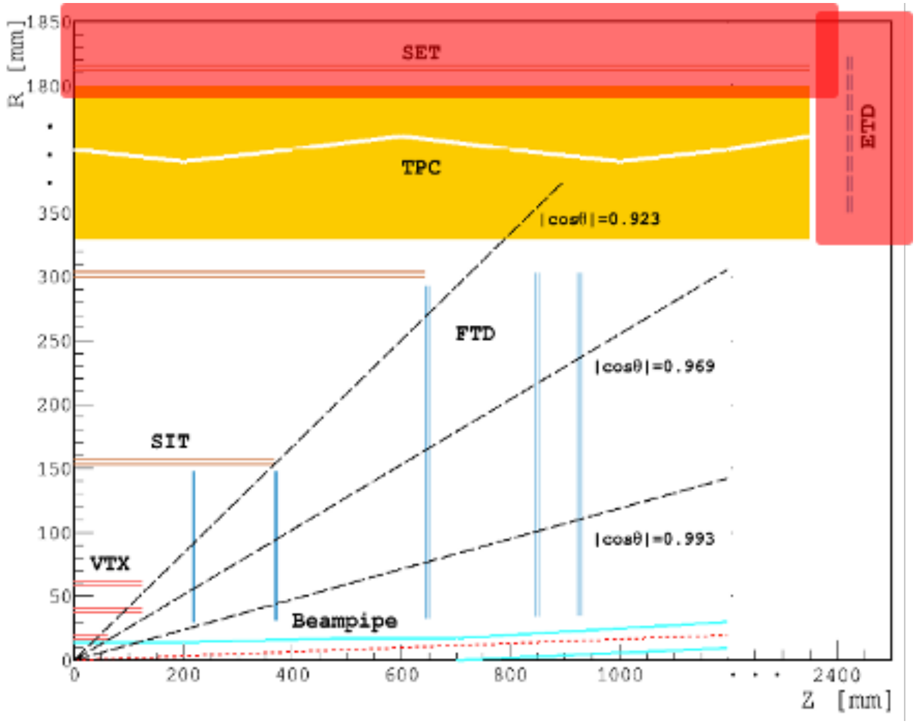
- At $\theta = 90°$, resolution dominated by
  - multiple-scattering (< 50 GeV)
  - single-point resolution (> 50 GeV)

Baseline Design from CDR

- Silicon External Tracker (SET)
  - Helps in extrapolating from TPC/DCH to Calorimeter
  - Provides hit time-stamps for bunch crossing separation
- Endcap Tracking Detector (ETD)
  - Improves reconstruction with reduced path in TPC/DCH

Area: [m^2]
SET: 53.5, ETD: 9.9
Total: **63.4**
Silicon: > **127**

Detector	Layer	Radius [mm]	+/- z [mm]	Material budget [X0]
SET	Layer3	1811	2350	0.65%
ETD	Disk	Rin: 419.3 / Rout 1822.7	2420	0.65%



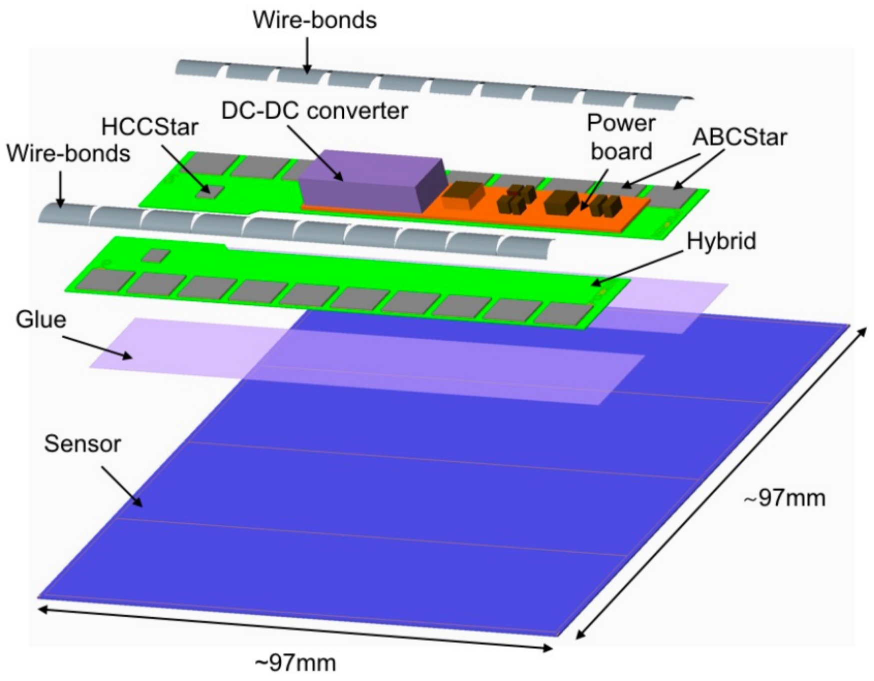
Components of SET and ETD with microstrip

- Sensor
  - Microstrip sensors with detection area of 10x10 cm^2, 50μm pitch, 200μm thickness
  - Two back-to-back single-sided microstrips with 7° stereo angle
- Readout electronics
  - Custom designed ASICs with deep sub-micron CMOS technology
  - ADC, zero suppression, sparsification, and possible time stamping
- Powering and cooling
  - DC-DC converter to reduce material and power dissipation in delivery system
  - Forced cooling gas flow to provide sufficient head reduction for sensors and electronics
- Mechanics and integration
  - Lightweight and stiff support structure based on Carbon fiber reinforced plastic material
    - Both TPC and DCH can provide sufficient support to the SET and ETD
  - Precise and fast system alignment with laser monitoring for integration

Silicon Strip Modules

- Design with mass production and low cost
  - large number of modules required for the strip detector
- Independent module operation
  - to avoid potential losses caused by one or several modules in the same line
  - each module can be disconnected from the bias line
  - E.g. HV multiplexer switch (MUX) controlled through detector control system (DCS)

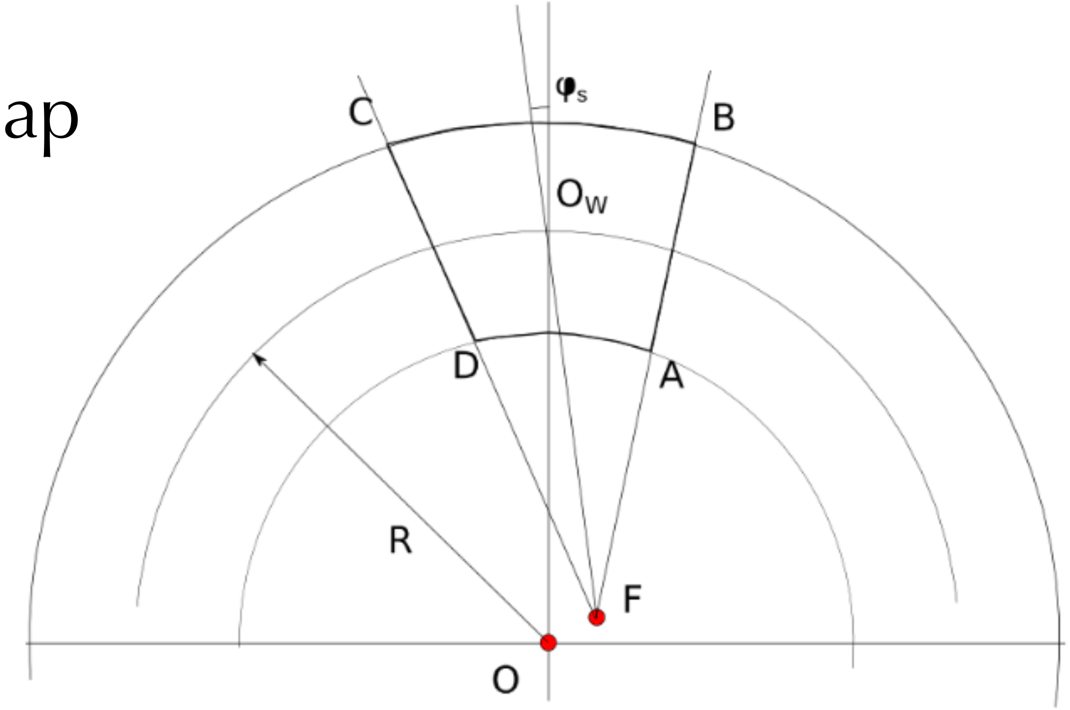
ATLAS ITk Strip Module



Silicon Strip Sensor

- Microstrip sensors with detection area of 10x10 cm^2, 50μm pitch, 200μm thickness
- p+ -on-n silicon microstrip sensors with slim-edge structure
- Two back-to-back single-sided microstrips with 7° stereo angle
- 8-inch line to be explored
- Different shapes for barrel and endcap

Area: [m^2]
SET: 53.5, ETD: 9.9
Total: **63.4**
Silicon: > **127**

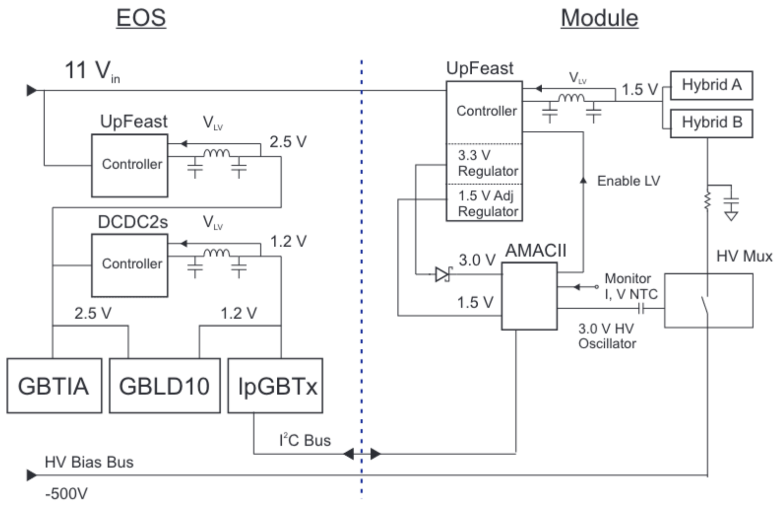


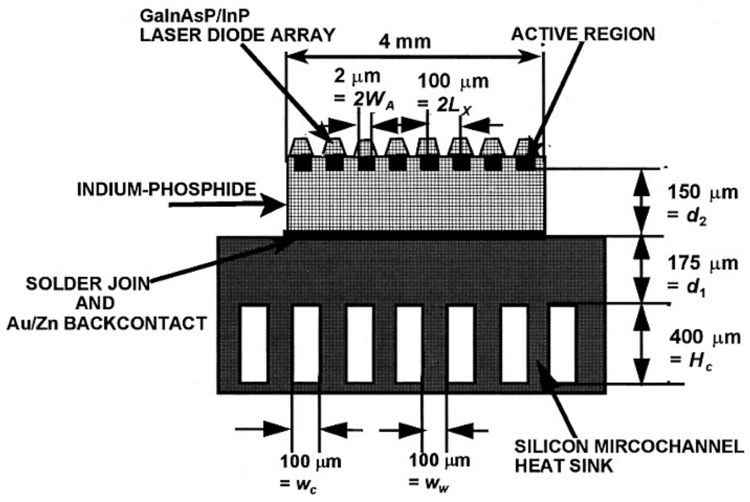
ASIC for Readout and control electronics system

- Functionality
  - Analogue to digital conversion
  - Zero suppression
  - Sparsification
  - Time stamping
  - control
- Analog front-end circuit
  - CSA: low noise, low power
  - Discriminator for binary readout
  - TOT with energy info to improve space reso.
  - Digital process on chip
  - Buffer length for trigger latency
  - Zero suppression, cluster finder algorithm
  - Command protocol and trigger interpretation compatible with DAQ
- Time stamp
  - Default time resolution is the BX clock cycle
- Power distribution
  - LV powering scheme based on DC-DC converter
  - Less power dissipation allows lower material budget
- Radiation tolerance
  - ELT layout for analog circuit
  - TMR for digital part

Powering and Cooling

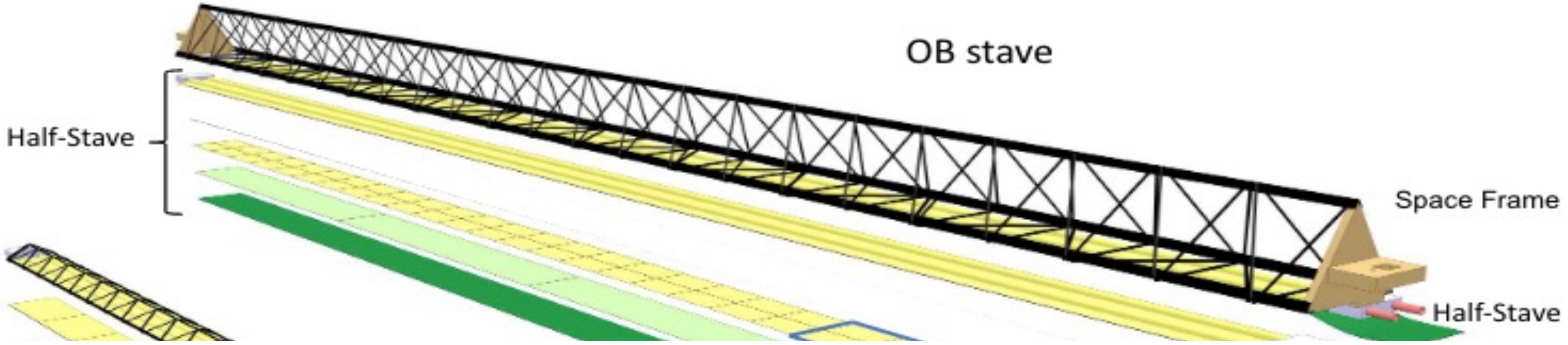
- Investigate novel powering scheme based on DC-DC converter
  - Being used by ATLAS and CMS silicon tracker upgrades
- Allows significant reduction in material budget for LV cables and less power dissipation in the delivery system
- Cooled gas flow may still feasible to conduct away heat
  - Look into other cooling techniques, e.g. silicon micro-channel cooling



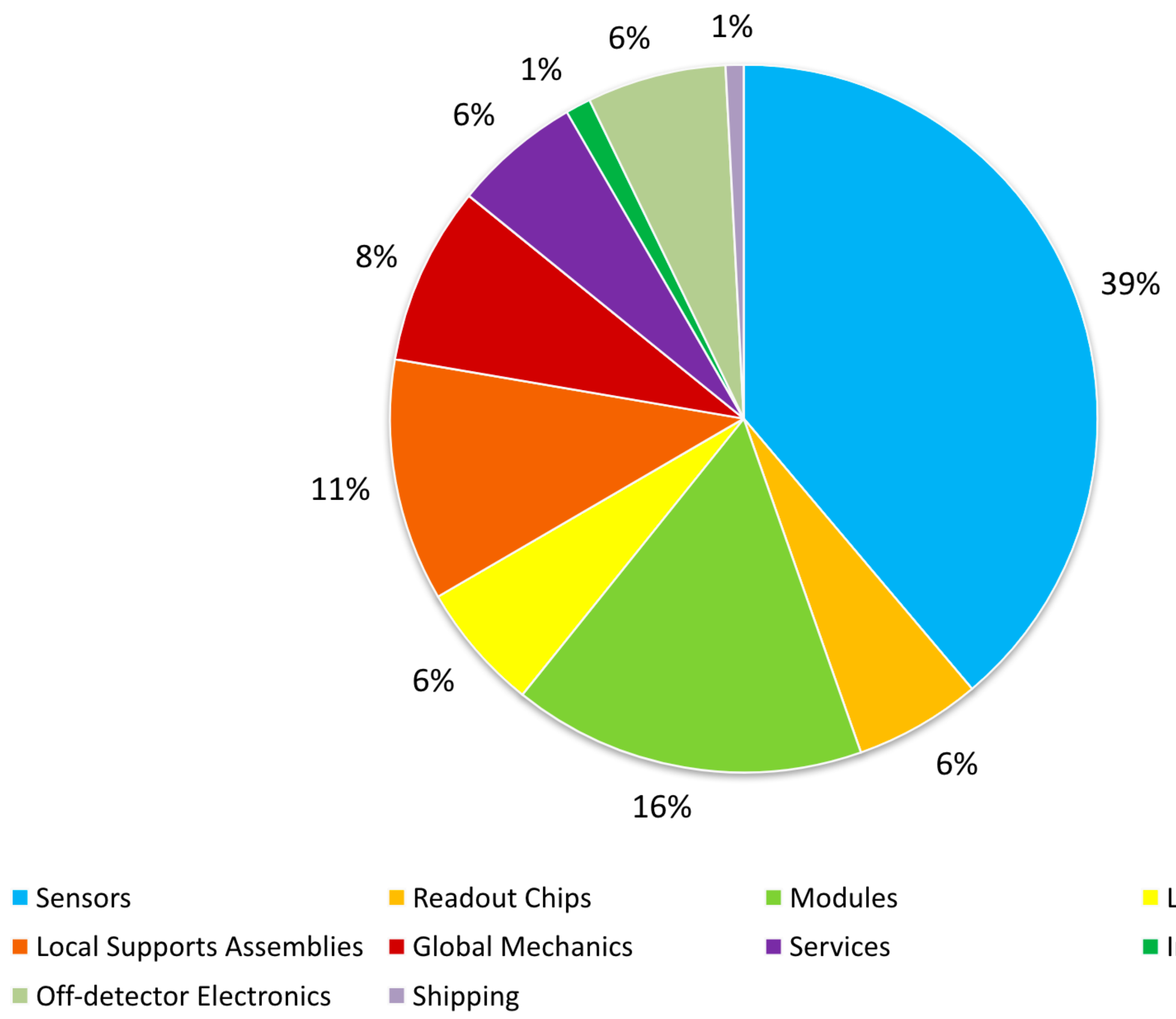


Mechanics and Integration

- Lightweight but stiff support structure built with Carbon fiber Reinforced plastic material
- Minimize overall quantity of material and facilitate construction and integration
- Laser monitoring system for precise and fast system alignment
- Well-understood physics events for final alignment
- Single Truss Structure



Cost estimation of Silicon Strip Outer Tracker



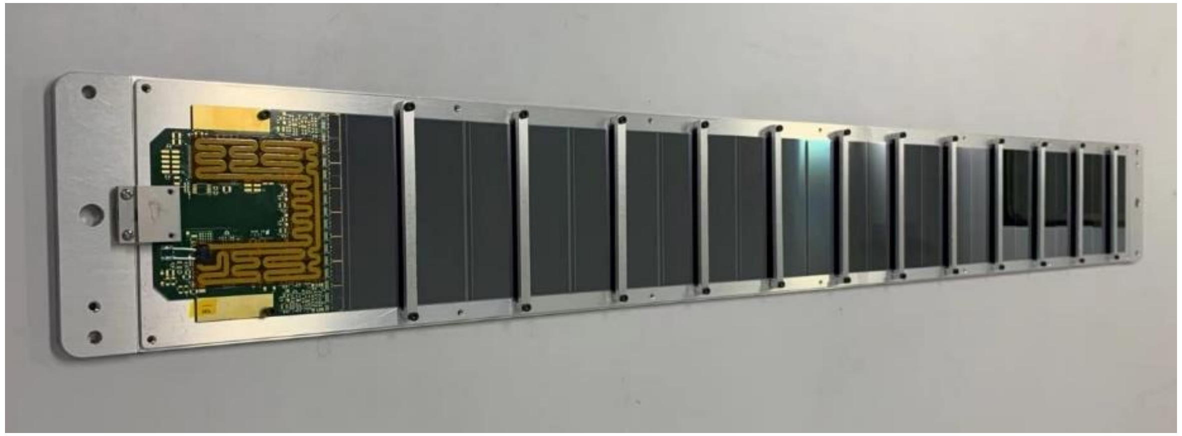
ATLAS ITk Strip: 60.75 MCHF (165 m^2)

CEPC SSD Outer Tracker: ~47 MCHF (127 m^2)

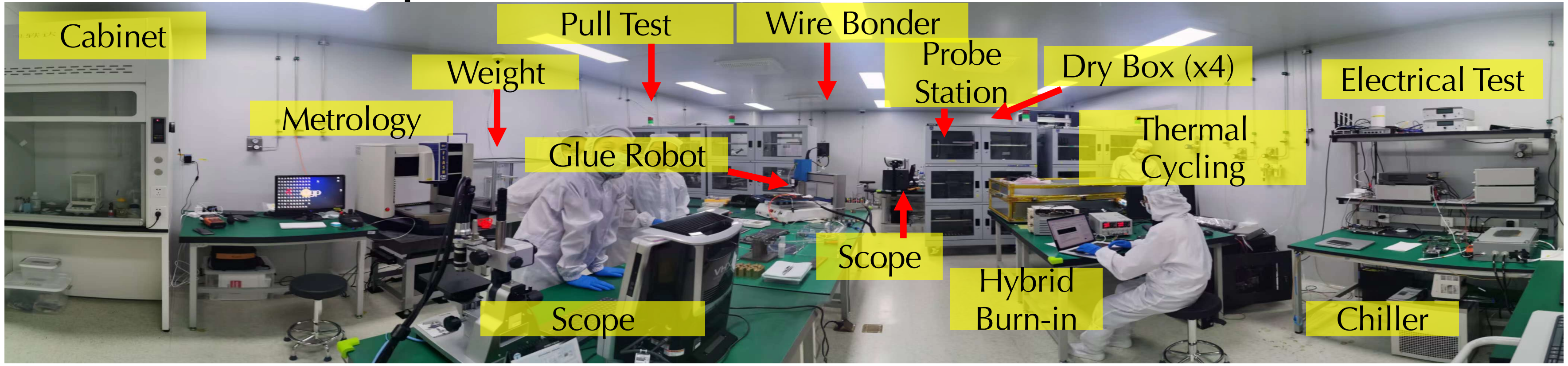
Existing Technical Experience at IHEP

LHCb UT

AMS L0 Ladder



- ATLAS ITk Strip



Roadmap towards TDR Silicon Strip Outer Tracker

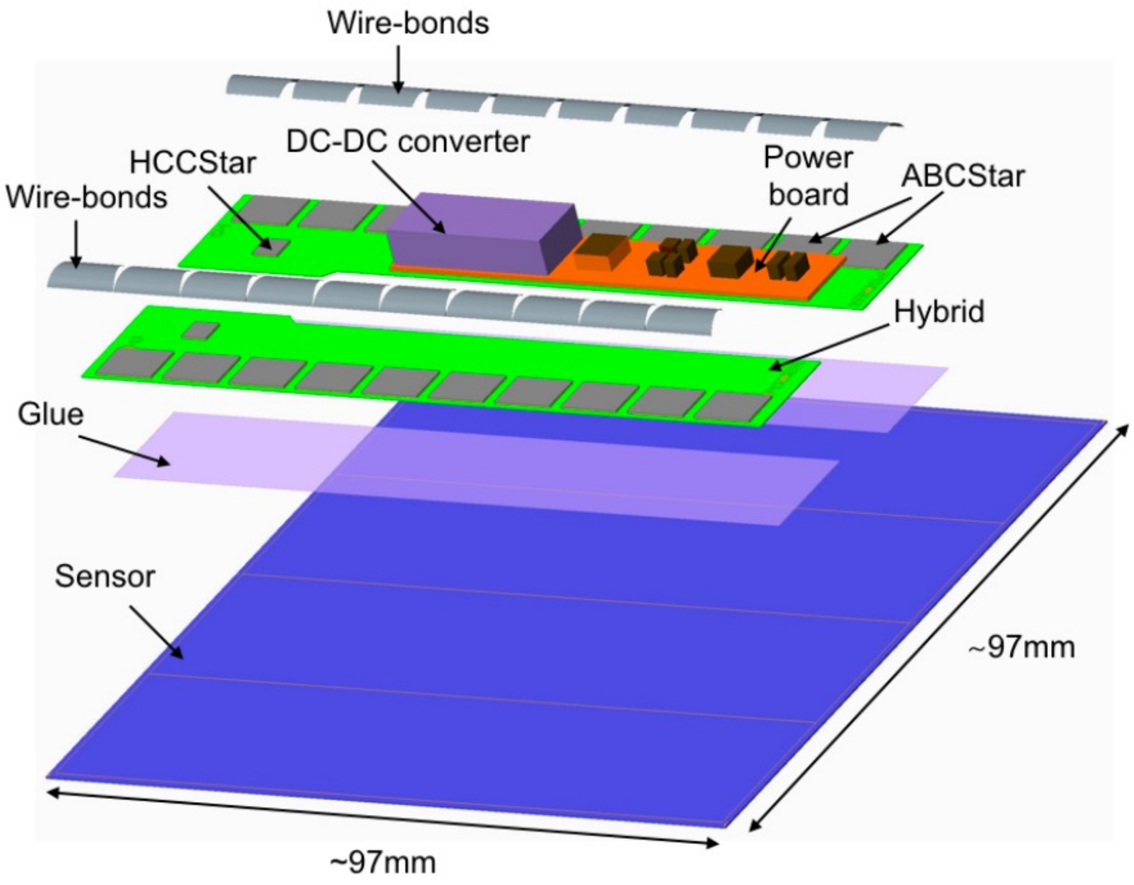
- Silicon microstrip sensors with slim-edge structure
- Front-end electronics with low power consumption and low noise
- Efficient powering and cooling techniques with low material budget
- Lightweight but robust support structure and mechanics
- Detector layout optimization, particularly in the endcap region

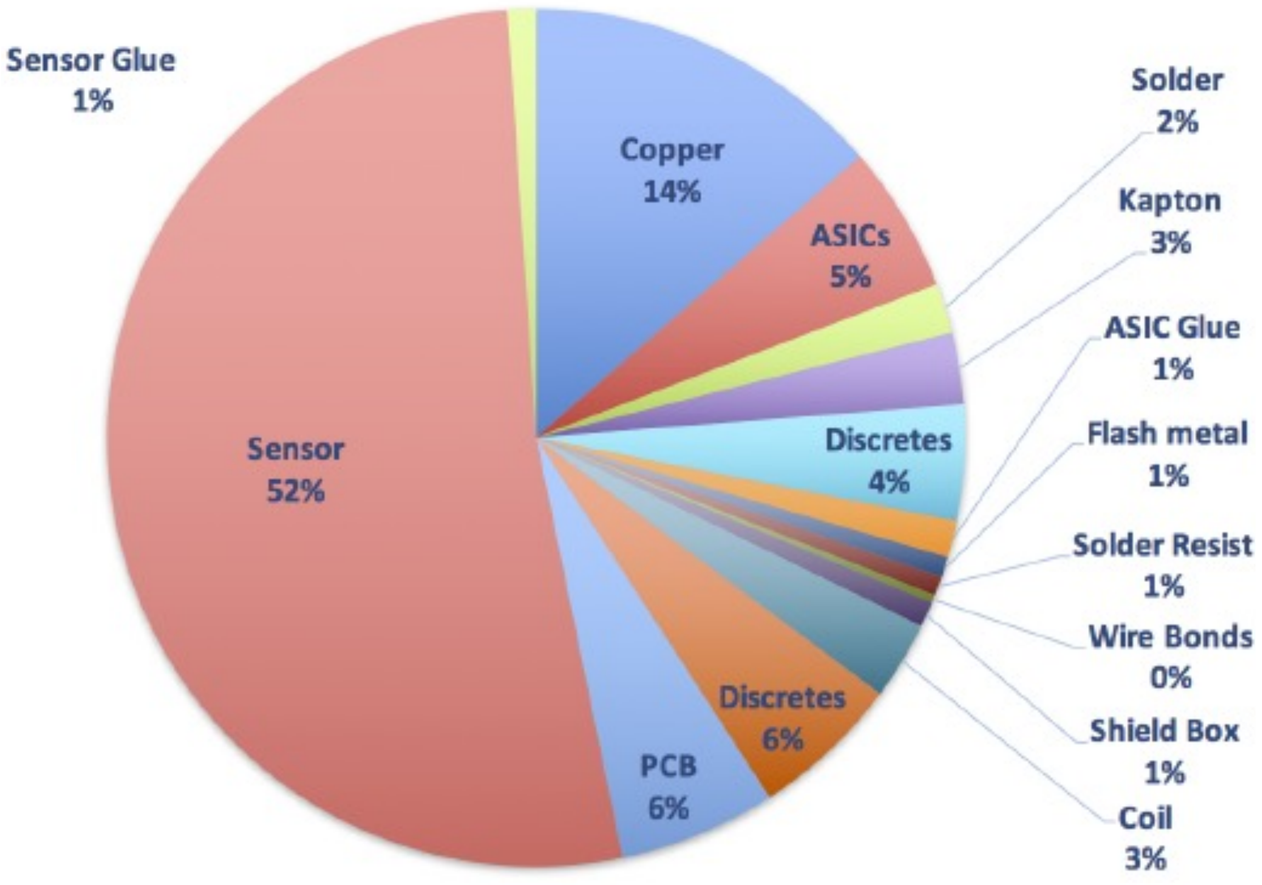
Overall goal: reduce cost while keeping performance

Backup

Strip Module Material Calculation

- ATLAS ITk Short Strip Module





Silicon Strip Sensor

CEPC

- Microstrip sensors with detection area of 10x10 cm^2, 50μm pitch, 200μm thickness
- p+ -on-n silicon microstrip sensors with slim-edge structure
- Two back-to-back single-sided microstrips with 7° stereo angle
- May consider cost-effective technology with less radiation
- 8-inch line to be explored

ATLAS ITk Strip

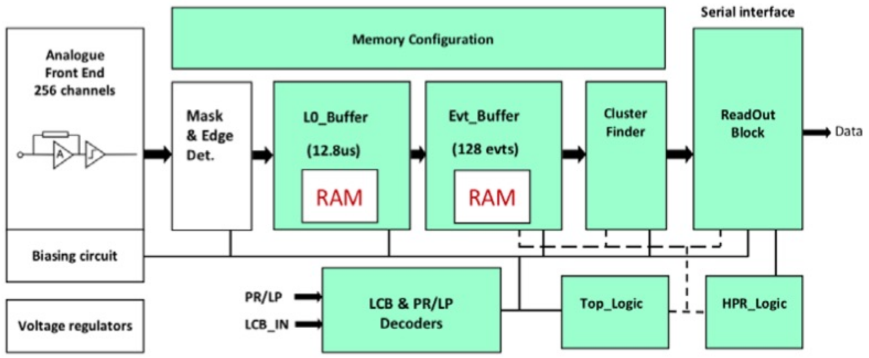
- AC-coupled n-type implants in p-type (n^+-in-p) FZ silicon bulk
  - large signal after irradiation compared with p-in-n in current SCT
- n^+-in-n higher cost (20%-50%) relative to n+-in-p
  - require double-sided processing reduces yield
  - more complicated steps in overall processing
- Strip pitch 75.5μm
  - 1280 readout strips
- On a stave, the stereo angle is achieved by rotating the modules on both sides by 26 mrad
- Chose 6-inch production
  - No large scale production of sensors on a 8-inch production line
  - Cost, schedule and yield would be highly uncertain

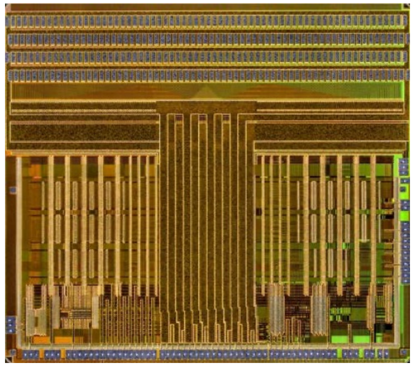
ATLAS ITk Strip Electronics

- Divide functionality into several ASIC chips
- Adapt to the geometry of sensor and module building

Acronym	Full Name	Basic functionality	Prototype	Production Chip
ABC	ATLAS Binary Chip	Converts incoming charge signal into hit information	ABC130	ABCStar
HCC	Hybrid Controller Chip	Interface between ABC130 and bus-tape	HCC130	HCCStar
AMAC	Autonomous Monitor and Control Chip	Provides monitoring and interrupt functionality	AMAC-I	AMAC-II
FEAST	FEAST	Synchronous Step-Down Buck DC/DC converter	FEAST	upFEAST

- Key parameters of ABC
  - Manufactured with 130nm CMOS process
  - 256 channels
  - Noise below 1000e- after irradiation
  - Gain ~85mV/fC
  - Average occupancy ~4 clusters per event
  - 12.8us FIFO
  - Data out 160Mbps

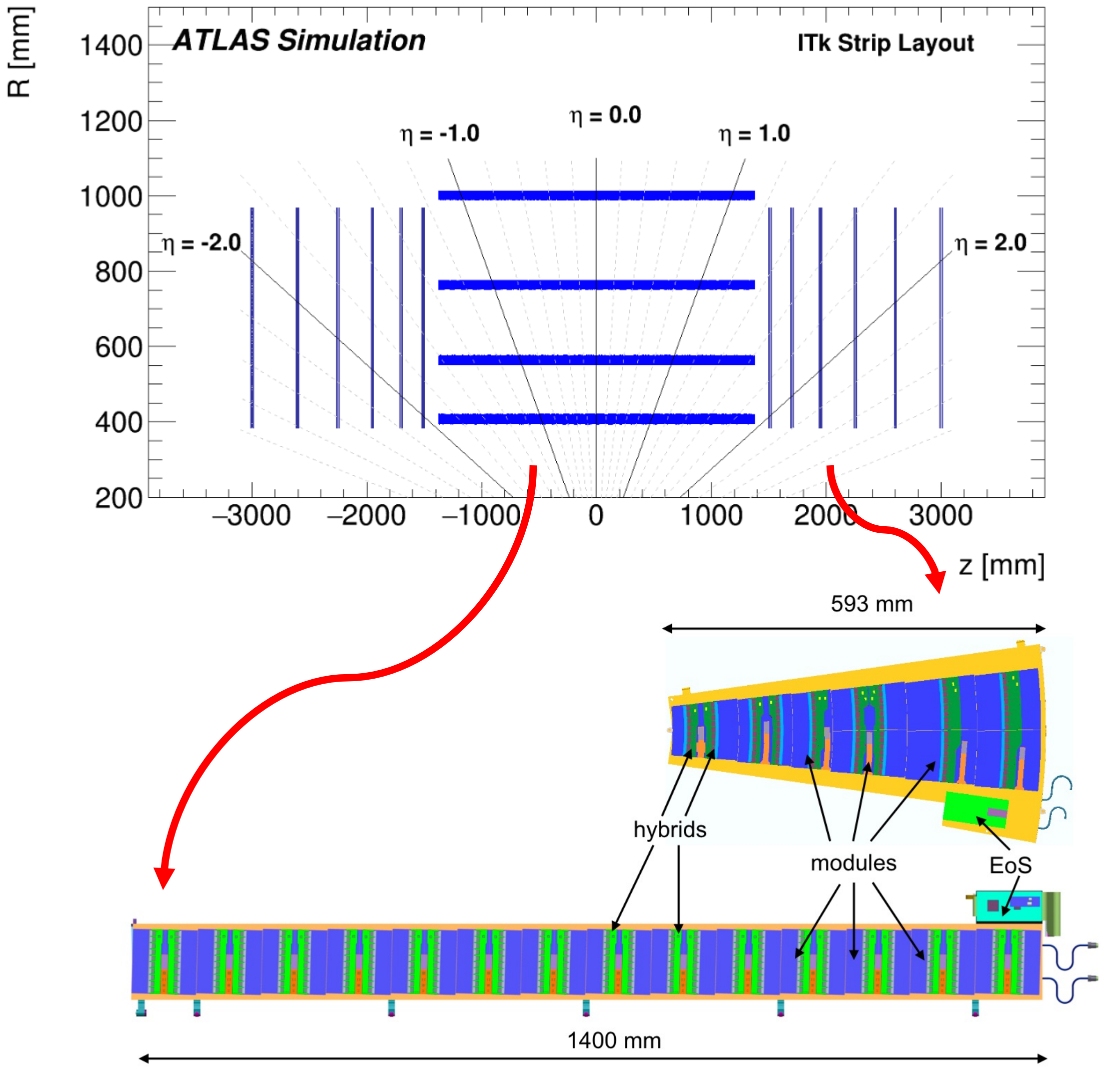




Cost Estimation for ASICs

- Time for ASIC R&D
  - > 3 MPW before the mass production
  - > 3 years of R&D, depends on manpower
- Estimated cost
  - Cost strongly depends on the technology feature size

Components of ATLAS ITk Strip Detector

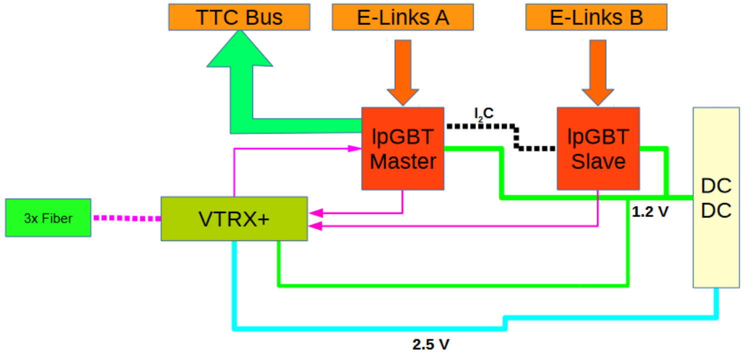


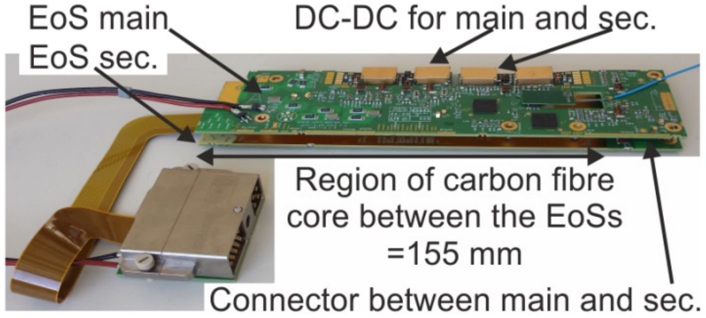
Barrel Layer:	Radius [mm]	# of staves	# of modules	# of hybrids	# of of ABCStar	# of channels	Area [m²]
L0	405	28	784	1568	15680	4.01M	7.49
L1	562	40	1120	2240	22400	5.73M	10.7
L2	762	56	1568	1568	15680	4.01M	14.98
L3	1000	72	2016	2016	20160	5.16M	19.26
Total half barrel		196	5488	7392	73920	18.92M	52.43
Total barrel		392	10976	14784	147840	37.85M	104.86
End-cap Disk:	**z-pos. [mm]**	**# of petals**	**# of modules**	**# of hybrids**	**# of of ABCStar**	**# of channels**	**Area [m²]**
D0	1512	32	576	832	6336	1.62M	5.03
D1	1702	32	576	832	6336	1.62M	5.03
D2	1952	32	576	832	6336	1.62M	5.03
D3	2252	32	576	832	6336	1.62M	5.03
D4	2602	32	576	832	6336	1.62M	5.03
D5	3000	32	576	832	6336	1.62M	5.03
Total one EC		192	3456	4992	43008	11.01M	30.2
Total ECs		384	6912	9984	86016	22.02M	60.4
Total		**776**	**17888**	**24768**	**233856**	**59.87M**	**165.25**

CEPC: > 126

Local Support Structure: Stave

- Low mass carbon fibre local support structure
- Embedded Ti cooling pipes with evaporative CO_2 (−40°C)
- Copper/Kapton co-cured bus tapes routing electrical services from and to modules
- End-of-Substructure (EoS) card facilitates the transfer of data, power and control signals between the modules and the off-detector system.
- lpGBT chips provide data serialisation
- Versatile optical link (VTRx+) transmit signals to the off-detector system. (VTRx+ converts electrical signal to optical signals)





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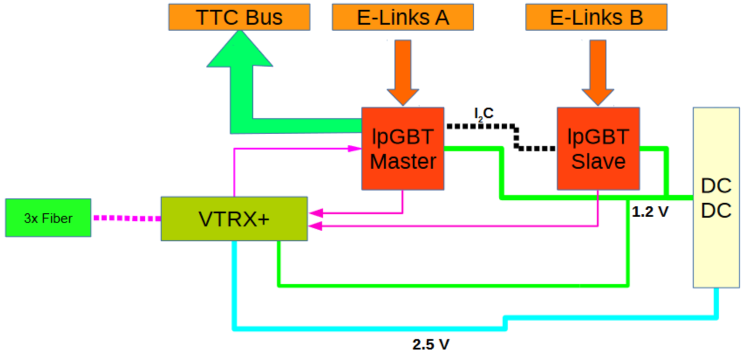
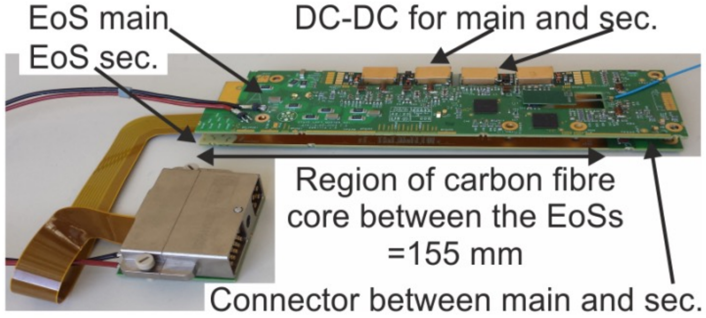
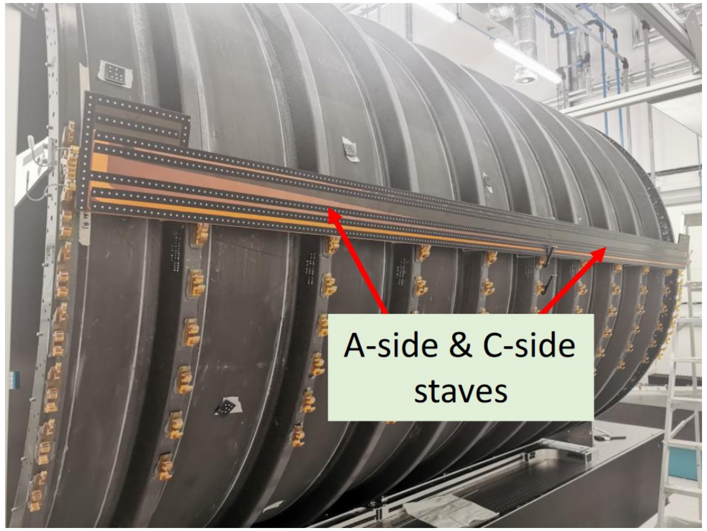


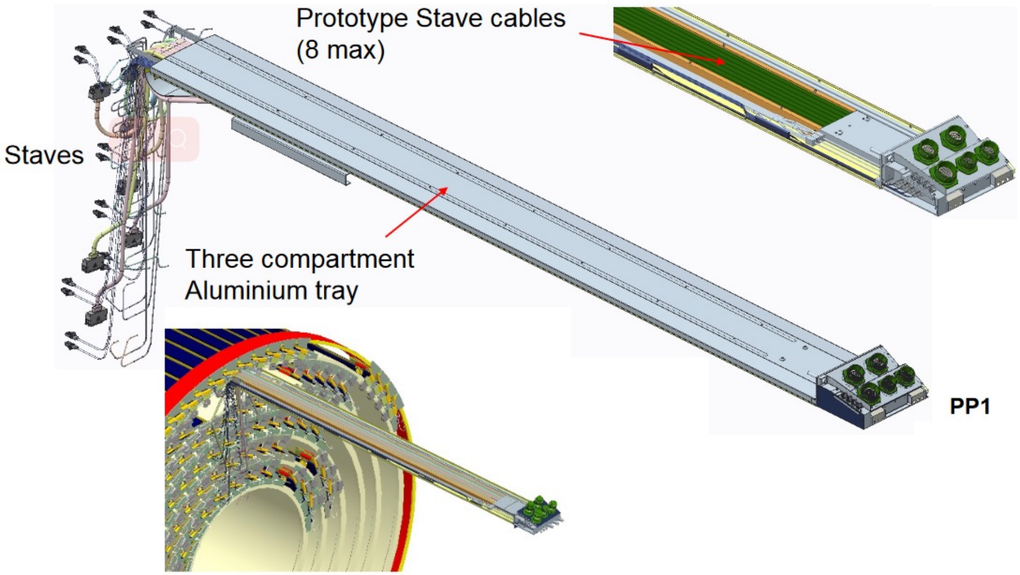


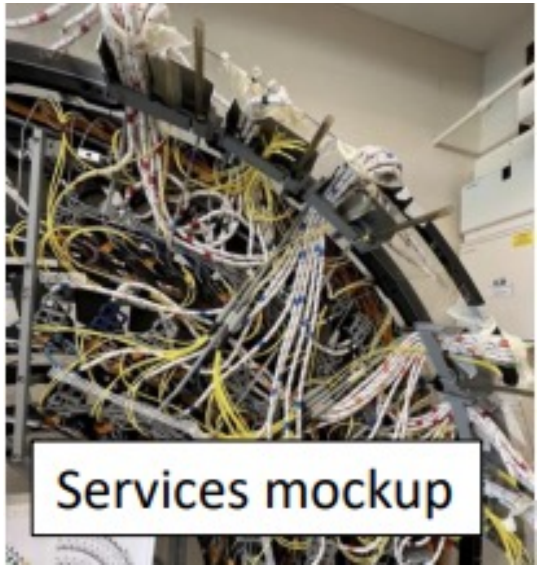
Strip Barrel Integration

- Staves will be inserted in four concentric Carbon cylinders
  - 392 barrel staves in total
- Stave insertion demonstrated at RAL using cylinder mockup and stave insertion prototype tooling
- Cylinder 3 and 2 are integrated first with LS module stave



Barrel Service Module





- The services comprise cooling pipes and associated manifolds, electrical cables and optical fibre
- Each service module supplies 8 staves
- Patch-panels (PP) allow electrical connectors to exit radially
- Kept outside the end-cap radii

AMS L0 SiDet Laboratory at IHEP

Visual 3D Measuring System
(not visible from this angle)

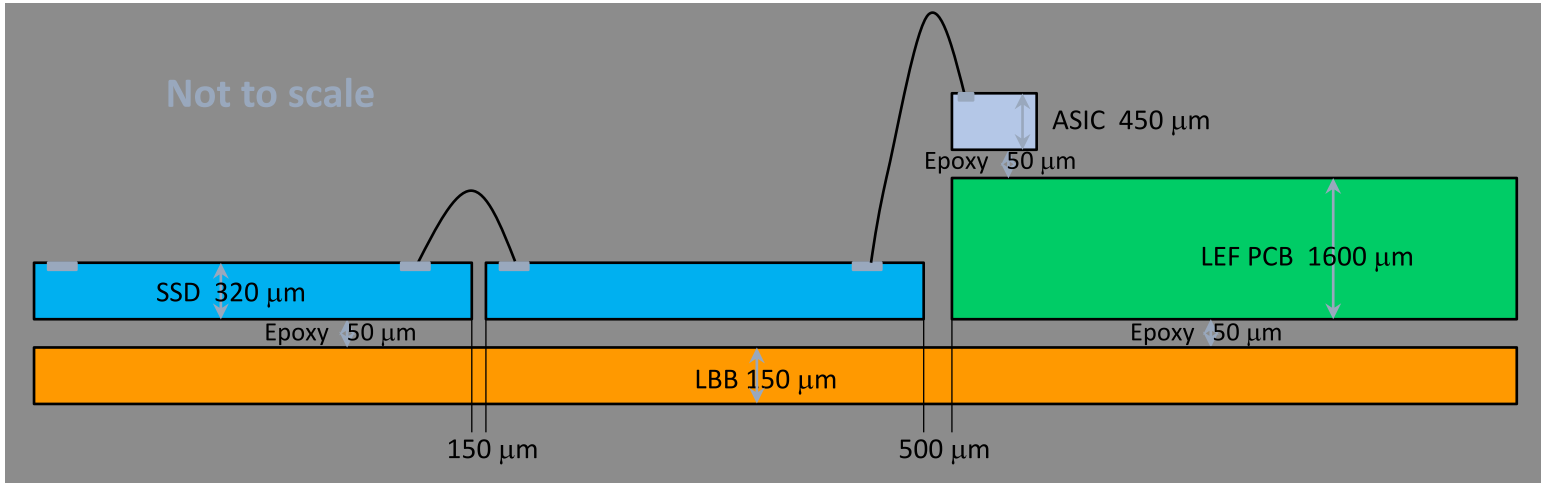
Wire Bonding Machine

Pull Tester
for Q/A of wire-bonding

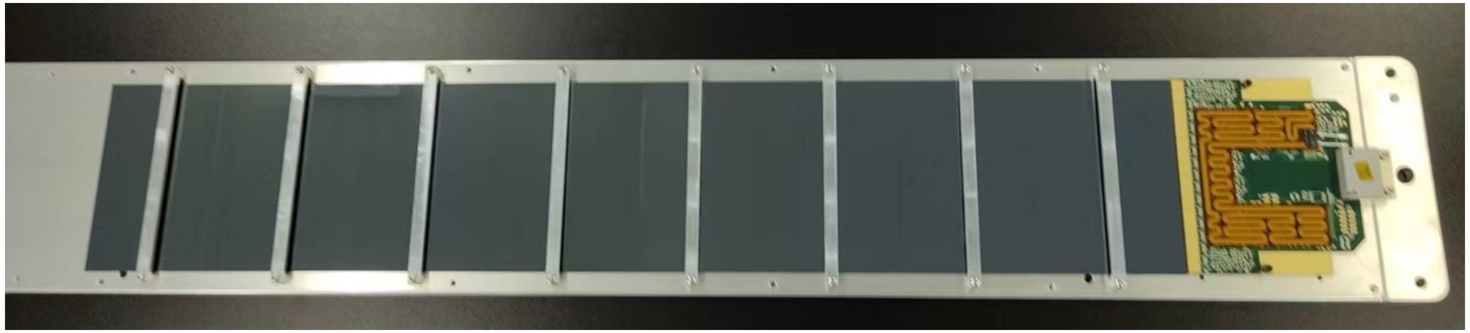
Gantry
for ladder assembling

Probe Station
for Silicon Strip Detector Q/A

Flatness and Protection



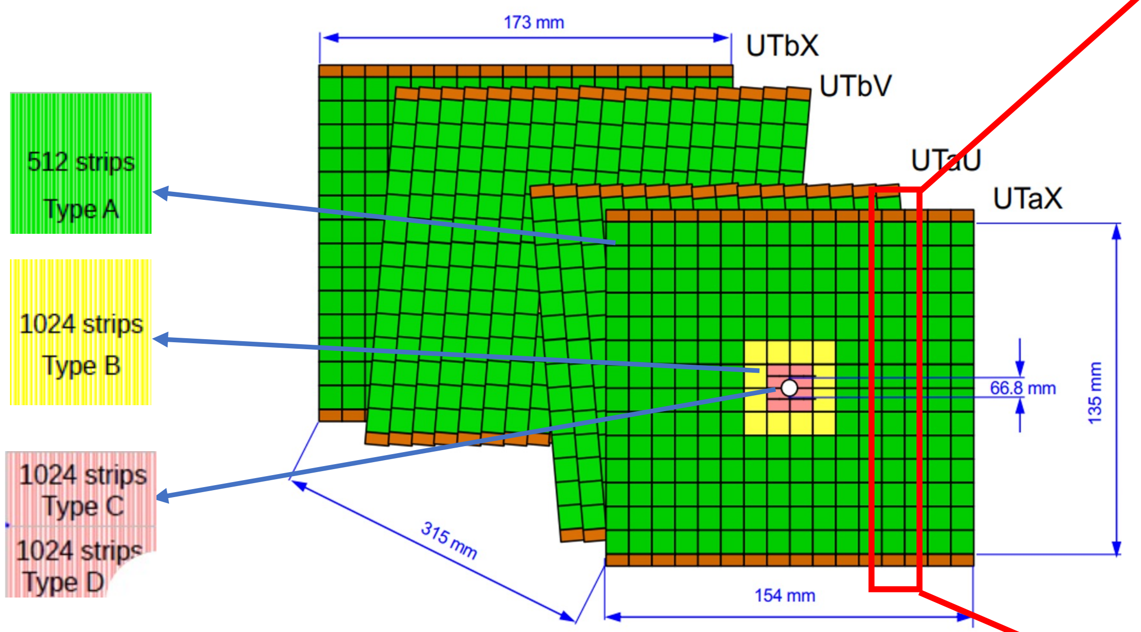
- We use vacuum to pickup and hold components in place. Vacuum is maintained during epoxy curing.
- During testing and transportation, straps (metal+foam) and 2 screws hold the ladder on the base of transportation box.

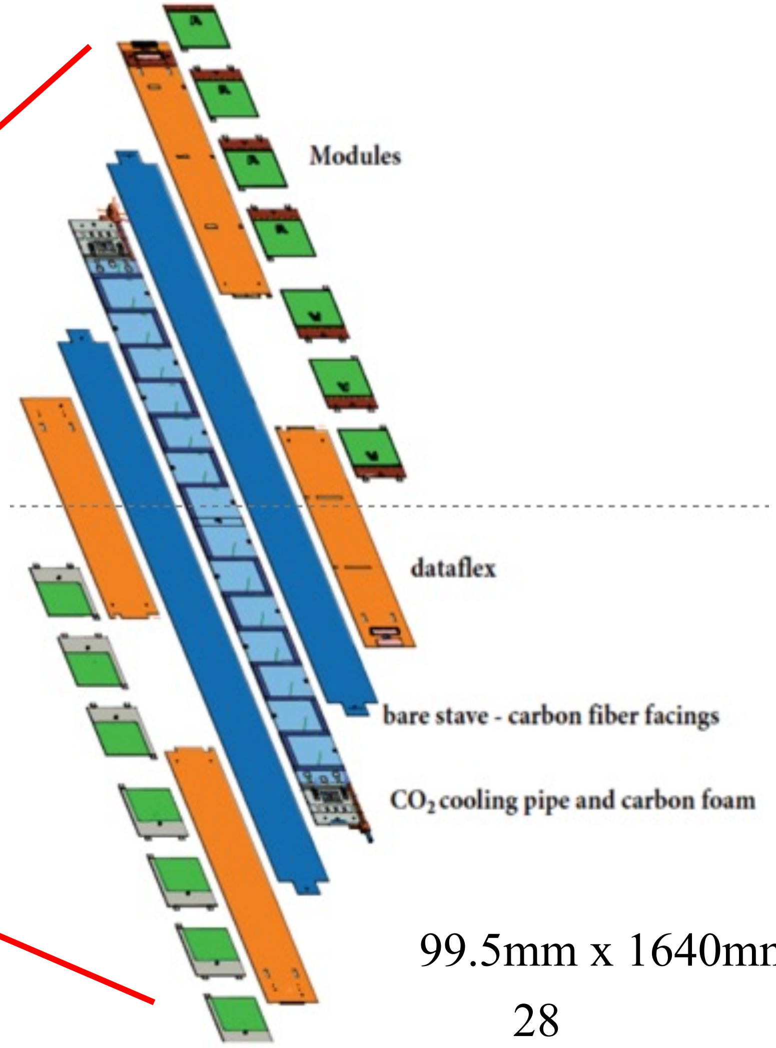


Prof Ting visited the AMS lab at IHEP on August 2, 2023

UT Detector

- Divided into A-side & C-side
- Consist of 4 layers of silicon strip detectors
  - organize in **68 staves**
  - **S-shaped** titanium cooling pipe
  - **Dower and data distribute in** Flex cables
- 4 types of modules with different silicon strip densities
- SALT (Silicon ASIC for LHCb Tracker) chip for front-end readout

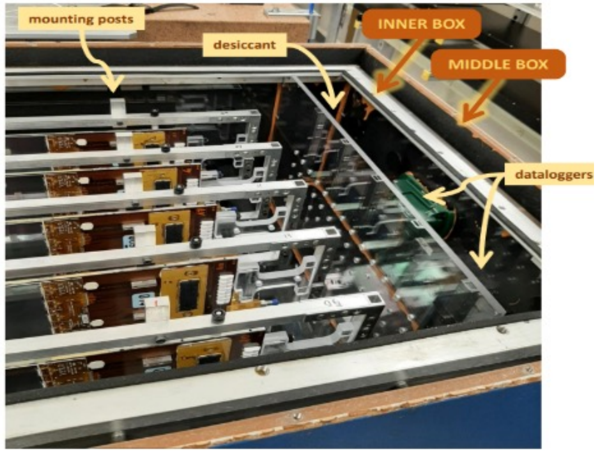




99.5mm x 1640mm

Stave Installation - Preparation

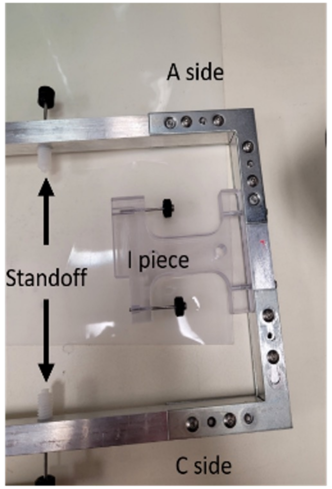
- Transport staves to CERN by shipment box, fixed on the strongback
- 2 cabinets are used to store staves (15 staves/cabinet) with dry air



The transport box

- 3 layers to give a better protect;
- Use dataloggers to record the temperature, humility and position information

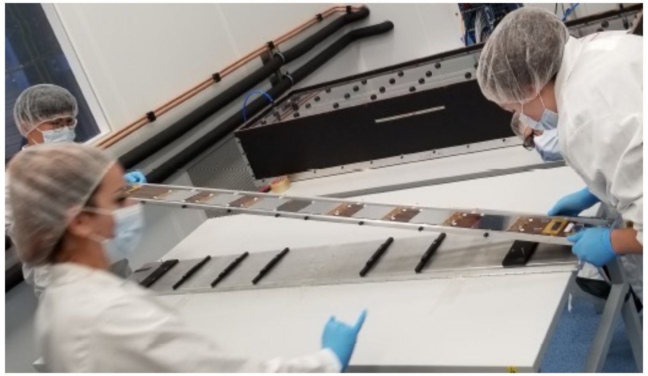
The strongback



The cabinet

1. Move to the stave plate, and remove the strongback
2. Check the bonding wire by magnifying glass (don't look directly above the stave)
3. Removal of protective caps (for cooling pipes & connectors)

Place carefully



A bad bonding example