环形正负电子对撞机
Circular Electron Positron Collider

中国科学院高能物理研究所
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CEPC requirement on electronics

Wei Wei

2023-10-24

Many thanks to Jingbo Ye, Jun Hu, Manqi Ruan, Zhijun Liang, Yunpeng Lu, Yiming Li, Huirong Qi, Mingyi Dong, Yong Liu, and Suen Hou…for the discussion

Outline

- **Motivation**
- **Detector background**
- **Requirements from the CEPC detectors**
- **Considerations for the CEPC electronics design**
  - The Frontend Electronics (FEE)
  - The Backend Electronics (BEE)
  - Common interface to other systems

Motivation

- **TDR is coming soon after 5 years R&D since CDR**
- **Several related discussions in previous workshops**
  - TDAQ discussion @ Shanghai 2020, Yangzhou 2021
    - Detector requirements for the TDAQ, especially data volume, were collected
  - The 4th conceptual detector design was proposed @ Yangzhou 2021
- **It is time to update and converge from all detector R&Ds to a electronics system design**

From the previous TDAQ discussion

	Vertex	Silicon Tracker	TPC	DC	ECAL	HCAL	DR CAL	Muon	LumiCal
Total Volume	4Gb/s/chip*5000 ~=20Tb/s	10Gb/s*4k=40 Tb/s	13.8GB/s	>=1TB/s	11.6+9GB/s	0.3+1.5GB/s	~40GB/s	300M B/s	2.1*2GB/ s
Zero-Suppressi on	Yes	1/(5-10),<10T B/s	Yes	YES,~=60G B/s	NA	NA	YES	YES	Yes,0.01
Trigger based	160Mb/s/chip*5 000	Same	Yes	60GB/s	YES	YES	YES	YES	21*2MBp s
Trigger(less)	Both,Trigger based prefer	Trgger based, triggerless possible	Triggerless possible	Trigger based	YES	YES	NA	No,Ma ybe	YES
clocks	NA	Yes	Yes	NA	NA	NA	NA	NA	NA

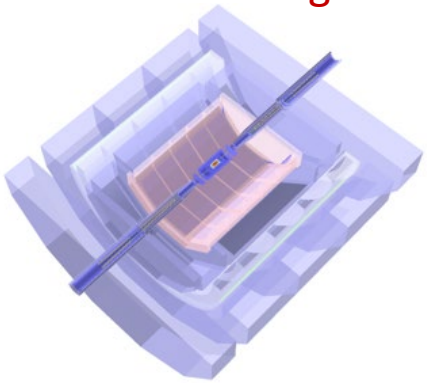
- **The discussions mainly focused on data rate calculation**
- **Not go into details of the electronics system**

ZA Liu, CEPC workshop 2020
Later updated in CEPC2021

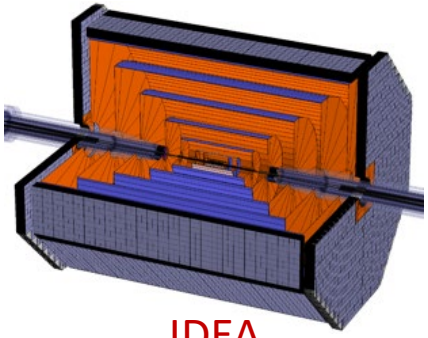
Detector Background: the CEPC Detector Designs

CEPC Detectors in CDR

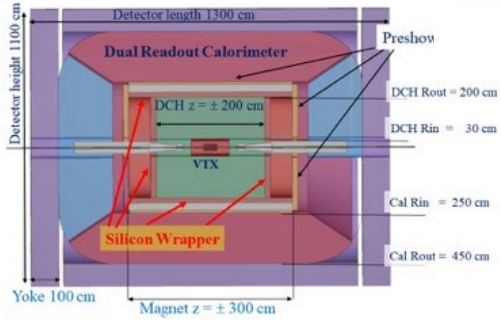
ILD-Like design



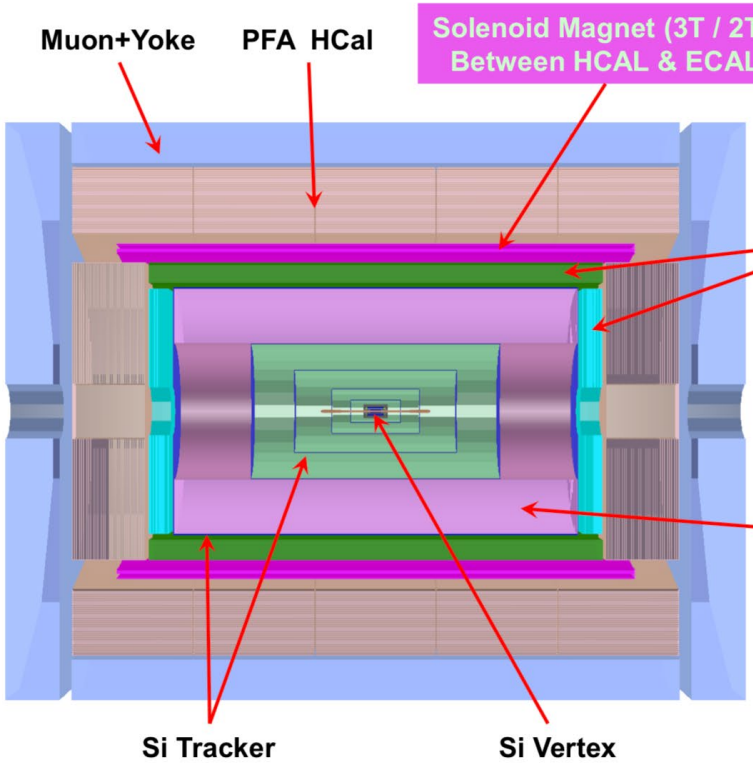
Full silicon



IDEA



The 4th Conceptual Detector Design



Advantage: the HCAL absorbers act as part of the magnet return yoke.

Challenges: thin enough not to affect the jet resolution (e.g. BMR); stability.

Transverse Crystal bar ECAL

Advantage: better π^0/γ reconstruction.

Challenges: minimum number of readout channels; compatible with PFA calorimeter; maintain good jet resolution.

Drift chamber that is optimized for PID

Advantage: Work at high luminosity Z runs

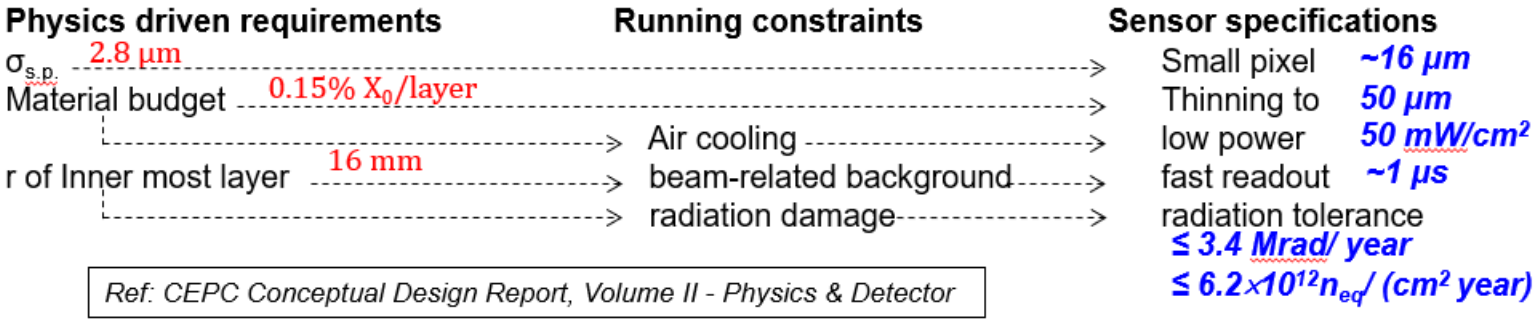
Challenges: sufficient PID power; thin enough not to affect the moment resolution.

JC Wang, CEPC workshop 2021

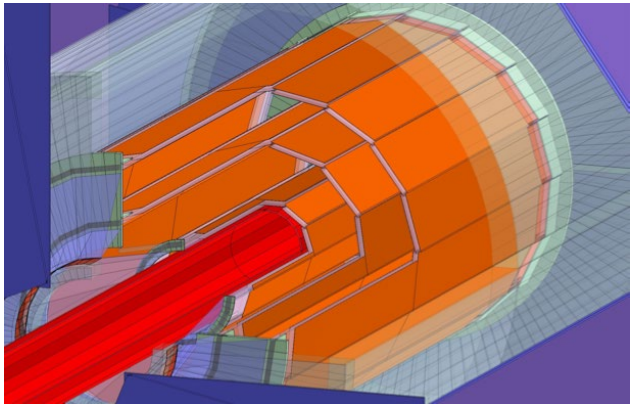
The main goal of this discussion

- **Collect requirements from related detectors on electronics**
  - Vertex, Tracker, TPC, Drift Chamber, CAL, LGADTOF, LumiCal…
- **Common question template on requirement**
  - On physics requirement
    - Detector target
    - Parameters that measures (T, E, dE/dx, dN/dx, …)
  - On signal processing
    - Detector channels for electronics
    - Counting rate
    - Signal characteristics (Q, I, V, rising/falling edge, width…)
    - Dynamic rage
    - Requirement on measurement (linearity, accuracy…)
    - Background noise
  - On overall system
    - Detector interface (cabling, socket, detector impedance …)
    - Power budget & material budget
    - Working conditions (temperature, cooling, special mechanics…)

Feedbacks from sub-detector systems - Vertex



Ref: CEPC Conceptual Design Report, Volume II - Physics & Detector

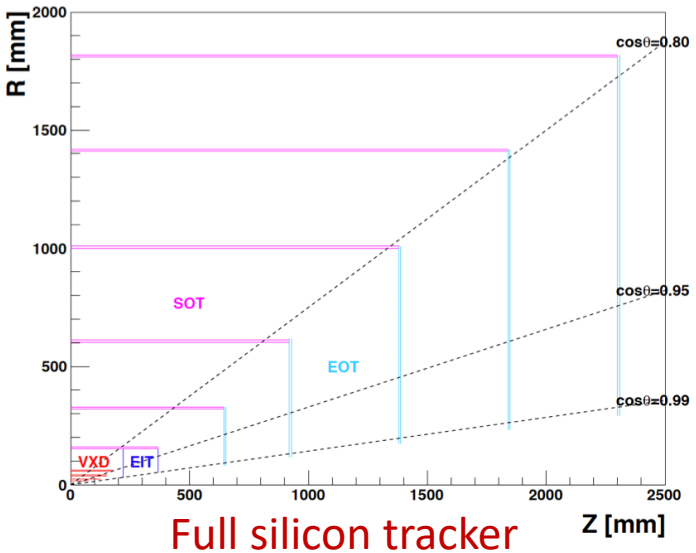


	R (mm)	|z| (mm)	Number of ladders	Number of chips
Layer 1	16	125.0	10	200
Layer 2	18	125.0		
Layer 3	37	125.0	22	440
Layer 4	39	125.0		
Layer 5	58	125.0	32	640
Layer 6	60	125.0		

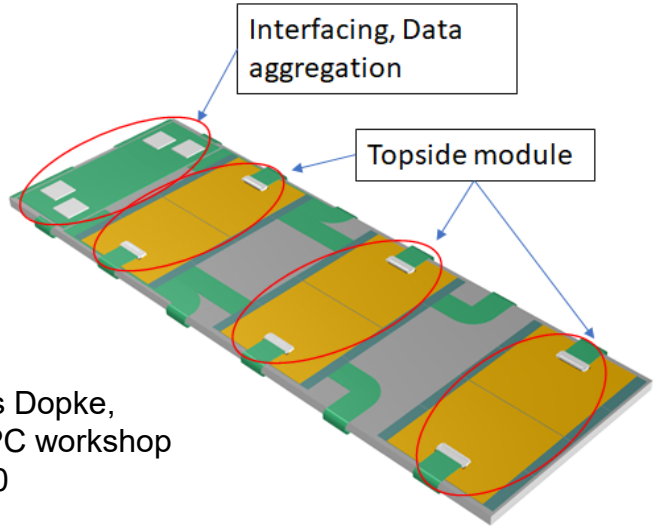
- **A thin pixel detector with a small pixel size**
  - Small electrode MAPS
- **Detector channels**
  - 64 double-sided ladders, ~1280 chips
  - ~ 0.5~1M pixels/chip
- **2D resolution ~3μm, with fast readout capability**
  - Hit rate ~40MHz/cm^2 @ W, ~32bit/hit
  - Timestamp with 25ns resolution for Z pole
  - Data rate
    - 205Gbps@Trigger；5.12Tbps@Triggerless
- **Overall system**
  - Lower material budget
    - Low power & air cooling & lower material mechanics
  - Radiation tolerance

The Tracker

Yiming Li



Full silicon tracker



Jens Dopke, CEPC workshop 2020

silicon tracker module

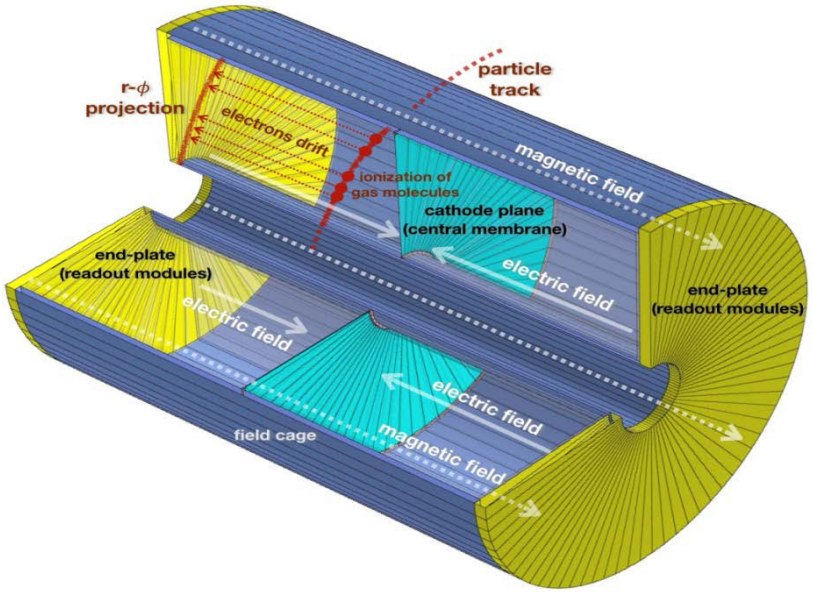
- **A large area silicon tracker with ~10μm spatial resolution @ r-φ**
  - ~70-140m^2 with ~50μm pixel pitch
  - Should be cost effective (like HVCMOS)
- **Hit rate and signal measurement**
  - 10^{-4} hit/cm^2/event @ Z, ~10bits per hit
    - 10b time stamp + 7b TOT
- **Detector channels**
  - ~60k modules (each with 4 chips)
  - 1Gbps data link per module and 10+ Gbps high speed link per structure
- **Overall system**
  - 160mW/cm^2 => 2.6W/module (O(100kW) for all)
  - Liquid cooling expected @-20 ℃

ATLASPix3 features

- TSI 180nm HV process on 200 Ωcm substrate
- Pixel size 50 × 150 μm^2
- 132 columns × 372 rows (20.2 × 21 mm^2 chip)
- Each pixel has 7-bit TOT + 10-bit timestamp
- Continuous / triggered readout with 8b10b / 64b66b coding
- Power consumption ~160 mW/cm^2.

TPC

Huirong Qi

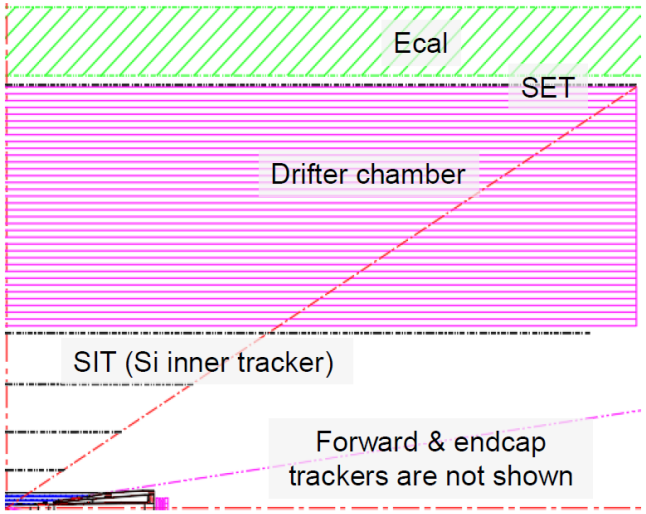


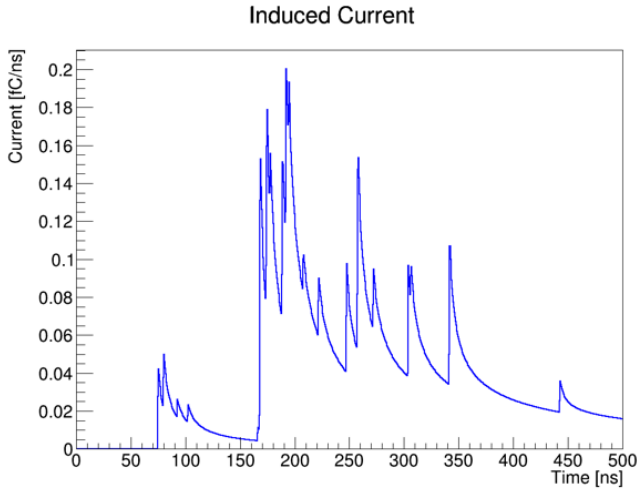
Parameter	Specification
Noise	<200e
Conversion gain	>15mV/fC
Peaking time (defaul)	100ns
Non lineartity	<1%
Cross talk	<0.3%
Dynamic range	>2000
Power consumption	<5mW/ch

- **~100μm spatial resolution @ r-φ**
  - Material budget: <1%X0 including outer field cage
  - GEM+μMEGAS / Pixel TPC
- **Hit rate and signal measurement**
  - Momentum resolution: ~10^{-4}/GeV/c
  - dE/dx resolution: <5%
  - Time resolution : ~100ns
- **Detector channels**
  - 5k chn/module; 84 module/endplate; 2 endplate => 840K channels => should be really low power
  - 6.5K ASIC chip if 128chn/chip
- **Data rate**
  - 48K chn/hit @10^{-4}/ BX / channel
  - 7b chn ID + 9b ADC per hit + 2B per ASIC = 22KB / BX = 110Gbps for the overall detector
- **Overall system**
  - CO_2 cooling
  - Trigger or triggerless

Drift Chamber

Mingyi Dong





- **A Drift Chamber optimized for PID**
  - better than 2σ K/π separation for P < 20GeV/c
- **Signal measurement**
  - dN/dx for cluster counting method
- **Signal characteristics**

Parameters	Value	Parameters	Value
Rising	0.5~1ns	Falling	~tens ns
Pulse width	Hundreds ns	Pulse spacing (overlapping)	few~dozen ns
Amplitude	Dozen~hundred nA	Pulse charge	Ten~dozen fC

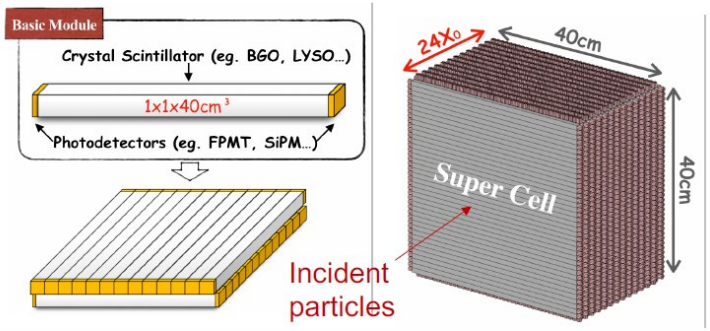
- **Detector channels and data rate**

		Higgs	Z
Trigger-less		256 Gbps	6.4 Tbps
Trigger	Trigger rate	1 kHz	100 kHz
	Max #wires/event	25k	10k
	bandwidth	20 Gbps	800 Gbps

50 peaks/wire*, 16bit/peak from F.Grancagnolo

FY Guo, CEPC workshop 2021

CAL



- **Long crystal bars with dual-end readout by SiPM/FPMT**
  - large dynamic and fast frontend for electronics – 5D CAL
  - Large number of chn: lower power & low cost

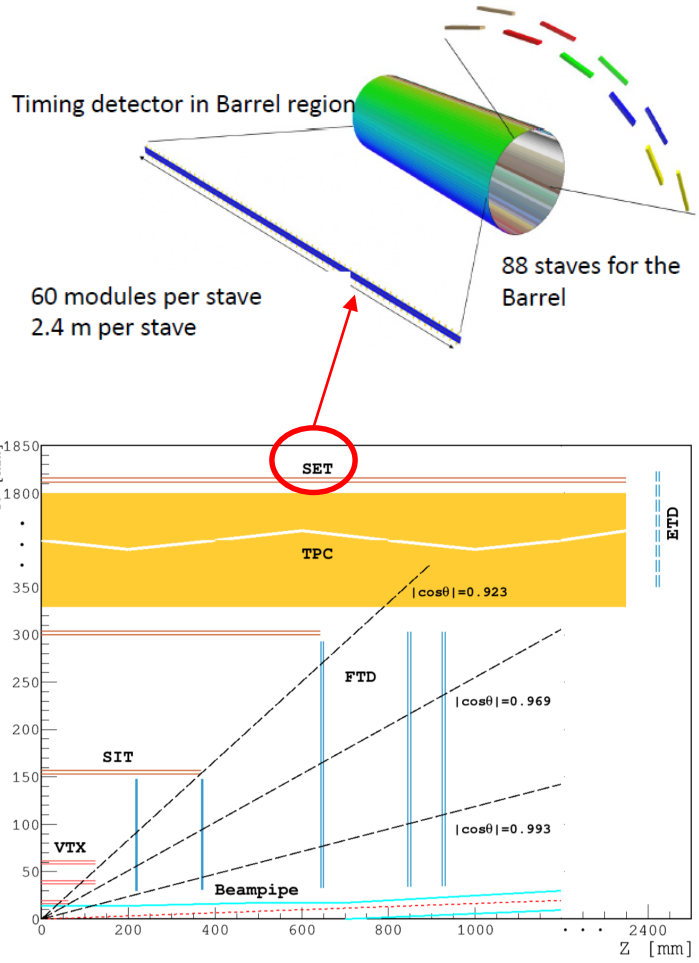
Key Parameters	Value/Range	Remarks
MIP light yield	~200 p.e./MIP	~8.9 MeV/MIP in 1 cm BGO
Dynamic range	0.1~10^3 MIPs	Energy range from ~1 MeV to ~10 GeV
Energy threshold	0.1 MIP	Equivalent to ~1 MeV energy deposition
Timing resolution	~400 ps	Limits from G4 simulation (validation needed)
Crystal non-uniformity	< 1%	After calibration
Temperature stability	Stable at ~0.05 Celsius	Reference of CMS ECAL
Gap tolerance	~100 μm	TBD via module development

ECAL options	#Channels [Million]	Occupancy [%]	#bit per channel	#readout channels/evt	Data Volume per event	Data rate at 100kHz
Crystal ECAL with long bars (Barrel)	0.85	3.4	32	28.9 k	116 kByte	11.6 GBytes/s
Crystal ECAL with long bars (Endcap)	0.36	6.2	32	22.4 k	90 kByte	9.0 Gbytes/s

ECAL options	#Channels [Million]	Occupancy [%]	#bit per channel	#readout channels/evt	Data Volume per event	Data rate at 100kHz
Scintillator HCAL Barrel	3.6	0.02	32	0.72 k	2.9 kByte	0.3 GBytes/s
Scintillator HCAL Endcap	3.1	0.12	32	3.72 k	15 kByte	1.5 Gbytes/s
RPC HCAL Barrel	32	0.004	8	1.28 k	1.28 kByte	0.13 GBytes/s
RPC HCAL Endcap	32	0.01	8	3.2 k	3.2 kByte	0.32 Gbytes/s

LGAD TOF

Zhijun Liang



Baseline detector concept in CDR

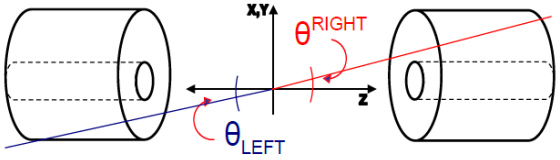
- **Recommended by the Int. Advisory Committee**
- **Detector concept**
  - Area of detector (Barrel : 50 m^2 , Endcap 20 m^2)
  - Strip-like sensor (4cm × 0.1 cm)
- A Timing detector and part of the tracker (SET)
  - Timing resolution: 30-50 ps
  - Spatial resolution: ~ 10 μm
- **Signal measurement**
  -

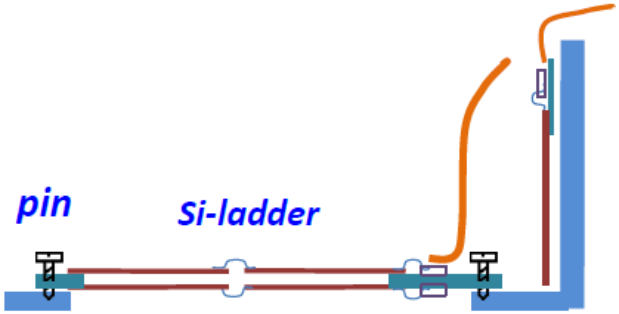
	ATLAS HGTD	CEPC TOF
Area (m^2)	6.4	~ 70
Granularity	mm^2 (1.3 mm ×1.3mm)	~ cm^2 (40m × 0.2mm)
Channel number	**~ 3.6 × 10^6**	**~ 7×10^6**
Module assembly	Bump bonding	Wire bonding at strip
MIP Time resolution	30-50 ps	30-50 ps
Spatial resolution	~ 300 μm	~ 10 μm
探测器信号幅度	2fC- 20fC	2fC- 20fC

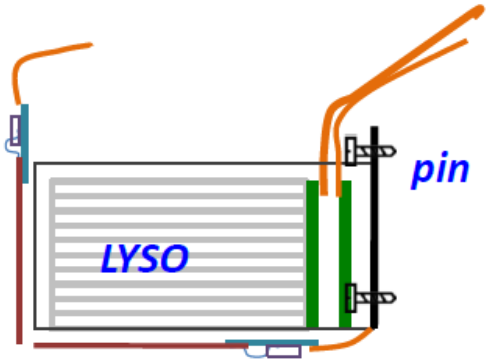
- **Data rate**
  - 200kHz event @ 16bit/event (9bTOT + 7bTOA)
  - 100k chips for 70m^2
- **Power: <** 2W per chip

LumiCal

Suen Hou





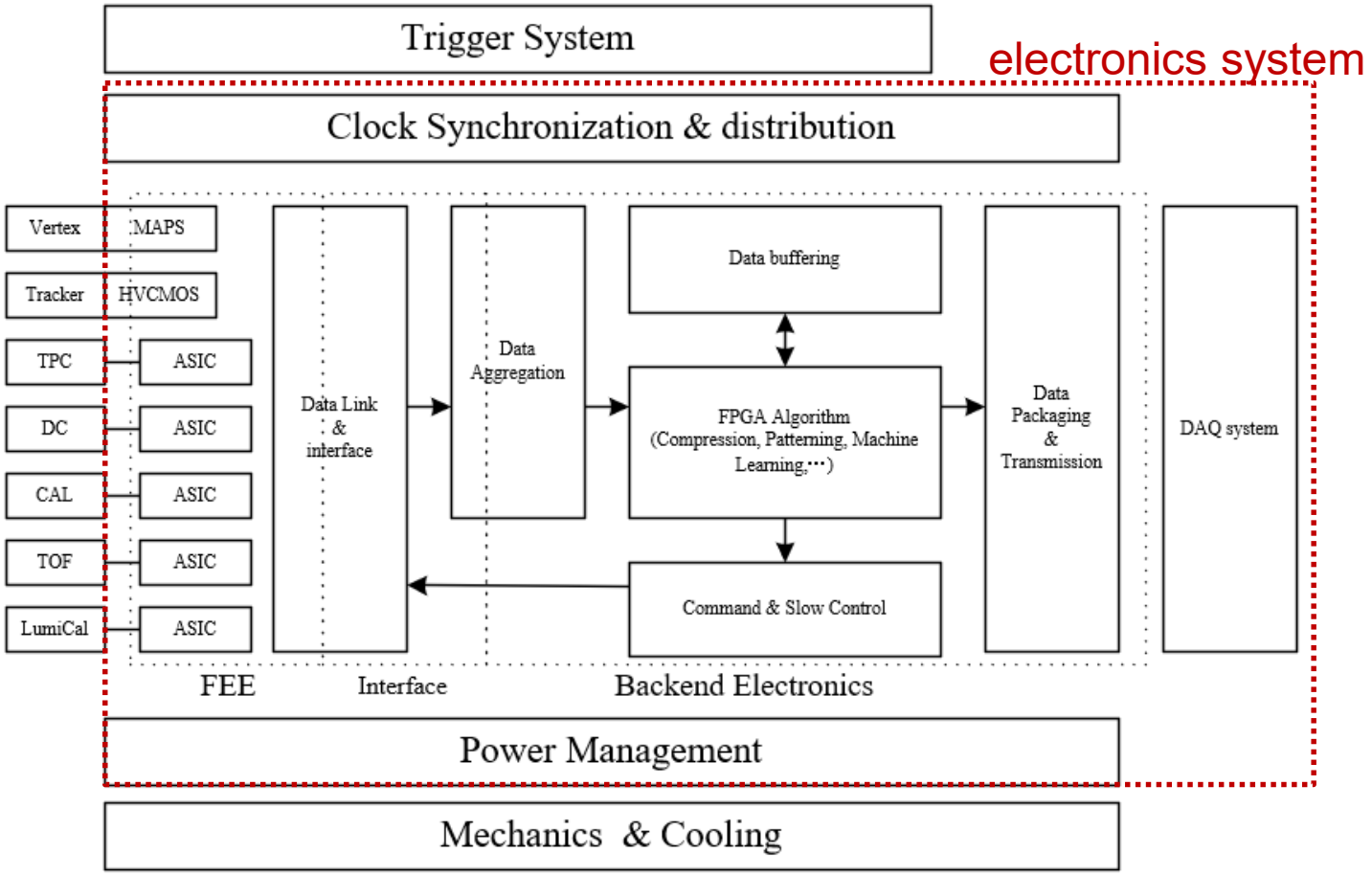


- **Detector concept**
  - measure the Bhabha scattering events for the integrated luminosity
  - Accuracy: 0.1% @ Higgs, 10^{-4} @ Z
- **Signal measurement**
  - e+e- and low energy photons
  - Using silicon strip + LYSO with SiPM

Parameters	Silicon strip	LYSO + SiPM
Signal processing	Ultra fast ADC, 50ns signal width, 25 B.C. separation	
Interface	10Gbps optical link, Triggerless	
Signal dynamic range	MIP	0.3~100GeV (like ECAL)
Channels	16K (2sides*2layers*4k)	14K (4 sets/side * 1.7K)
Event rate	0.003 events /b.c.	0.00016 events/b.c.
Power limit	40 chips @10W	10W per set

- **Data volume:** ~160 Mbps

Consideration of the CEPC electronics system



- **Q: (except Front ASIC) can we make the electronics system in a unified style?**
- **Q: what is the border between detector/FEE, FEE/data interface, frontend/backend, electronics/trigger, …?**

From detectors to (analog) frontend electronics

	Vertex	Tracker	TPC	DC	CAL	TOF	LumiCal
Detector for readout	CMOS Sensor	HVCMOS	GEM / Pixel	Drift chamber	SiPM	Strip-LGAD	Si Strip SiPM
Main Func for FEE	X+Y	XY + nsT	E + nsT	Cluster counting	E + psT	X + psT	X for strip E for SiPM
Channels per chip	500k Pixelized	50k Pixelized	128 / Pixelized	-	32~128	128	32~128
Ref. Signal processing	XY address + timestamp	Timestamp + TOT	Wave + ADC/ Pixel	Ultra fast PA + ADC	TOT + TOA/ ADC + TDC	ADC + TDC / TOT+TOA	ADC
Main challenge for FEE	• Small pixel size • Fast readout • Low power	• Large area • Cost effective • Low power	• Low power ADC with high sampling rate	• Ultra fast PA • Ultra fast ADC	• ~10^4 dynamic range • ~400ps timing • Huge channel Low power	• ~30ps timing	• Fast ADC
Other Comments	CIS technology an issue	HVCMOS technology an issue		Technology for PA an issue	• All challenges combined • Should be cost effective		

- **Dedicated AFEs have to be designed while various but major challenges have to be solved**

Detector R&D activities widely conducted, while…

Projects overview: FTE

PBS	Task Name	Team	Faculty	Postdoc	Students	Engineers
	Total:		**156**	**12**	**56**	**16**
	CEPC Detector R&D Project					
1	**Vertex**					
1.1	**Vertex Prototype**	China+ international collaborators	21		17.2	3.5
1.2	**ARCADIA CMOS MAPS**	INFN, Italy	55 people, mostly staff INFN and University Associates			
2	**Tracker**					
2.1	**TPC Module and Prototype**	IHEP, Tsinghua	3		4	1
2.2	**Silicon Tracker Prototype**	China, UK, Italy	50		4	5
2.3	**Drift Chamber Activities**	INFN, Novosibirsk	2.5	2.4	1.8	0.8
3	**Calorimetry**					
3.1	**ECAL Calorimeter**					
3.1.1	Crystal Calorimeter	IHEP, Princeton + others	1.3		1.5	
3.1.2	PFA Sci-ECAL Prototype	USTC, IHEP	1.9		2.5	
3.2	**HCAL Calorimeter**					
3.2.1	PFA Digital Hadronic Calorimeter	SJTU, IPNL, Weizmann, IIT, USTC	2.1	1.8	2.6	0.3
3.2.2	PFA Sci-AHCAL Prototype	USTC, IHEP, SJTU	2.3	0.8	4	
3.3	**Dual-readout Calorimeter**	INFN, Sussex, Zagreb, South Korea	4.2	2.2	6.8	1.3
4	**Muon Detector**					
4.1	Scintillator-based Muon Detector	Fudan, SJTU	1.2		2.1	0.2
4.2	Muon and pre-shower µRWELL-	INFN, LNF	2	1.5	1	0.3
5	**Solenoid**					
5.1	LTS solenoid magnet	IHEP+Industry	2	0	1	0.5
5.2	HTS solenoid magnet	IHEP+Industry	1.5	0	1	0.5
6	**MDI**					
6.1	LumiCal Prototype	AC, IHEP	1	1	2	1
6.2	Interaction Region Mechanics	IHEP	0.5	0.3	1.5	2
8	**Software and Computing**	IHEP, SDU	7	2	3	0

- **R&Ds for various detectors, wide collaborations, large amount of man power, however…**

Joao Costa, CEPC workshop 2021

Frontend electronics R&D activities

Projects overview: FTE

PBS	Task Name	Team	Total: 156 Faculty	12 Postdoc	56 Students	16 Engineers
	CEPC Detector R&D Project					
1	Vertex					
1.1	Vertex Prototype	China+ international collaborators	21		17.2	3.5
1.2	ARCADIA CMOS MAPS	INFN, Italy	55 people, mostly staff INFN and University Associates			
2	Tracker					
2.1	TPC Module and Prototype	IHEP, Tsinghua	3		4	1
2.2	Silicon Tracker Prototype	China, UK, Italy	50		4	5
2.3	Drift Chamber Activities	INFN, Novosibirsk	2.5	2.4	1.8	0.8
3	Calorimetry					
3.1	ECAL Calorimeter					
3.1.1	Crystal Calorimeter	IHEP, Princeton + others	1.3		1.5	
3.1.2	PFA Sci-ECAL Prototype	USTC, IHEP	1.9		2.5	
3.2	HCAL Calorimeter					
3.2.1	PFA Digital Hadronic Calorimeter	SJTU, IPNL, Weizmann, IIT, USTC	2.1	1.8	2.6	0.3
3.2.2	PFA Sci-AHCAL Prototype	USTC, IHEP, SJTU	2.3	0.8	4	
3.3	Dual-readout Calorimeter	INFN, Sussex, Zagreb, South Korea	4.2	2.2	6.8	1.3
4	Muon Detector					
4.1	Scintillator-based Muon Detector	Fudan, SJTU	1.2		2.1	0.2
4.2	Muon and pre-shower µRWELL-	INFN, LNF	2	1.5	1	0.3
5	Solenoid					
5.1	LTS solenoid magnet	IHEP+Industry	2	0	1	0.5
5.2	HTS solenoid magnet	IHEP+Industry	1.5	0	1	0.5
6	MDI					
6.1	LumiCal Prototype	AC, IHEP	1	1	2	1
6.2	Interaction Region Mechanics	IHEP	0.5	0.3	1.5	2

	Vertex	Tracker	TPC	DC	CAL	TOF	LumiCal
Dedicated ASIC exists?	Y	Y	Y	-	Y/N	-	-
Candidate chips	Jadepix / MIC Taichupix	HVCMOS on SMIC55	WASA (AFE + ADC)	-	-	-	-
Chips used for R&D	Jadepix / MIC Taichupix / CPV	ATLASPix3	CASAGEM / Gridpix	PA box + ADC module	SPIROC PIST	ALTIROC	-

- **Requirements to electronics not only from specification, but a deeper involvement in dedicated designs**

Data link from FEE to backend

	Vertex	Tracker	TPC	DC	CAL	TOF	LumiCal
Data rate per chip	160Mbps @trigger / 4Gbps @triggerless	1.28Gbps@triggerless	-	-	-	$6.4* 10^{-3}$ bit/event/chip	-
Data rate per module	3.2Gbps@Trigger / 80Gbps@Triggerless	O(Gbps)@ module O(10Gbps)@ structure	-	-	-	-	-
Overall data rate	205Gbps@Trigger / 5.12Tbps@Triggerless	~40Tbps	110Gbps	800Gbps@ Trigger / 6.4Tbps @triggerless	93Gbps + 72Gbps		33.6Gbps

- **Q: high speed serial link needed inside FE chips?**
  - maybe yes for vertex & tracker, especially for triggerless mode
- **Q: data aggregation chip needed at the module/structure level?**
  - maybe yes for vertex & tracker
- **Q: possible to follow a common protocol & interface for data link?**
  - Interface designs may vary due to the CMOS process, protocol can be unified
  - Cabling? Optical? Or even wireless?
  - Has to be rad-tol

From FEE to BEE

- **Dedicated algorithm in FPGA may have to vary from detectors**
  - Related to triggering, data compression, machine learning
  - Data aggregation for different AFE, if it is done in FPGA
- **Rest are possible to be designed in a unified style**
  - Clock synchronization & distribution
  - Data buffering
  - Data packaging and transmission to DAQ
  - Powering
  - Slow control
  - Issue: most has an interface with other system (TRG, DAQ, Mechanics …), not well defined yet
- **Q: major challenges exist with huge data rate, especially triggerless**
  - Very likely, new methodology has to be involved, yet no R&D
- **Q: do we need special algorithm for new physics approach, like PFA?**
  - Needs input from physics simulation
- **Issue: yet not a dedicated BEE system R&D for CEPC**

Interface between (Lvl 1) Trigger and Electronics

- **Common Question: Trigger or Triggerless?**
  - For some sub-detector, data volume really an issue for triggerless
  - Part of the detectors on trigger, rest triggerless?
    - Smart & local track/cluster finding to compress data? While R&D required
- **Q: who needs TRG input? Who contributes to TRG?**

	Vertex	Tracker	TPC	DC	CAL	TOF	LumiCal
get TRG	Y	Y	Y	Y	Y	Y	Y
Generate TRG info	N	N	Y	Y	Y	Y	Y
Data volume an issue for triggerless?	Maybe 5.12Tbps	Maybe 40Tbps	-	Maybe 6.4Tbps	-	-	-

- **Q: where in electronics, AFE or BEE, to communicate with TRG?**
  - If in ASIC AFE, trigger interface has to be defined asap before finalization
    - The latency and data buffering is also a critical issue for the chip design
  - Issue: need a overall consideration on TRG strategy, not only on calculation of the data volume

Interface with other systems

- **Clocking**
  - How to synchronize with BX clock?
    - Multiple bunch spacings: Higgs: 680ns; W: 210ns; Z: 25ns
  - What clock needed for different detector?
- **Power management**
  - Overall powering design maybe too early for CEPC
  - Consideration on AFE powering has to start
    - Serial powering? Rad-tol powering blocks?
- **Cooling**
  - Has to be integrated closely with electronics system
  - Designs greatly depend on the cooling strategy, especially for AFEs
    - Air cooling or liquid cooling? Or Mixed?
- **Mechanics**
  - Special mechanic scheme has to be generally defined for the design of AFE
    - e.g. Vertex on long Flex, ECAL module organization for HG…
  - Technology vender for low material still an issue
    - e.g. Aluminum Flex Cable for Vertex not available
- **Needs input if any special requirements to electronics exist**

What to do next?

- **Further and thorough discussion with other systems**
  - A topical workshop on CEPC electronics may be more effective
- **R&Ds and time needed for the major challenge**
  - Each R&D cost at least ~5 to 10 year if from scratch
  - ASIC developed for specific detectors involved in each detector system
  - Real time data compression and machine learning algorithm
  - Rad-tol ASICs for common applications
    - Data link chips & unified protocol
    - Powering chips (LDO, DC-DC) and module
  - R&D for the possible wireless communications
- **Manpower a big issue**
  - Please ref to the talk given by Paulo in the plenary session, on how many people involved for LHC

Summary

- Detector requirements to electronics system preliminarily collected
- Many questions, waiting to answers
- Various AFE await for a dedicated design, yet not a clear shape and plan of a overall electronics design for CEPC
- Some critical considerations must be taken now

Thank you very much for your attention !

Reference all based on previous workshops of CEPC, if not listed

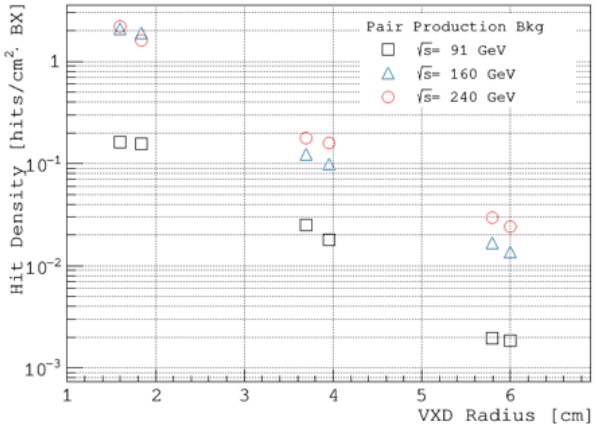
Requirements of the CEPC Detector from Physics

The physics motivations dictate our selection of detector technologies

Physics process	Measurands	Detector subsystem	Performance requirement
$ZH, Z \to e^+e^-, \mu^+\mu^-$ $H \to \mu^+\mu^-$	$m_H, \sigma(ZH)$ $\mathrm{BR}(H \to \mu^+\mu^-)$	Tracker	$\Delta(1/p_T) =$ $2 \times 10^{-5} \oplus \frac{0.001}{p(\mathrm{GeV})\sin^{3/2}\theta}$
$H \to b\bar{b}/c\bar{c}/gg$	$\mathrm{BR}(H \to b\bar{b}/c\bar{c}/gg)$	Vertex	$\sigma_{r\phi} =$ $5 \oplus \frac{10}{p(\mathrm{GeV})\times\sin^{3/2}\theta}(\mu\mathrm{m})$
$H \to q\bar{q}, WW^*, ZZ^*$	$\mathrm{BR}(H \to q\bar{q}, WW^*, ZZ^*)$	ECAL HCAL	$\sigma_E^{\mathrm{jet}}/E =$ $3 \sim 4\%$ at 100 GeV
$H \to \gamma\gamma$	$\mathrm{BR}(H \to \gamma\gamma)$	ECAL	$\Delta E/E =$ $\frac{0.20}{\sqrt{E(\mathrm{GeV})}} \oplus 0.01$

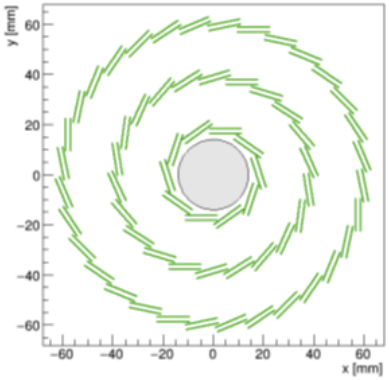
- Flavor physics ⇒ Excellent PID, better than 2σ separation of π/K at momentum up to ~20 GeV.
- EW measurements ⇒ High precision luminosity measurement, δL / L ~ 10^{-4}.

以CEPC顶点探测器为例



- 探测器方案
  - 信号特征、动态范围
    - 阈值~200e，动态范围~1000e
  - 感兴趣量
    - 位置分辨：3~5μm
  - 事例率
    - Hit Density from background：2.5hits/bunch/cm^2 for Higgs/W; 0.2hits/bunch/cm^2 for Z
    - Bunch Spacing： Higgs: 680 ns; W: 210 ns; Z: 25 ns
  - 其他要求
    - 物质量：0.15%
  - 探测器规模（Taichu原型机）
    - 三层：Ladder共约64个
    - 双面ladder共含芯片1280片

	R (mm)	|z| (mm)	Number of ladders	Number of chips
Layer 1	16	125.0	10	200
Layer 2	18	125.0		
Layer 3	37	125.0	22	440
Layer 4	39	125.0		
Layer 5	58	125.0	32	640
Layer 6	60	125.0		



以CEPC顶点探测器（Taichu）为例

- 电子学方案
  - MAPS像素探测器@small electrode ——物质量、阈值200e
  - 像素尺寸：16~25μm——位置分辨
  - 计数率：40MHz/cm^2
- 触发方案
  - 不参与触发，仅接收触发
- 数据处理方案
  - 数字像素、像素自触发
  - 像素地址编码——感兴趣量
  - 辅助时间戳来帮助高计数率Trigger ID判断
- 数据率
  - 触发后数据率：160Mbps/chip （50kHz触发率）
  - Triggerless：4Gbps/chip
  - 读出方案：高速串行
- 数据量
  - Ladder ： 3.2Gbps@Trigger；80Gbps@Triggerless
  - 探测器总体：205Gbps@Trigger；5.12Tbps@Triggerless

Main specs of the full size chip for high rate vertex detector

- **Bunch spacing**
  - **Higgs: 680ns; W: 210ns; Z: 25ns**
  - **Meaning 40M/s bunches (same as the ATLAS Vertex)**
- **Hit density**
  - **2.5hits/bunch/cm^2 for Higgs/W; 0.2hits/bunch/cm^2 for Z**
- **Cluster size: 3pixels/hit**
  - **Epi- layer thickness：~18μm**
  - **Pixel size：25μm×25μm**
- **Hit rate: 120MHz/chip @W**

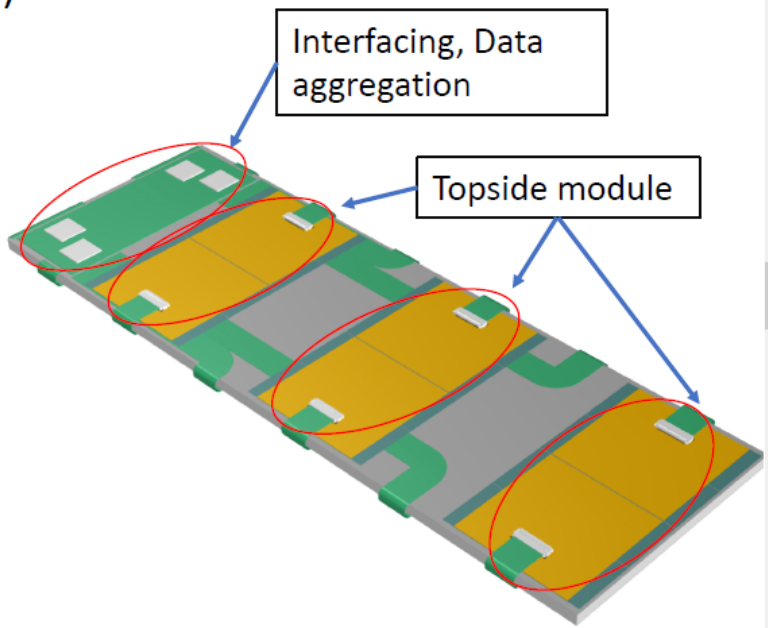
- Two major constraints for the CMOS sensor
  - Pixel size: < 25μm* 25μm (σ~5μm)
    - aiming for 16μm*16μm (σ~3μm)
  - Readout speed: bunch crossing @ 40MHz
- None of the existing CMOS sensors can fully satisfy the requirement of high-rate CEPC Vertex Detector
- TID is also a constraint
  - 1~2.5Mrad/year as required in MOST2 is achievable

For Vertex	Specs	For High rate Vertex	Specs	For Ladder Prototype	Specs
Pixel pitch	<25μm	Hit rate	120MHz/chip	Pixel array	512row×1024col
TID	>1Mrad	Date rate	3.84Gbps --triggerless ~110Mbps --trigger	Power Density	< 200mW/cm^2 (air cooling)
		Dead time	<500ns --for 98% efficiency	Chip size	~1.4cm×2.56cm

Ladder

What might the silicon tracker look like

- Many large-scale structures (call them local support) supporting smaller units (call them modules) mechanically and electrically
  - Medium Speed links per module to deliver data (Gb/s)
  - High Speed link(s) per structure to transfer aggregated data from multiple modules (10+ Gb/s)
- 50m^2 of silicon based on active sensors at current reticule sizes:
  - About 150k active sensor chips
  - About 40k “modules”
  - As per previous numbers: O(4k) high speed links
- Expecting a particle/track occupancy of about 10^{-4}/cm^2/event in Z-mode
  - I work based on that, not involved enough with the physi to look at other numbers, but they’ll be “easier”

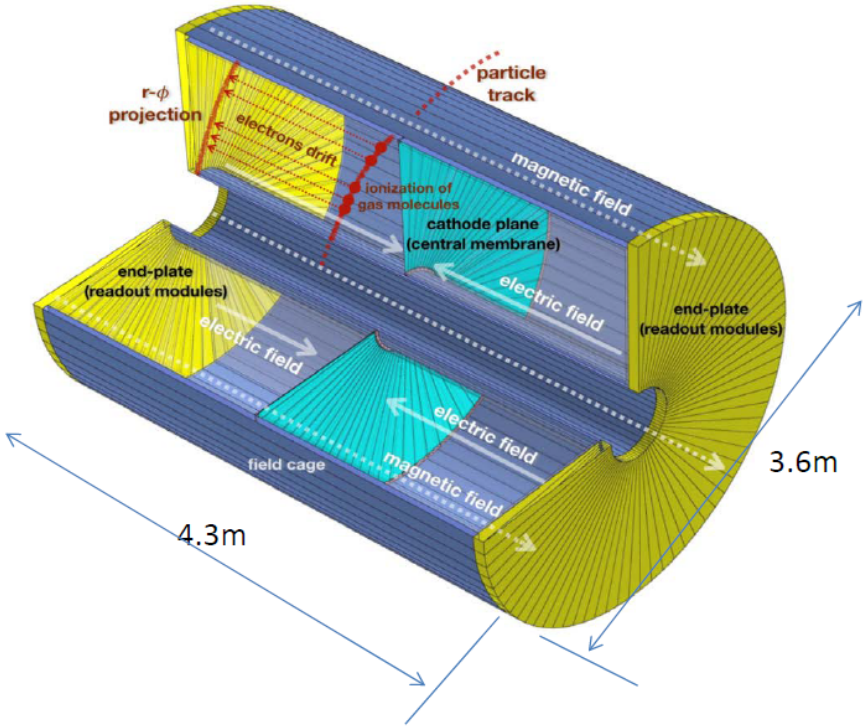


TPC

Overview of TPC concept

TPC detector concept:

- Under 2-3 Tesla magnetic field (Momentum resolution: ~10^{-4}/GeV/c with TPC standalone)
- Large number of 3D space points(~220 along the diameter)
- dE/dx resolution: <5%
- ~100 μm position resolution in rφ
  - ~60μm for zero drift, <100μm overall
  - Systematics precision (<20μm internal)
- TPC material budget
  - <1X_0 including outer field cage
- Tracker efficiency: >97% for pT>1GeV
- 2-hit resolution in rφ : ~2mm
- Module design: ~200mm×170mm
- Minimizes dead space between the modules: 1-2mm



TPC detector concept

Requirements of TPC for TDAQ - I

Reference info from ALICE TPC / STAR TPC (in operation) and ILD TPC (future)

- **Pads TPC (example)**
  - There is full size TPC detector with the outer radius of 1.8m and inner radius of 0.3m. All of the two endplate mounted in two sides.
  - Every channel will be connected in the small pad(1mm*6mm), thus the total number of channels is 5000/module*84/endplate*2=840K channels.
  - Each ASIC has 128 channels and there is 6.5K ASIC chips integrated with the FEE and DAQ.
  - The bunch crossing (BX) rate is 40 MHz and we need to deal with every BX at one IP in circular collider.
  - Low power consumption FEE readout

Experiment / Timescale	Application Domain	MPGD Technology	Total detector size / Single module size	Operation Characteristics / Performance	Special Requirements / Remarks
LHCb MUON DETECTOR > 2010	Hadron Collider / B-physics (triggering)	3-GEM	Total area: ~ 0.6 m^2 Single unit detect: 20-24 cm^2	**Max.rate**:500 kHz/cm^2 **Spatial res.**: ~ cm **Time res.**: ~ 3 ns **Rad. Hard.**: ~ C/cm^2	Redundant triggering
ATLAS MUON UPGRADE CERN LS2	Hadron Collider (Tracking/Triggering)	Resistive Micromegas	Total area: 1200 m^2 Single unit detect: (2.2x1.4m^2) ~ 2-3 m^2	**Max. rate**:15 kHz/cm^2 **Spatial res.**: <100μm **Time res.**: ~ 10 ns **Rad. Hard.**: ~ 0.5C/cm^2	Redundant tracking and triggering; Challenging constr. in mechanical precision
CMS MUON UPGRADE CERN LS2	Hadron Collider (Tracking/Triggering)	3-GEM	Total area: ~ 143 m^2 Single unit detect: 0.3-0.4m^2	**Max. rate**:10 kHz/cm^2 **Spatial res.**: ~100μm **Time res.**: ~ 5-7 ns **Rad. Hard.**: ~ 0.5 C/cm^2	Redundant tracking and triggering
ALICE TPC UPGRADE CERN LS2	Heavy-Ion Physics (Tracking + dE/dx)	4-GEM / TPC	Total area: ~ 32 m^2 Single unit detect: up to 0.3m^2	**Max.rate**:100 kHz/cm^2 **Spatial res.**: ~300μm **Time res.**: ~ 100 ns **dE/dx**: 11 % **Rad. Hard.**: 50 mC/cm^2	- 50 kHz Pb-Pb rate; - Continues TPC readout - Low IBF and good energy resolution
CEPC TPC DETECTOR CDR	e+e- Collider (Tracking + dE/dx)	GEM+Micromegas or Pixel TPC	Total area: ~ 2x10 m^2 Single unit detect: up to 0.04m^2	**Max.rate**:>100 kHz/cm^2 **Spatial res.**: ~100μm **Time res.**: ~ 100 ns **dE/dx**: <5%	- Higgs run - Z pole run - Continues TPC readout - Low IBF and dE/dx

Crystal ECAL: specifications

Key Parameters	Value/Range	Remarks
MIP light yield	~200 p.e./MIP	~8.9 MeV/MIP in 1 cm BGO
Dynamic range	0.1~10^3 MIPs	Energy range from ~1 MeV to ~10 GeV
Energy threshold	0.1 MIP	Equivalent to ~1 MeV energy deposition
Timing resolution	~400 ps	Limits from G4 simulation (validation needed)
Crystal non-uniformity	< 1%	After calibration
Temperature stability	Stable at ~0.05 Celsius	Reference of CMS ECAL
Gap tolerance	~100 μm	TBD via module development

Challenges/issues…

- Crystal size optimization, as well as realistic ECAL geometry design
- Sophisticated software for long bar crystal ECAL
- New BGO crystal with lower light output and faster decay time (collaboration with SIC-CAS)
- Limitation from SiPM dynamic range
- Radiation damage

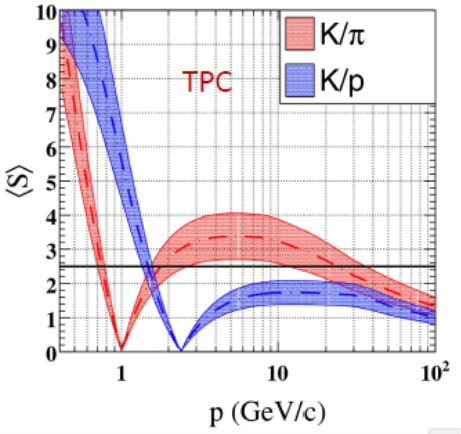
LGAD development for CEPC time of flight detector: Motivation

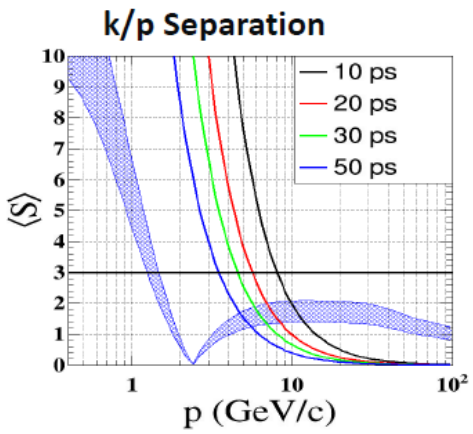
- CEPC will produce 10^{12} Z boson at Z pole: Rich flavor physics program
- **Particle separation problems** of Gas detector (dE/dx) for CEPC flavor physics:
  - **0.5-2 GeV for K/pi separation, >1.5 GeV for K/p separation**
- **CEPC International Advisory Committee: one of the key recommendations**

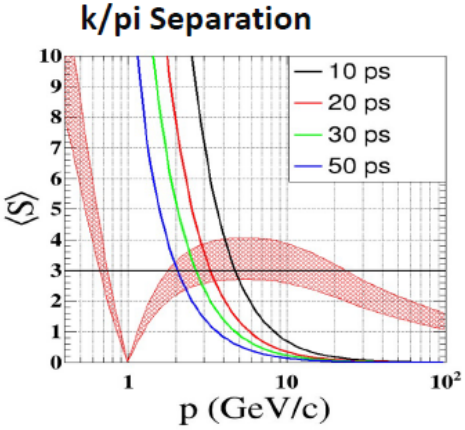
Precision timing detector should be determined as a matter of urgency (4D track)

- **Timing detector is complementary to gas detector:** improves the separation ability

0 - 4 GeV for K/pi separation, **0 – 8 GeV** for K/p separation







1. **探测器名和基本功能（比如TPC，测带电粒子径迹）：**
   LumiCal, 测量加速器束流e^+e^- 碰撞亮度 Luminosity
   架设在束流管 ±z = 700 mm，法蓝内外，探测低角度电子，
   在e^+e^- 碰撞时区内，筛选 Bhabha 弹性碰撞正负电子对事例，
   Monte Carlo QED 计算探测器事例量，反推出 Integrated Luminosity。
   准度要求 10^{-4}。
2. **需要探测的物理量（比如时间，能量，原初电离dE/dx, 原初电离束团数dN/dx, 闪烁光，等等）：**
   探测粒子： Ebeam 正负电子, 及跟随的 Final State Radiation 低能光子 (>~ 1GeV)
   在 bunch crossing 25 nsec，分辨束流正负电子弹性反射
   硅探测器： 电子 theta, phi 角度, 极端驱近 1 uRad 精准位置，
   LYSO 晶调： 标定 >Ebeam/2 电子，及区隔邻近的 FSR 光子
3. **探测器对电子学输出的通道数，**
   电子碰撞点硅条探测器: 每侧两层共4层，每层4k ch. 总共16k 通道数
   LYSO 晶条 SiPM 读出: 每侧 分前(2X0) 后(17X0) 共4套 LYSO
   每套 170cm^2, 需1.7k ch. 总共 7k通道数
4. **单通道预计计数率，**
   Z lumi Lmax = 115 x 1034/cm^2s, LumiCal Bhabha 探测器覆盖截面 100 nb
   Event rate = (246x10^{-33}) x (115 x 10^{34}) /sec = *115 kHz*
   Event rate / 25 ns bunch crossing = 0.003 events /b.c.
   lowest theta (束流管上/下) hot LYSO 3x3 mm^2 6-cell cluster
   event fraction = 0.12, **最热区每LYSO cell事例量 ➔ 0.00016 events/b.c.**

5. **信号特征：电荷？电流？电压？上升、下降时间，宽度？**
   硅条: PN 二级 25k 电子电荷, ADC 需要极快, 宽 50 ns 内, 在 25 ns B.C. 前后事例分辨开
   LYSO SiPM: ADC 需要极快, 宽 50 ns 内, 在 25 ns B.C. 前后事例分辨开, 12bit 100 GeV 线性能量测量
6. **信号传输方式（比如同轴电缆，PCB，接插件），阻抗特性。**
   前端PCB 缆线空间紧迫，可能放 ADC， serializer 接 10 Gbps 光纤读出
   不做 trigger, 接 FPGA 做事例筛选
7. **最小、最大信号（也就是动态范围）。**
   硅条 测 MIP 单点电离电荷
   LYSO SiPM 比照 ECAL 量测 300 MeV 到 100 GeV 电子
8. **对数字化的要求（LSB, 精度，线性度）。**
   LYSO SiPM 比照ECAL,
   需要监测 Pileup, 因此，每25 ns B.C. 做一次 Signal Level comparator 确认临接事例讯号是否被叠高
9. **探测器的工作温度和范围，如果电子学需要散热，可否和探测器温控在一起？有无对电子学的功耗限制和多少。**
   LumiCal 硅条及 SiPM 工作温度跟顶点探测器一致，约20 ºC
   LumiCal 每层硅条 4k 通道需 40颗读出chip 估计发热 10W 内，
   LYSO 每套 1.7k 通道也在 10W 内。 每Z侧 40W，地线接到束流管冷确面。

From detector to frontend electronics

- 汇总分类
- 有关信号特征
  - 电子、光子
- 信号处理需求
  - 位置测量
  - 幅度、电荷测量
  - 时间测量
  - 3D、4D、5D
- 通道规模
  - 和成本考虑

Common requirement for the backend

- 前端到后端接口
- 后端到DAQ接口
- 后端到slow control接口
- 电子学到机械接口（散热）
- 电子学整体接口（电源规划、时钟同步……）