Elec-TDAQ progress on CEPC Ref-TDR

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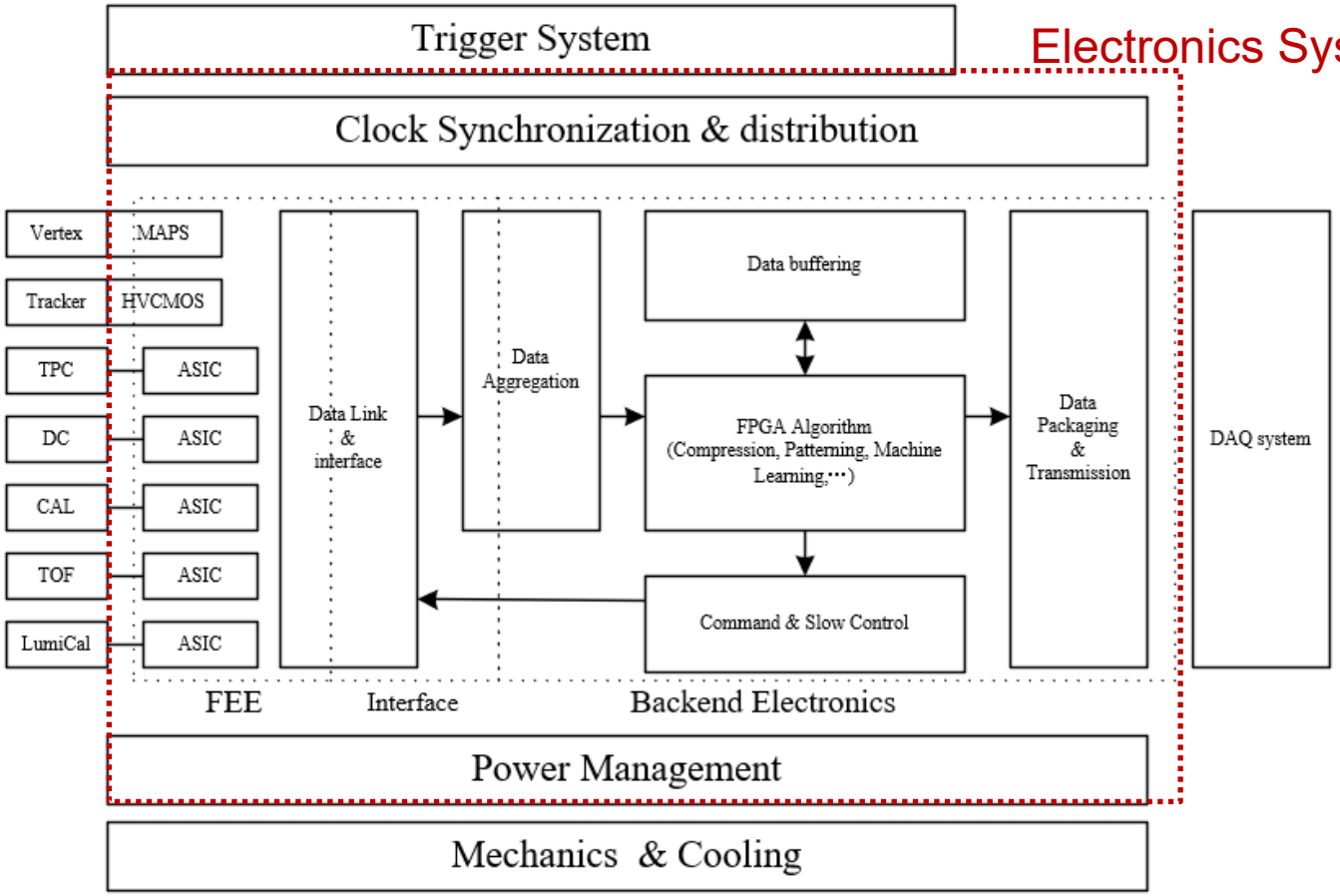
On behalf of the Elec-TDAQ system of the CEPC Ref-TDR

2024-03-25
CEPC Day

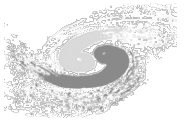
Elec-TDAQ overall framework



- **Two main recent targets:**

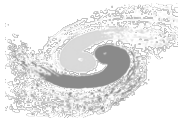
1. **To collect the detailed requirements from all sub-dets**
2. **To define the preliminary readout frame & strategy of Elec-TDAQ**

Status of the sub-det readout framework



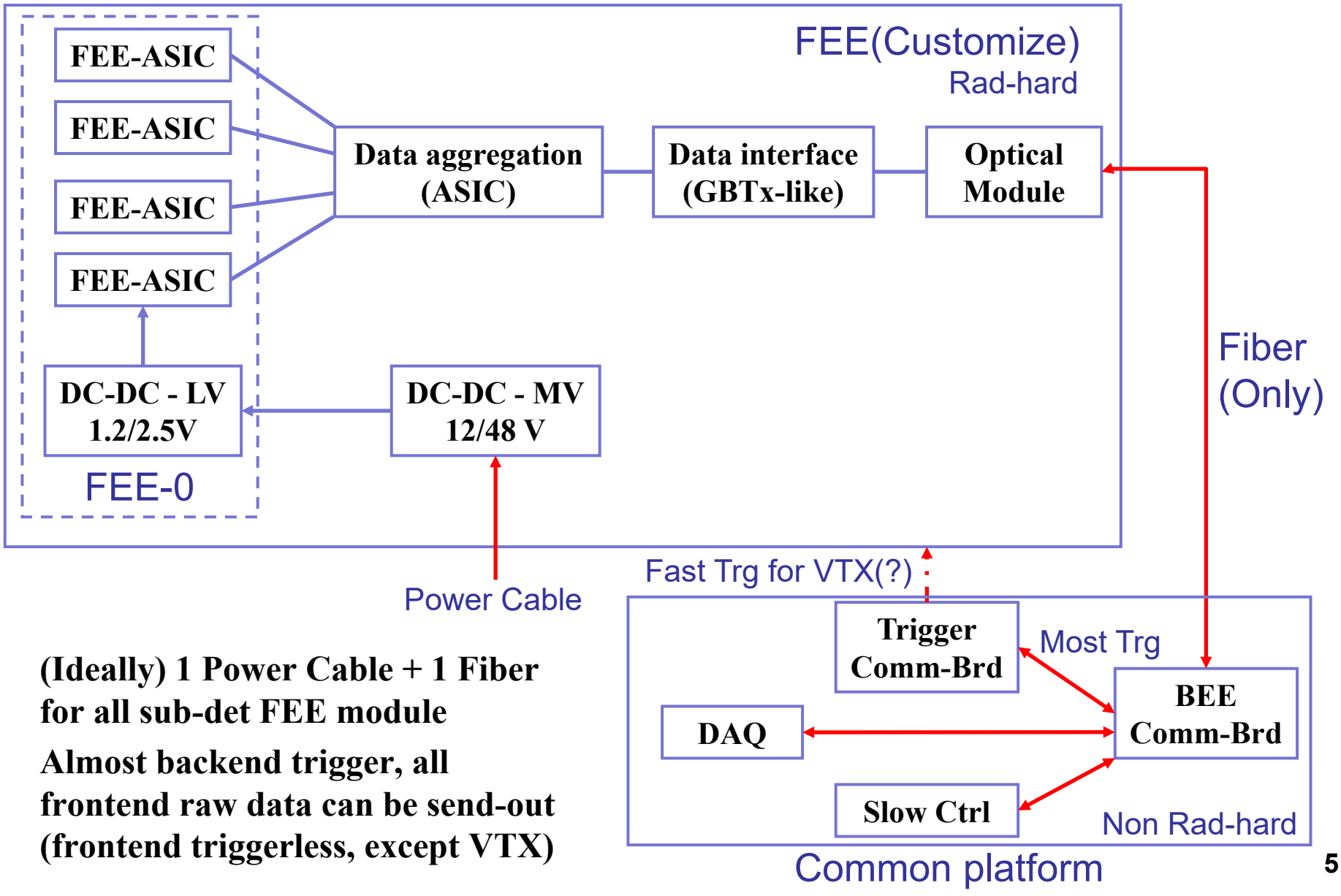
- **Most readout architecture of sub-dets can be compatible with the proposed "backend" Elec-TDAQ framework, with frontend "triggerless" data readout**
  - **BEE capability: 10 Gbps/link**
  - **Most data rate per module < 100 Mbps**
- **Preliminarily defined:**
  - **Vertex: prototype exists, fast trigger strategy needs further discussion**
  - **TPC & DC**
    - **TPC: initial R&D for pixel TPC**
    - **DC: R&D based on COTS exits**
  - **Si Out Tracker (SET)**
    - **Readout architecture compatible with LGAD-TOF & Si Strip**
    - **Si Strip relatively mature, TOF needs full R&D of ASIC & clocking**
  - **Muon**
    - **R&D exists, can be simplified according to CEPC's needs**

Status of the sub-det readout framework



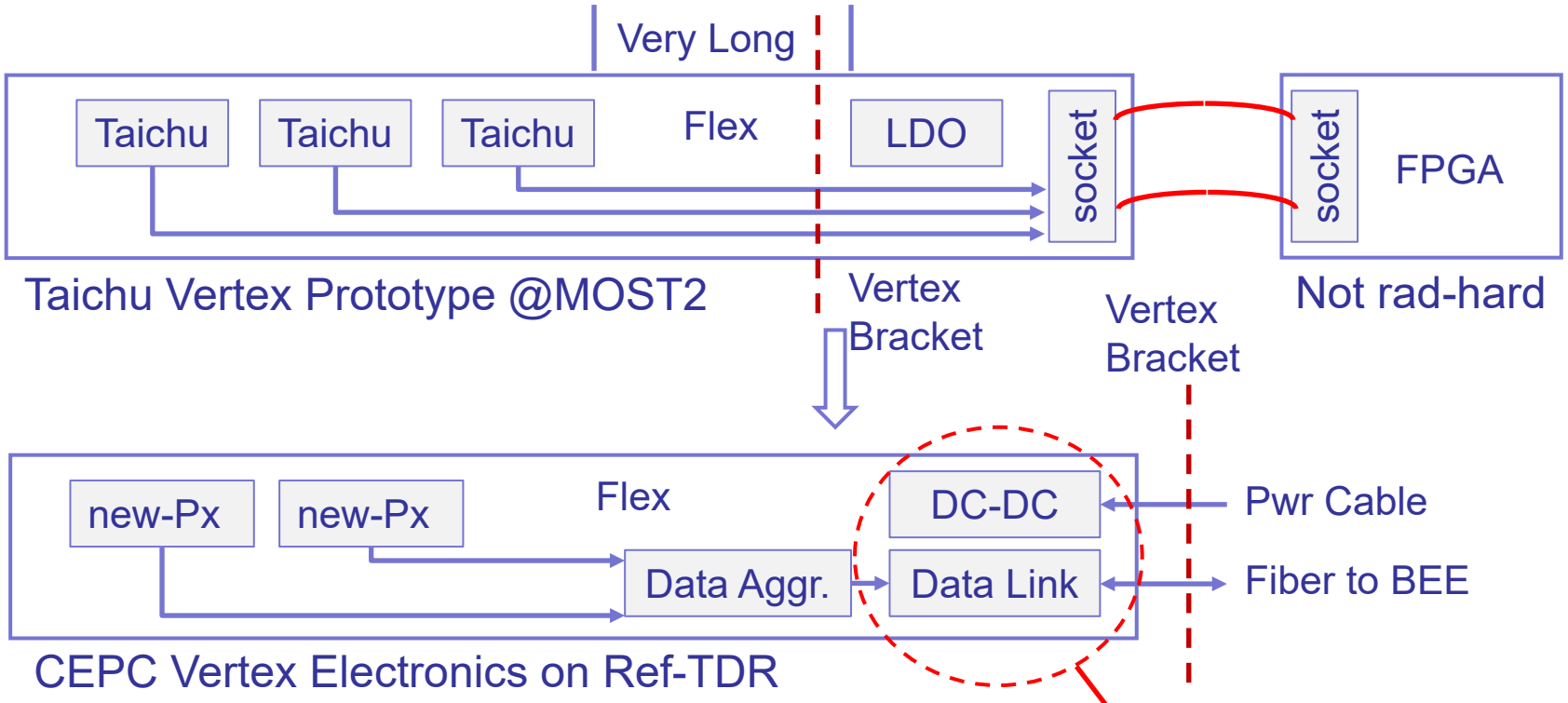
- **With proposal, needs further discussion**
  - **Si Inner Trk (or Si Pixel Trk)**
    - **Readout architecture can be compatible with SET, need further information of background rate for scheme finalization**
  - **ECAL & HCAL**
    - **Readout scheme proposed after discussion with sub-det, need to confirm with mechanics due to the space challenge**
  - **LumiCal**
    - **Preliminarily considered to be compatible with the SiPM & Pixel readout**

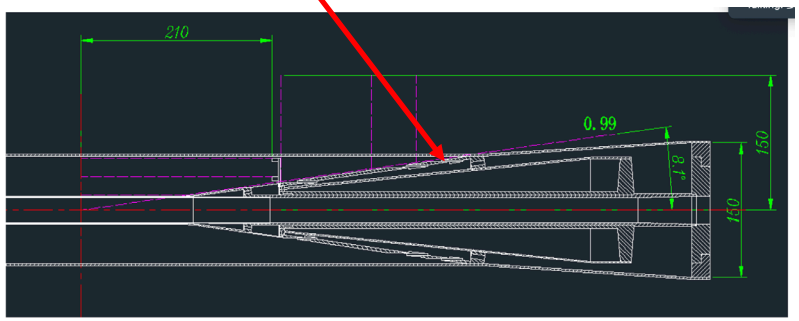
Proposal of general readout strategy of CEPC Elec



- **(Ideally) 1 Power Cable + 1 Fiber for all sub-det FEE module**
- **Almost backend trigger, all frontend raw data can be send-out (frontend triggerless, except VTX)**

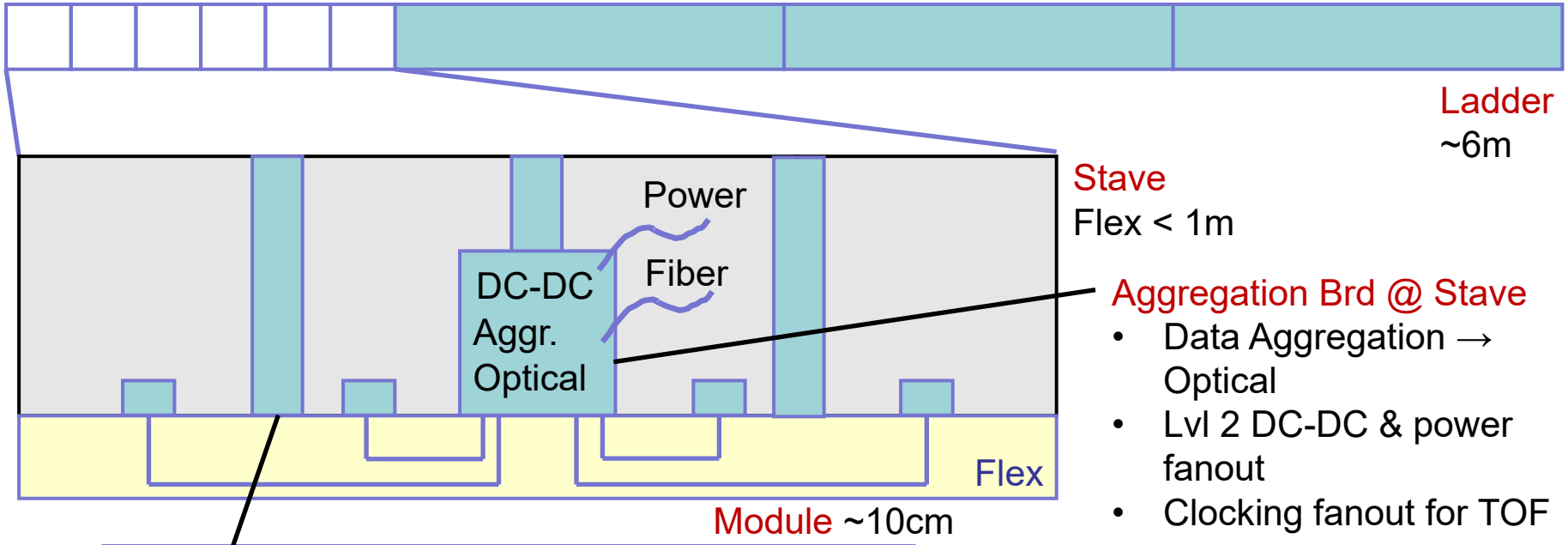
Elec scheme - Vertex





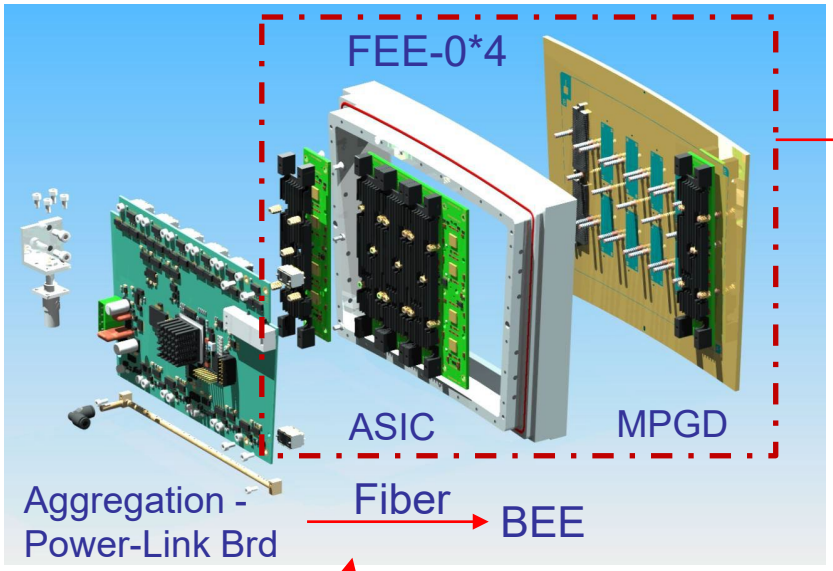
- **Q: height & area & power limit for power & optical module**
- **Q: (probably the only sub-det) need fast trigger to save power & data rate**
- **Q: proposed to design two sized chips for optimized layout of Inner / Med+Outer layer**

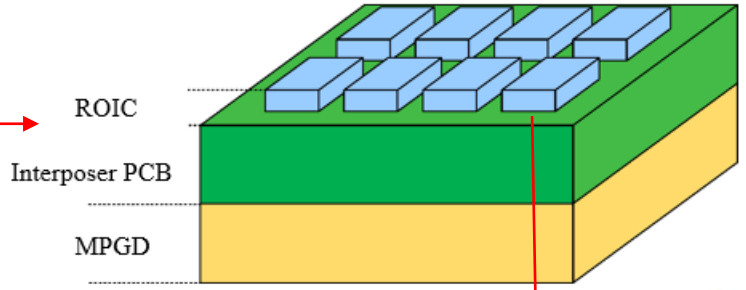
Elec scheme – Silicon Tracker



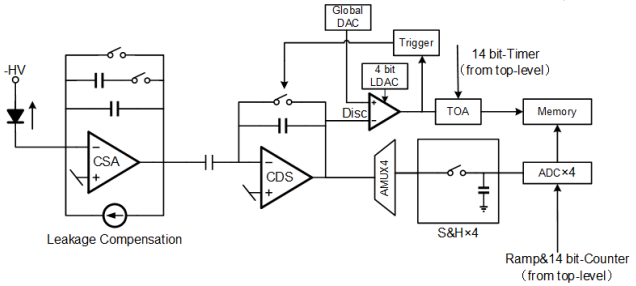
- **Si Pixel Tracker, TOF, Si Strip, can all be compatible with the readout framework**
- **1 Pwr + 1 Fiber for each stave**
  - **Data rate: Mostly < 1Mbps/stave**
  - **~ 30Mbps for SIT Innermost**
- **For high precision timing, clocking fanout needs careful thinking**

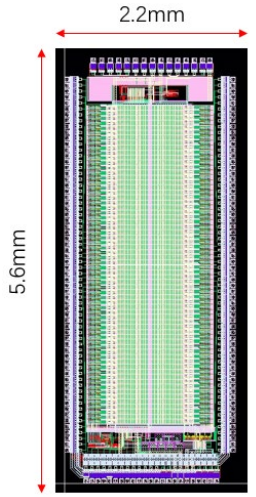
Preliminary readout scheme of Pixel TPC



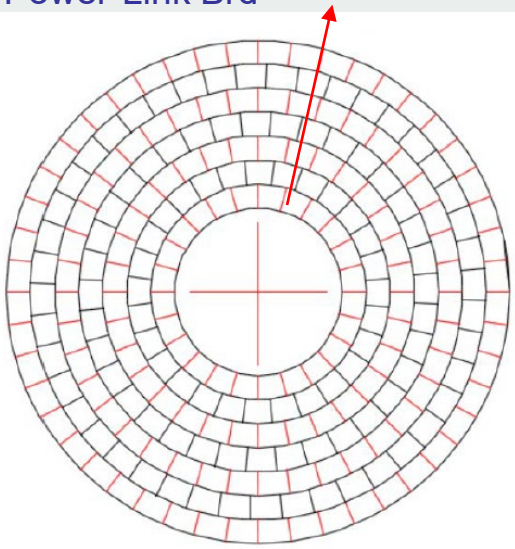


An integrated board with ASIC & MPGD, N(now 4) for a module
0.5mm*0.5mm / pixel





128 chn ASIC, Q+T measurement
142.8k pixel/module → 1115 chip/module→ 279 chip/FEE-0

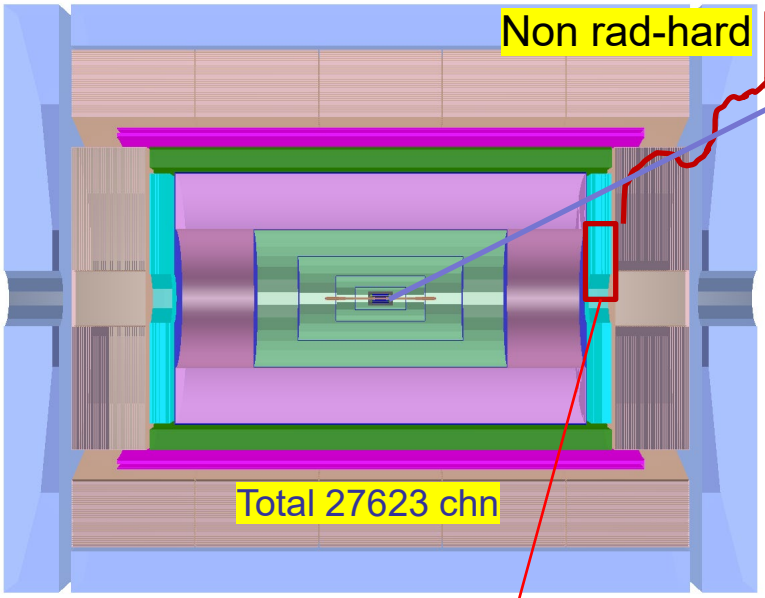


~258 Module/Endplate

Power:
Limit: <10 kW/endplate ~ 39.7 W/module ~10 W/FEE-0
35mW/ASIC ~ 280μW/chn

Data rate:
80 particles/BX, 12,000 hit/particle, 32(48)b/hit, @ 40M BX Z pole
1 Module: ~100 Mbps(@ innermost)

Preliminary readout scheme of Drift Chamber



cosθ

FEE Unit *32

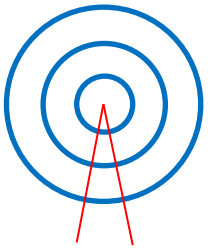
BEE

Detector

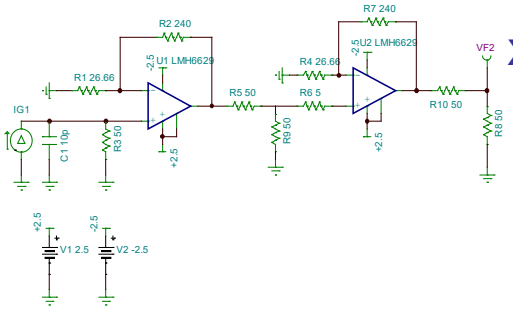
ADC
ADC
ADC
FPGA

Data Collector

Start
.....
Trigger

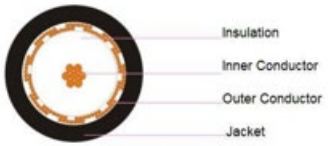


12 chn
Grp by sector



High Bandwidth Preamp
100mW/ch -> 2.7kW

x12



Analog signal on Cable
2.8mm per co-ax
12 signals + 1 Power
3dB attenuation @ 280MHz

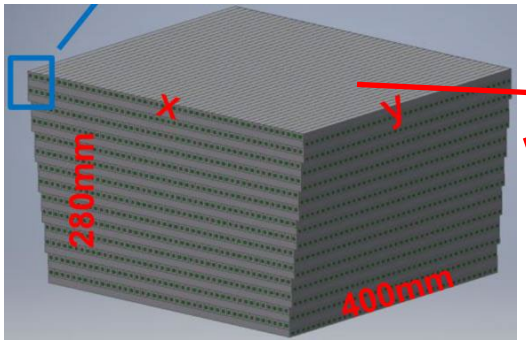
ADC
ADC
ADC
x12

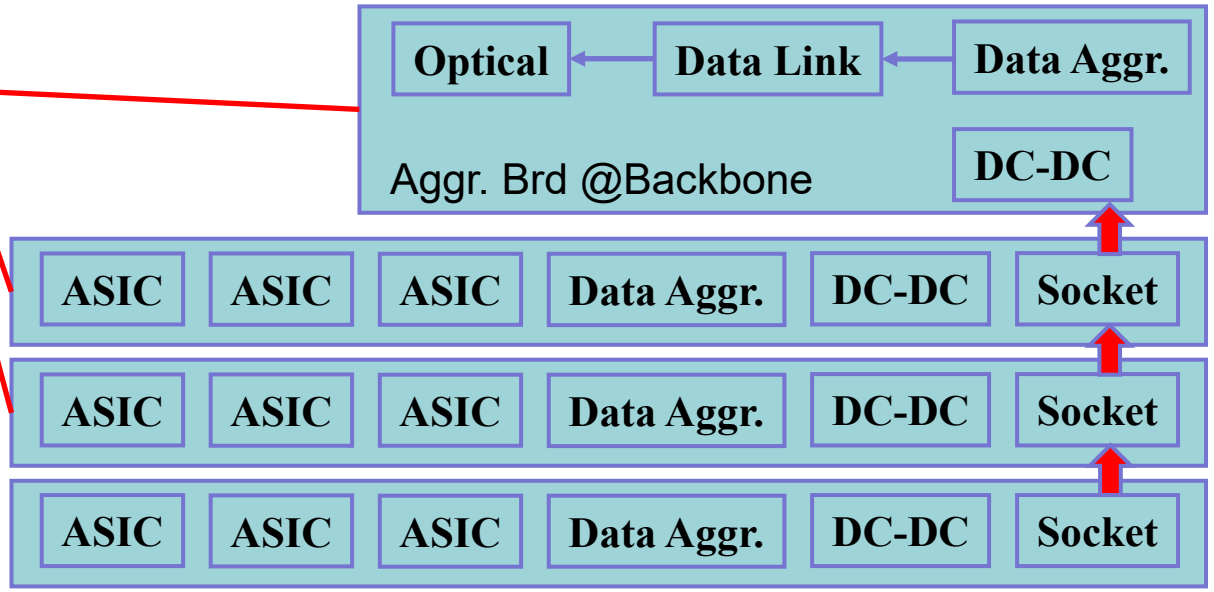
FPGA
RAM

Fiber
To BEE

ADC @1.3Gsps 12bit
RAM to average 12 chn in a sector
Read by wave envelope of 1.5 us with waveform-- compatible with calibration requirement (0.5Gbps/ 12chn)

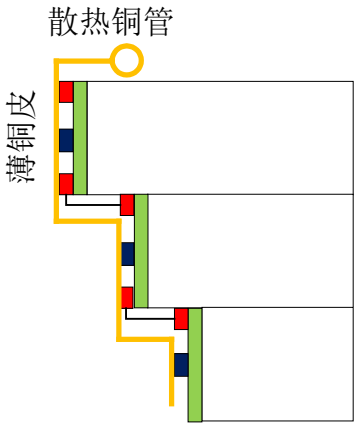
Elec scheme – ECAL



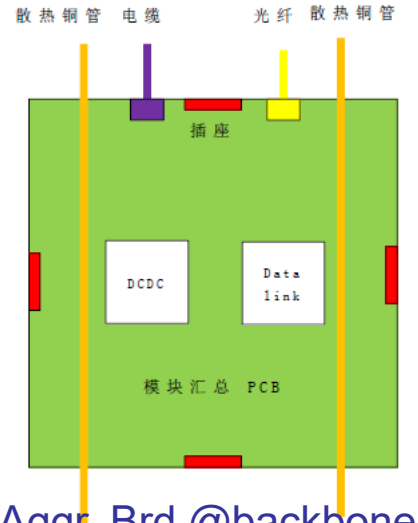


FEE Brd @Side

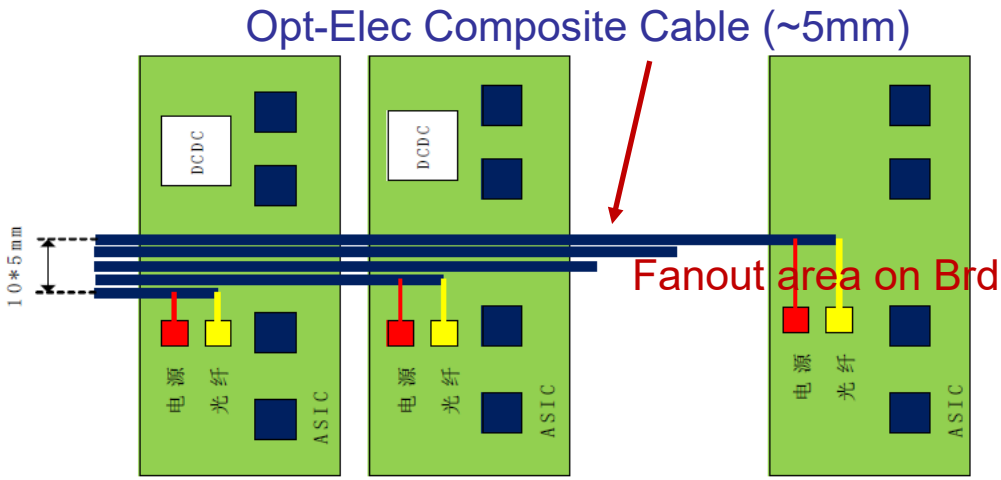
- **Q: limited room for fanout & DC-DC module**
  - ~ 5mm height
- **Q: limited heat dissipation capacity**
  - Proposed by Cu tube & sheet ?



FEE Brd @Side

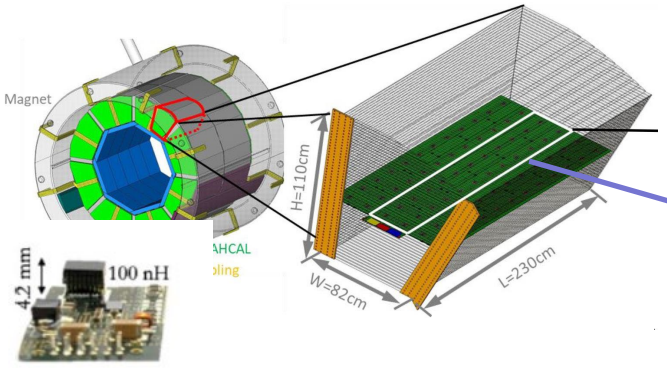


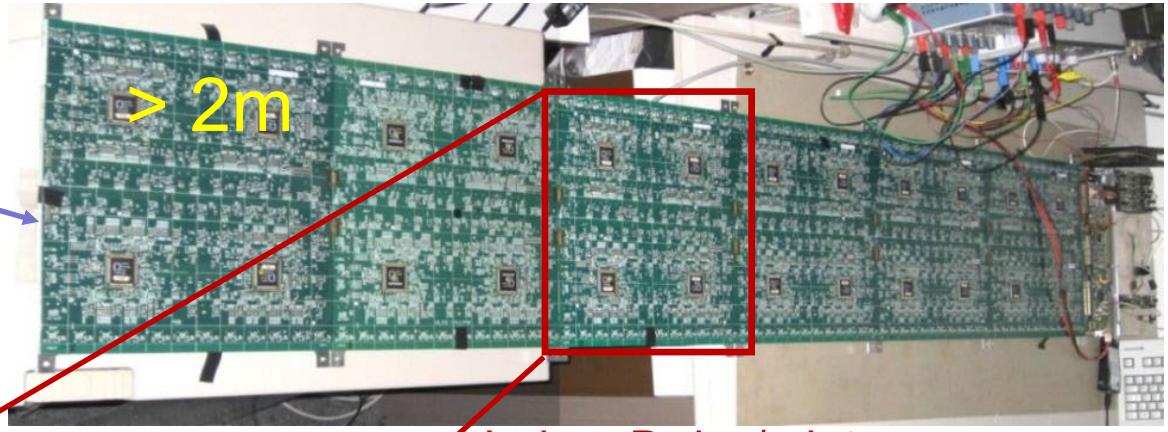
Aggr. Brd @backbone



Barrel fanout @half barrel

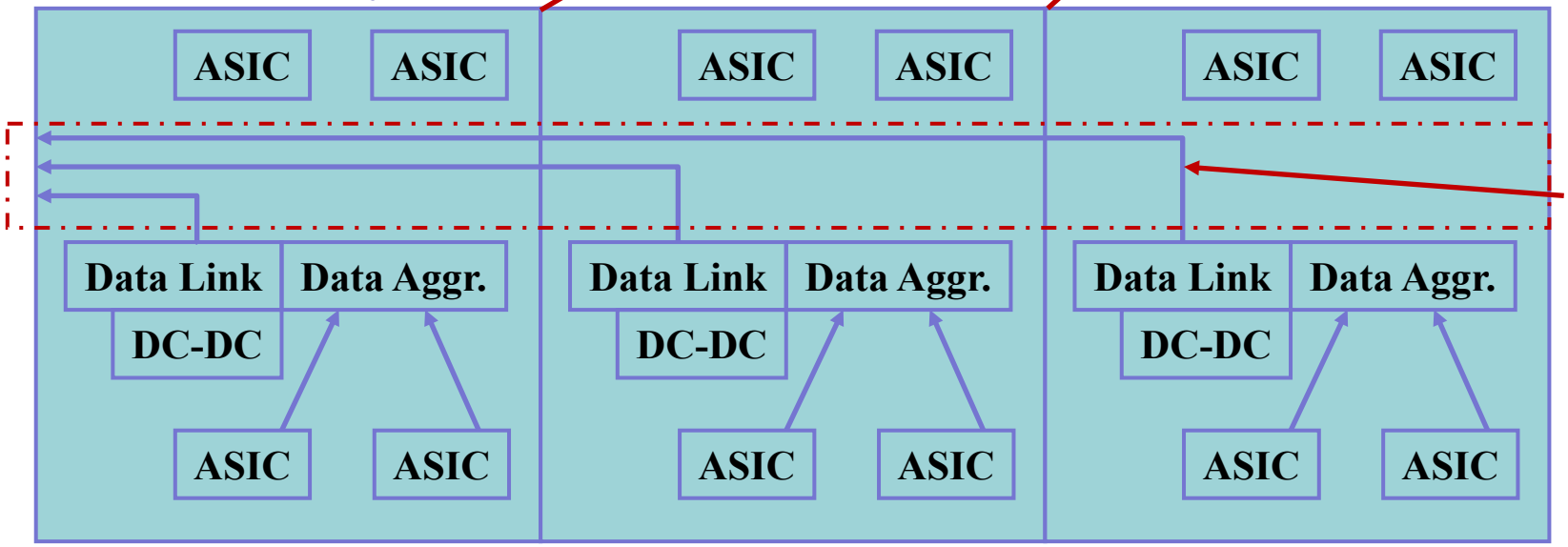
Elec scheme – HCAL





Glass+SiPM evenly distr. on the top side

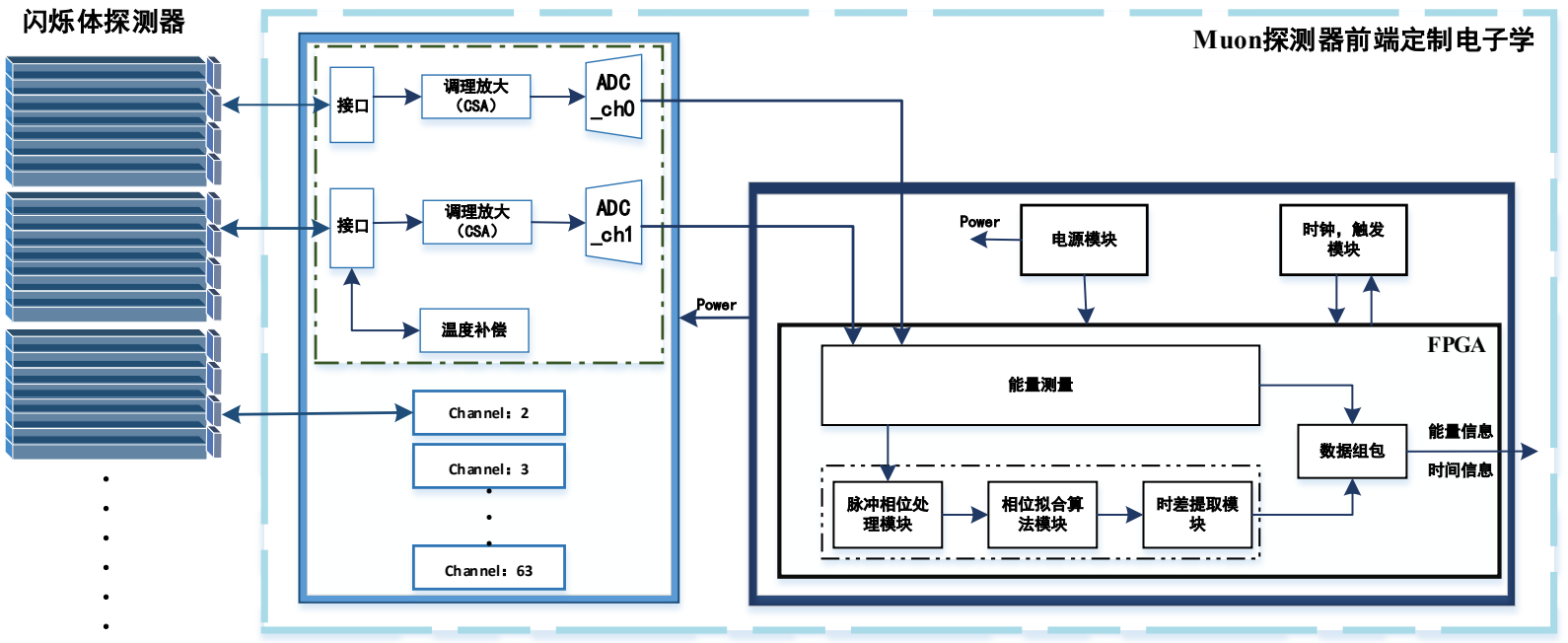
Indep. Brd w/o inter-conn.



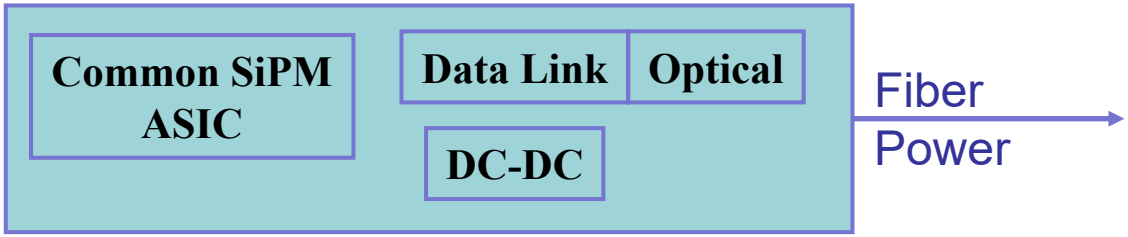
Fanout area by opt-elec composite cable

- **Q: high challenge on limited height: 6.7mm including PCB (height of power (ind) & optical & cable)**
- **Q: heat dissip. proposed to rely on the absorber (issue: the Elec is fully at backside)**

Elec scheme – Muon

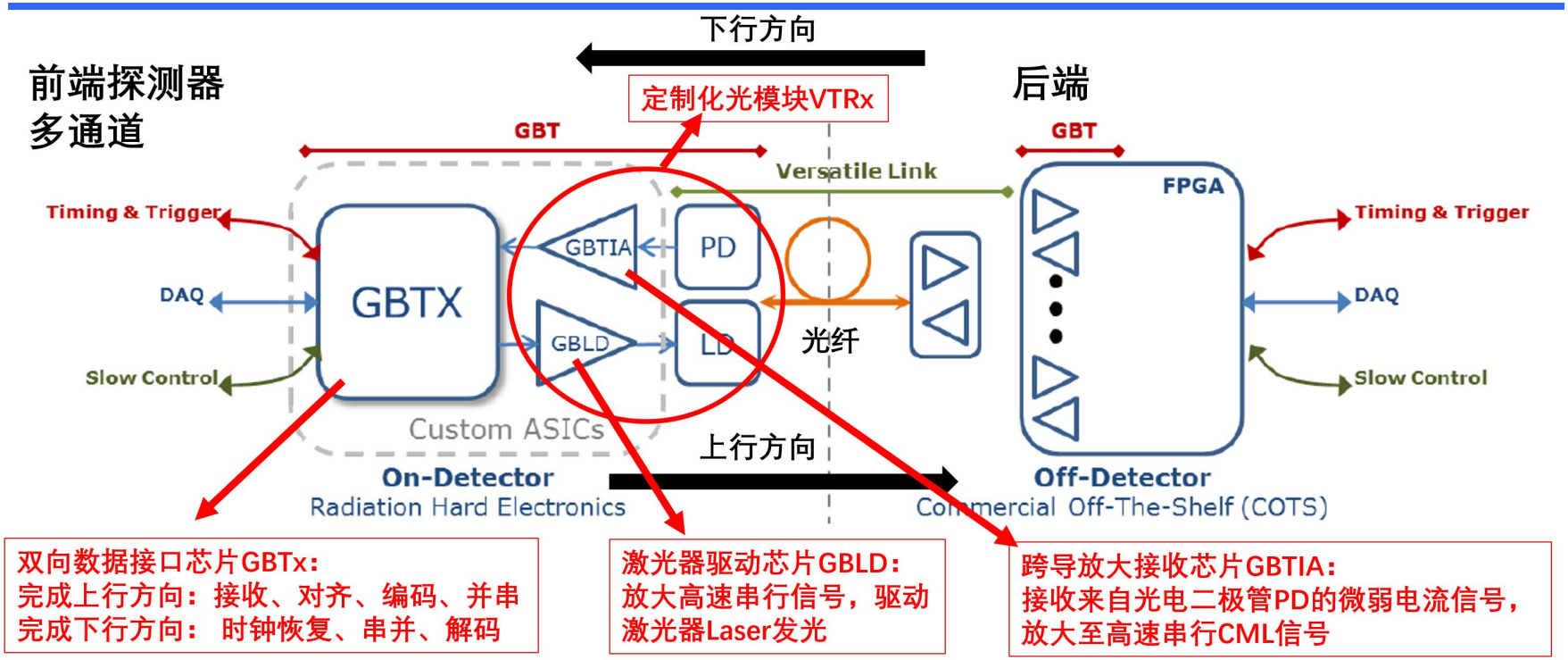


Muon Elec R&D



CEPC Muon FEE

Common framework on Data Link



CERN研发的GBT系列芯片等构建起双向光纤数据传输系统：

✓GBTx：双向数据接口芯片

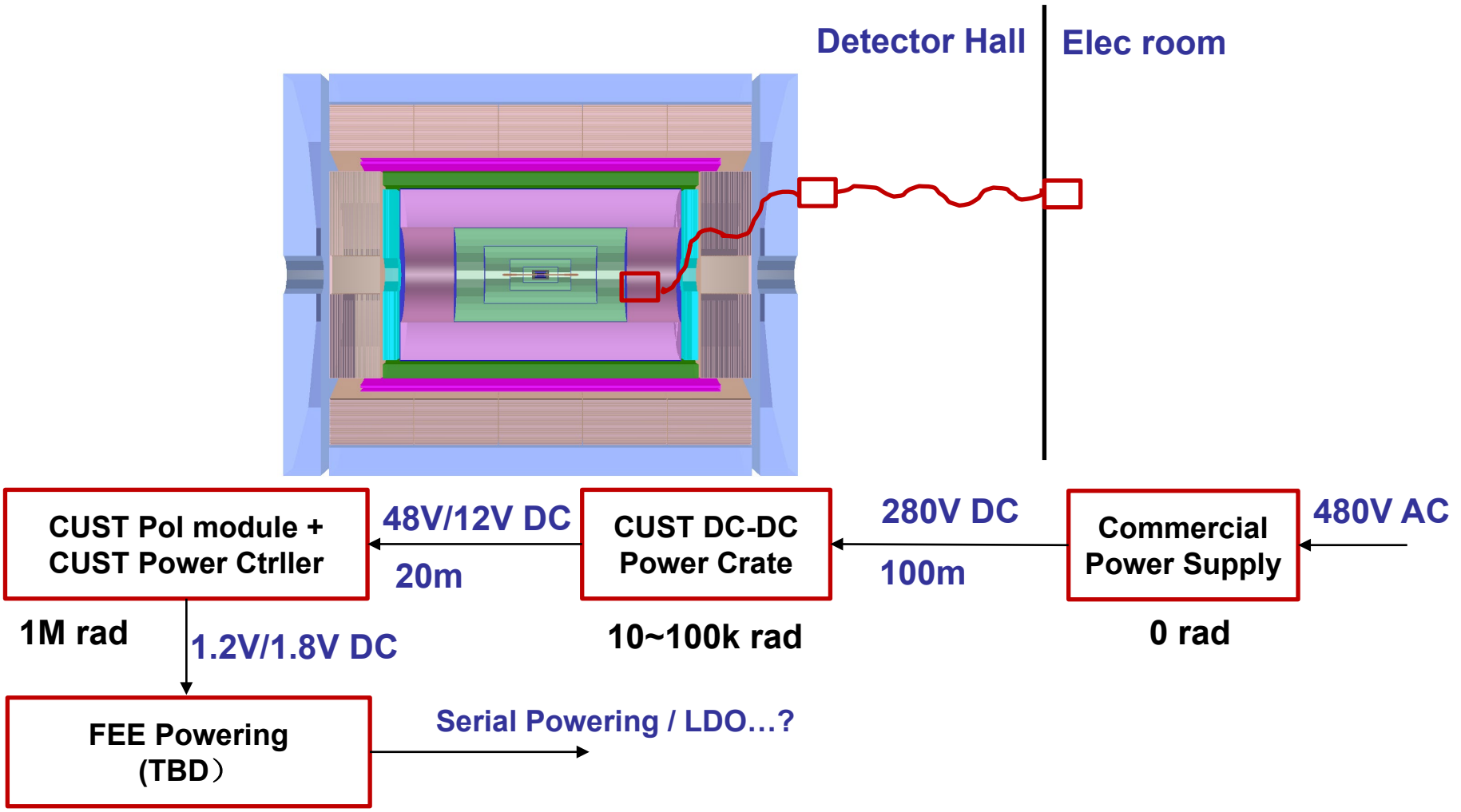
✓GBLD：激光器驱动芯片 （**LD: Laser Driver**）

✓GBTIA：跨导放大芯片 （**TIA: Transimpedance Amplifier**）

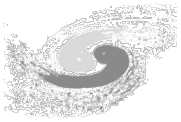
✓**VTRx光模块**

✓抗辐照 **400Mrad** 总剂量 （**CERN在Phase II升级中对于Link系统的要求**）

Common framework on Power

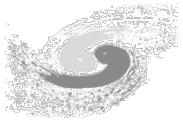


Summary on current framework



- **Detectors can almost still keep with "triggerless" feature**
  - **All FEE raw data go to BEE losslessly**
    - **Except for the (innermost) Vertex**
  - **Trigger will almost communicate only with BEE**
    - **"Backend trigger" based**
    - **Both hardware / software trigger still possible**
    - **Still needs special consideration on Vertex (how to generate Fast Trg)**
- **All FEE module based on a similar framework:**
  - **ASIC – Aggr. – Data Link – Fiber + DC-DC – Pwr Cable**
  - **Minimized the module interconnection design, maximize the common platform design for BEE + Trigger**
    - **A highly compact & scalable system**
  - **Based on a successful design of GBTx-like chip & rad-hard DC-DC module**
    - **Size & height of the optical & DC-DC modules still with high challenges**
    - **Backup plan if failed: back to the cable based architecture**

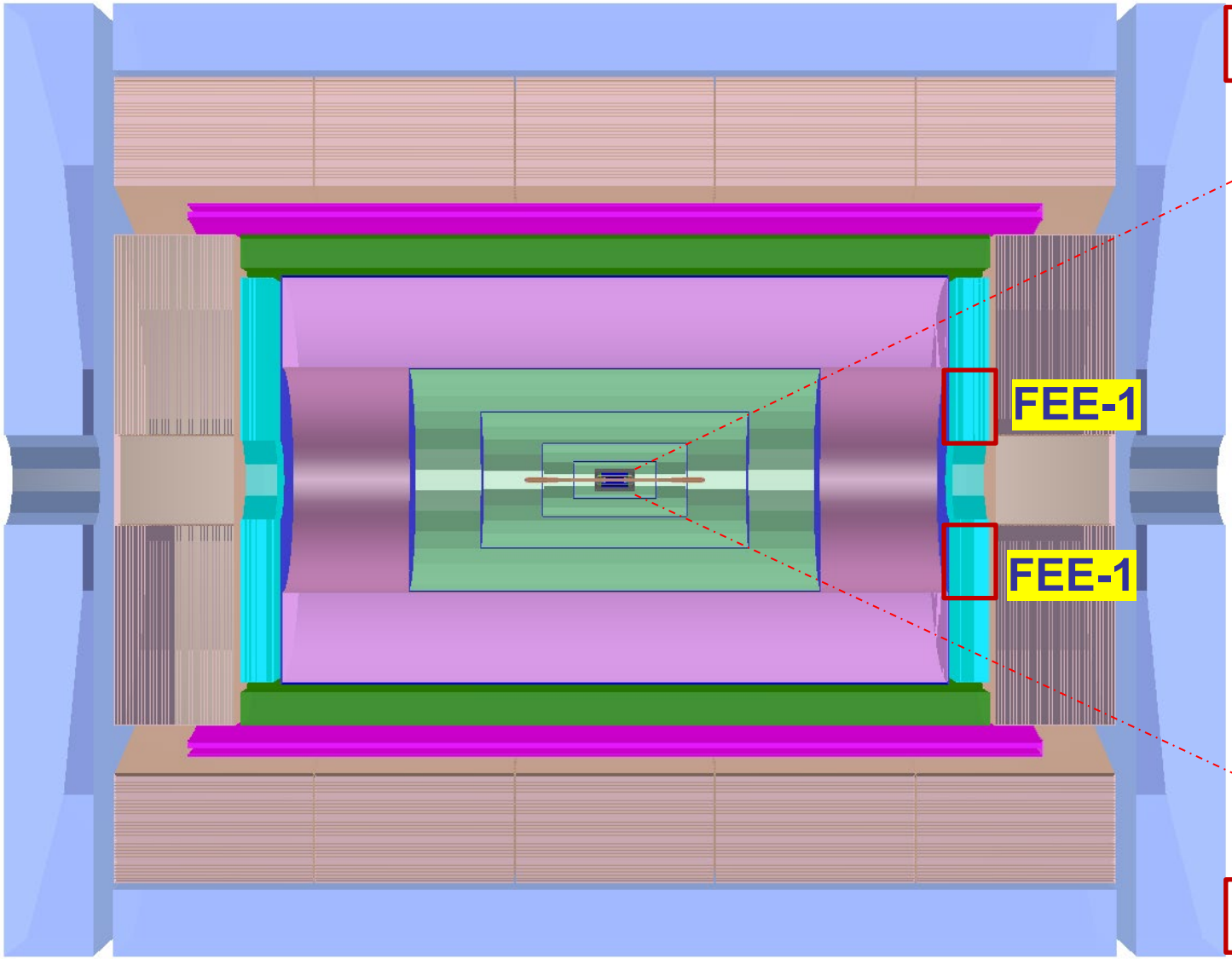
Recent Plan



- **Review the detector inputs on data rate**
  - **Conclude with limited data rate nodes for the Data Link**
- **Review the power and voltage requirements**
  - **Conclude with limited number of DC-DC design**
- **To define the Elec-Trigger framework**
- **To refine the FEE-ASIC design for each sub-det**

Backup

Elec scheme – TPC & DC



FEE-1:
A rad-hard (analog) FEE

FEE-2:
Non rad-hard FEE for data buffering, in low dose region (TPC may not need)