

Progress on CEPC TPC Readout Electronics

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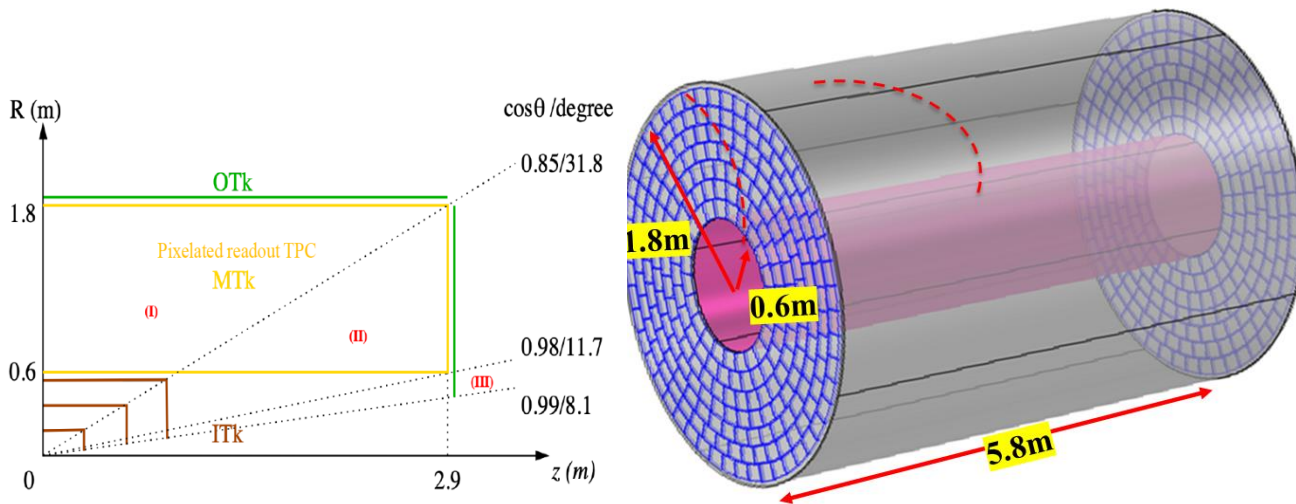
2024/05/15

Outlines

- Motivation
- Progress on pad readout electronics
- Progress on pixel readout electronics
- Summary

Motivation

- TPC can provide large-volume high-precision 3D track measurement with stringent material budget
- High granularity readout TPC can operate at Higgs run in **3.0T** and Tera-Z run in **2.0T**
 - CEPC CDR \rightarrow TDR: pad (1mm x 6mm) \rightarrow pixel (0.5mm x 0.5mm)



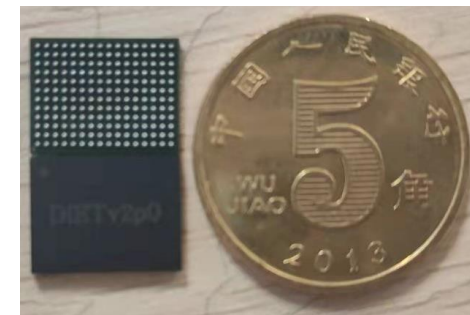
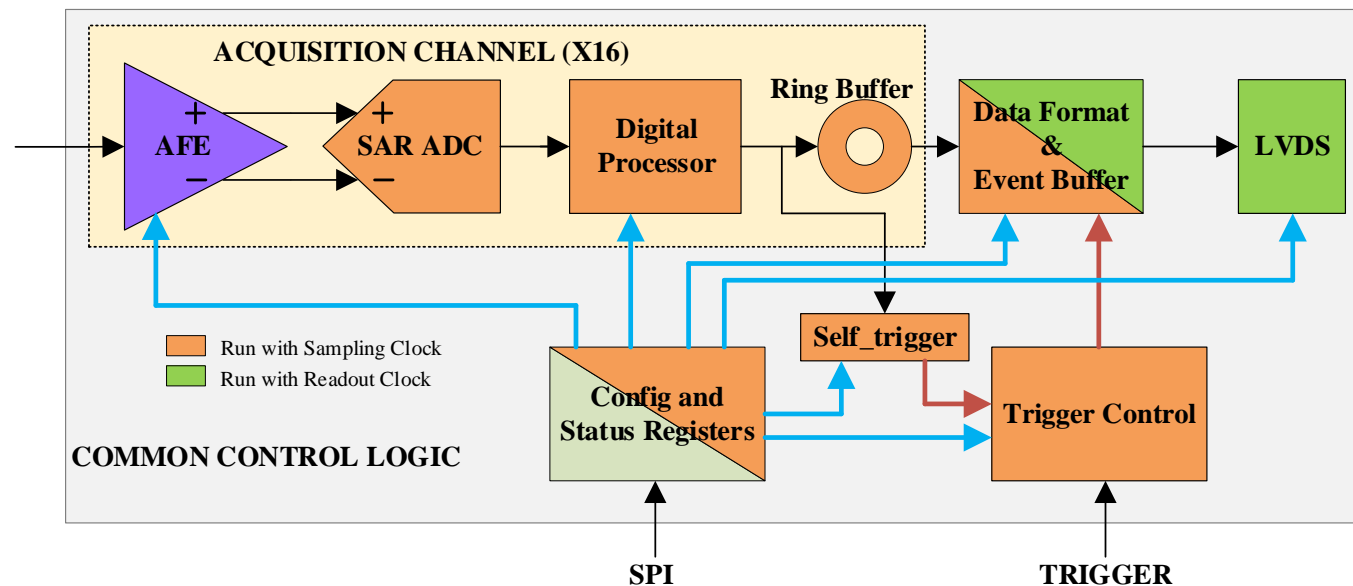
Update detector geometry in CEPC TDR

Parameters ⁴	Higgs run	Z pole run
B-field	3.0T	2.0T
Pad size (mm)/All channels	0.5mm × 0.5mm / 2 × 3 × 10⁷	0.5mm × 0.5mm / 2 × 3 × 10⁷
Material budget barrel	$\approx 0.012 X_0$	$\approx 0.012 X_0$
Material budget endcap	$< 0.20 X_0$	$< 0.20 X_0$
Points per track in rφ	2200 ↑	2200 ↑
σ_{point} in rφ	$\leq 100\mu\text{m}$ (full drift) ↑	$\leq 300\mu\text{m}$ (full drift) ↑
σ_{point} in rz	$\approx 0.1 - 0.5$ mm (for zero – full drift) ↑	$\approx 0.4 - 1.0$ mm (for zero – full drift) ↑
2-hit separation in rφ	$< 0.5\text{mm}$ ↑	$< 0.5\text{mm}$ ↑
K/π separation power @20GeV	$\leq 3\sigma$ ↑	$\leq 3\sigma$ ↑
Momentum resolution normalised:	$a = 1.82 \text{ e-}5$	$a = 3.32 \text{ e-}5$
$\sigma_{1/pT} = \sqrt{a^2 + (b/pT)^2}$	$b = 0.60 \text{ e-}3$	$b = 0.92 \text{ e-}3$

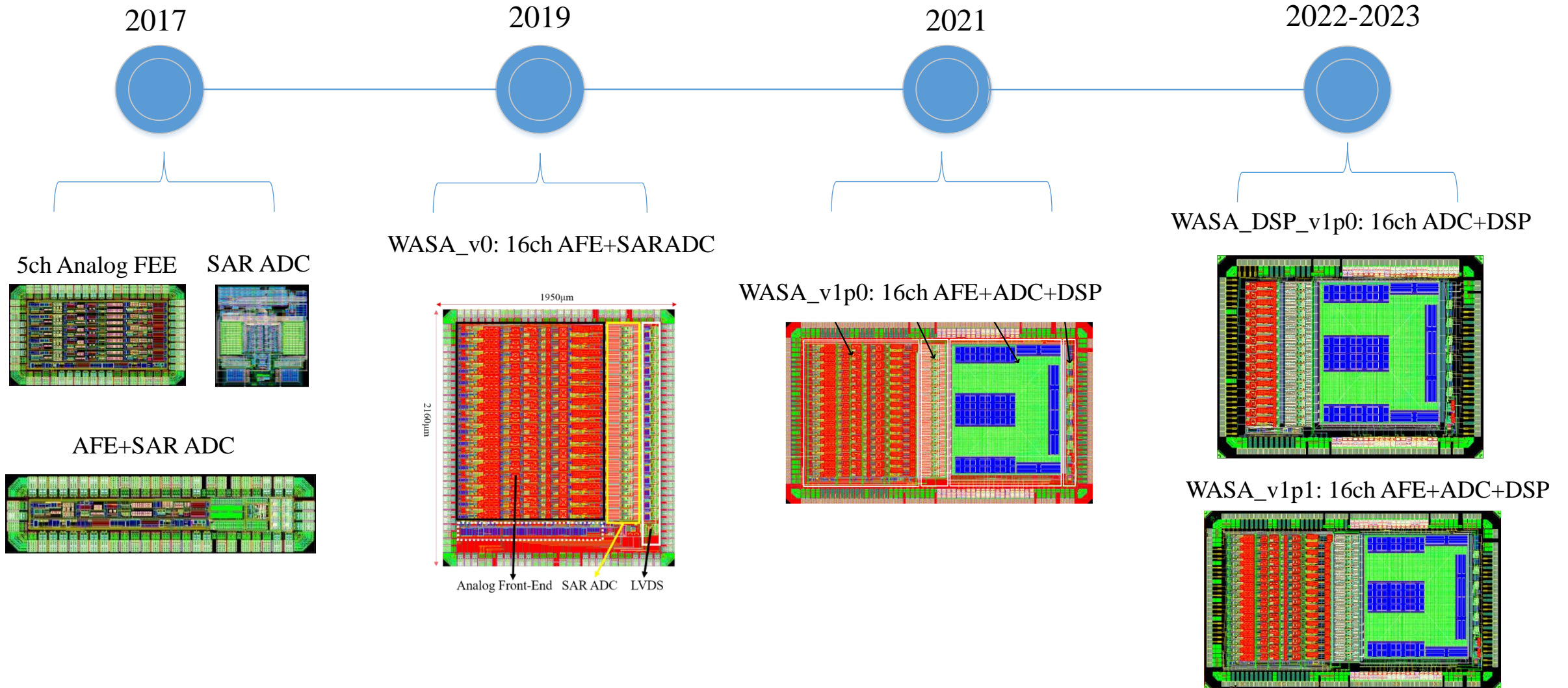
From Hui Rong's slides

Pad readout: WASA

- A **low power** and **highly integrated** FEE ASIC in 65 nm CMOS
 - Analog Front-End: Preamplifier + CR-RC shaper
 - SAR ADC: 10bit, up to 100MSPS
 - DSP: baseline correction and digital trapezoid filter
 - Trigger logics and data buffer



Pad readout: WASA



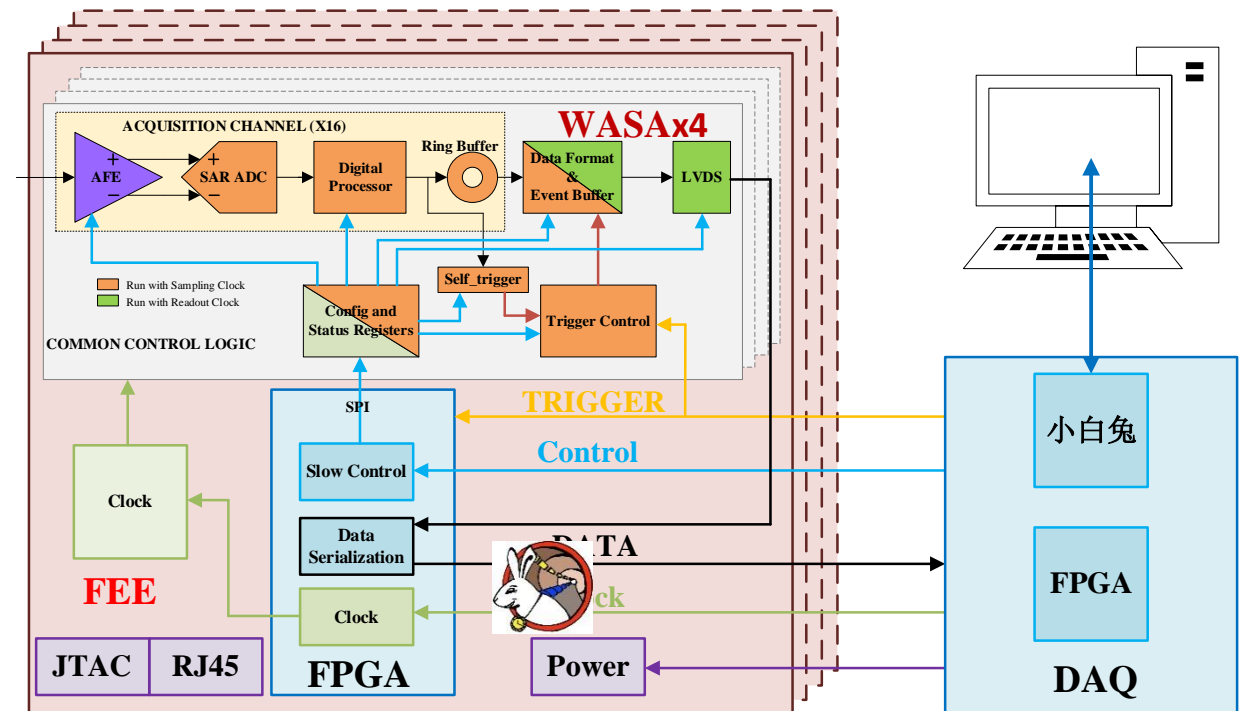
Performance of the WASA chip

- Compare to current TPC FEE ASICs

	PASA+ALTRO	Super-ALTRO	SAMPA	WASA_v1
TPC	ALICE	ILC	ALICE upgrade	CEPC
Pad Size	4x7.5 mm ²	1x6 mm ²	4x7.5 mm ²	1x6 mm ²
No. of Channels	5.7 × 10 ⁵	1-2 × 10 ⁶	5.7 × 10 ⁵	2 x × 10 ⁶
Readout Detector	MWPC	GEM/MicroMegas	GEM	GEM/MicroMegas
Gain	12 mV/fC	12-27 mV/fC	20/30 mV/fC	10-40 mV/fC
Shaper	CR-(RC) ⁴	CR-(RC) ⁴	CR-(RC) ⁴	CR-RC
Peaking time	200 ns	30-120 ns	80/160 ns	160-400 ns
ENC	370+14.6 e/pF	520 e	246+36 e/pF	569+14.8 e/pF
Waveform Sampler	Pipeline ADC	Pipeline ADC	SAR ADC	SAR ADC
Sampling Rate	10 MHz	40 MHz	10 MHz	10-100 MHz
Sampling Resolution	10 bit	10 bit	10 bit	10 bit
Power: AFE	11.7 mW/ch	10.3 mW/ch	9 mW/ch	1.4 mW/ch
Power: ADC	12.5 mW/ch	33 mW/ch	1.5 mW/ch	0.8 mW/ch@40 MHz
Power: Digital Logics	7.5 mW/ch	4.0 mW/ch	6.5 mW/ch	2.7 mW/ch@40 MHz
Total Power	31.7 mW/ch@10MHz	47.3 mW/ch@40 MHz	17 mW/ch@10 MHz	4.9 mW/ch@40 MHz
CMOS Process	250 nm	130 nm	130 nm	65 nm

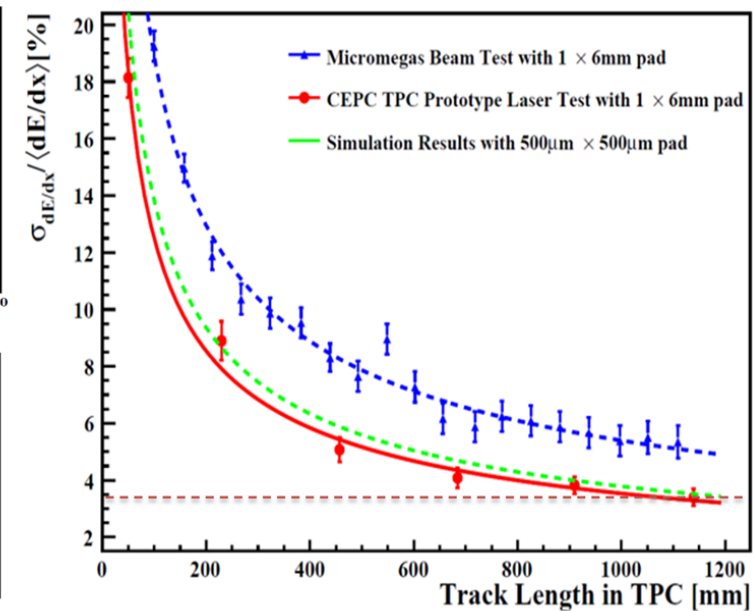
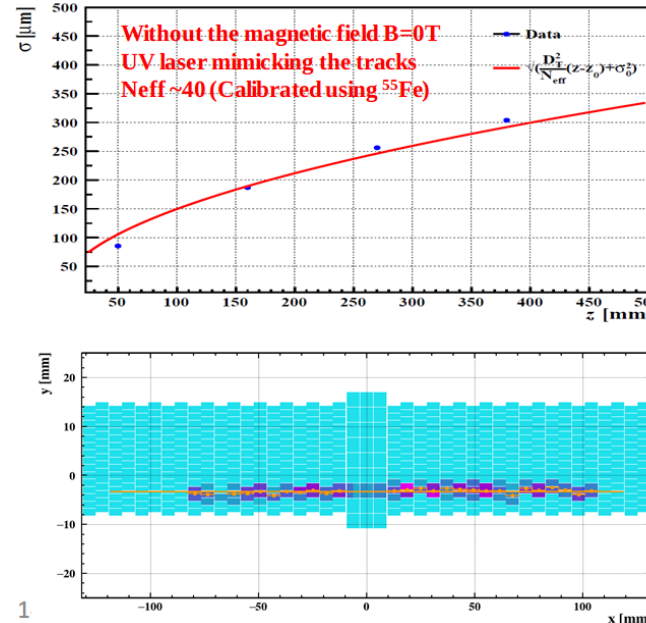
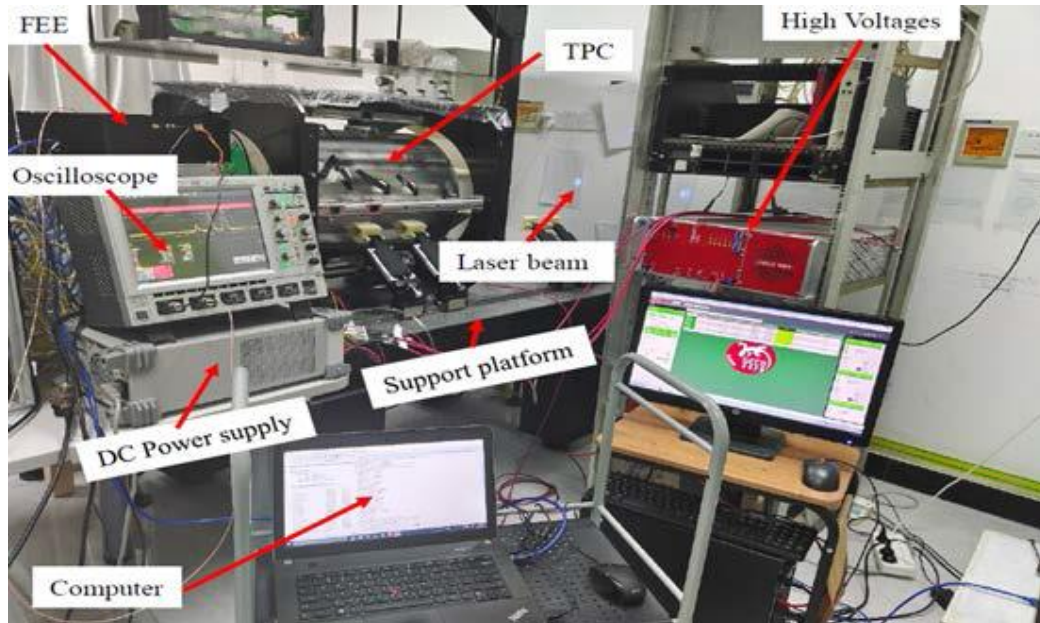
Scalable TPC readout electronics

- FEE based on WASA chips
- DAQ based on white rabbit
- Looking for other applications:
 - TPC for reactor neutrino
 - Fission TPC
 - Neutron imaging



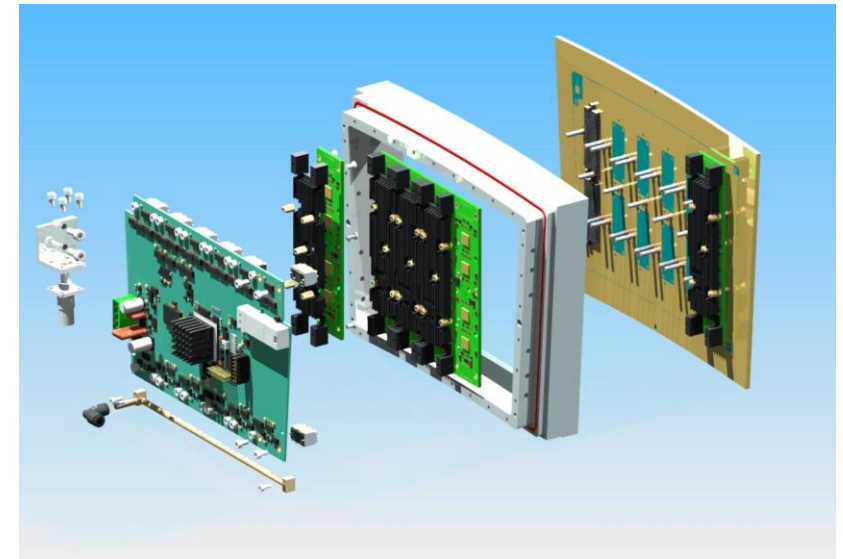
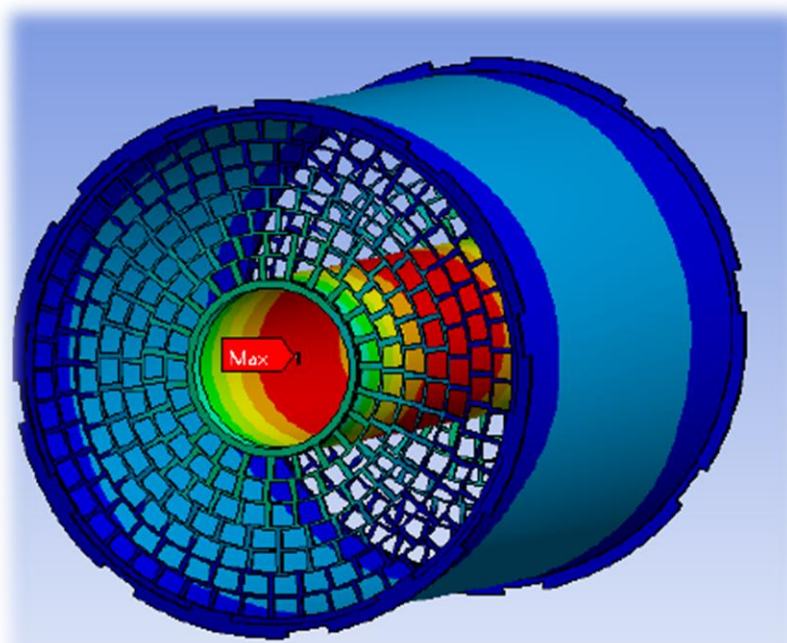
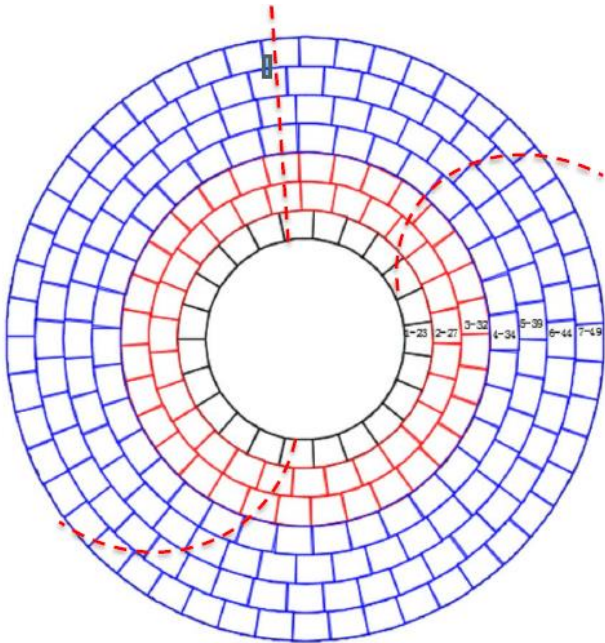
Application in TPC prototype

- Achievement by far from TPC module and prototype
 - Spatial resolution of $\sigma_{r\phi} \leq 100\mu\text{m}$ by TPC prototype
 - dE/dx for PID: $< 3.6\%$ (as expected for CEPC baseline detector concept)



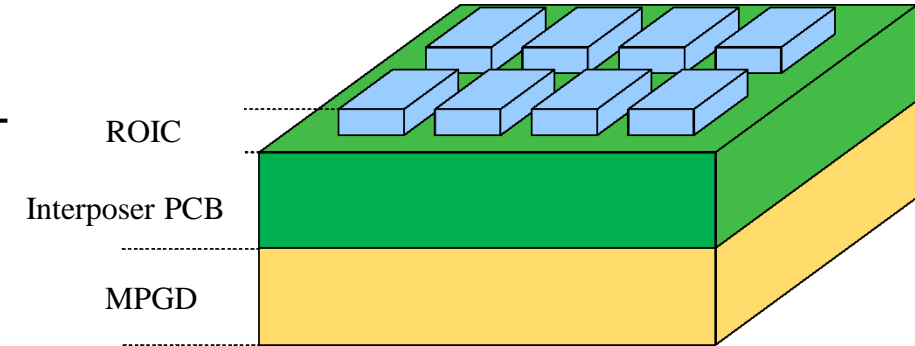
Pixel Readout: Overview

- End-plate: inner radius = 0.6 m, outer radius = 1.8 m
- Pixel size : 0.5mm x 0.5mm \rightarrow 3×10^7 ch. per endplate
- Divided to 248 modules/endplate in 21cm x 17cm



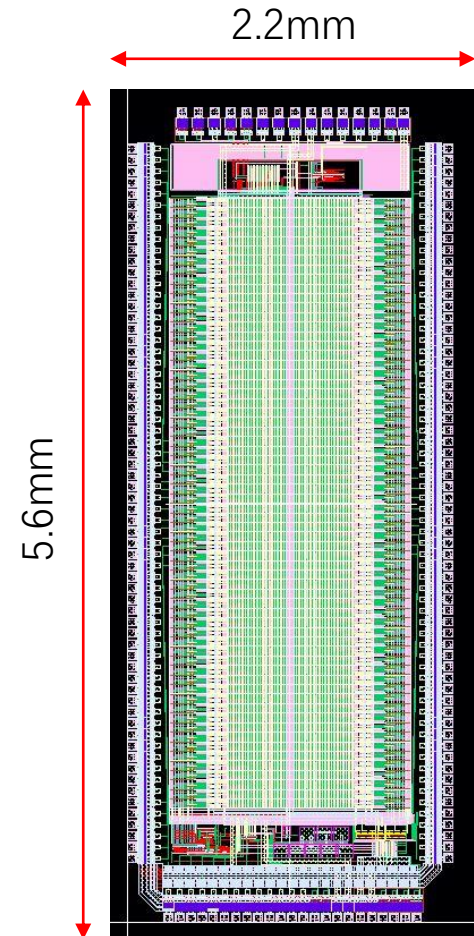
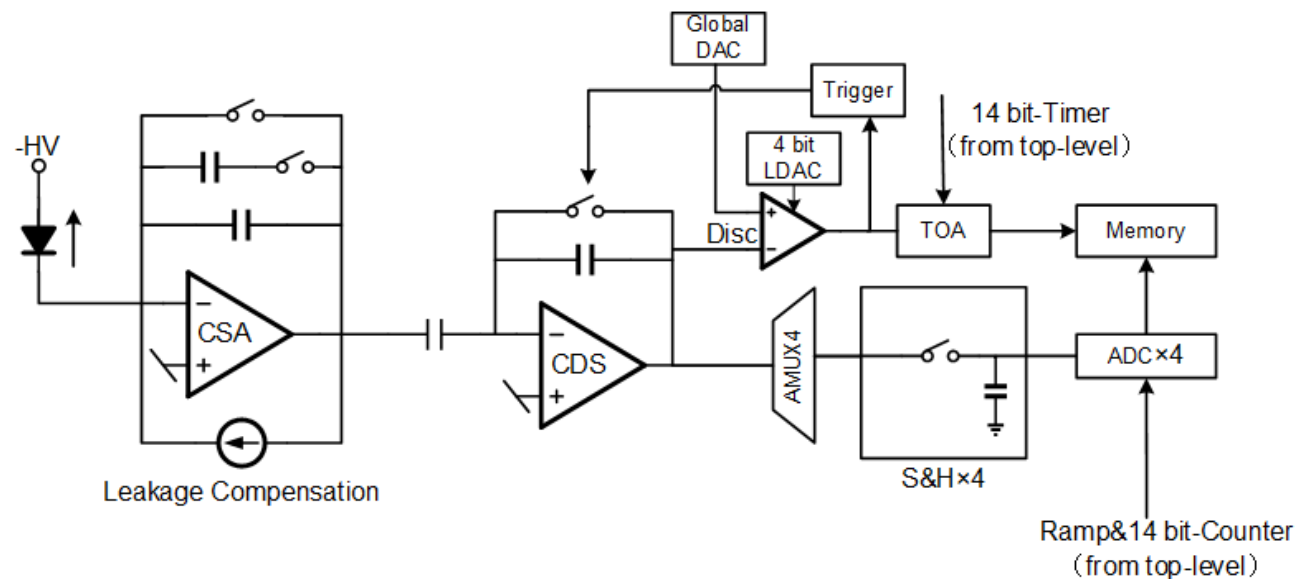
Pixel Readout: Scheme design

- Multi-ROIC chips + Interposer PCB as RDL
- High metal coverage, 4-side buttable
- Low power Energy/Timing measurement ASIC
 - ~100 e noise
 - 5 ns drift time resolution
 - 100 mW/cm² (250uW/ch) ~ 35.7 W/module ~ 6 kW/endplate



Pixel Readout: TEPIX ROIC

- Charge Sensitive Preamplifier(CSA)
- CDS amplifier provides additional gain and noise shaping
- 14-bit Wilkinson type ADC each pixel
- Timing discriminator with 14-bit TOA (Time of Arrival) information

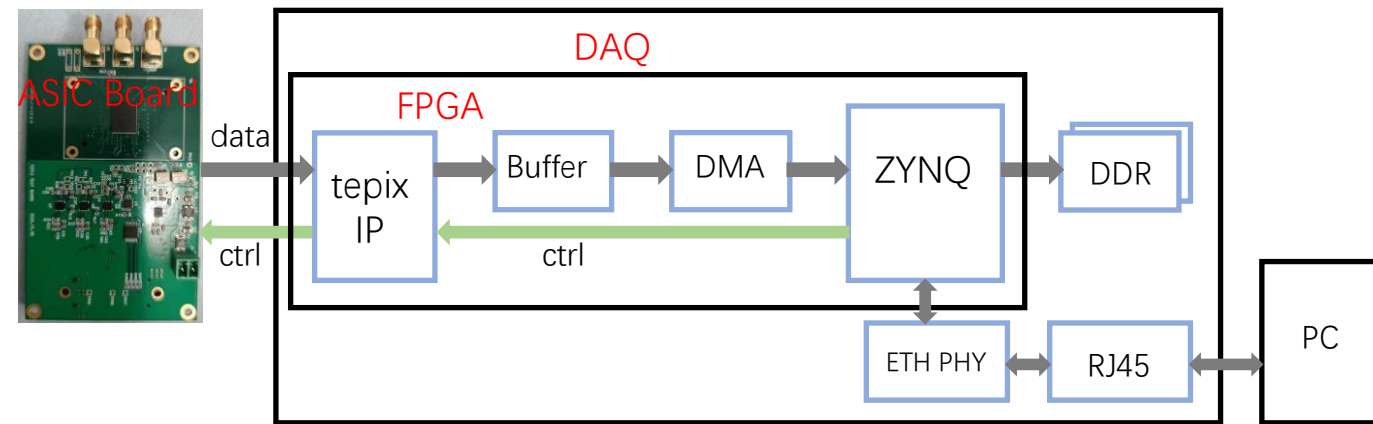


Pixel Readout: TEPIX ROIC

- Test setup



Test system for TEPIX

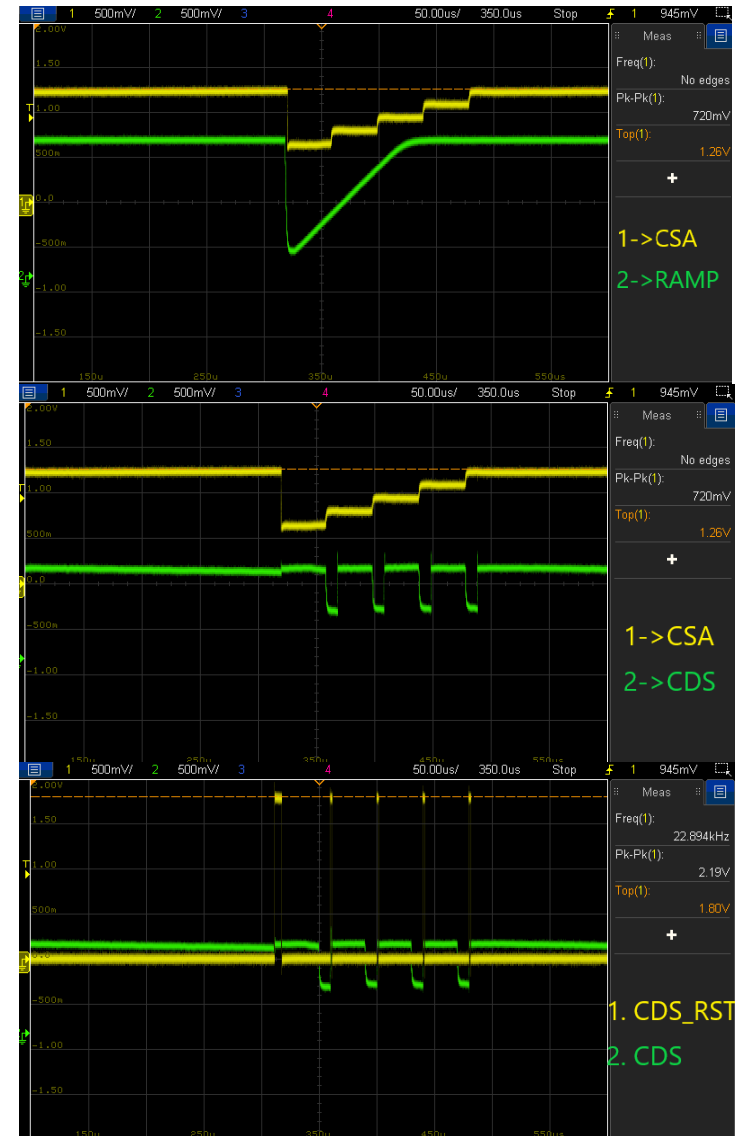


TEPIX test firmware

Pixel Readout: TEPIX ROIC

- Test results
 - Power consumption: 360 $\mu\text{W}/\text{ch}$
 - Final goal: $\sim 100\text{mW}/\text{cm}^2$

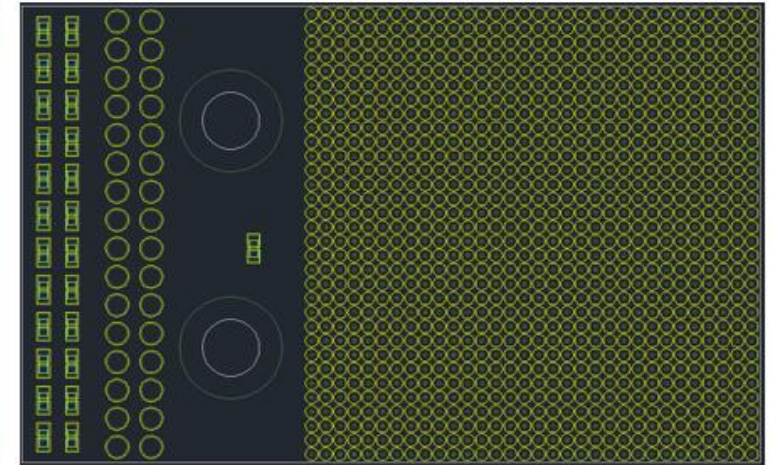
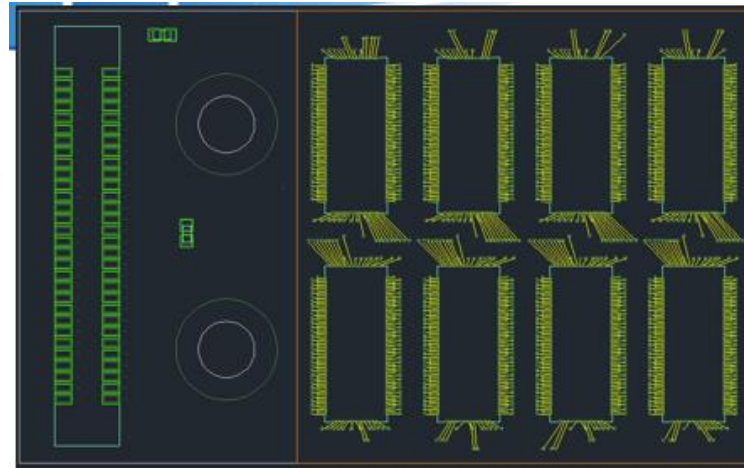
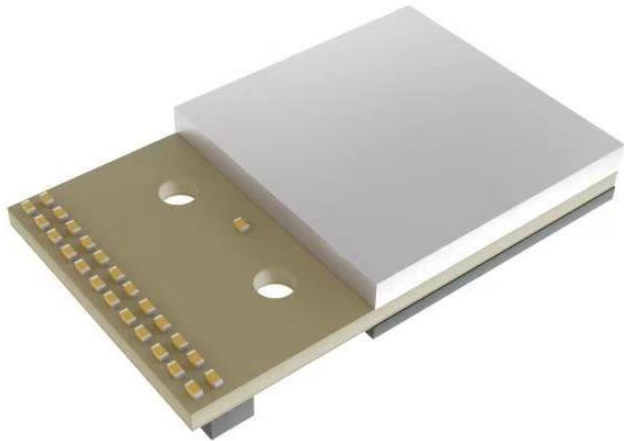
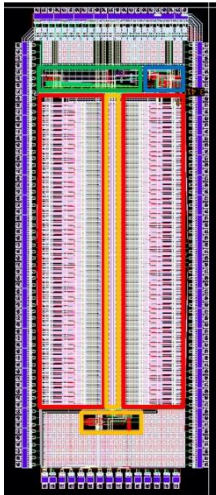
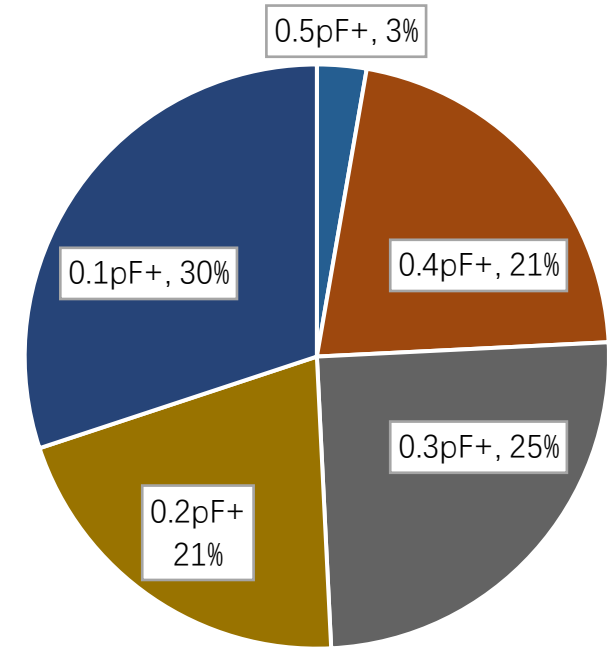
Power	Voltage (V)	Power (mW)
AVD	1.774	28
SVD	1.79	0
VDD	1.785	18
Total		46



RAMP、CSA、CDS waveforms

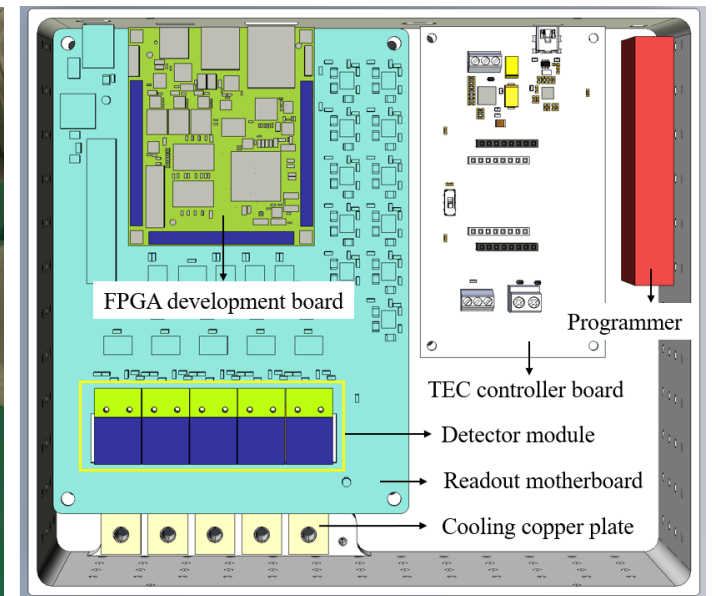
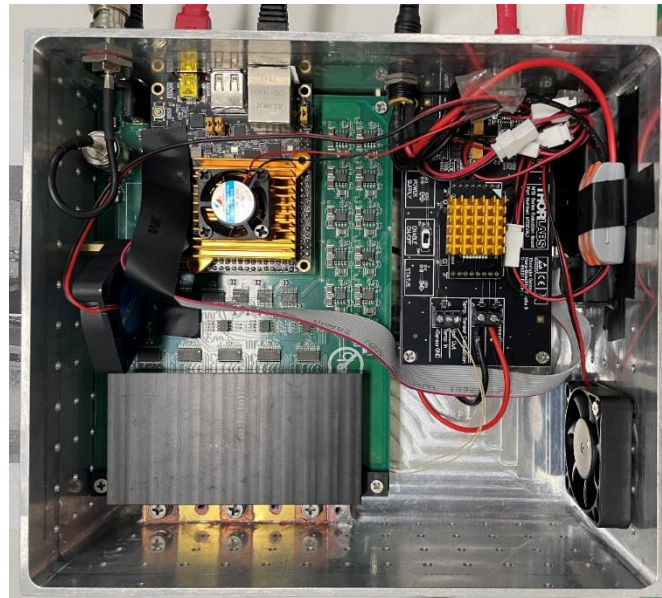
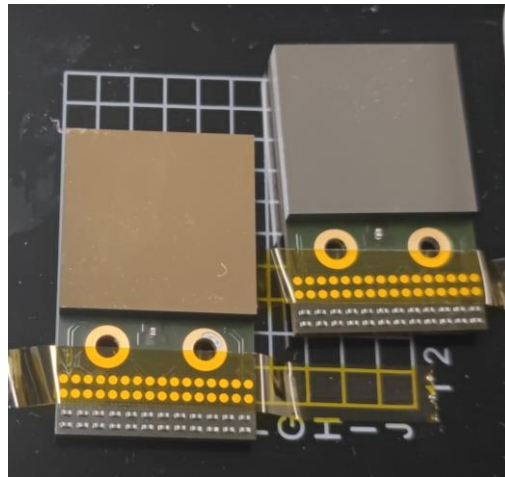
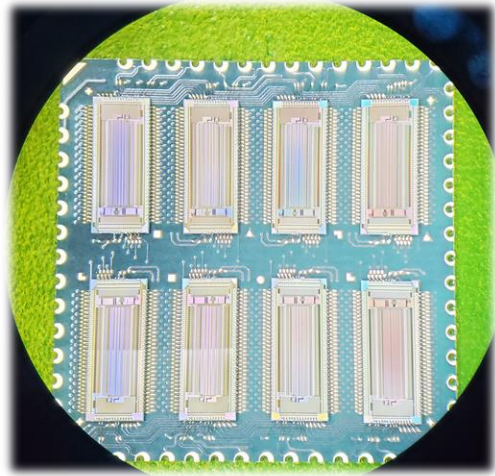
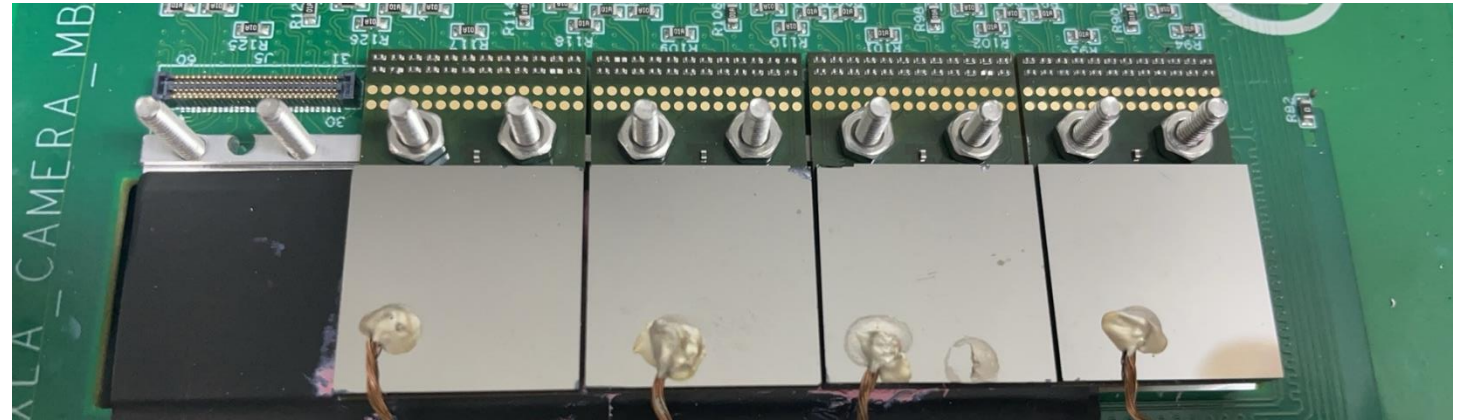
Pixel Readout: RDL module

- X-ray photon counting detector module
 - 128 ch photon counting ROIC, similar to TEPIX
 - 8 chips in the same RDL module
 - Parasitic capacitance optimized



Pixel Readout: RDL module

- Assembly and Tests
 - 3-side buttable
 - TEC cooling



Summary

- A low power readout ASIC WASA for CEPC TPC has been successfully developed and evaluated
 - The power consumption is 4.94 mW/ch @ 40 MHz
 - ENC = 569 e+14.8 e/pF @ gain=10 mV/fC
- Pixel TPC readout R&D for CEPC TDR on going
 - Two version ROIC chips have been developed and the second version chip shows promising
 - RDL module has been designed and evaluated
 - Next step: beam test in September and new RDL module design