LumiCal电子学

Suen Hou, Lei Zhang

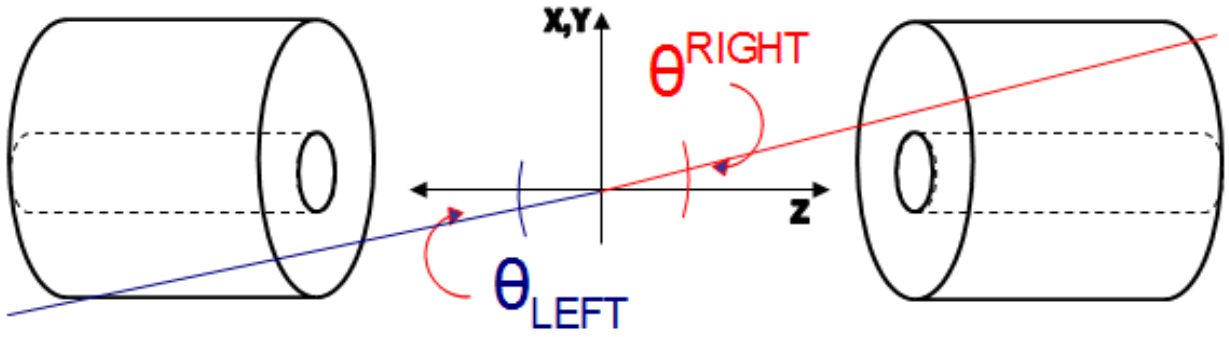
On behalf of the CEPC LumiCal team

Outline

- Readout speed
  - Per- bunch crossing
- Si strip design
  - Pitch size: multiple scatter
- Crystal Cal
- Trigger and DAQ

LumiCal overview

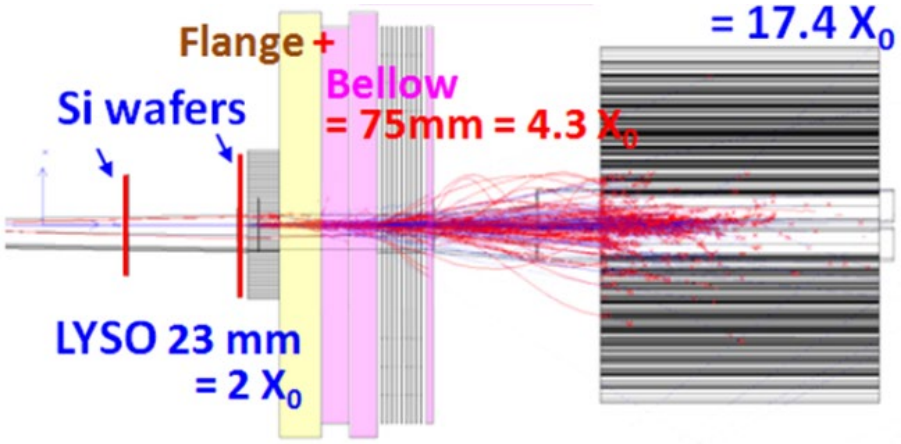
- Select Bhabha events to measure the integrated luminosity
  - Trigger back to back event
  - Targeted precision: 0.01%
- Potentials for other physics programs
  - Involving with the central detector

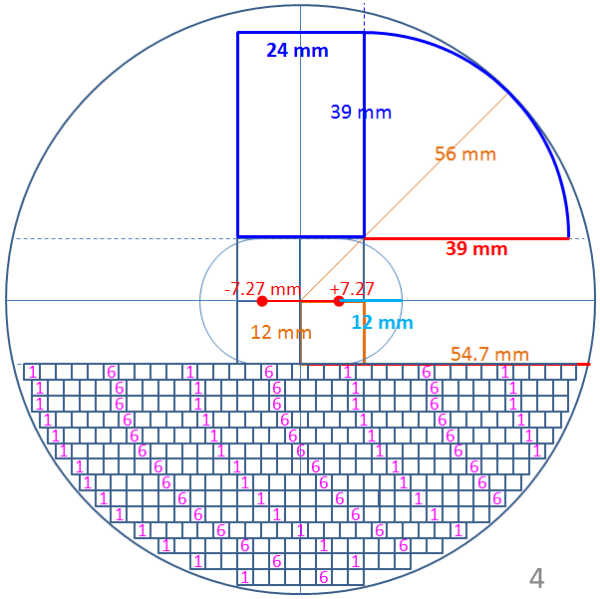


$$\Delta\theta \equiv \theta_{RIGHT} - \theta_{LEFT}$$

LumiCal overview

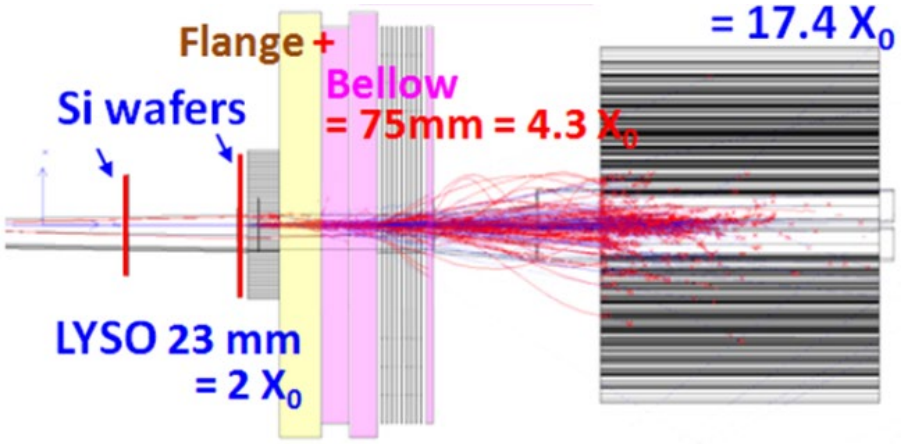
- Two silicon detector at 56cm and 64 cm from IP
  - Identify electron from photon
- LYSO Crystal:
  - Before flange, z = 56~70 cm: 2 X_0 LYSO = 23 mm
  - After flange, z= 90~110 cm: 17 X_0 LYSO 200 mm
  - Flange+Bellow : ~60 mm, 6 X_0

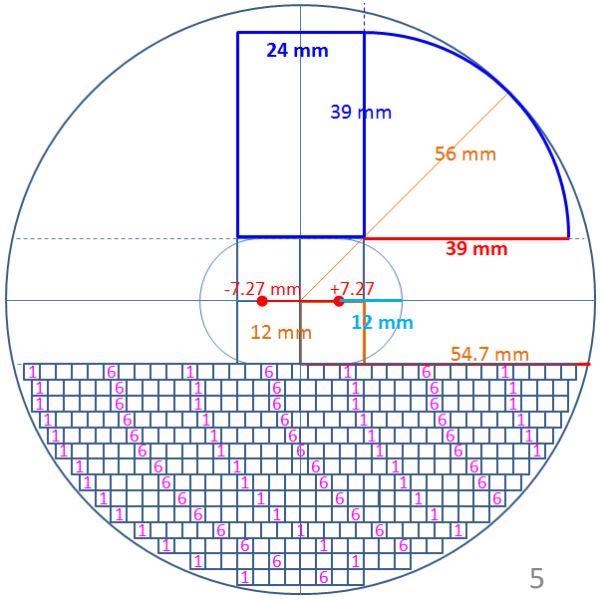




Readout speed

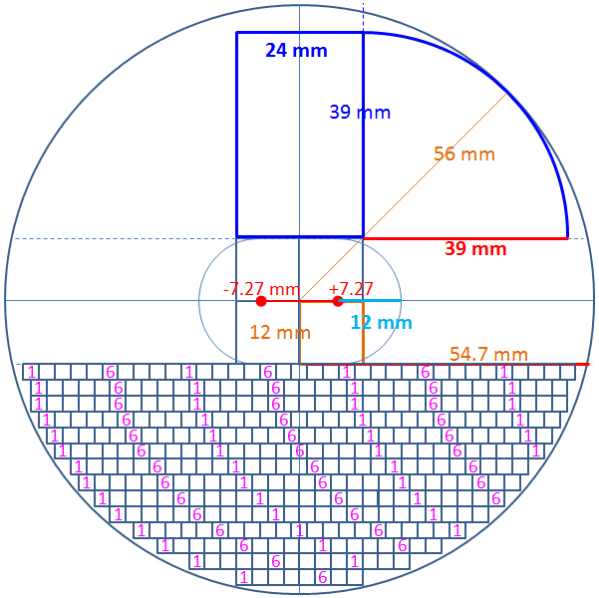
- Readout the “image” on each bunch crossing @ 25 ns
  - Expect the pileup under control

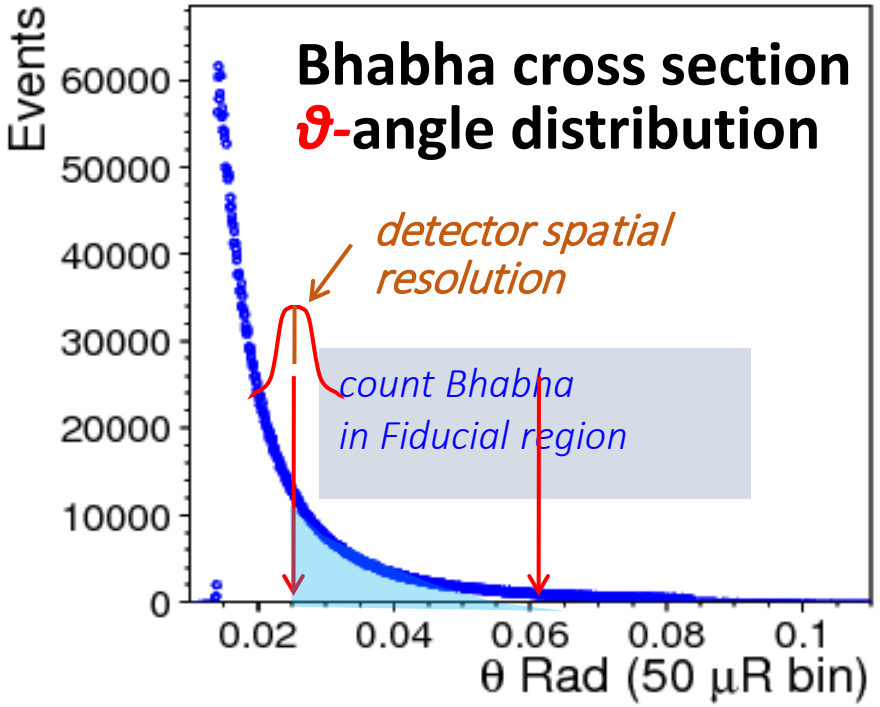




Si strip detector

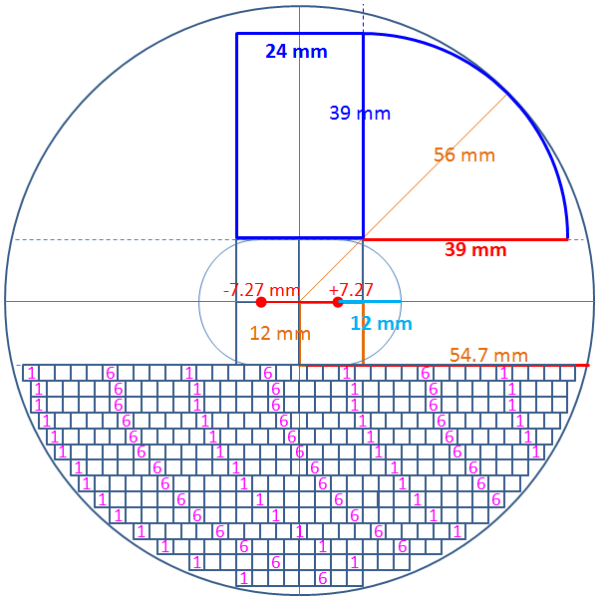
- Simple rectangle shape with 50 um pitch should be fine
  - Resolution on theta for resolving the multiple scattering
  - Requirement on phi to reduce the pileup
- A comparator in each pitch may be needed to identify pileup

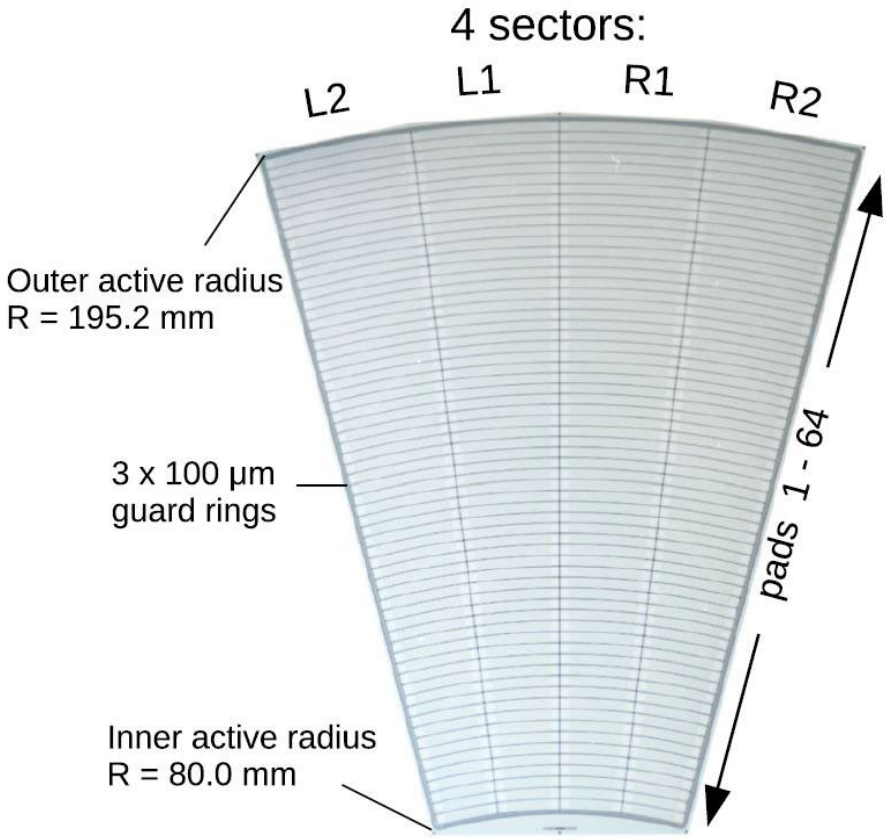




Si strip detector

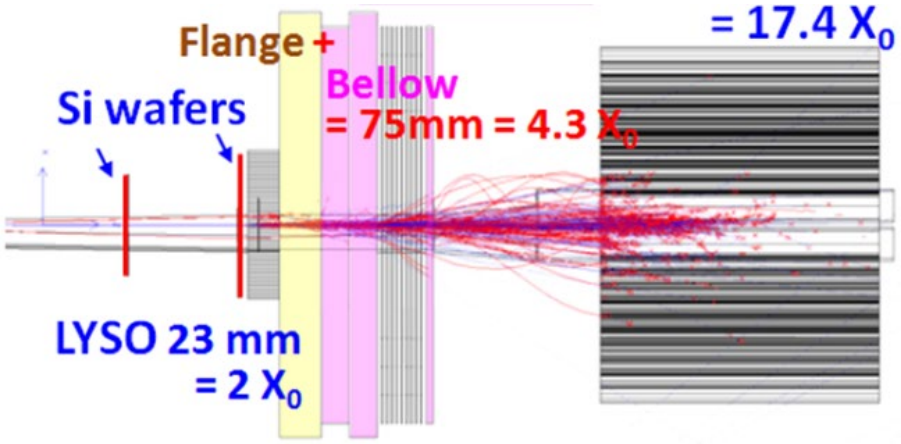
- One example (SiW from ILC FCal)
  - We don't need curved shape
  - Segmented phi design can be used

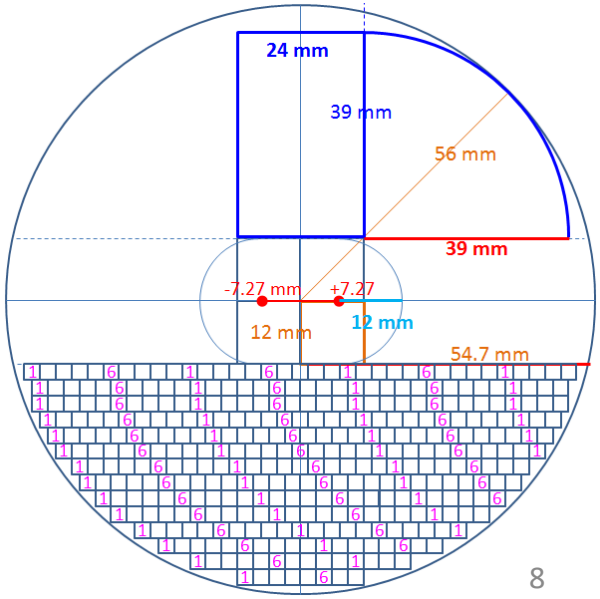




Crystal Calo

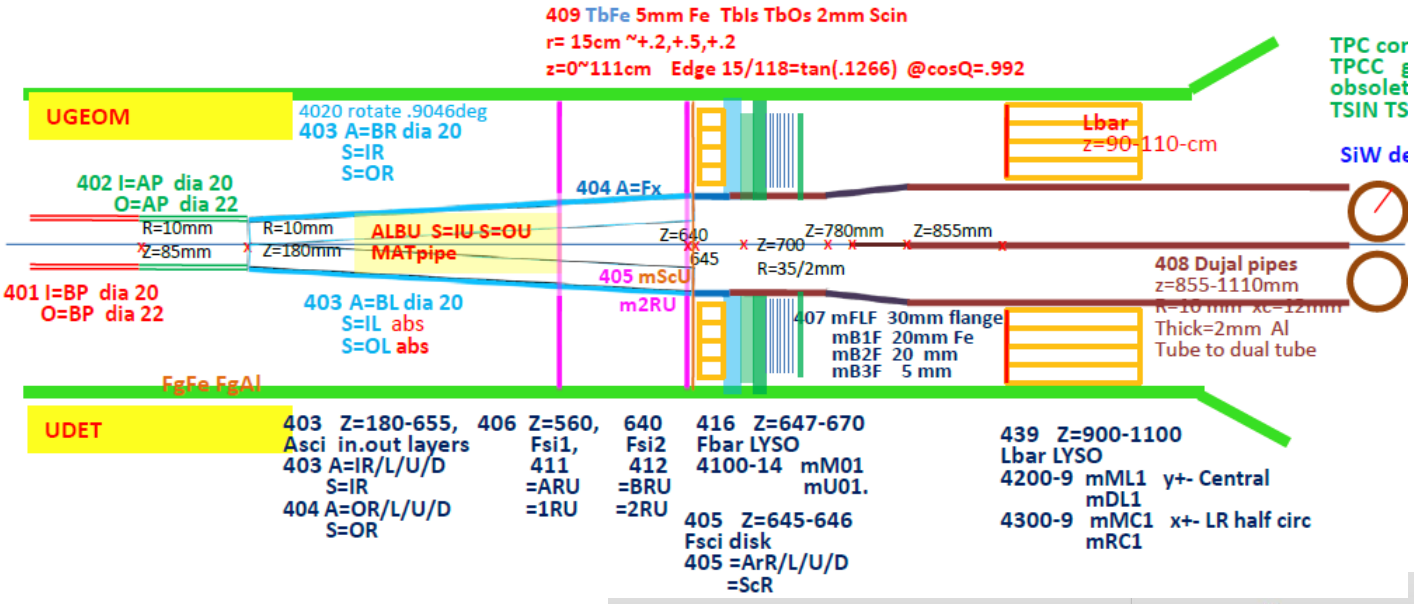
- Crystal size: 3*3*200 (mm)
  - Integrated readout
  - Above 30GeV EM shower, only measure tail (after ~6.3 X_0)
  - Precision: Delta E/ E about with 1024 bits

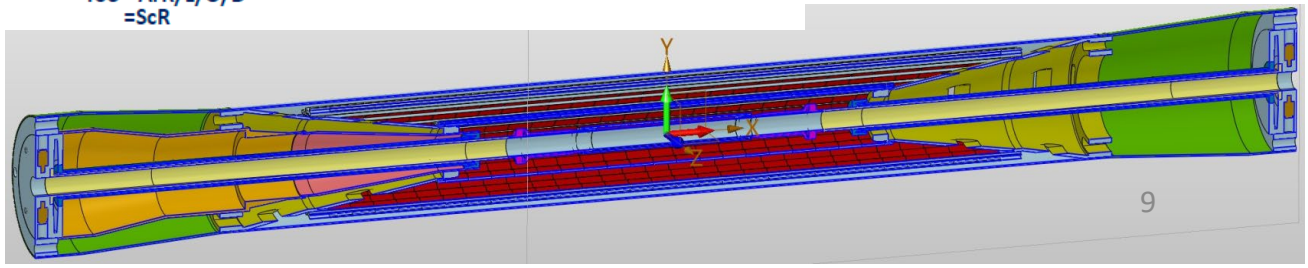




Trigger strategy

- Two sides signal to select back-to-back Bhabha events
  - ~2m cabling, sum of one quarter energy
- Align events with the central detector, for other physics programs
- Need to consider buffer and synchronization





backup

Bhabha event rates Z (@50MW)

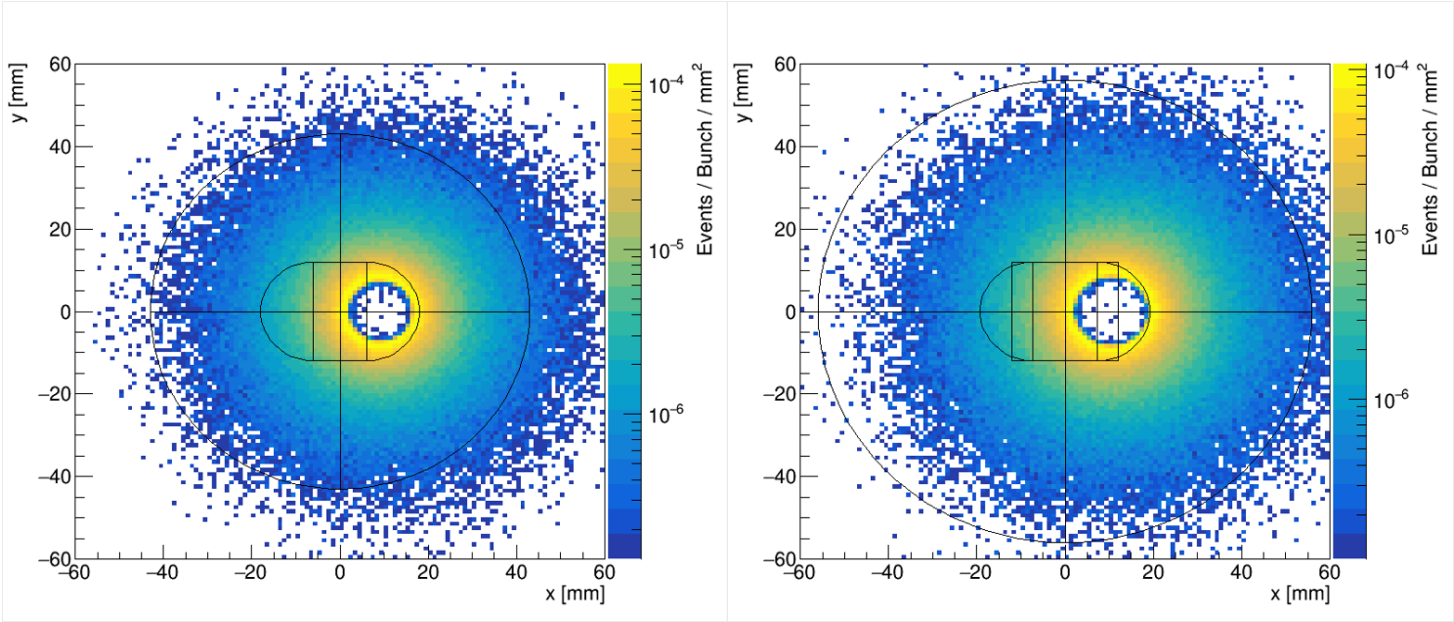


图4.12产生子计算每次束团对撞Z @50MW模式下粒子击中分布

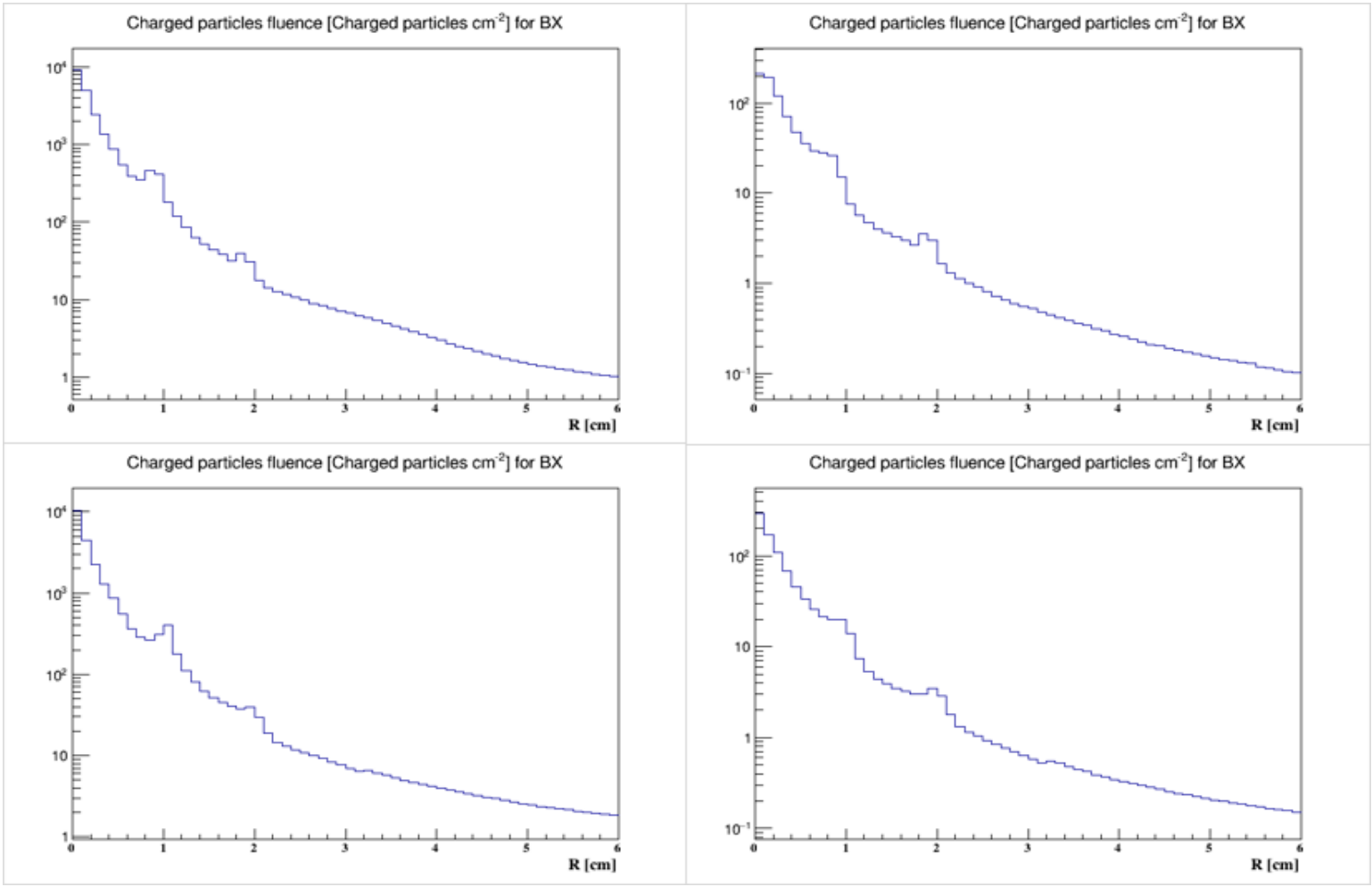


图4.14成对产生本底CDR结果，单位为 $cm^{-2}\ bunch^{-1}$

（左侧为Higgs模式，右侧为Z模式，上半部分为560mm处硅片，下半部分为640mm处硅片）

Overview of central detectors

前端数据率需求汇总

	Vertex	Pix Trk	TOF	Si Strip	TPC	DC	ECAL	HCAL
Detector for readout	CMOS Sensor	HVCMOS	Strip-LGAD	Si Strip	Pixel PAD	Drift Chamber	SiPM	SiPM
Main Func for FEE	X+Y	XY + nsT	X + 50psT	X	E + nsT	Analog Samp.	E + 400psT	E + 400psT
Channels per chip	512*1024 Pixelized	768*128 (2cm*2cm @25um*150um)	128	128	128	-	8~16	8~16
Ref. Signal processing	XY addr + BX ID	XY addr + timing	ADC+TDC/TOT+TOA	Hit	ADC + BX ID	Ultra fast PA + ADC	TOT + TOA/ ADC + TDC	TOT + TOA/ ADC + TDC
Data Width /hit	32bit (10b X+ 9b Y + 8b BX + 5b chip ID)	48bit （10b X+7b Y +8b BX + 8b TOT + 8TOA + 5b chip ID）	40~48bit （7b chn ID + 8b BX + 9b TOT + 7b TOA+5b chip ID ）	32bit (7b chn ID + 8b BX + 5b chip ID)	48bit (7b chn ID + 8b BX + 11b chip ID + 12b ADC + 10b TOA)	Wave @14bit 1.3Gbps	48bit(很极限) (8b BX+ 10b ADC + 2b range + 9b TOT + 7b TOA+ 4b chn ID + 8b chip ID)	48bit (8b BX+ 10b ADC + 2b range + 9b TOT + 7b TOA+ 4b chn ID + 8b chip ID)
Data rate / chip	160Mbps/chip@Trigger Innermost	~30Mbps/chip Innermost	<kHz/chip	<kHz/chip	~70Mbps/modu Inmost	~500Mbps/modu/sec	<100MHz/module（基线？）	<100MHz/module
Data aggregation	10~20:1, @160Mbps	?:1 @1~30Mbps	1. 10:1 @kbps 2. 10:1 @O(10kbps)	1. 10:1 @kbps 2. 10:1 @O(10kbps)	1. 279:1 FEE-0 2. 4:1 Module	On FPGA	1. 4~5:1 side brd 2. 7*4 / 14*4 back brd @ O(10Mbps)	< 10:1 (40cm*40cm PCB – 4cm*4cm tile – 16chn ASIC)

Wei Wei's slides at CEPC electronics meeting