status report on vertexing

WANG Meng

on behalf of the vertex detector group

Beijing, 2014.3.19

organization & manpower

- IHEP
  - OUYANG Qun (欧阳群, co-convener)
  - seniors:
    LU Yunpeng (卢云鹏), DONG Mingyi (董明义),
    QIN Zhonghua (秦中华), ZHU Hongbo (朱宏博),
    LOU Xinchou (娄辛丑, BIG BOSS)
  - graduate students:
    JU Xudong (鞠旭东) – sensor technology
    XIU Qinglei (修青磊) – simulation
- SDU
  - WANG Meng (王萌, co-convener)
  - ZHANG Liang (张亮, senior) – sensor technology
  - LIU Qingyuan (刘清源, PhD student) - simulation

activities

- bi-weekly group meetings
- presentations
  - CPS as vertex detector for future collider experiments, Mingyi Dong, 2013.10.23
  - SOI像素技术用于顶点探测器的调研, Yunpeng Lu, 2013.11.04
  - Development of Sensor Technologies for the ILC vertex detector, Liang Zhang, 2013.11.19
  - Hybrid Pixel for CEPC Vertex Detector, Hongbo Zhu, 2013.12.04

incomplete survey on pixel technologies

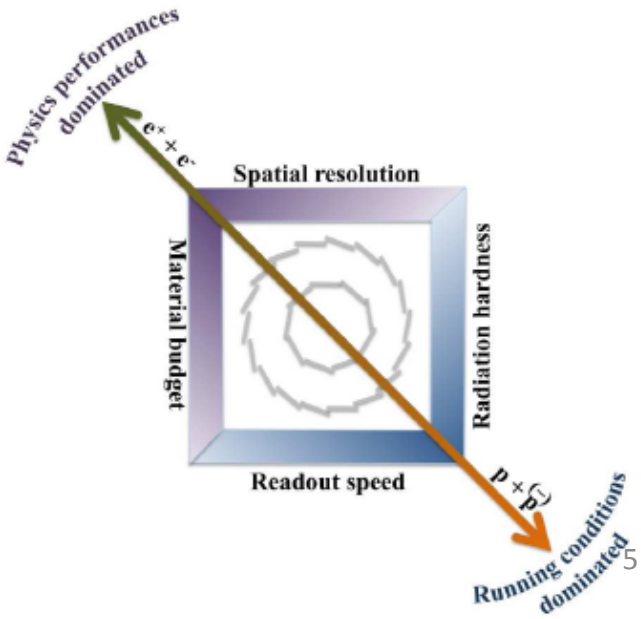
- monolithic pixel detector technologies
  - CMOS Pixel Sensor (CPS)
  - Fine Pixel CCD (FPCCD)
  - DEPleted Field Effect Transistor (DEPFET)

➔ CPS is a strong candidate for ILD

	Spatial resolution	Speed	Material budget	Radiation tolerance	Integration	S/N	Cost
CPS	+	+	+	+	++	-	++
FPCCD	++	-	-	-	+	+	-
DEPFET	+	+	+	+	-	+	-

CPS – CMOS Pixel Sensors

- achievements (primarily for ILD by IPHC-Strasbourg)
  - rolling-shutter readout suited to $\sqrt{s} \leq 500$ GeV
  - double side ladders featuring 0.6% X_0
  - VXD using CPS comply with $\sigma_{s.p.}$, $t_{r.o.}$ and power requirements for $\sqrt{s} \leq 500$ GeV
- R&D directions
  - Fast (low power) & high resolution & thin pixel sensor for continuous readout
  - High level signal processing & transfer integrated on small pixels
  - Fast, coarse resolution, very low power and thin sensors adapted to large sensitive areas
  - Large area pixel sensors
- our next step
  - investigate CMOS process options
  - choose an appropriate R&D direction
  - build and test a prototype

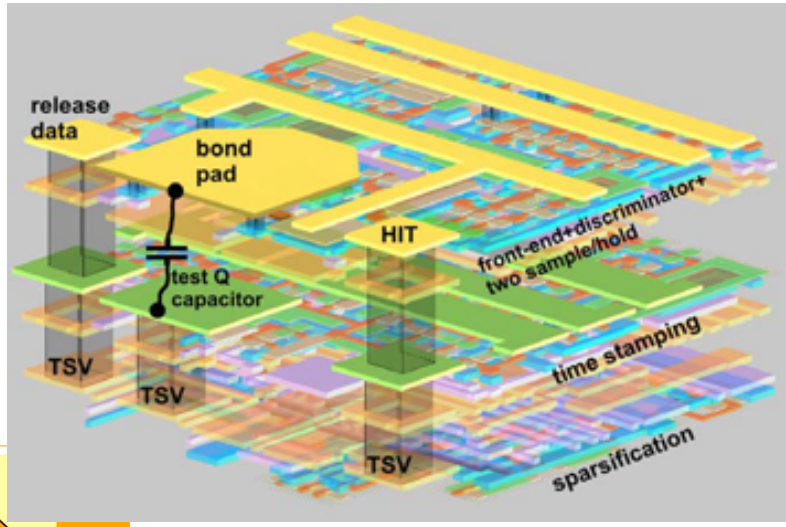


SOI – Silicon on Insulator

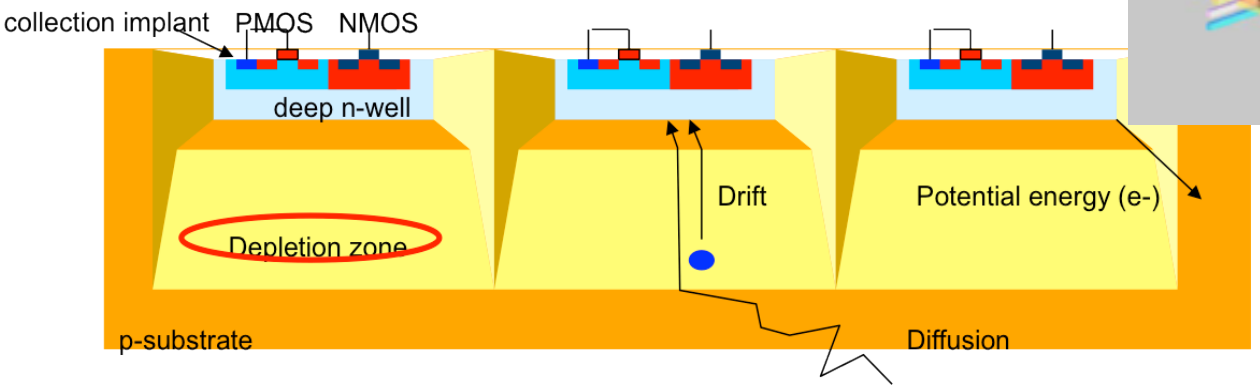
- a monolithic pixel with full depleted layer
- small pixel size
- also an option for SiD
- R&D needed on radiation tolerance and the shielding between sensor and circuits
  - could be improved by double SOI process

hybrid pixel detector

- traditional technology NOT suitable for ILC:
  - too thick: sensor (300 um) + ASIC (200 um)
  - too large pixel: bump/pitch (~20/50 um)
- new ideas needed
  - 3D integration technology
  - HV CMOS sensors



proposal for SiD

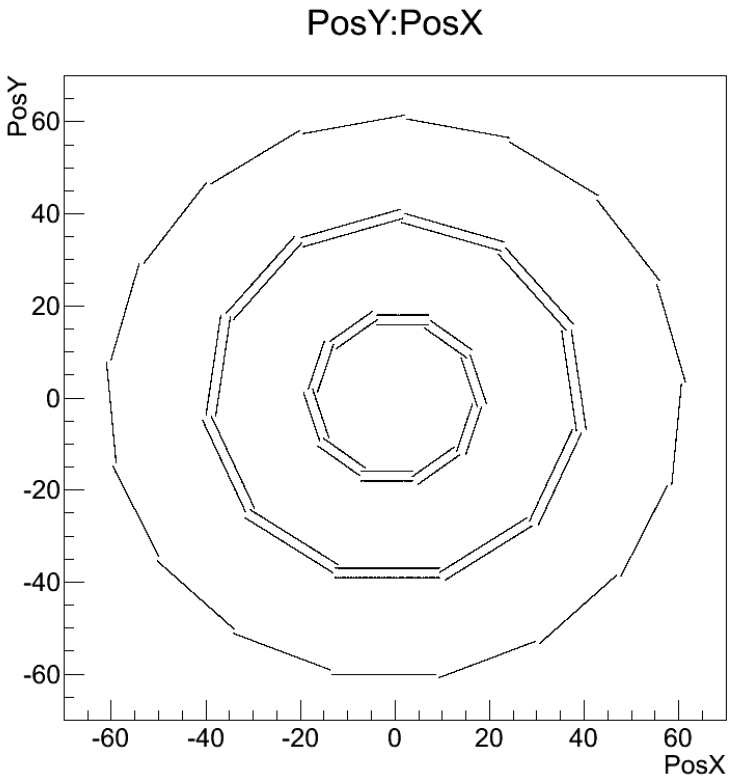


simulation progress: Mokka

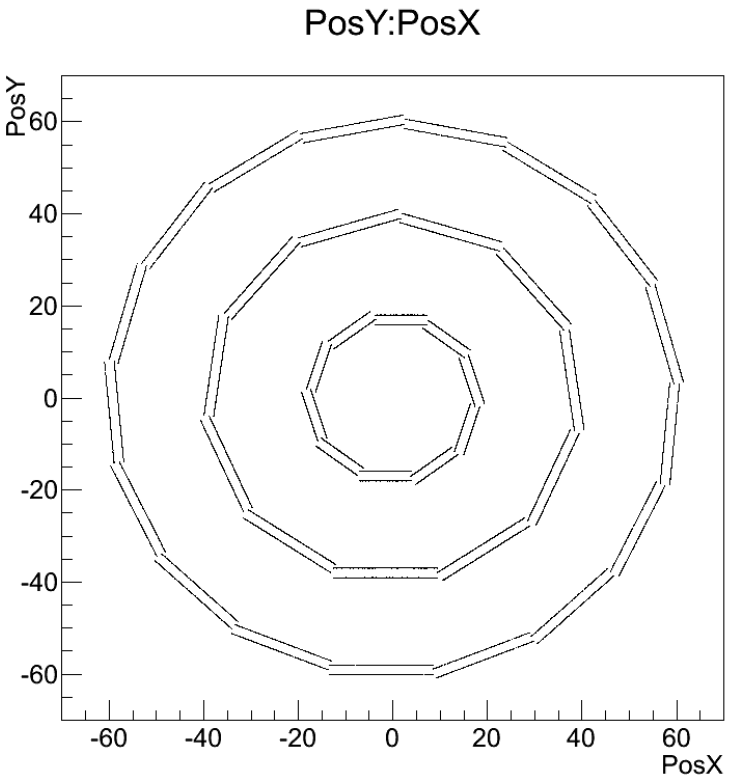
- database modification
  - models03: add a model CEPC_CDR based on ild_o2_v06
  - vxd4CEPC00: a copy of vxd07
  - host: lxplus01.hepg.sdu.edu.cn
- VXD modification
  - super-driver: SVxd04CEPC
  - sub-driver: vxd04

geometry comparison

VXD of CEPC_CDR



VXD of ILD_o2_v06



pre-CDR preparation

- a special meeting held on 2014.1.10
- table-of-contents drafted
- tasks assigned to individuals

VTX TOC (draft)

- introduction
  - relevant physics motivation: tag displaced vertices from b, c and tau decays
  - detector challenges and performance requirements: resolution, material, speed, radiation
- baseline design
  - layout, sensors, electronics & DAQ, structure design
- sensor options
  - possible technology: CPS (CMOS pixel sensor), DEPFET, SOI (silicon on insulator), 3D, FPCCD (fine pixel charged coupled device), Chronopixel (time-stamping)
  - new concepts
  - R&D status
- simulation and reconstruction
- mechanics and integration
- critical R&D
- cost

summary

- the group is organized in good shape.
- a variety of pixel technologies have been surveyed.
- some R&D's on CPS and SOI technology are in progress.
- simulation work just started.
- **pre-CDR** will be our top priority in the year.

- more students needed!
- please contact us if you are interested in!!