# 核电子学与探测前沿技术与应用

## --高速数据传输、计算与互连架构

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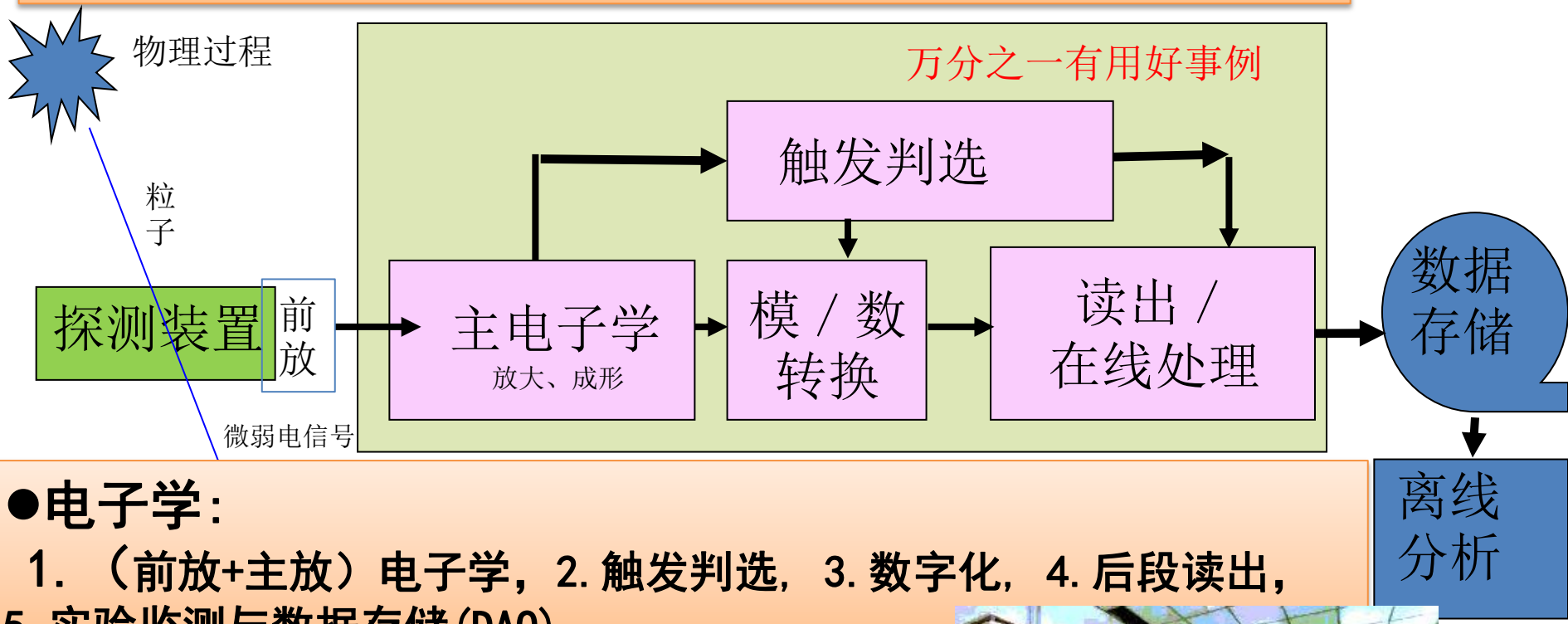
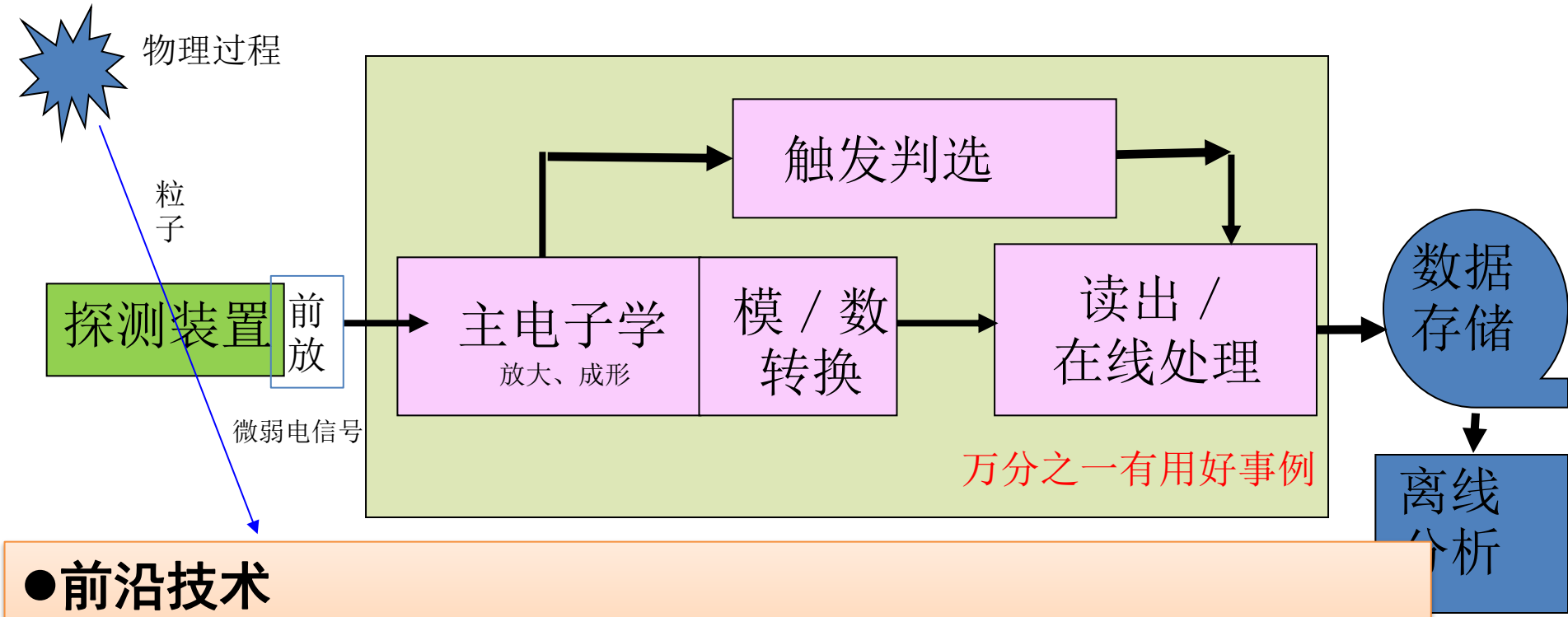



**●电子学：**

**1.（前放+主放）电子学，2. 触发判选，3. 数字化，4. 后段读出，5. 实验监测与数据存储(DAQ)**

# 一. 物理实验的基本构成

## ●试验装置及其演变：

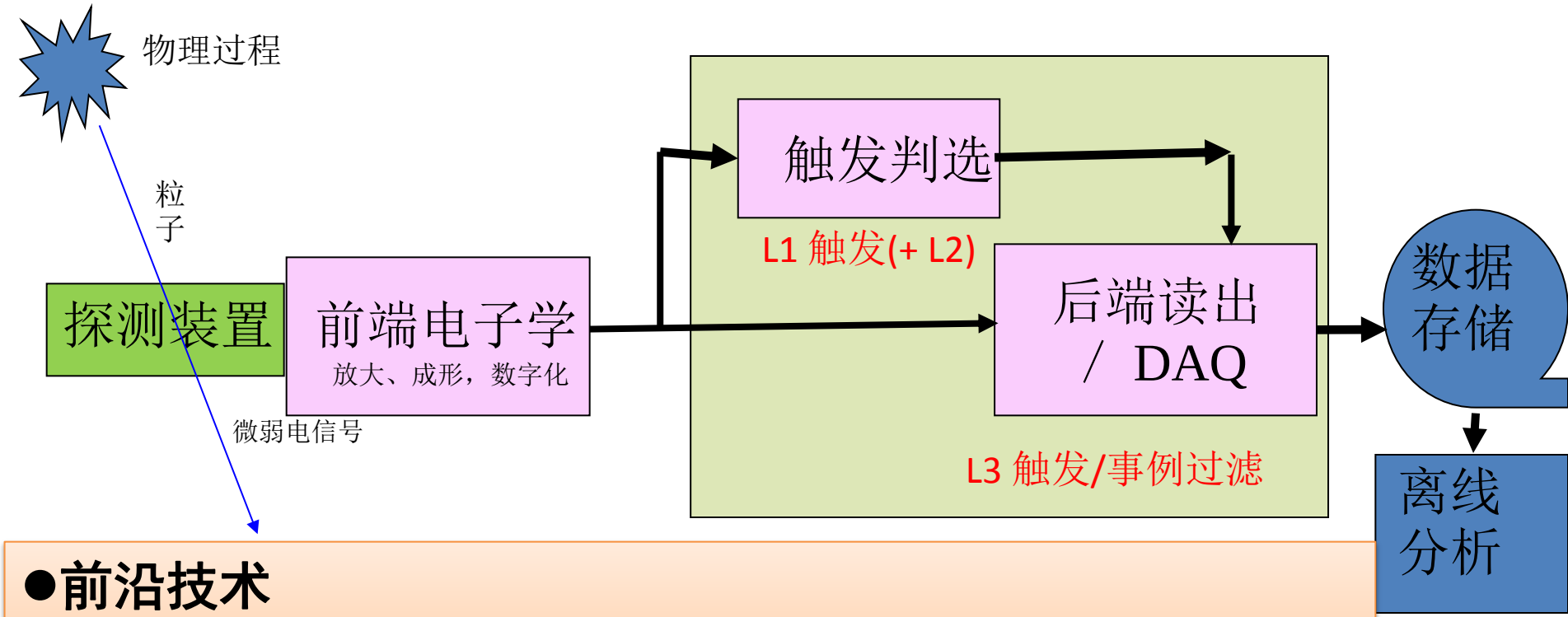



## ●前沿技术

1. 混合(前放，主放，数字化）2. FPGA信号与数据处理，
3. 读出（嵌入式CPU） 4. 系统架构（NIM, CAMAC)

# 一. 物理实验的基本构成

## ●试验装置及其演变：




## ●前沿技术

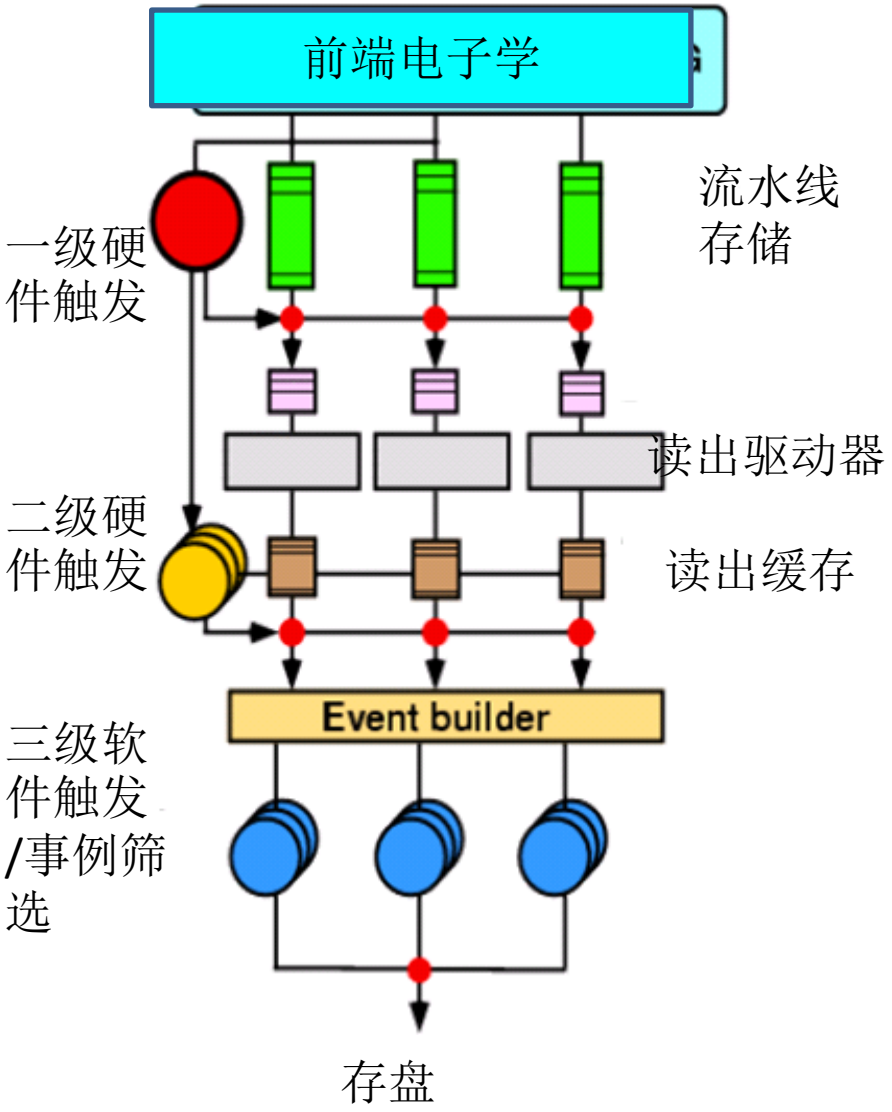
1. ASIC（放大、成形，数字化), 2. FPGA触发数据处理,
3. GPU/CPU事例过滤, 4. 系统架构(VME，CPCI)

# 目前采用的技术

- 分级触发
  - A. 一级硬件电子学
  - B. 二级硬件处理器
  - C. 三级计算机软件
- 体系架构
  - ◆ VME或CPCI
  - ◆ 没有硬件互联
- 当前技术的局限性

  —硬件触发方案需要基于单元合并简化，不易解决信号堆积的情况

  — 500Mb/秒的数据带宽，制约系统整体速度，乃至高事例率系统的触发效率



# 一. 物理实验的基本构成

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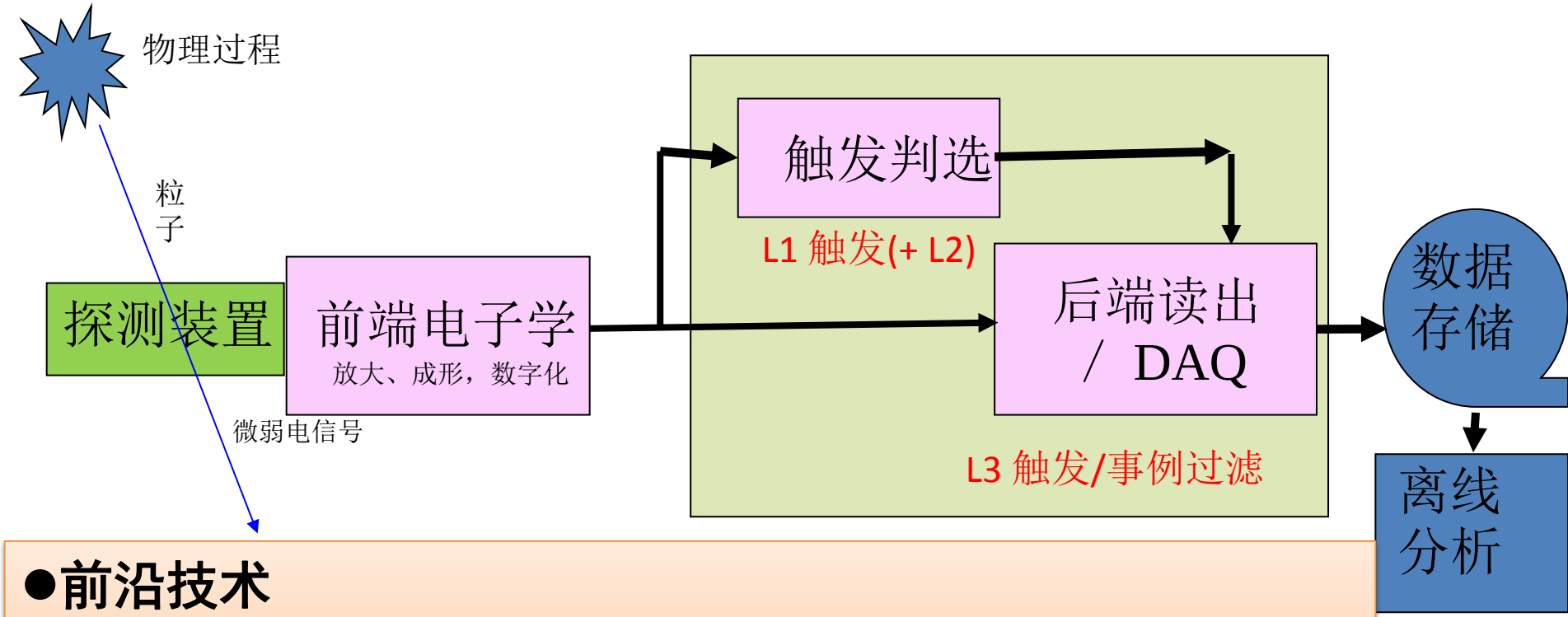


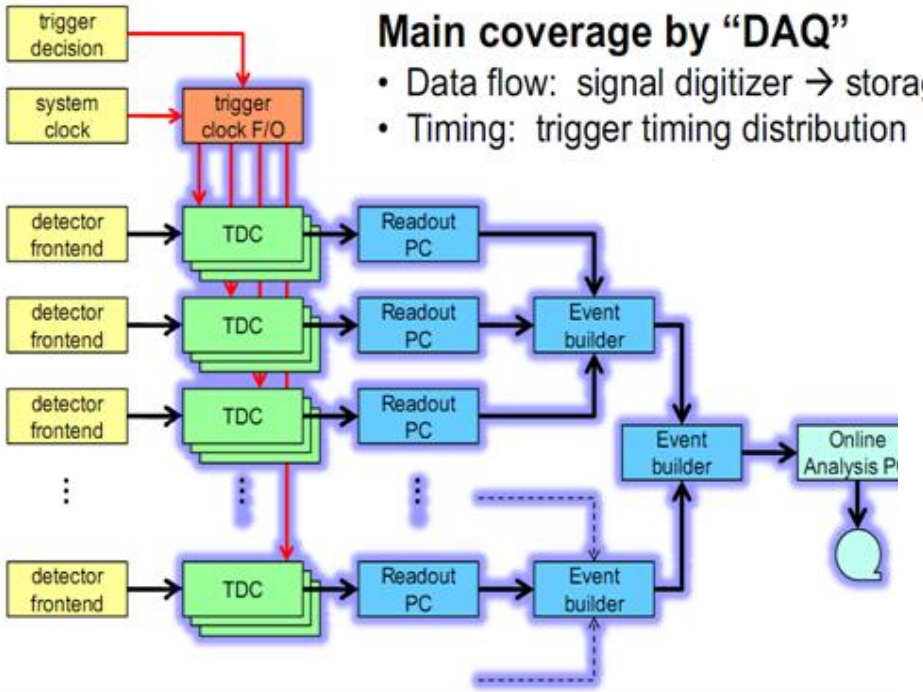

## ●前沿技术

1. ASIC（放大、成形，数字化), 2. 光纤高速数据传输, 3. FPGA触发数据处理，4. GPU/CPU事例过滤, 5. 系统架构(ATCA/uTCA/xTCA)

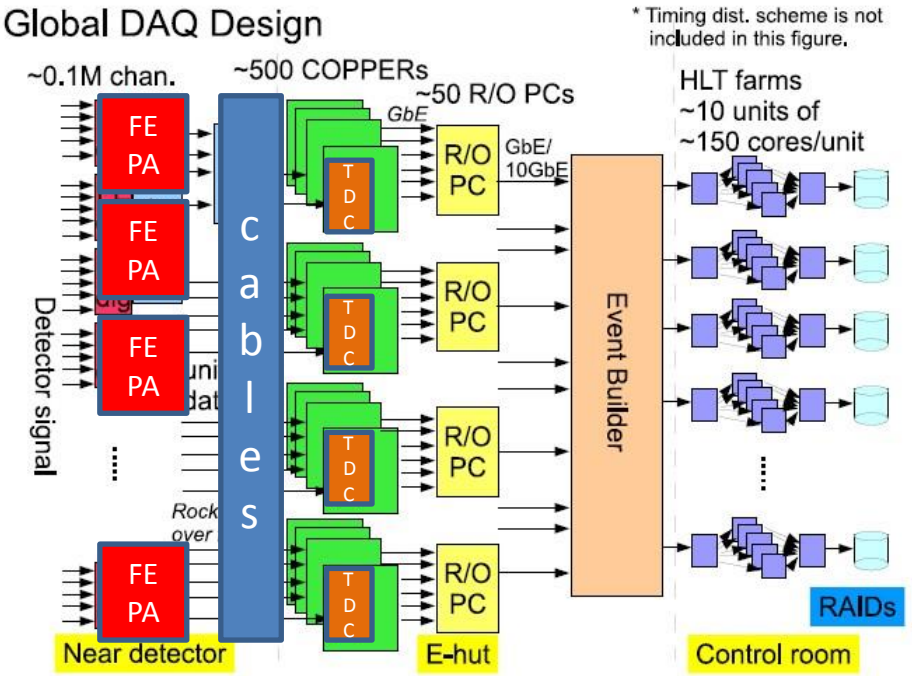
# 一. 光纤高速数据传输与互联

# 范例一：Belle II 实验系统

Belle 实验（放大+甄别器+TDC+读出）




Belle II Preliminary DAQ Structure



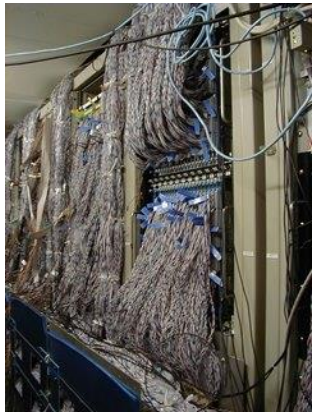

- Belle II DAQ
  - 前放
  - 电缆
  - 数字化平台/COPPER

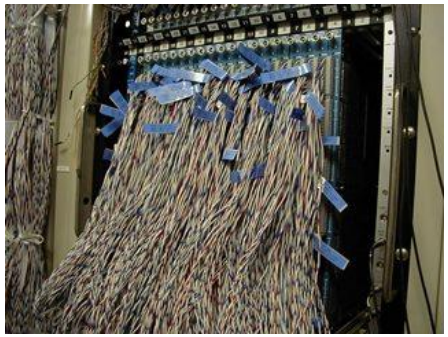
# BELLE II 数据获取

☑不足与困扰之处

长电缆架构结构复杂，地线回路干扰，数量多成本高。





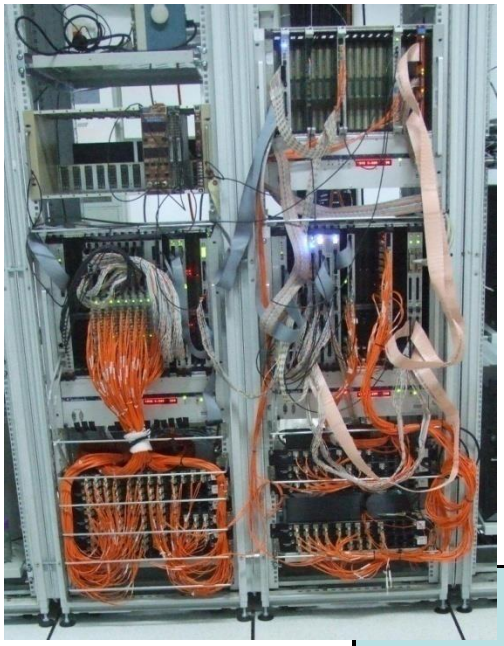


☑新方案（Gary+Zhen-An）

☑ 2008 ITOH/Nakao 教授参观BESIII并进行了探讨

利用BESIII　光纤传输经验
完全重新设计前端电子学
统一的探测器读出模块+标准HSLB
决定邀请高能所触发组参加Belle II 合作

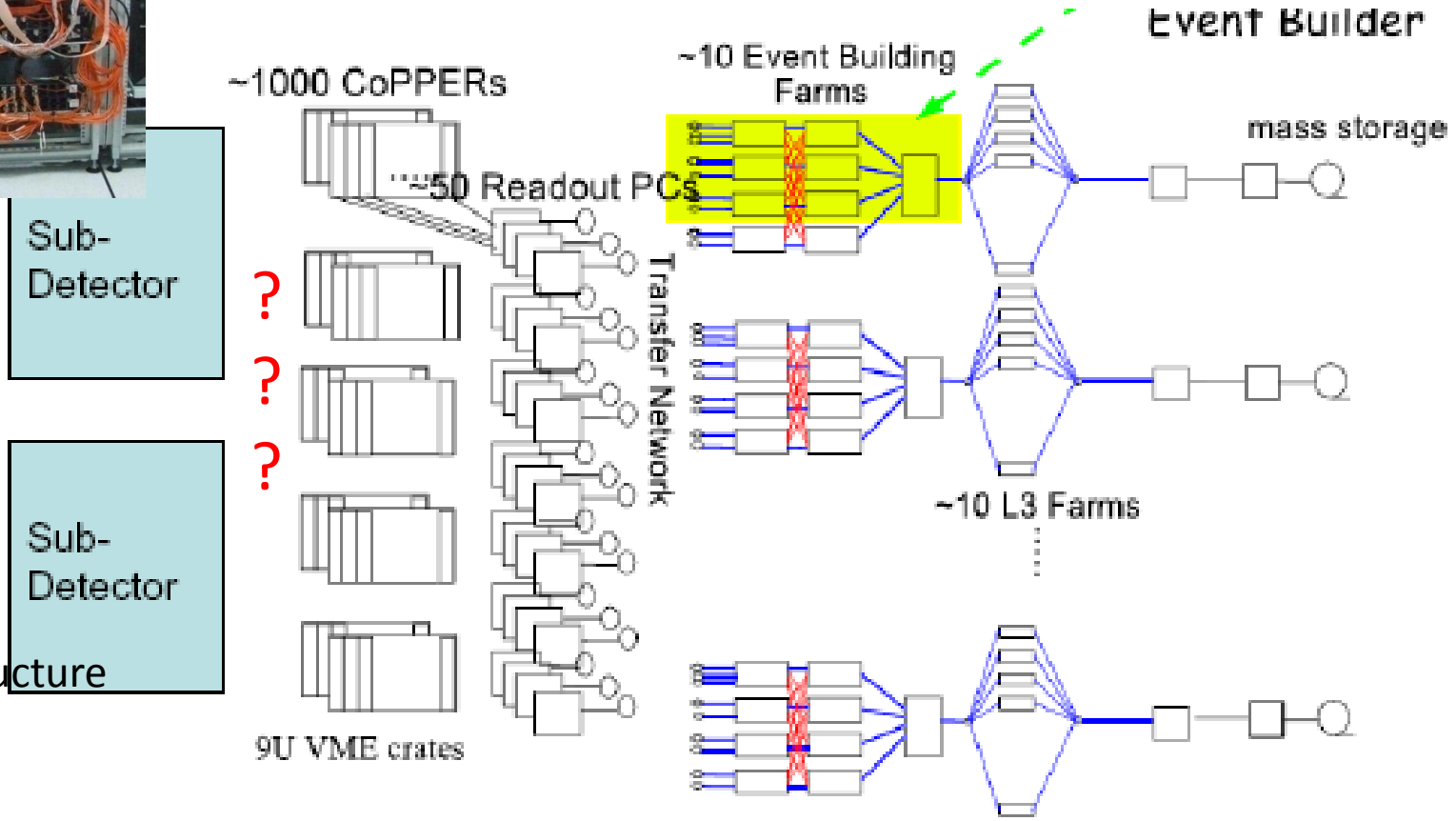
# Belle II Hardware Collaboration



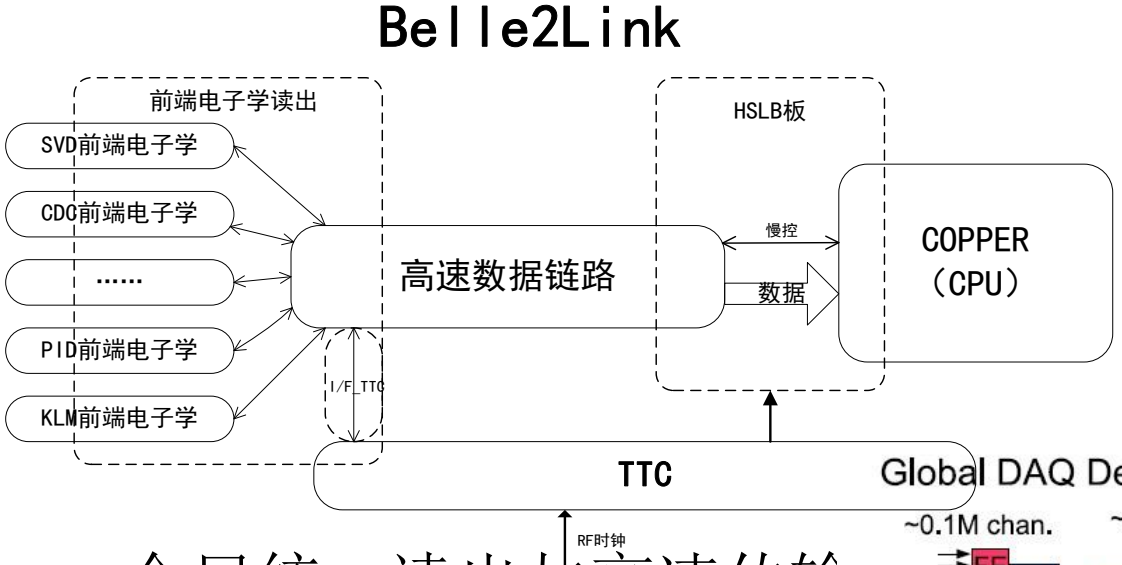
- BESIII experience/Fiber + SEDES
- All FEE will be redesigned
- COPPER is kept at KEK

BESIII Trigger

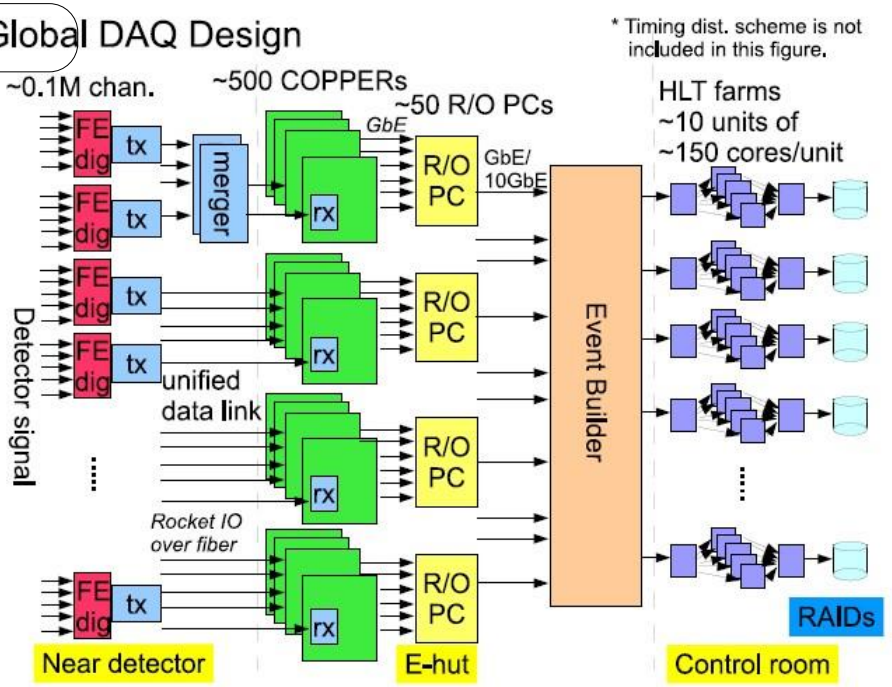
Belle II DAQ structure



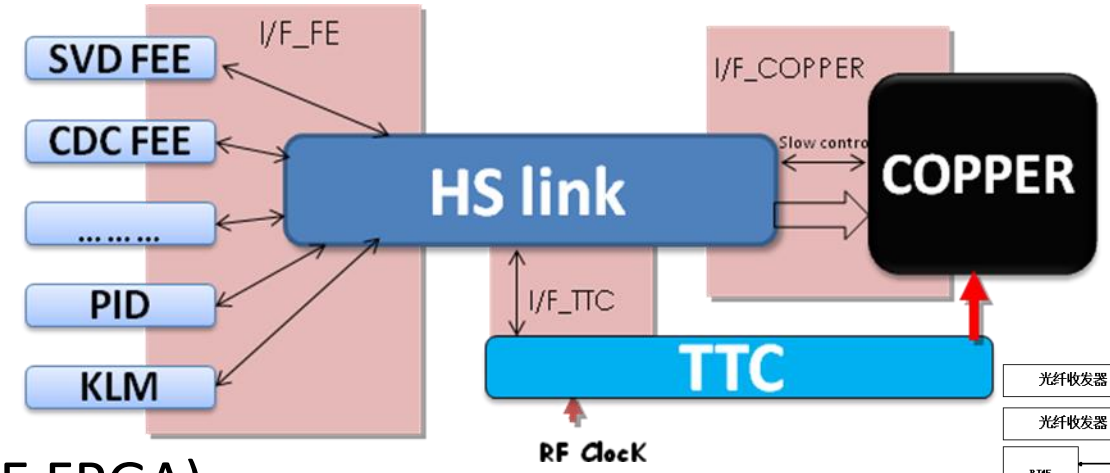
# 高能所的任务之一

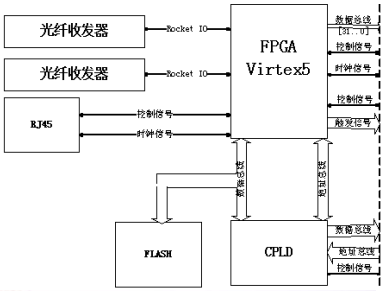


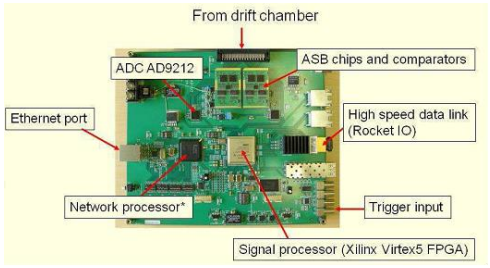

- 全局统一读出与高速传输
  - 方案设计
  - TDR编写
  - 样机研制（硬件，软件）
  - 样机系统研制与HSLB量产
  - 所有系统移植（工作组）
  - Belle II 系统联调

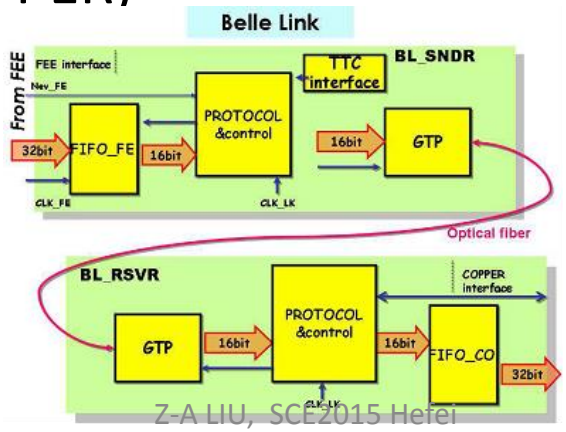


- 全局统一读出与高速传输(Belle2link)
  - 硬件
    - FEE
    - HSLB
    - COPPER
  - 软件
    - 上位(FEE FPGA)
    - 下位(HSLB,COPPER)



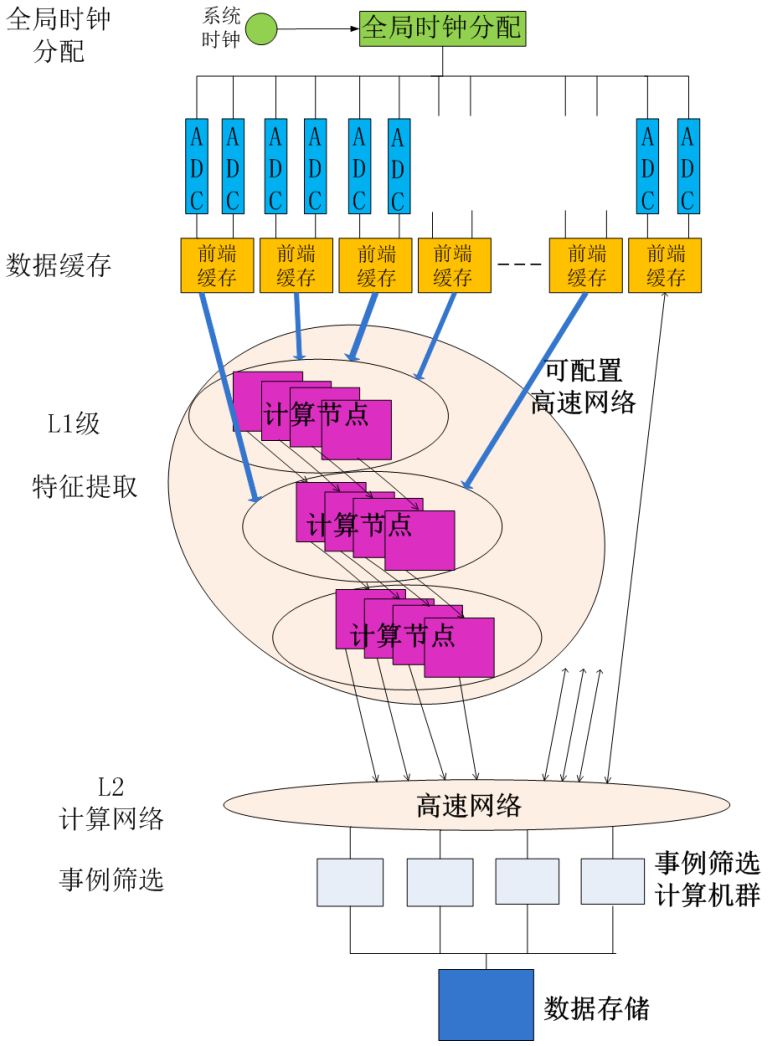




# 光纤高速数据传输与互联小结

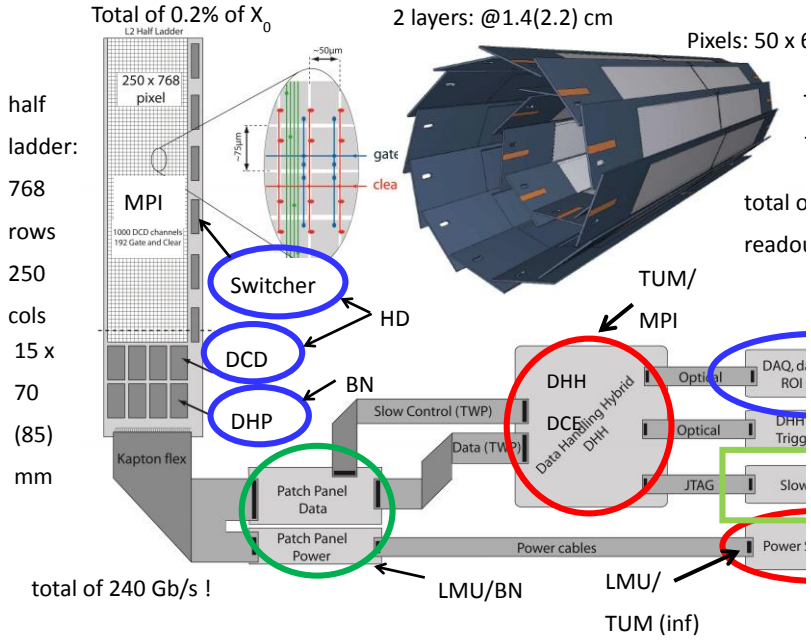
- LHC：　2001-2009，　1.6Gbps
- BESIII：　2002-2008，　1.75Gbps
- Belle II：2009　2.5Gbps
- PANDA：2010　3.124Gbps
- DEPFET：2011　6.4Gbps
- CMS：　2014　9.6/10Gbps

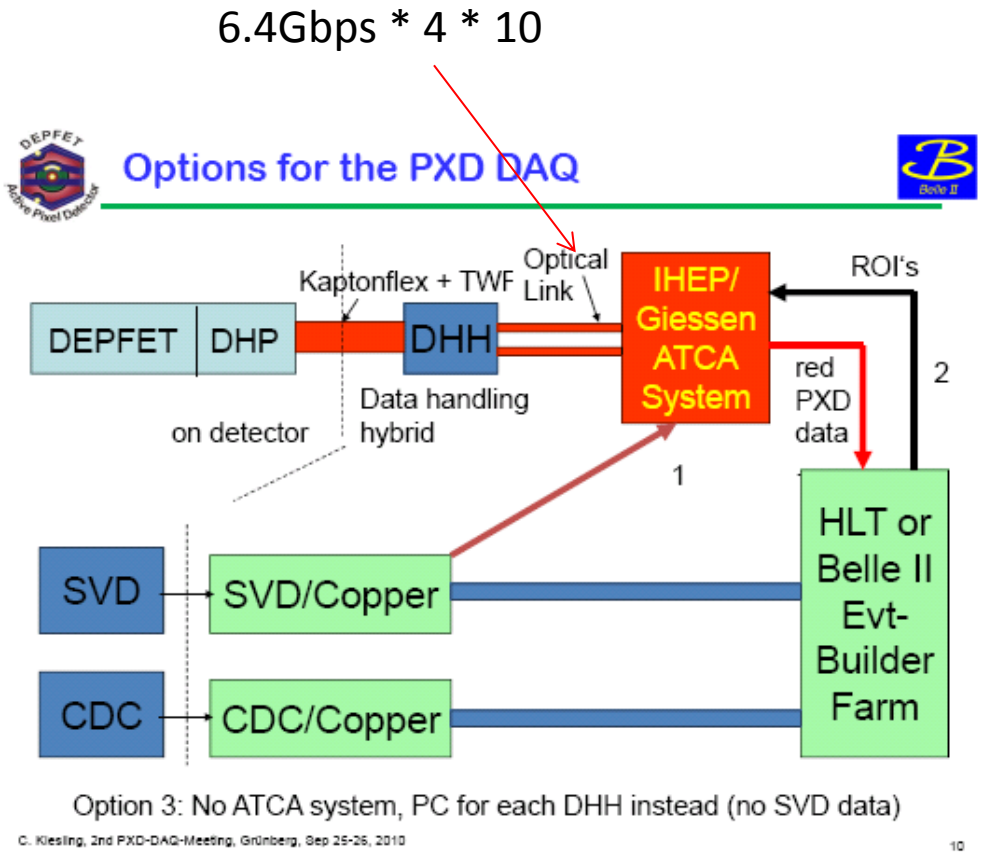
# 范例2 PANDA实验系统

- 3.125Gbps
- FEE -> 触发
- 触发间互联
- 触发-> DAQ



# 范例3 DEPFET硅像素探测器(PXD)DAQ系统

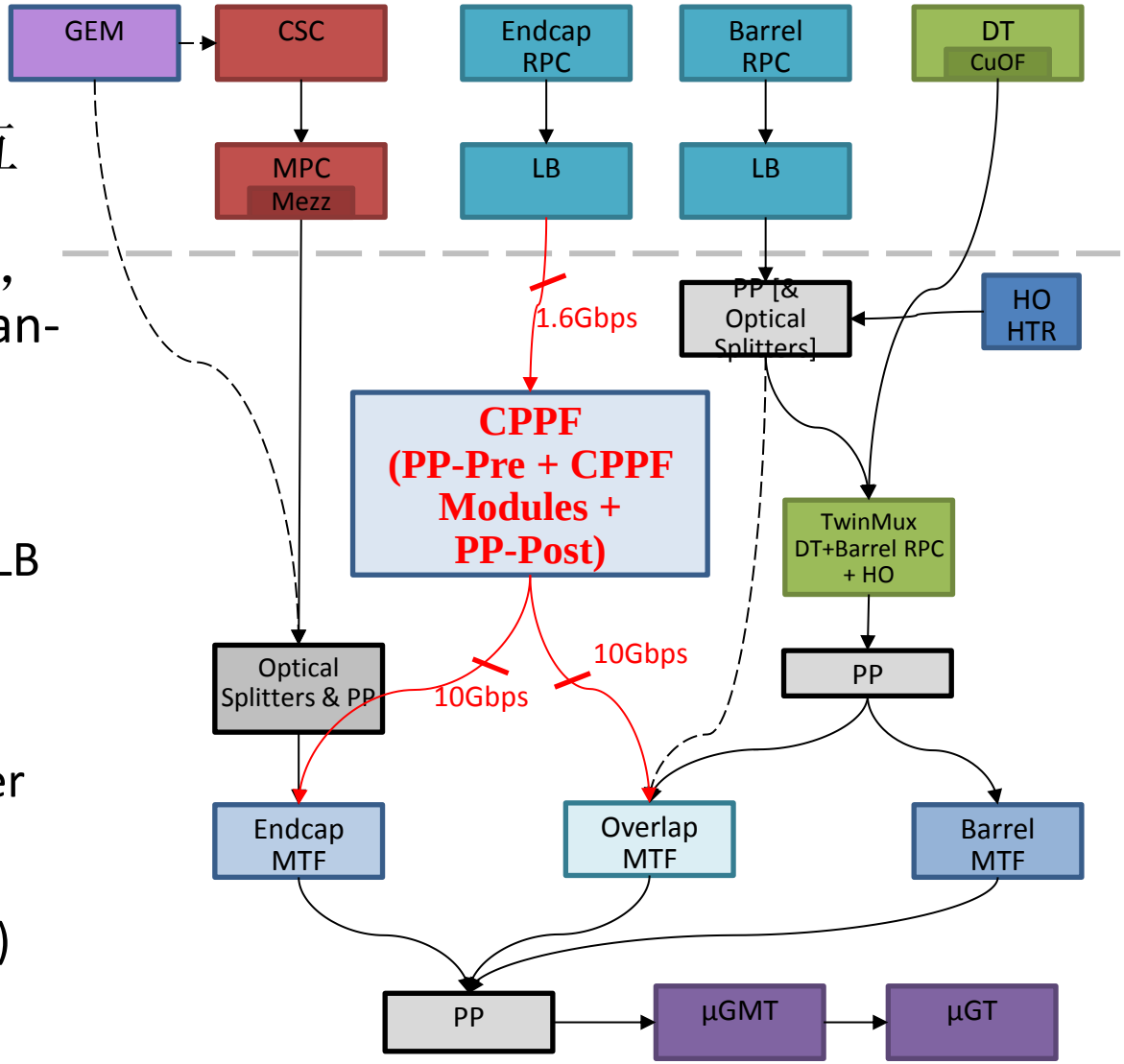



- 数据量太大
  - 240Gb/s
  - 大于Belle II 其他总和
- 压缩到1/10

# 范例4 CPPF in CMS Trigger Phase I Upgrade

- CMS 老系统1.6Gbps
- 新系统 输入输出及互联 10Gbps
- CPPF： Concentration，Pre-Processing, and Fan-out
- Components
  - Patch Panel(PP-Pre) for fibers from RPC-LB of 1.6 Gbps
  - CPPF modules (Key Module)
  - uMTCA shelf + Power + Shelf Manager + AMC13
  - Patch Panel(PP-Post) for fibers to Endcap and Overlap MTFs



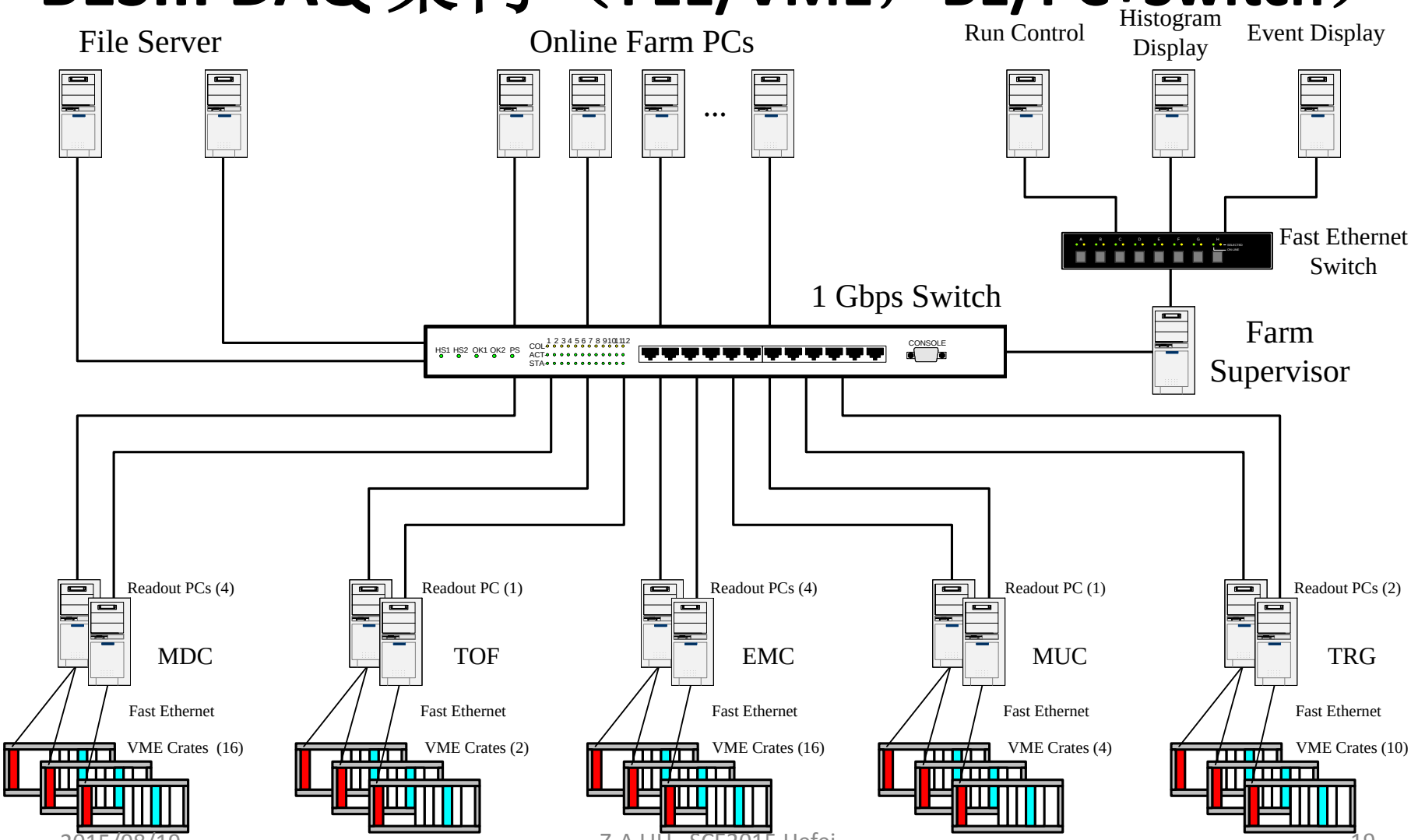
# CPPF Board Prototype Design

特点

- 输入: **Four** 12ch MiniPoD (1.6Gbps/10Gbps, total 76Gbps/480Gbps )
- 输出: **Two** 12ch MiniPoD (10Gbps/ch, total 240Gbps)
- FPGA
  - -- XC7VX415T-2FFG1157C(48 GTH)
  - -- XC7K70T-2FG484C
- Flash
  - -- PC28F00AG18
- DDR3(reserve Processing)
  - -- MT41J64M16(1

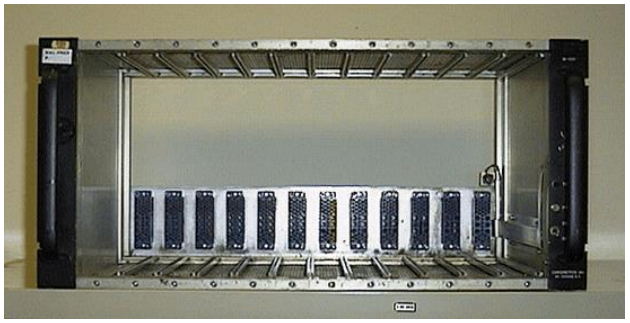
# 二。 ATCA/uTCA/xTCA 新型系统架构

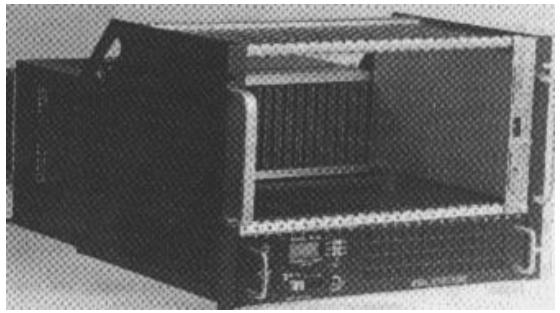
## BESIII DAQ 架构（FEE/VME，BE/PC+Switch）



# 核仪器标准的简史

- 1960年代
  - 英国卢瑟福实验室开创核电子学的标准
  - 欧洲核子研究中心CERN和美国实验室同期开展
  - 美国国家标准局和核仪器插件委员会建立了NIM标准
- 70-80年代建立了另2个标准CAMAC，FASTBUS，并被研究领域得到广泛应用
  - 核谱测量、粒子物理、医学物理、加速器仪器、加速器控制、航空航天、工业控制等
- ***目前这些标准仍在使用，但显局限性***
- ***90年代借用工业标准VME（VXI等）***
- ***2000年后CPCI***

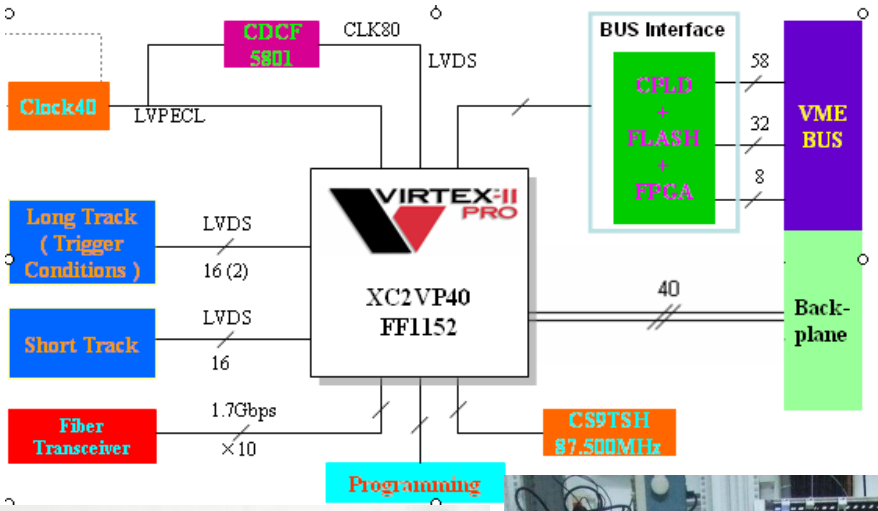


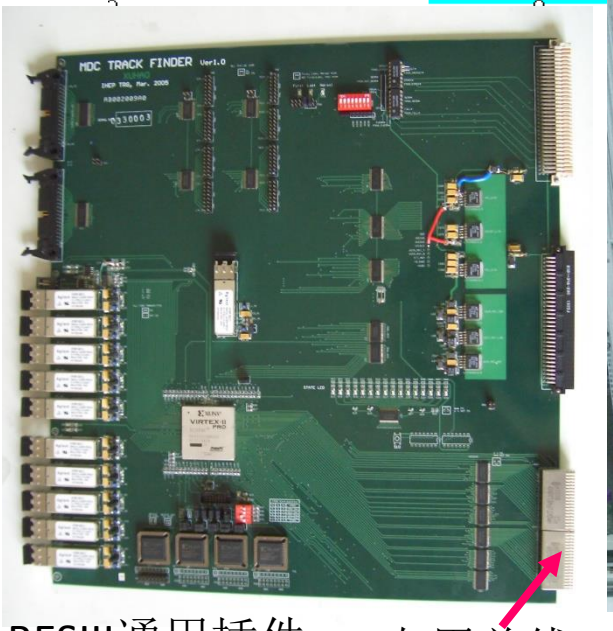


# 核仪器研制的现状及研究

## 标准与技术的演变　　05年

- 标准是有寿命的，但其演化要缓慢温和
  - 物理实验中的标准已经有些过时，但很多系统却仍然在使用
  - 微电子工业的巨大进展需要新的平台来展现他的优点,目前的平台已不适应:
    - 高速处理芯片4Gsps
    - 集成电路的功能已经把原来插件完成的功能在一片可变成逻辑器件FPGA中实现
    - 片上处理器提供了可变成控制和并行数据处理能力
    - 通用硬件设计配以不同的固件得以实现多种功能设计
    - 片上串并/并串转换能力3-10Gbps
- 需要新的标准




BESIII通用插件

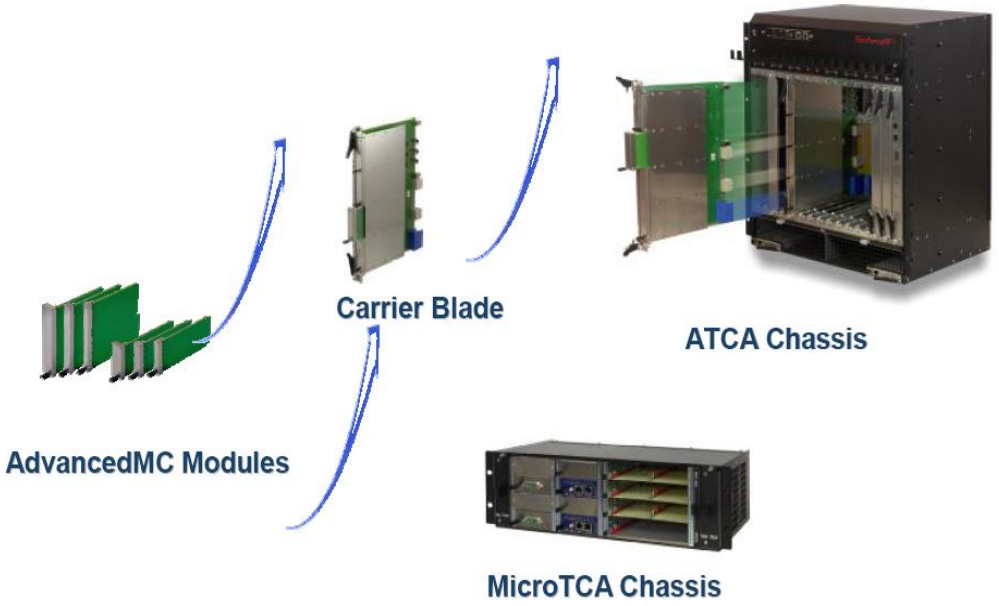
专用总线

205Gb/秒同步传（BESIII）

# 工业新标准ATCA/MTCA

- 电信领域大多数基于CPCI、VME总线的处理器系统，总线带宽已经成为制约系统处理能力的瓶颈。VME64X的总线带宽为320Mb/s，已经不能满足要求高吞吐量、低延迟的系统。随着对更高系统带宽、总线速度、实时性、系统可靠性、温度范围、散热及更小空间等方面越来越高的要求，迫切需要一种新的运算架构来满足信号处理的需求。
- PICMG协会ATCA委员会由代表了工业和电信设备制造商及终端用户的105个公司组成，其目标是建立、修改并计划在2002年底发布新的规范——ATCA。经过12个 月的奋战，PICMG3.0规范——先进的通讯计算机构架（ATCA）如期发布。

- 低成本、小尺寸的应用，PICMG协会又在ATCA构架的基础上提出了MicroTCA构架，该技术在2006年逐渐成熟。



# 核仪器新标准是什么

- ATCA
  - 优点
    - 高速IO及互连10Gb/s
    - 高可用性HA ~99.999%
    - 智能管理
- MicroTCA (MTCA)
  - ATCA的优点
  - 半高度
- AdvancedMC（AMC）
  - 小插板

高能物理实验再次借鉴工业标准（电信）？

这是一个很好的思路！

# 谁在用（想用）ATCA？

## Who else is using ATCA?

The group of experimenters includes several major laboratories representing different fields of use and a range of applications.

IHEP

- Active programs are showing up most notably at
  - DESY for XFEL and JET
- Other laboratories
  - ILC, IHEP, KEK, SLAC, FNAL, ANL, BNL, FAIR, ATLAS at CERN, AGATA, large telescopes, Ocean Observatories
- Investigating ATCA solutions for future upgrades
  - Both the CMS and ATLAS detectors
- Setting up prototype experiments to test its potential
  - ILC and ITER

ATCA is being adapted without significant change as a platform for generic data acquisition processors requiring high throughput and bandwidth.

Most of these programmes put the emphasis on **High Availability**

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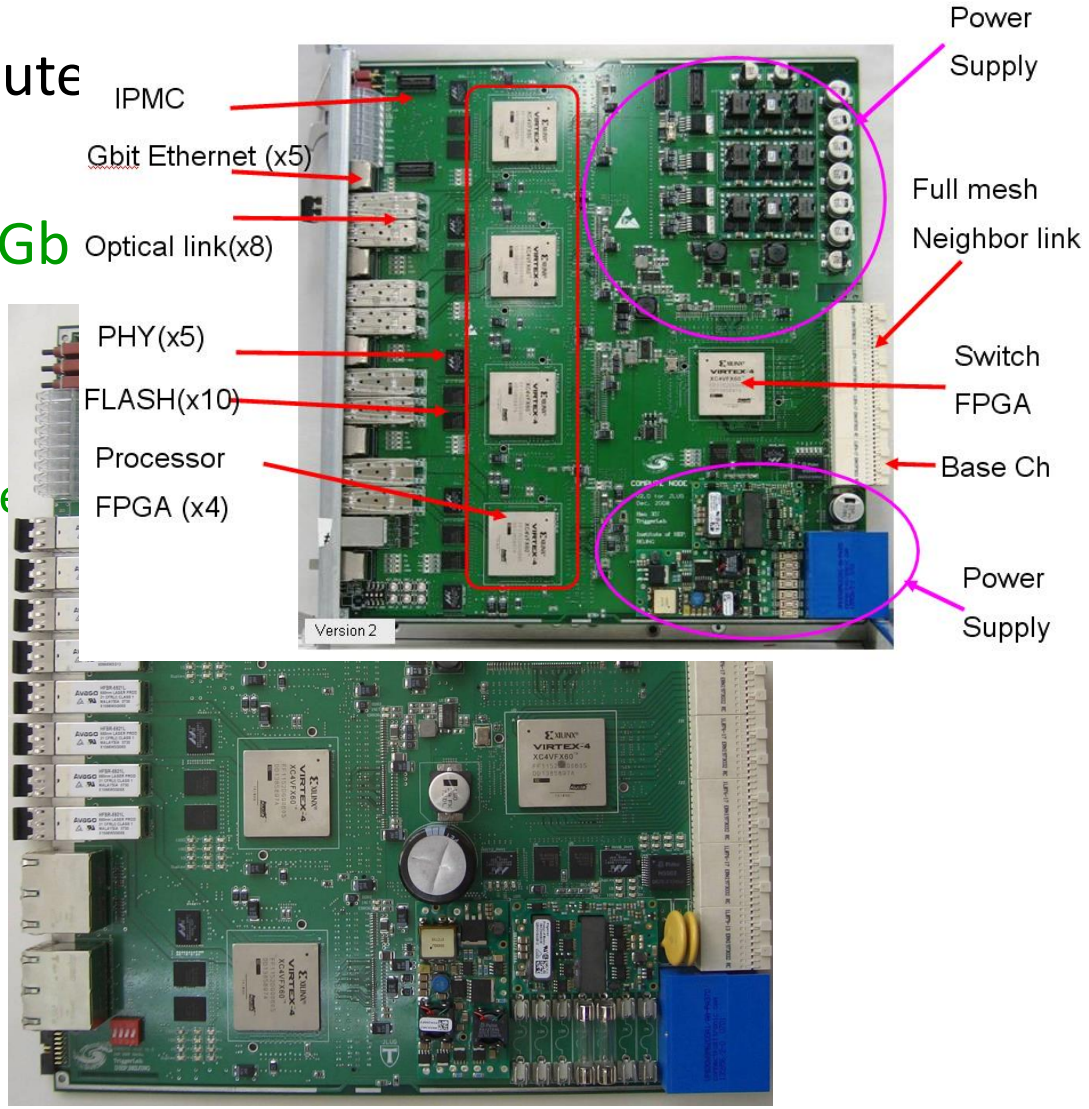
B. Gonçalves | Paris, February 2, 2009 | NI - Big Physics Round Table

# 高能所：高性能节点计算机的设计

- High Performance Compute Power:
  - 5x (Virtex-4 FPGA + 2Gb DDR2)
- ~32Gbps Bandwidth
  - 13x RocketIO to backplane
  - 5x Gigabit Ethernet
  - 8x Optical Link
- 2 Embedded PowerPC in each FPGA
  - Real time Linux
- ATCA compliant
- 完成第二板

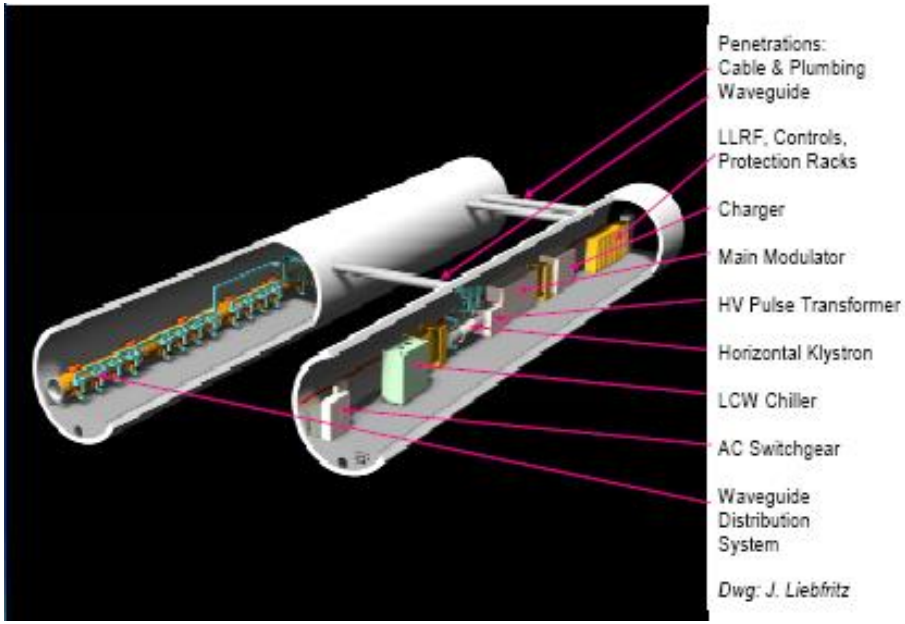



高能所设计的基于ATCA和FPGA的高性能处理板

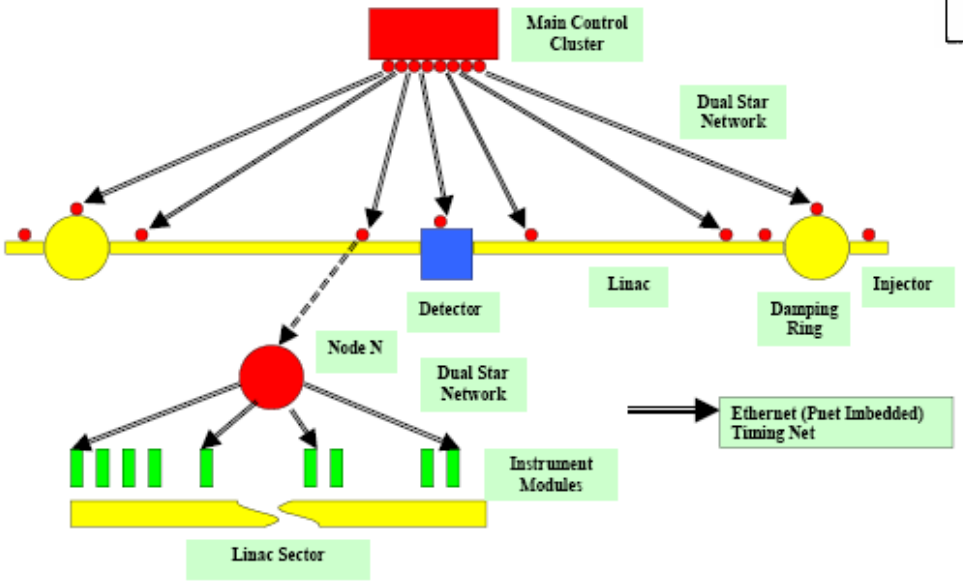
# 国际上其它实验室的相关研究

- 德国DESY在 XFEL 1 km 电子直线加速器领先设计 (~1/20th an ILC)
  - LLRF, 连锁保护，束线仪器
  - ATCA + MicroTCA
- SLAC 开始用MTCA对3km电子直线加速器进行更新

# 国际直线对撞机




| Scheduled Operating Hours: 6500 | | | |
|---|---|---|---|
| | Weight | Availability | Unscheduled Outage (hours) |
| $e^-$ Inj, Source and Linac | 1 | 0.99 | 66 |
| $e^-$ DR and Compressor 1 | 1 | 0.99 | 66 |
| $e^-$ Booster Linac and Comp. 2 | 1 | 0.99 | 66 |
| $e^-$ Main Linac | 3 | 0.97 | 195 |
| $e^-$ Final Focus and Dumpline | 1 | 0.99 | 66 |
| **Subtotal $e^-$ machines:** | **7** | **1** | **458** |
| $e^-$ Inj, Source and Linac | 1 | 0.99 | 66 |
| $e^+$ Source and Linac | 1 | 0.99 | 66 |
| $e^+$ Pre-damping Ring | 1 | 0.99 | 66 |
| $e^+$ DR and Compressor 1 | 1 | 0.99 | 66 |
| $e^+$ Booster Linac and Comp. 2 | 1 | 0.99 | 66 |
| $e^+$ Main Linac | 3 | 0.97 | 66 |
| $e^+$ Final Focus and Dumpline | 1 | 0.99 | 66 |
| **Subtotal $e^+$ machines:** | **9** | **1** | **589** |
| **Totals:** | **16** | **0.85** | **1047** |




- 下一代加速-国际直线对撞机(ILC)要求
  - 高可用率（high ***availability)***
- ***高数据产生率（>500Gbps）***
- ***解决办法ATCA/MTCA？***
  - HA ~99.999%
  - 波特率 10Gbps

# ITER 欧洲核聚变项目

## Control and Data Acquisition in fusion: towards ITER relevant solutions

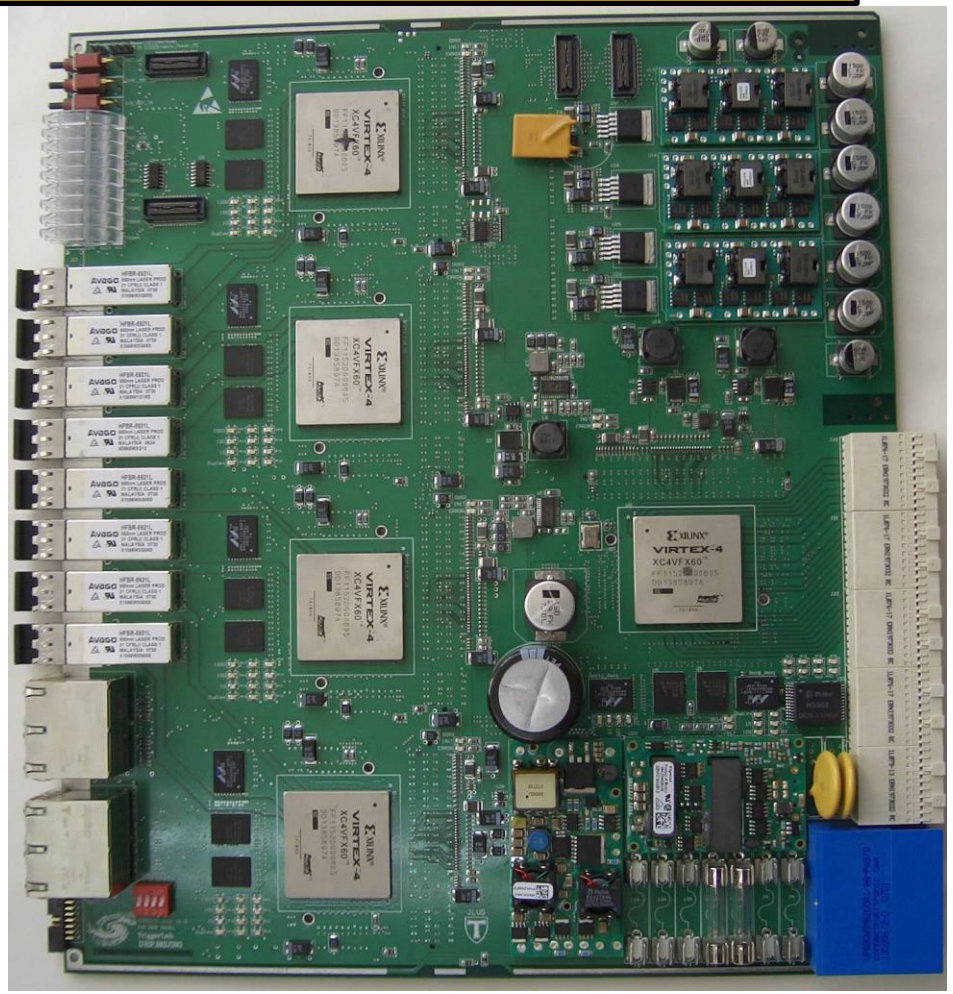
| VME | PCI | ATCA | … (R&D) |
|---|---|---|---|
| •ISTTOK<br>•TCV<br>•TJ-II<br>•TCA/Br<br>•MAST | •JET | •JET | •ITER |
| •JET | •ETE | •ISTTOK<br>•Compass | |

ITER LIDAR
conceptual design

Control and Data acquisition activities build upon Fusion specific needs

# Why xTCA

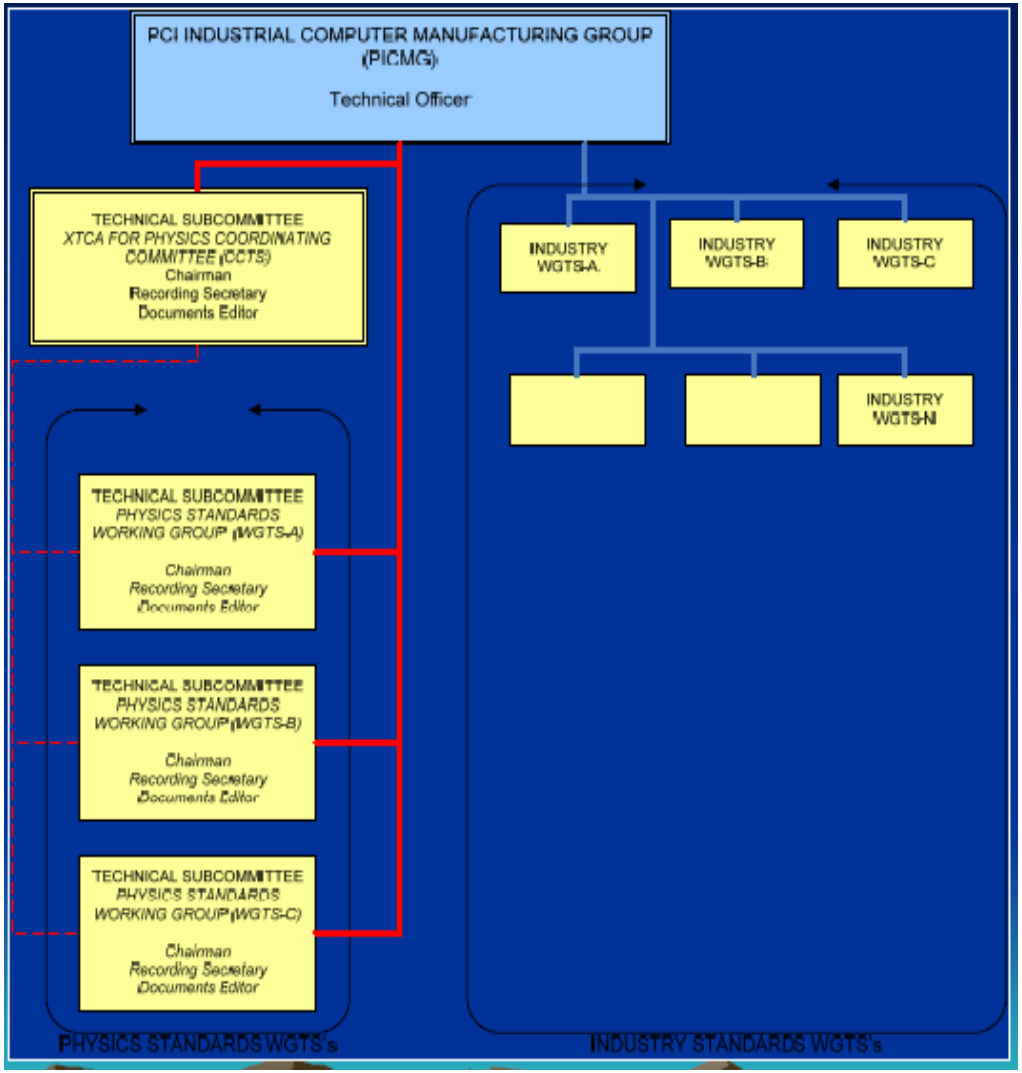
- ATCA 缺点：
  - 高8U，不适合控制用
  - 没有后插板
  - 没有定义子板及信号
  - 没有定义后插板（~~HA~~）
  - 没有控制信号…
- MTCA缺点：
  - 没有后插板
  - 没有定义子板及信号
  - 没有定义后插板（HA）
  - 没有控制信号…
- AMC缺点：
  - 互联？
  - 控制信号
  - 信号管脚定义
  - …




高能所计算节点板

制定新标准：xTCA for Physics

# xTCA for Physics 协议标准委员会




2009年3月10日在PICMG下成立 xTCA for Physics 协调委员会（CCTS）

- IHEP, SLAC, FNAL, DESY 发起单位
- 40多厂商参加
- 选举产生了事务人员
  - 主席：SLAC Ray Larsen
  - 会议秘书：三环公司 Augustus Lowell
  - 文件编辑：高能所刘振安

# xTCA for Physics 大事

- 2007年5月 在FNAL第一次ATCA workshop
- 2007年5月 IEEE RT07 ATCA 专题
- 2008年初讨论建立新标准的可行性
- 2008年10月在Dresden第二次ATCA workshop
- 2008年10月IEEE NSS ATCA 专题
- 2009年5月高能所第三次 xTCA workshop
- 2009年5月高能所 IEEE RT09 ATCA 专题
- 2010年5葡萄牙里斯本 第四次 xTCA workshop
- 2010年5月葡萄牙里斯本 IEEE RT1 xTCA 专题
- 2011年10月在西班牙瓦伦西亚第五次xTCA workshop
- 2011年10月在西班牙瓦伦西亚NSS/MIC xTCA 专题
- 2012 Berkeley/2013 Desy/2014 奈良研讨会

# CCTS的路线图

- 组织工作组每周二开技术讨论电话会
- xTCA for physics
  - Extensions to specifications 协议文本的起草
  - Guidelines 设计指引
  - Open source solutions 开源软件的编制
  - Building on existing xTCA base under PICMG rules 依照PICMG规则构建xTCA骨架
  - Spec approval by PICMG membership PICMG成员验收
  - Collaborating with industry for product development & support 工业界的密切合作

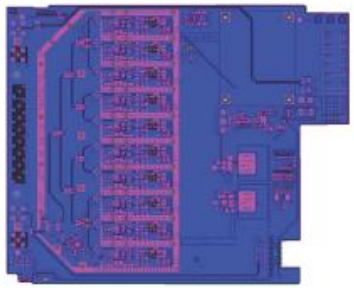
# xTCA 技术协调委员会月会

xTCA Coordinating Committee Meeting Agenda
Jul 30, 2015 0700-0800 Pacific Daylight – Live Meeting

1. Call to Order – Chair Ray Larsen
   a. PICMG Patent Call – Secretary Gus Lowell
   b. Roll Call, member changes since last meeting – Secretary
   c. Approval of Minutes of last meeting – Secretary
2. Review of Purpose & Scope of Coordinating Committee – Chair Ray Larsen
3. 3-slide reports from Technical Subcommittees
   a. Hardware WG (Timing, Synchronization & IO) – Chair Robert Downing
      SOW-Roadmap-Progress
   b. Software WG (Interoperability, high availability guidelines) – Chair Stefan Simrock
      SOW-Roadmap-Progress
4. 1-slide reports from Lab members
   a. DESY
   b. FNAL
   c. IHEP
   d. IPFN
   e. ITER
   f. CERN
   g. SLAC
5. 1-slide reports from Industry
   - Submit single slides in advance to larsen@slac.stanford.edu
6. 1-slide report from PICMG, MTCA Summit etc
7. New Business
8. Next Meeting Topic Suggestions
9. Motion to Adjourn

# 德国汉堡DESY进展

## Status Report DESY



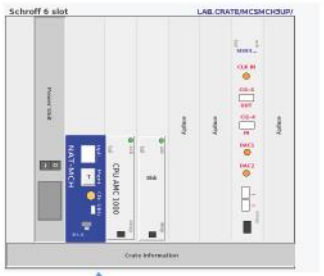
Two AMC's ready:
Full MTCA.4 specs

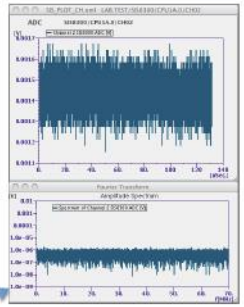
µRTM's:
RF receiver: soldering
Test board for optical fibers: ready
Pulse shaper: in production

Next step:
IPMI software for µRTM

28. Oct. 2010 Kay Rehlich, DESY

## Status Report DESY (2)





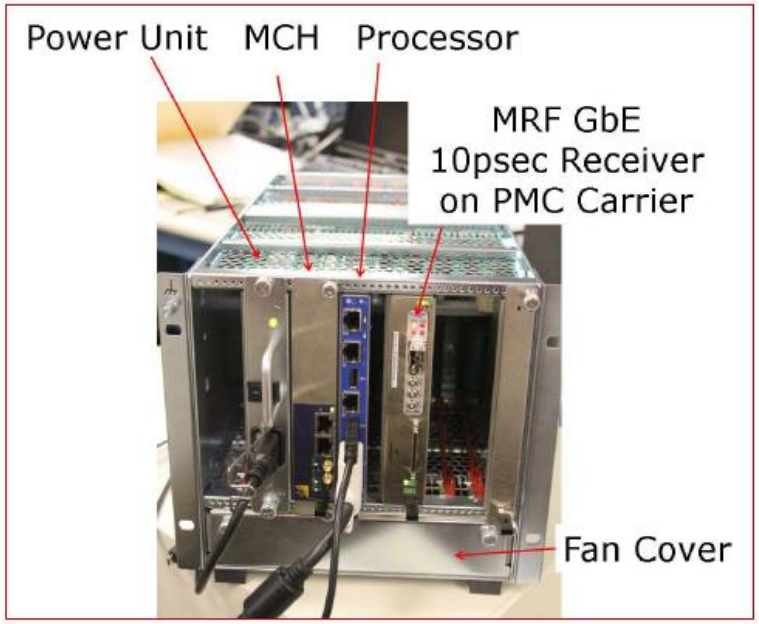
JAVA application to
Display management data
and control system integration.

Two shelfs according
to MTCA.4 operational


28. Oct. 2010 Kay Rehlich, DESY

# 美国SLAC进展

## MTCA.4 Development Platform (SLAC)




MTCA.4 platform proposed for major SLAC Linac controls upgrade

Interim Timing System

- Micro-Research PMC Event Receiver (EVR) on double M
- LSST- Large Synoptic Survey Telescope
-
- ba
- us
- Sy
-
- Sc
- wi
- tir

Note – RTM I/O Connector Area designed prior to PICMG 3.8 Spec

Generic Massively Parallel Processor & Hub Switcher 0.5 Tb/s Throughput System
10 Gbps Channels – *Courtesy M. Huffer, SLAC*

SLAC xTCA Update - R. Larsen 102

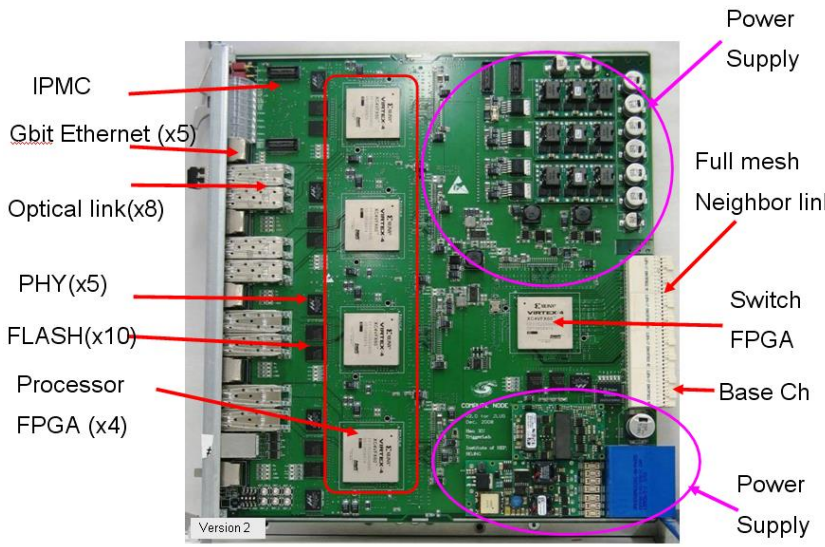
SLAC xTCA Update - R. Larsen 102810

6 PICMG

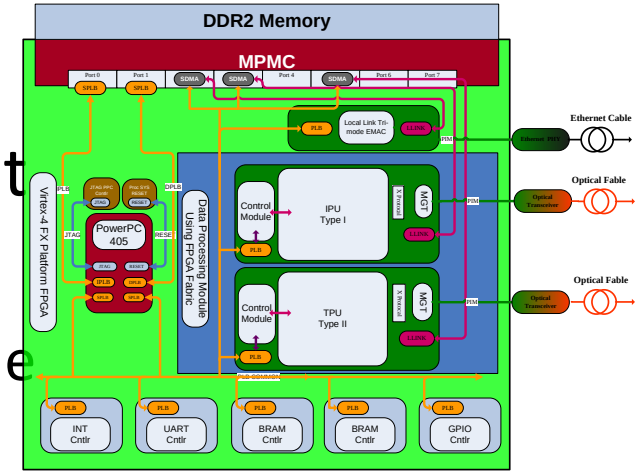
# Ongoing XTCA Development at IHEP

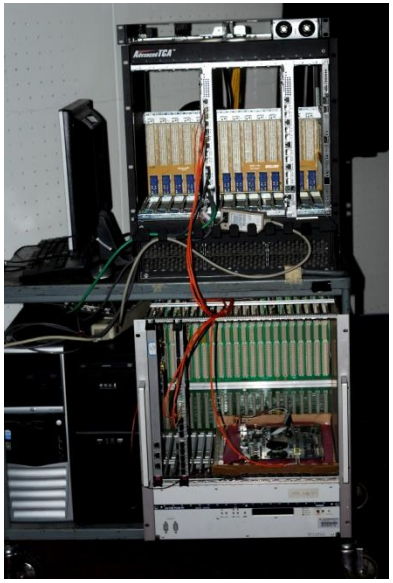
- DAQ R&D for PANDA at GSI, Germany
  - Ver.2 of Computer Node (CN,ATCA) successful
  - Demo system established
  - Moving to XTCA( xTCA Carrier + AMC)
- PXD/DAQ design for Belle II at KEK, Japan
  - XTCA Carrier (layout)
  - AMC with FPGA+4G Memor
- R&D for LUMI at IHEP, Chin
  - newdesign

# Ongoing XTCA Development at IHEP

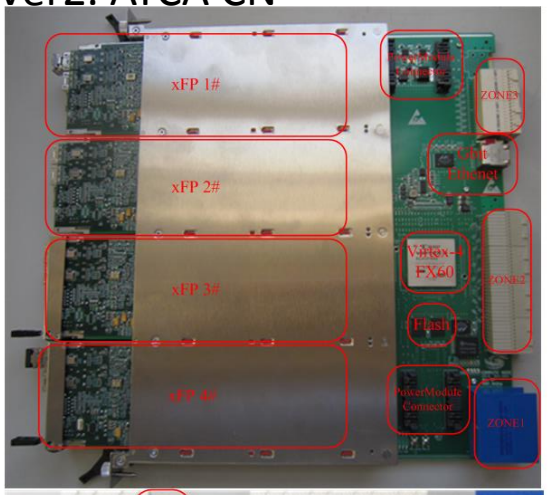



Ver2. ATCA CN



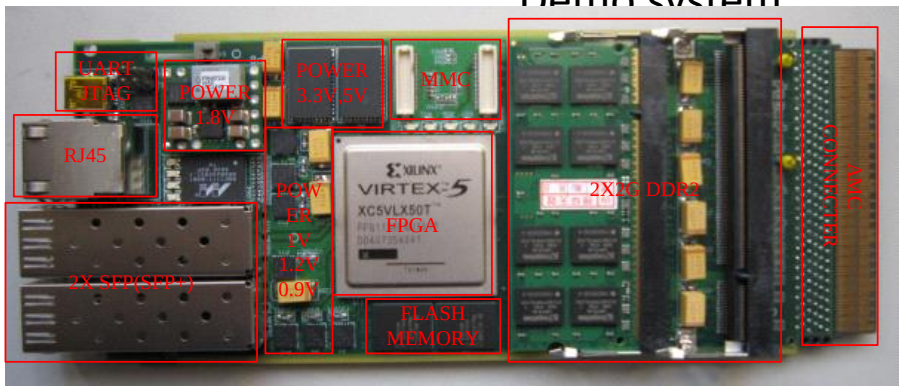



Demo system





AMC

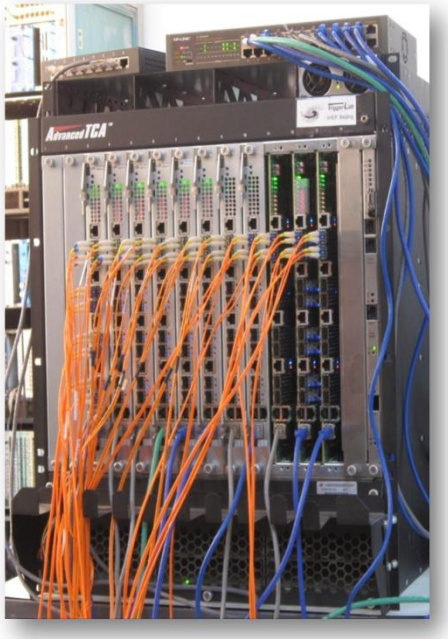


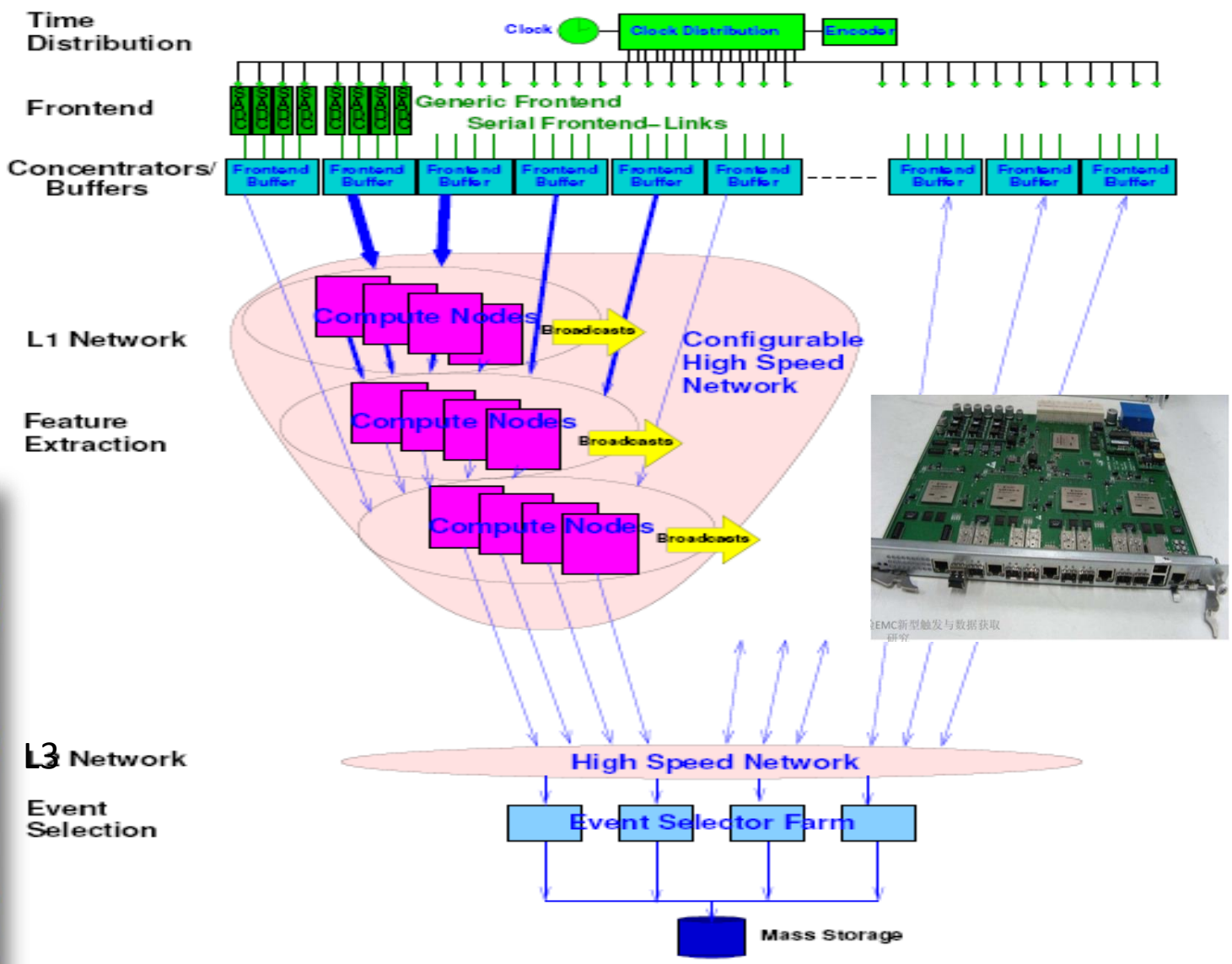

XTCA Carrier with AMC

参见其他报告

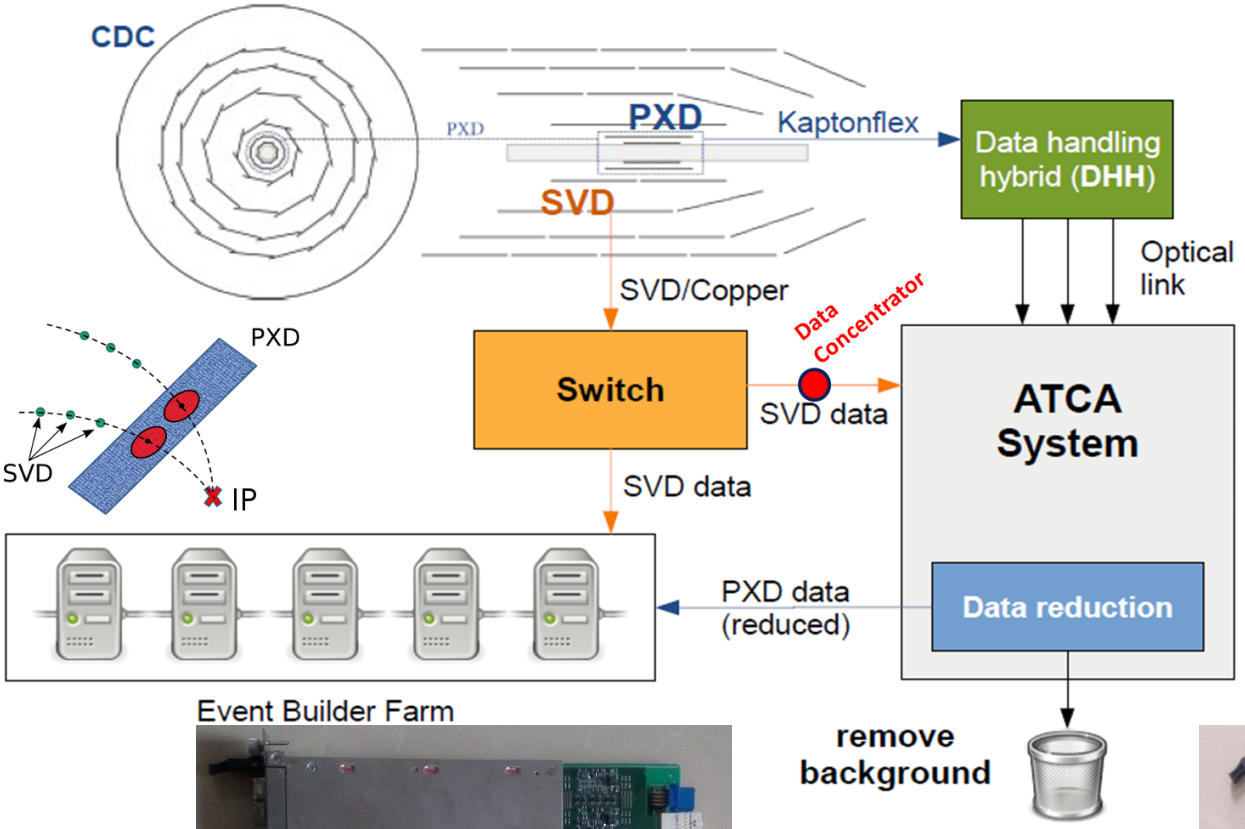
# 范例5 Application in PANDA TDAQ

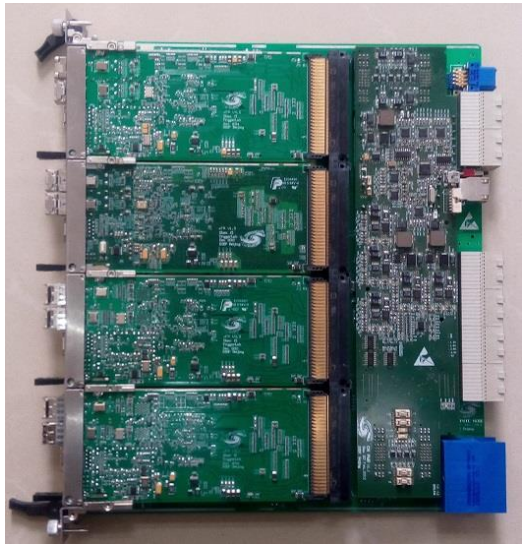
- Compute Node in ATCA, later in xTCA





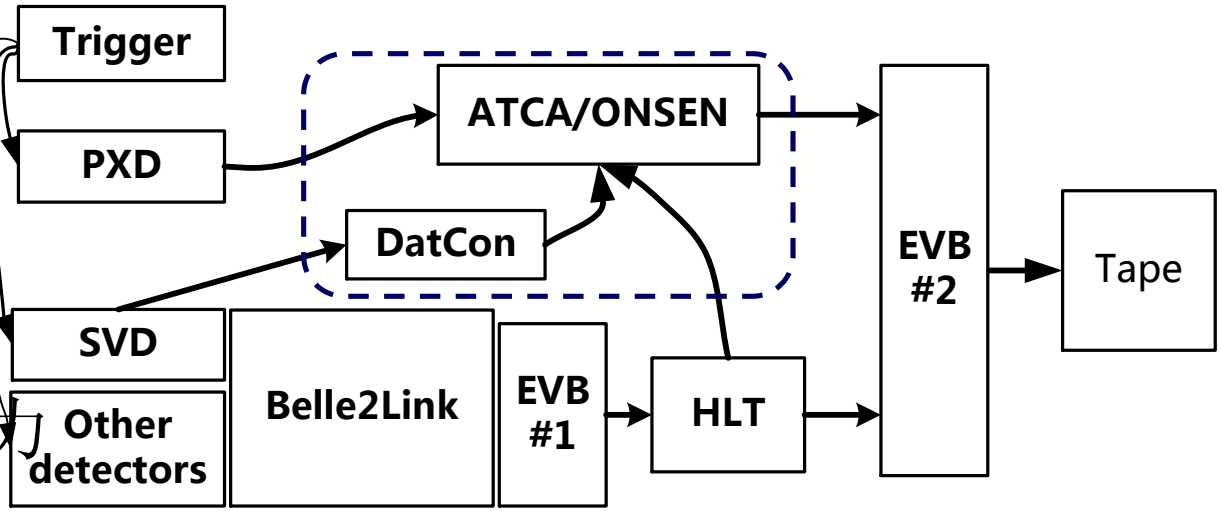
# 范例6 Belle II/PXD 触发数据压缩算法原理

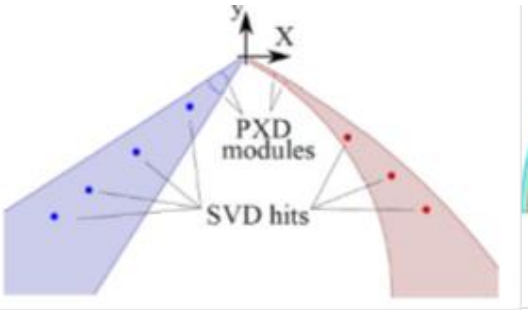


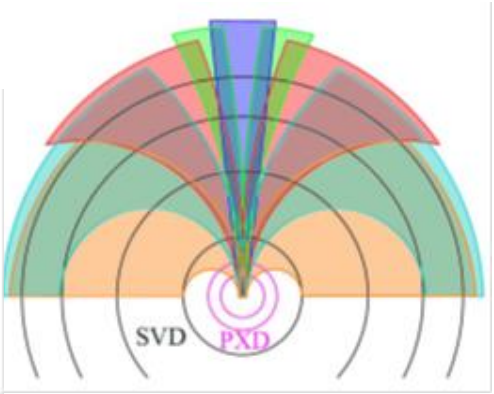



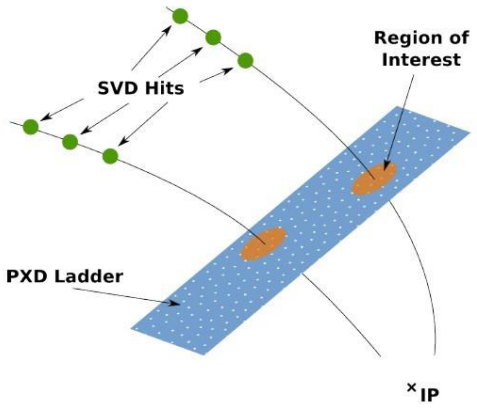
# 研究方案 2

- DEPFET数据获取（压缩）方案
  - 基于硬件触发
  - 利用SVD数据
  - 径迹反推
  - 寻找ROI
  - 提取数据
- 难点
  - 强大实时计算能力
  - 算法
  - 5秒大存储



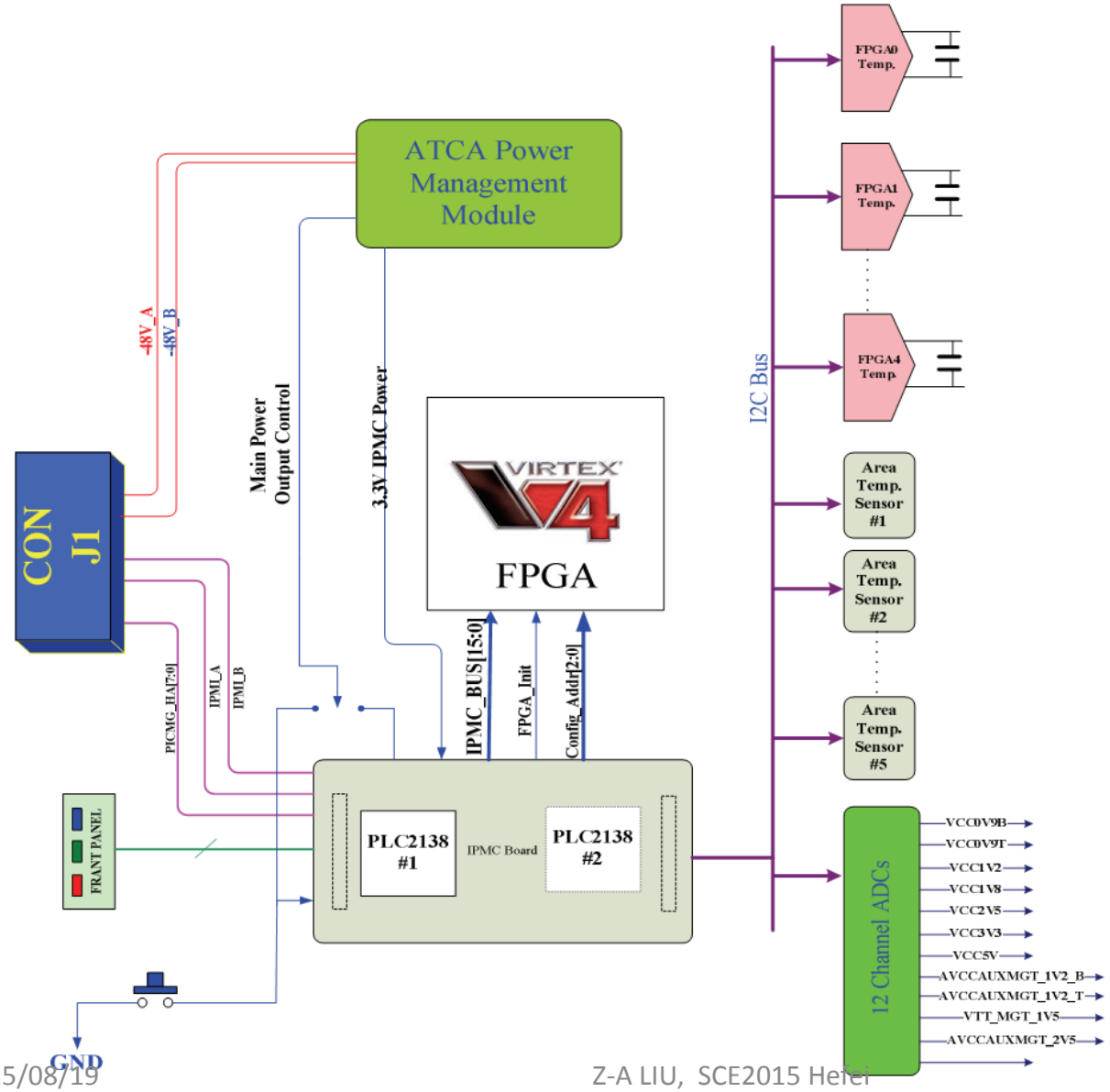



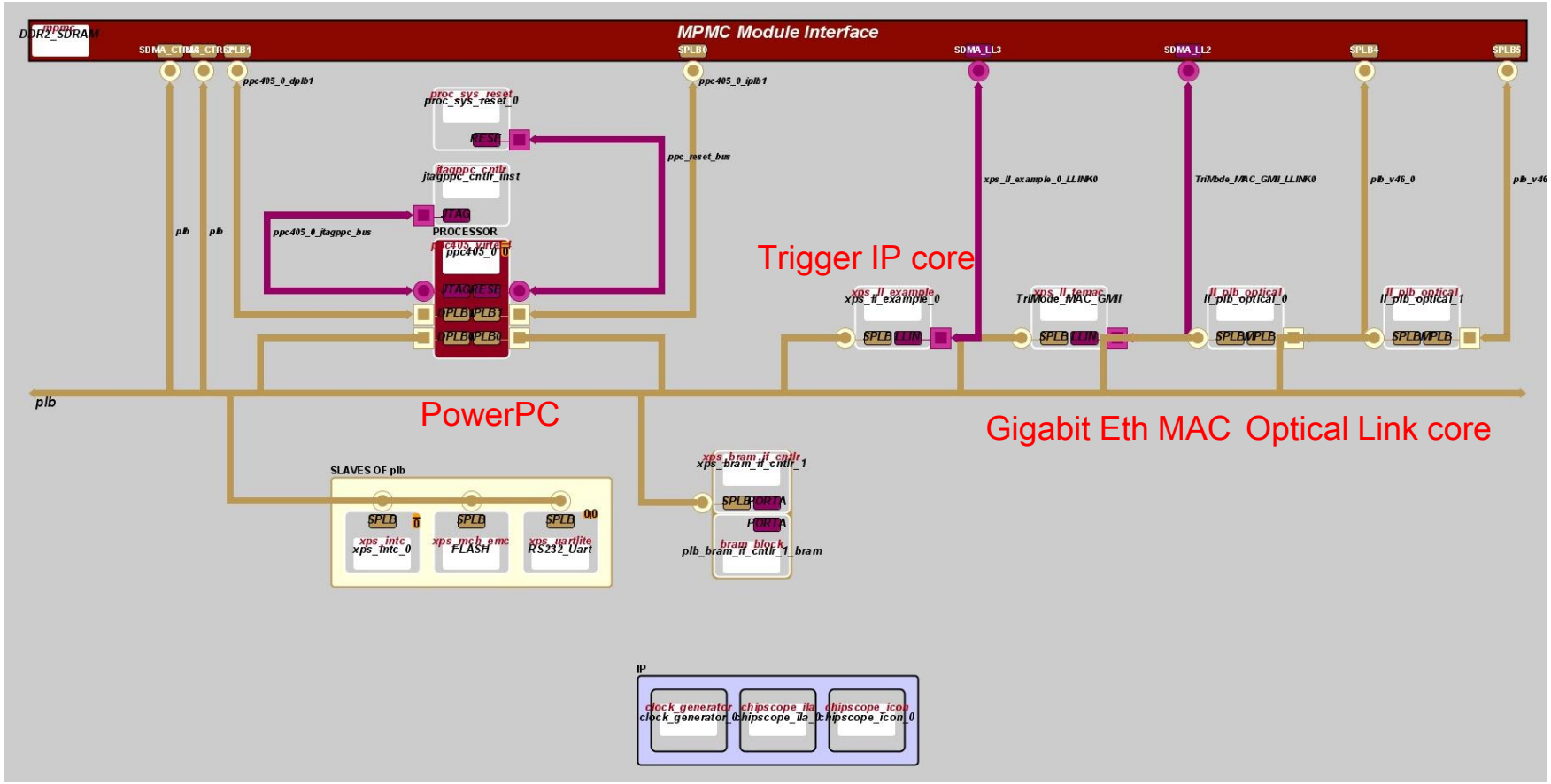
# 三。FPGA 算法实现

# 通用硬件平台—计算节点



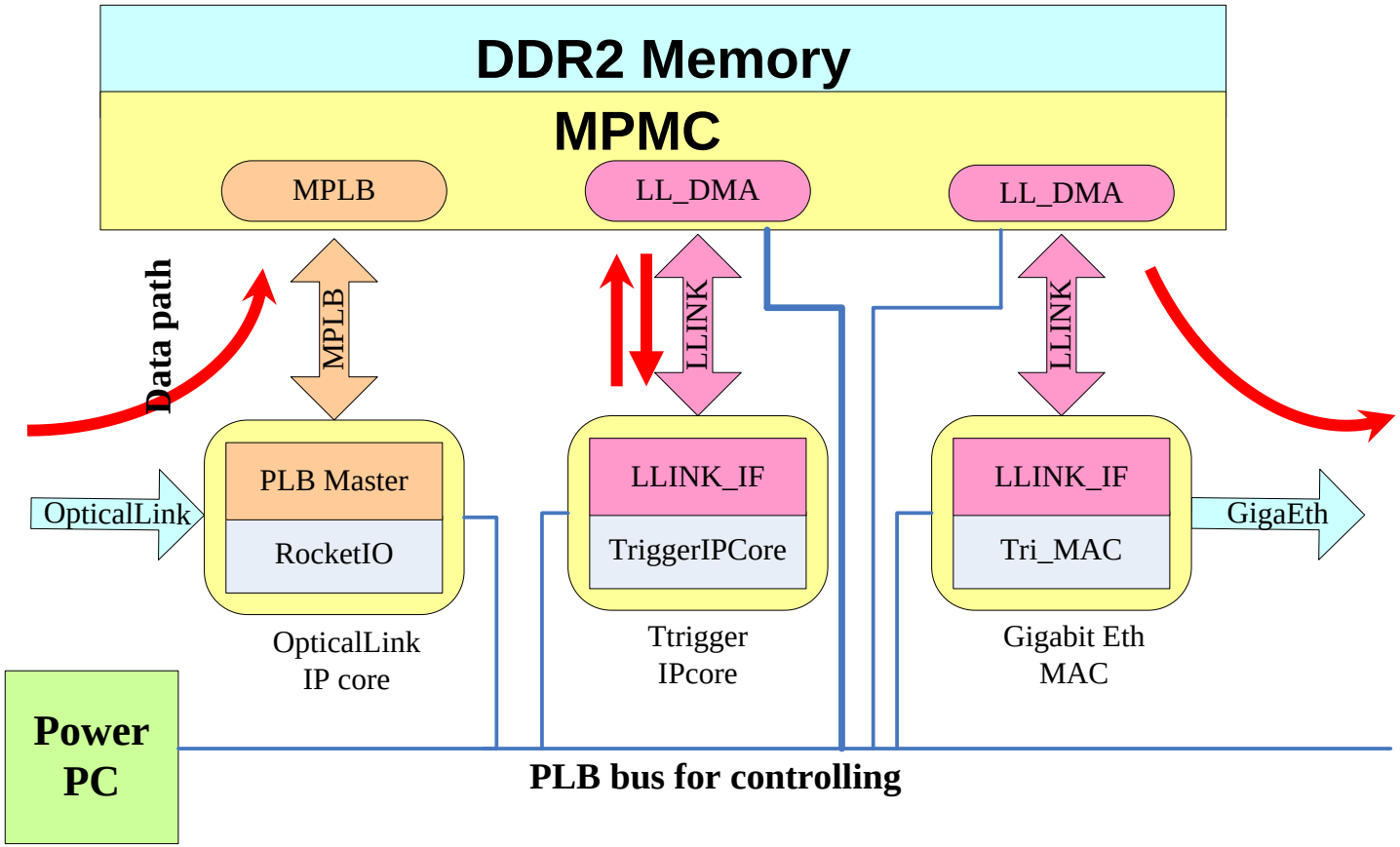

- 板级监测
- 控制管理

# System on Programmable Chip



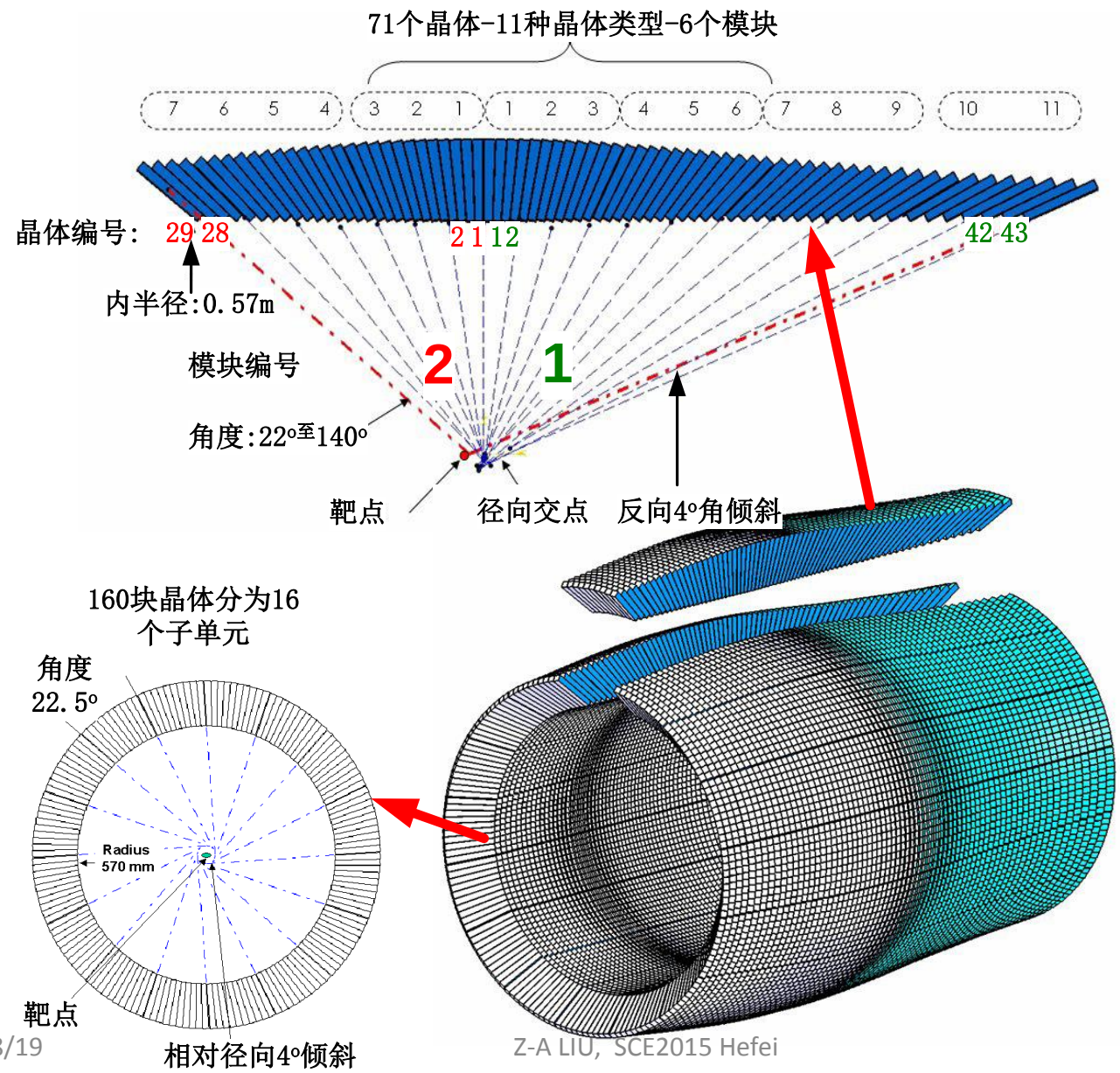

- 基于Xilinx FPGA内嵌的PowerPC硬核和一些开源的IP和构建一个通用的硬件系统,移植开源Linux来实现系统管理以及UDP/TCP 协议栈的处理
- 在线触发算法设计成专用IP核以及基于多端口内存控制器实现片上数据交换模块

# 数据流的问题




- 从高速光口接收到的粗数据在DDR2内缓存（通过PLB主设备：低延时，高带宽）
- 数据从DDR2发送到触发算法IP核以及处理结果写回DDR2（通过LocalLink DMA设备，更加灵活，高带宽）
- 结果通过Gigabit Ethernet送出（通过UDP/TCP，标准设计）

# EMC探测器

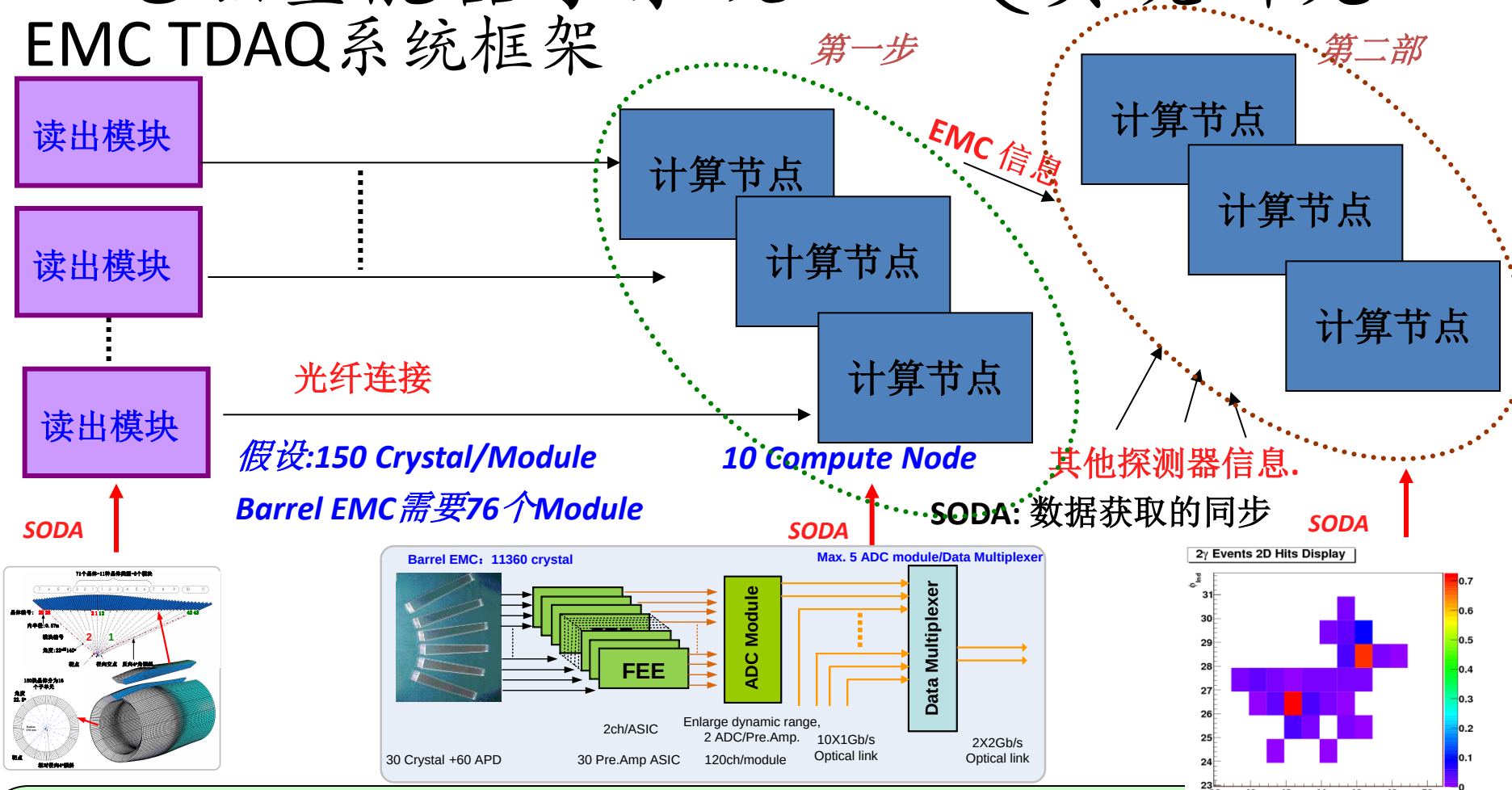



**Barrel EMC:**

**11360块晶体**

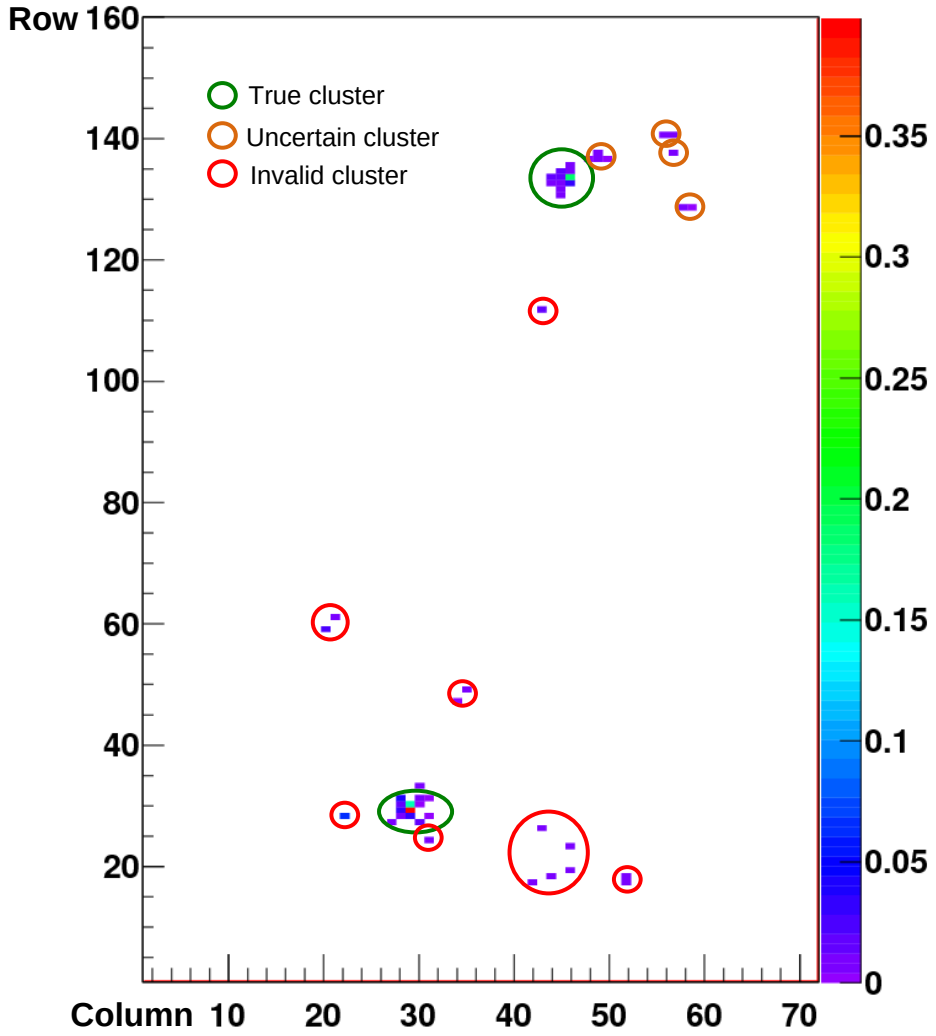
# 电磁量能器子系统TDAQ实现研究

- EMC TDAQ系统框架

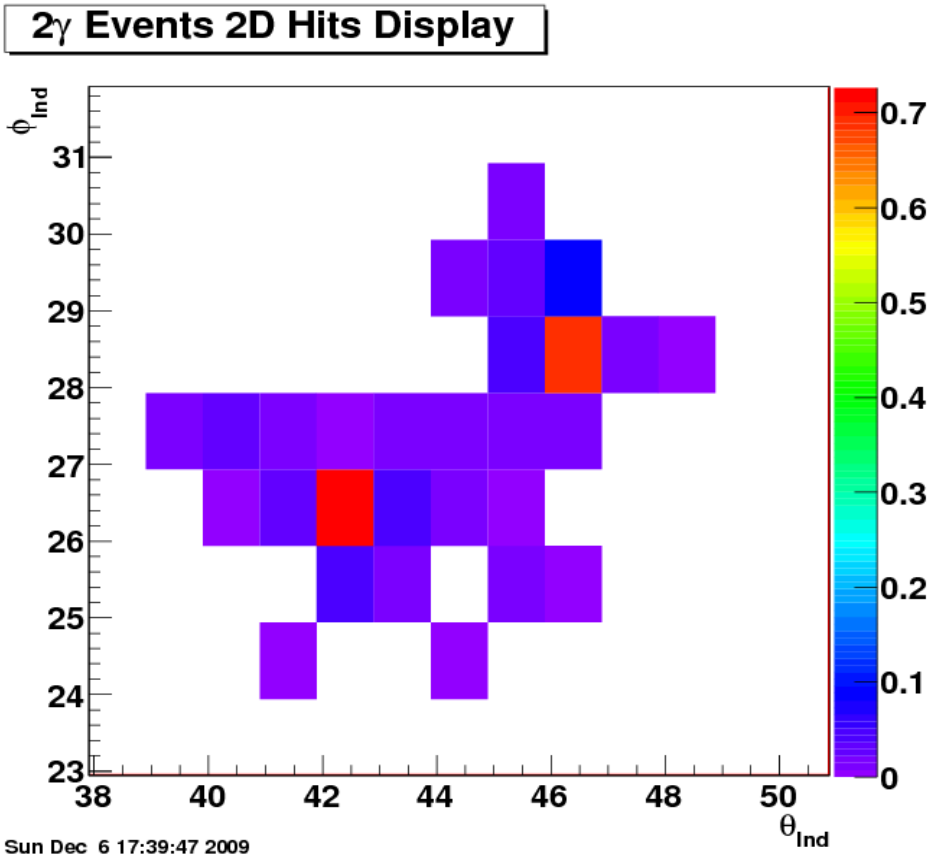



| 任务 | | 结果 |
|---|---|---|
| 1. 信号特征提取(时间, 幅度)<br>2. 数据零压缩 | 1. 簇团寻找<br>2. 簇团特征提取<br>3. 模式识别 | 1. 相关性<br>2. 物理参数计算<br>3. 事例组建 | 在北京完成了功能验证测试,PANDA合作之TDAQ第一个系统,成为了其他系统设计的样板 |

# 簇团重建需要解决的问题



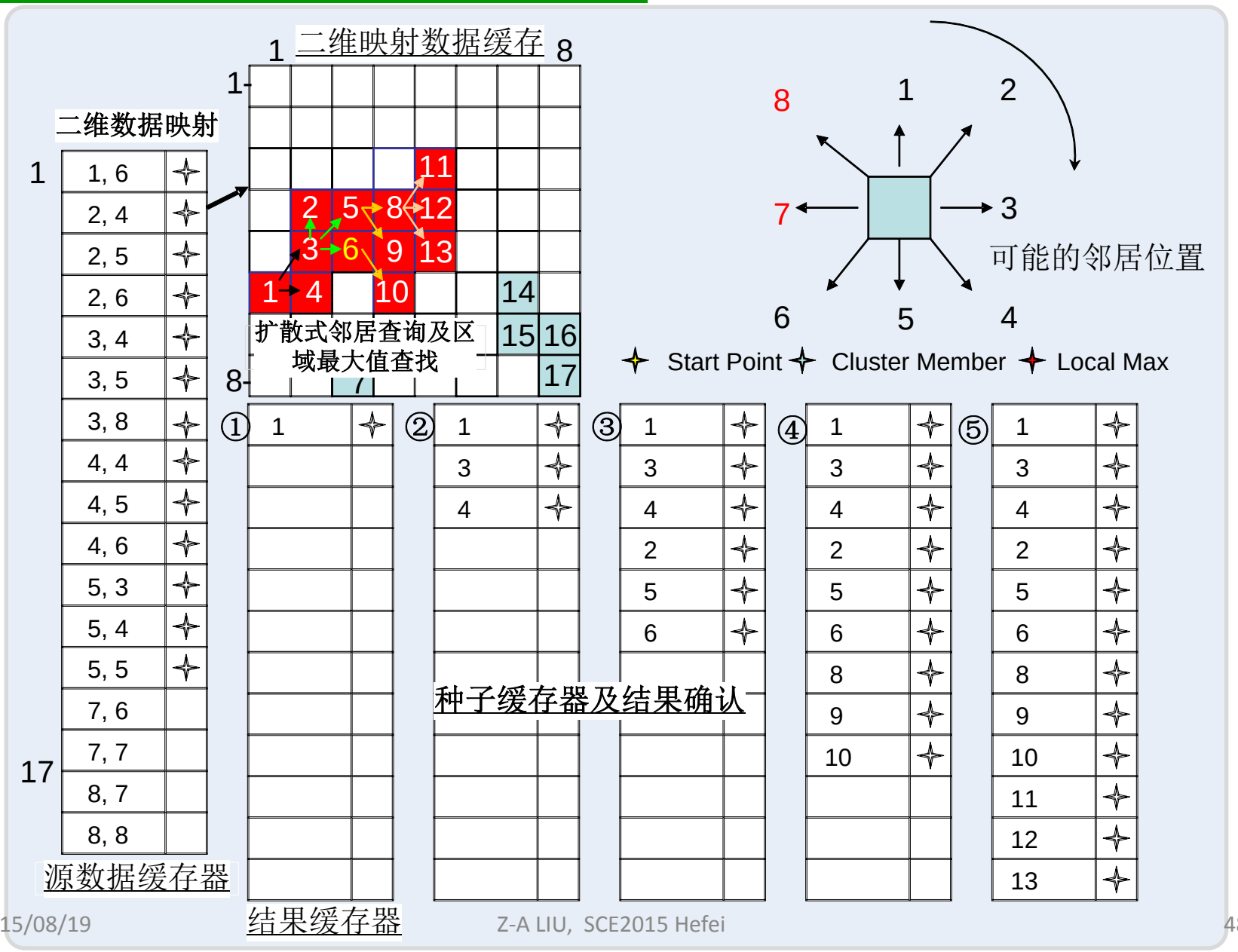

- 簇团查找




- 重叠簇团的处理
- 重建簇团信息:能量,位置

- 在线簇团重建：速度，效率

# 二维簇团查找算法


二维映射数据缓存
二维数据映射
扩散式邻居查询及区域最大值查找
可能的邻居位置
Start Point
Cluster Member
Local Max
种子缓存器及结果确认
源数据缓存器
结果缓存器

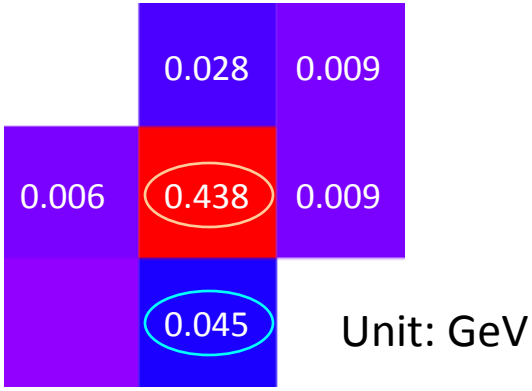
# 寻找区域最大值

为了避免找到假的区域最大值，需要选择更加严格的判选条件

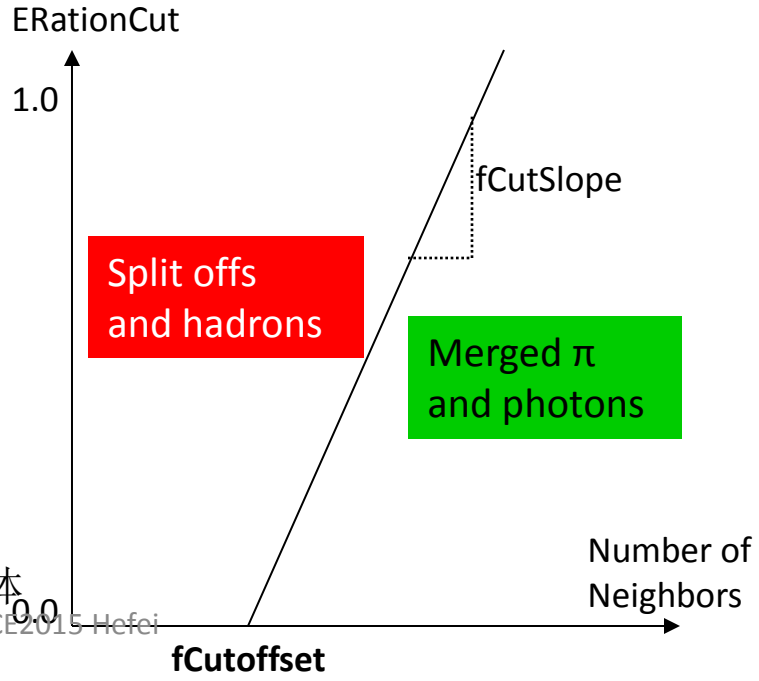
- ✓ Eseed>20MeV
- ✓ ERatio<ERatioCut

$$ERatio = \frac{MaxEofNeighbors - fERatioCorr}{MaxE - fERatioCorr}$$

$$ERatioCut = fCutSlope \times (NumberofNeighbors - fCutoffset)$$



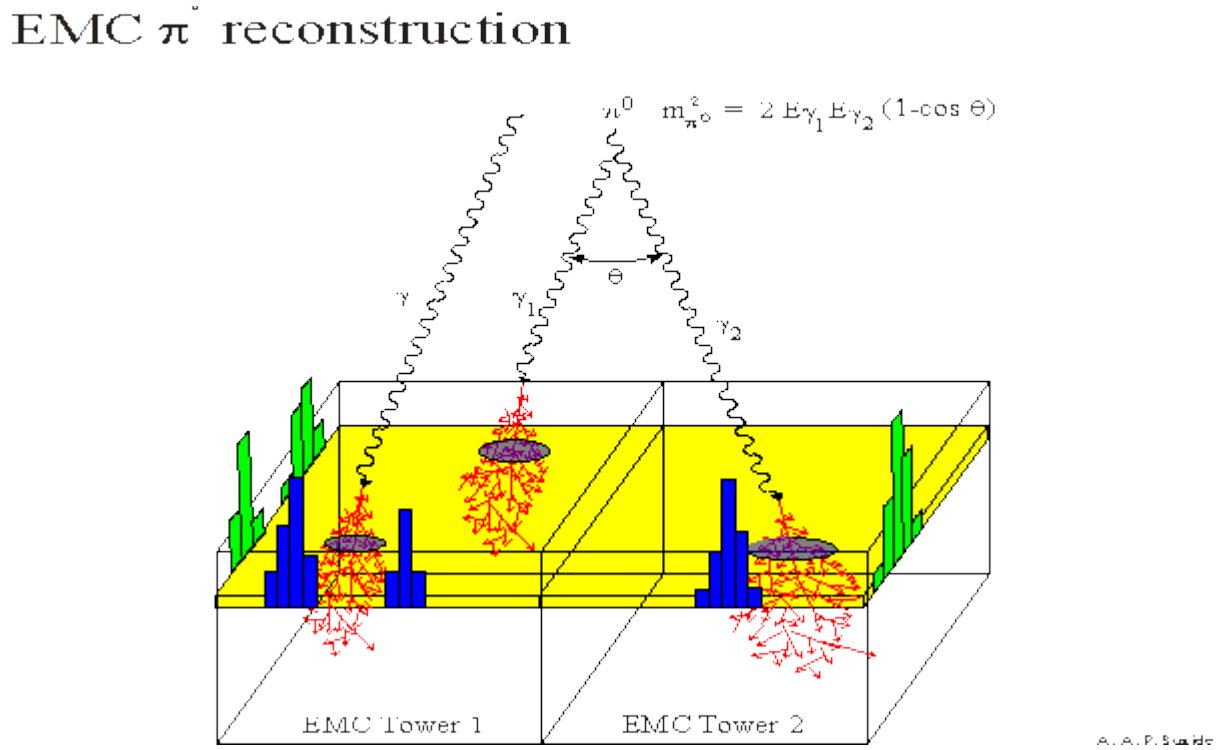

Unit: GeV




一个模拟的簇团有一个区域最大值以及6个相邻晶体

# 簇团位置计算

- 带电粒子必须提供簇团位置来与径迹探测器做匹配；
- 光子位置重建准确性对 $\pi_0$ 质量的重建影响特别大；




$$Wi = Ei$$

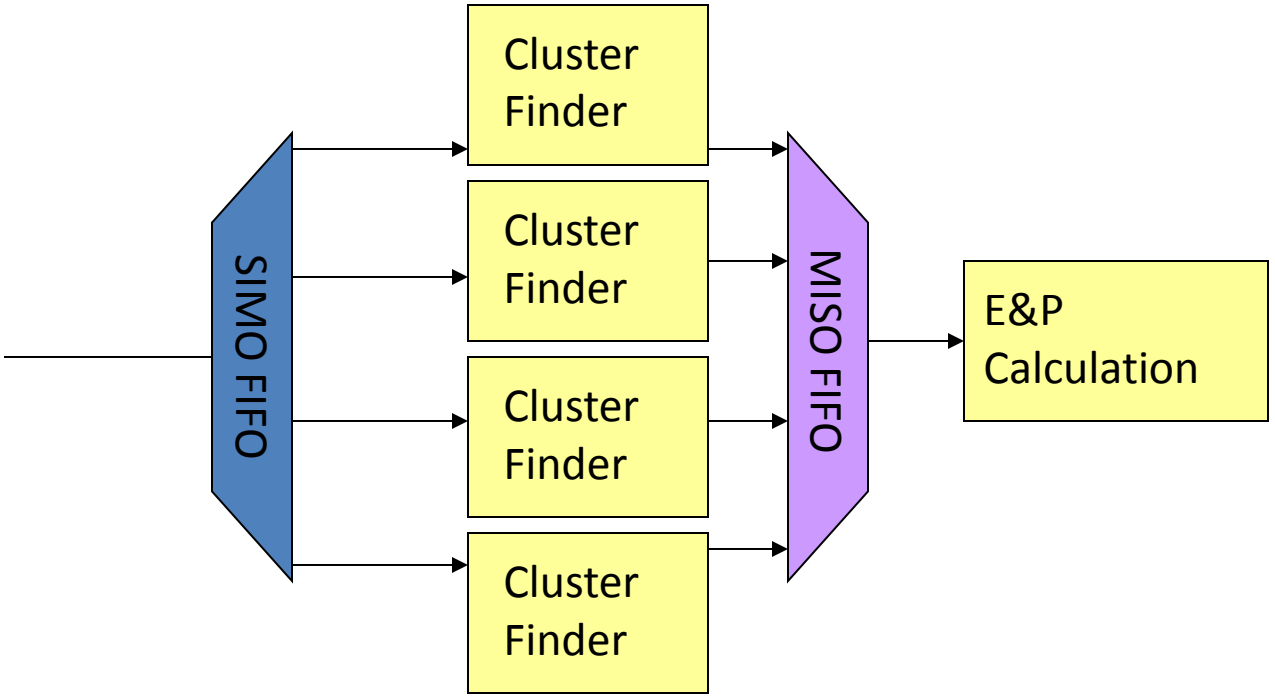
$$Xcal = \frac{\sum_i Wi * Xi}{\sum_i Wi}$$

权重

线性权重位置计算

# 适合V4Fx60 FPGA的设计

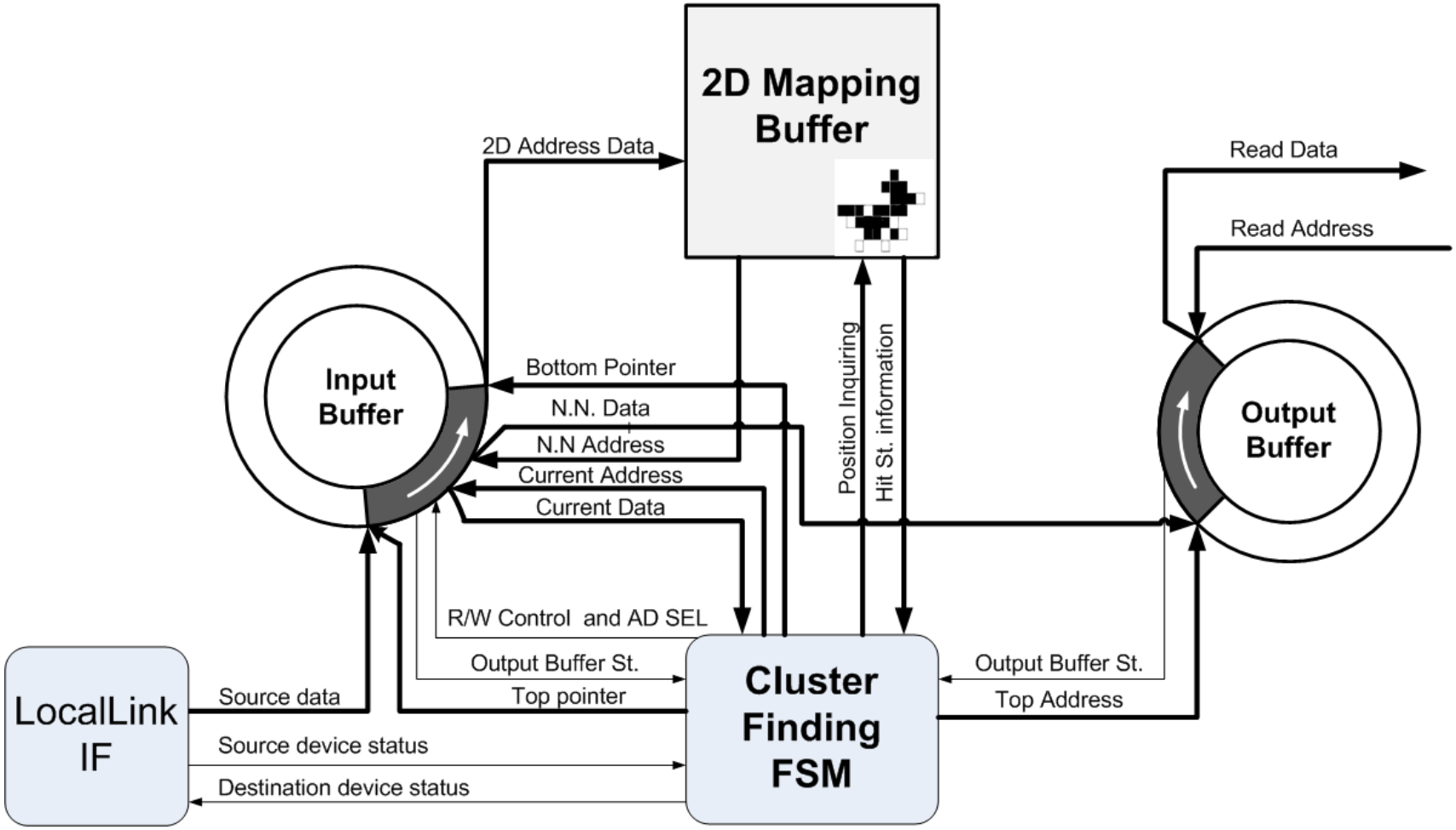
- 能量/位置计算模块速度较快，能完全流水线运行
- 从资源使用量上看，这是最优的配置



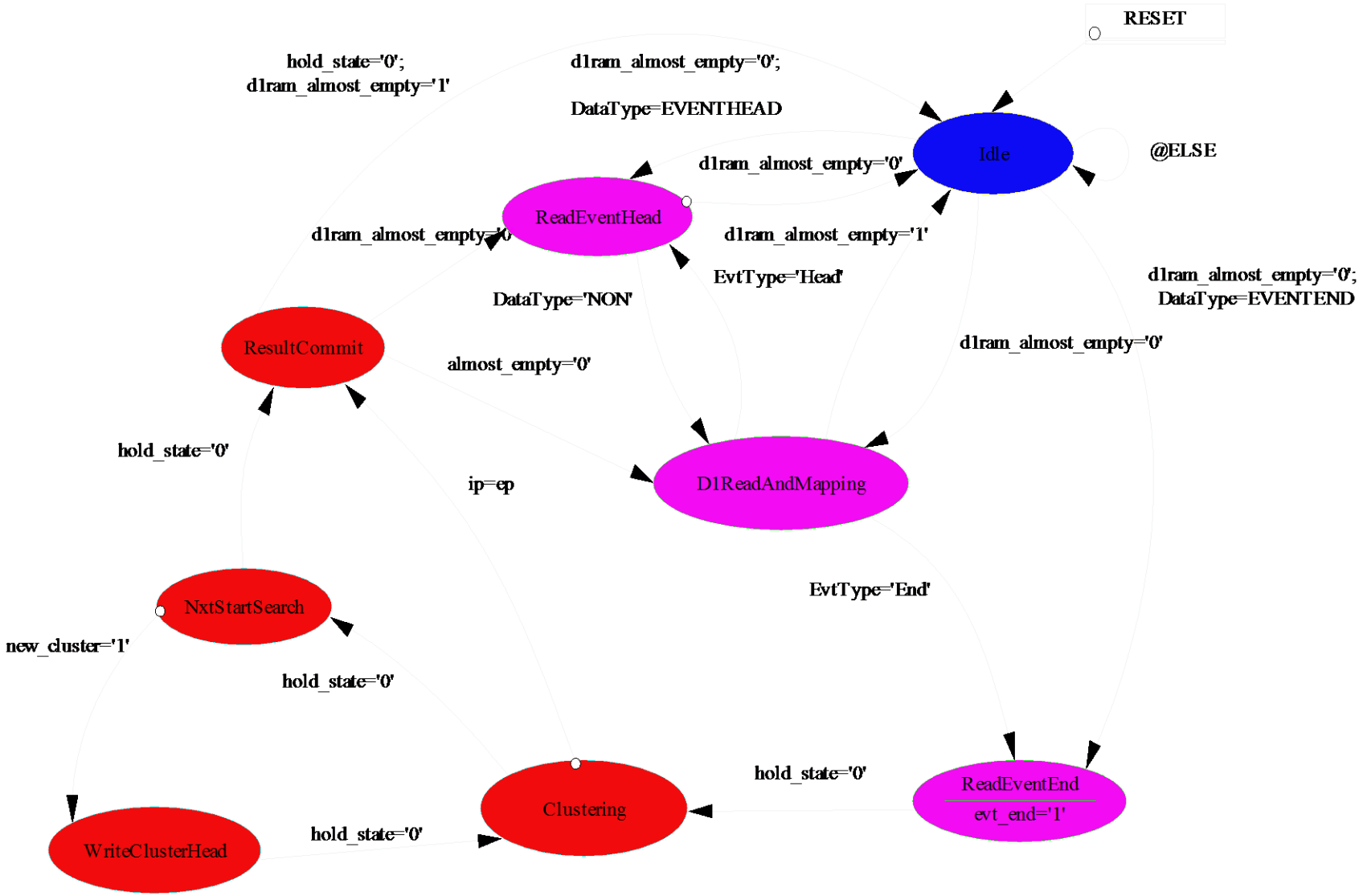

- 4 Cluster Finder + 1 Energy and Position Calculation

400KHz Events/FPGA=>1.6MHz/CN

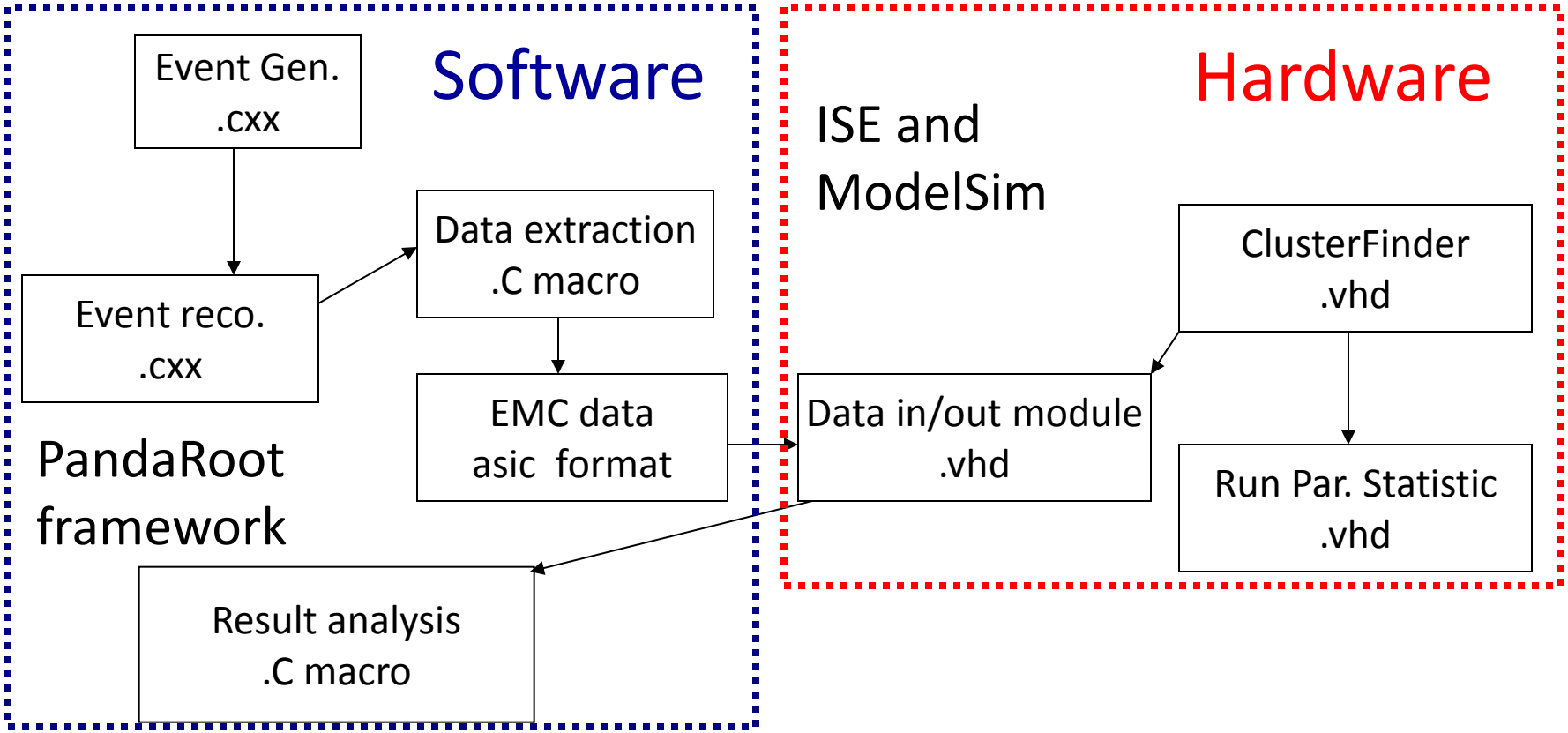
# Cluster Finder 模块框图



# 簇团查找有限状态机


RESET
Idle
@ELSE
ReadEventHead
hold_state='0';
d1ram_almost_empty='1'
d1ram_almost_empty='0';
DataType=EVENTHEAD
d1ram_almost_empty='0'
d1ram_almost_empty='1'
EvtType='Head'
DataType='NON'
d1ram_almost_empty='0';
DataType=EVENTEND
ResultCommit
almost_empty='0'
d1ram_almost_empty='0'
hold_state='0'
ip=ep
D1ReadAndMapping
EvtType='End'
NxtStartSearch
new_cluster='1'
hold_state='0'
hold_state='0'
ReadEventEnd
evt_end='1'
Clustering
hold_state='0'
WriteClusterHead

# 逻辑验证方法


Software
Hardware
Event Gen.
.cxx
Event reco.
.cxx
Data extraction
.C macro
EMC data
asic format
PandaRoot
framework
Result analysis
.C macro
ISE and
ModelSim
ClusterFinder
.vhd
Data in/out module
.vhd
Run Par. Statistic
.vhd

# 总结

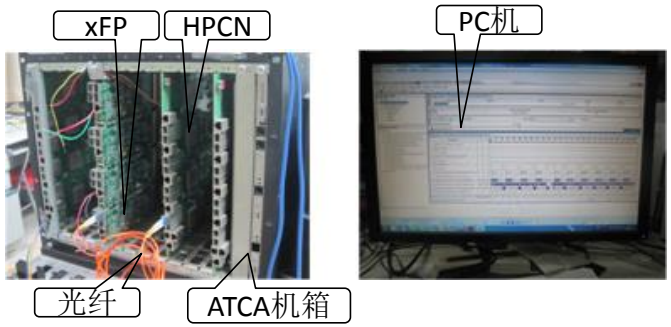
- 本报告简介电子学在与计算技术相关的发展
  - 高速数据传输与互联
  - 新型互联架构
  - FPGA算法实现
- 这些国际领先的技术及应用案例都是高能所发展的，并在国际合作项目中得到应用

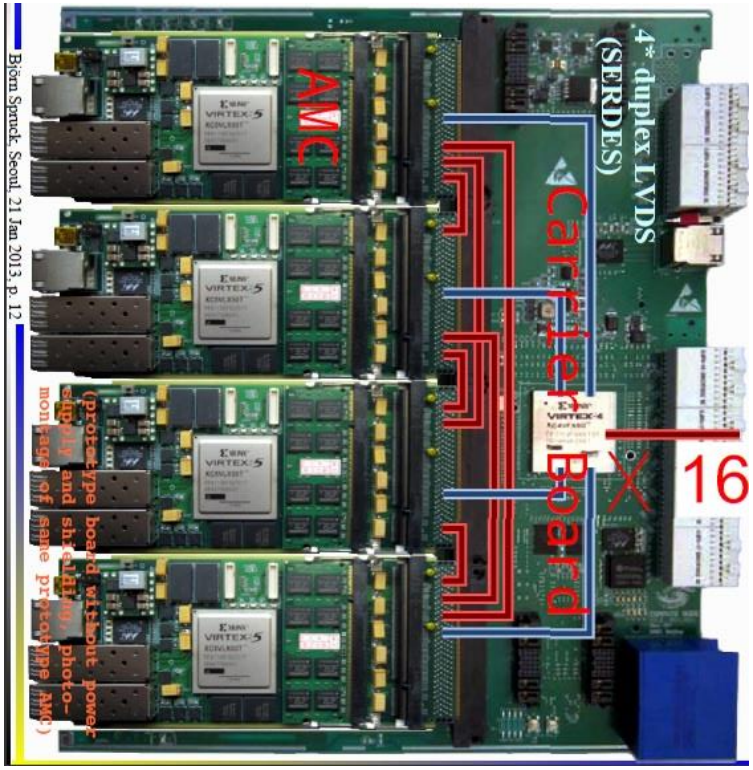
谢谢！

# 备用

# 研究方案 2 （续）

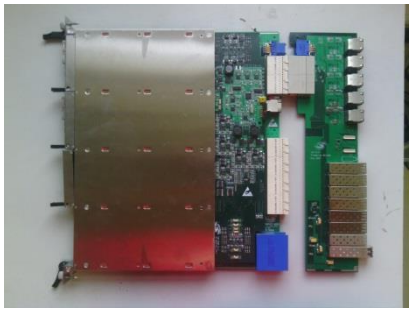
- ONSEN
  - 软件
  - 硬件
    - 1 ATCA 机箱(采购)
    - 2 机箱管理器(采购)
    - 1 电源(采购)
    - 10 计算节点CN(研建)
      - 1 个ATCA 载板
      - 1 个电源板
      - 4 个 xFP/AMC板
      - 5 MMC 智能管理子板



PXD for BELLE - II
DEPFET Collaboration
design and mockup by
MPI Munich
backward
forward
Red Bull
ENERGY DRINK

# Development of MTCA/xTCA/ATCA based instrumentation for particle physics at IHEP



PICMG®

TIPP2014

Amsterdam, Netherland, June 2-7 2014

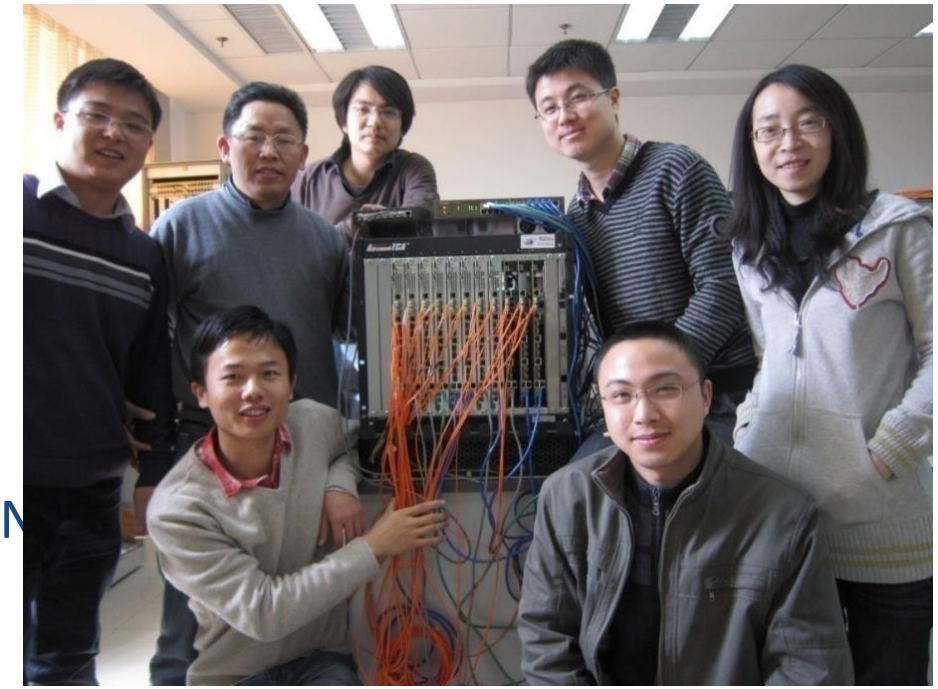

Zhen-AN LIU

TrigLab/IHEP Beijing

Member & Officer PICMG/xTCA for Physics Committee

# Outline

- Overview of xTCA for Physics
- Activities in IHEP/TrigLab
  - ATCA complaint
  - MicroTCA complaint
  - xTCA complaint
  - IPMC and MMC
- Applications
  - PANDA TDAQ
  - BESIII Luminosity Readout
  - Belle II PXD-DAQ/SVD-DACON
  - TREND FEE and Readout
  - LLRF R&D
  - CMS Mu Trigger concentrator
- Summary

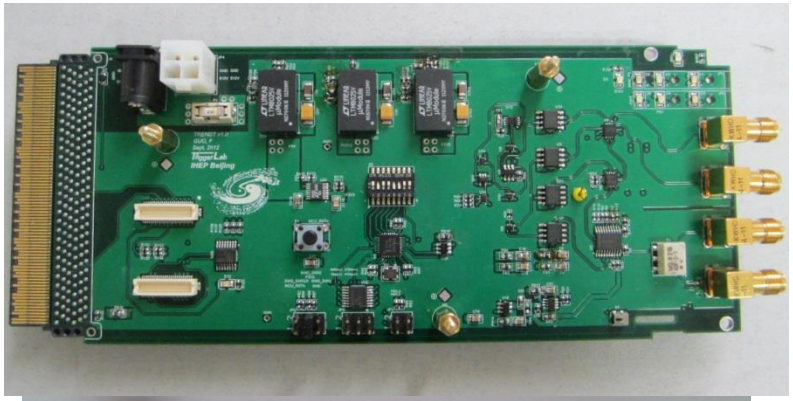


# xTCA workshops

- International Linear Collider, XFEL
  - 2004 - ATCA, MTCA intro paper NSS-MIC, Rome
  - 2005 – ILC Snowmass Conference + Availability Workshop @ Grömitz on ATCA for *high availability*
  - 2007 – 1st xTCA workshop, IEEE RT2007 Fermilab
  - 2008 – 2nd xTCA workshop, IEEE NSS-MIC Dresden
  - 2009 –xTCA for Physics subcommittees formed under PICMG open source telecom standards ~200 vendors
  - 2009 – 2013 - IEEE Workshops 3-6 at Beijing, Lisbon, Valencia, Berkeley, DESY (1st & 2nd DESY workshops)
  - 2014 - 7th Annual IEEE Workshop Nara Japan last week, 3rd DESY workshop Dec. 2014

# Activities in IHEP/TrigLab-MicroTCA

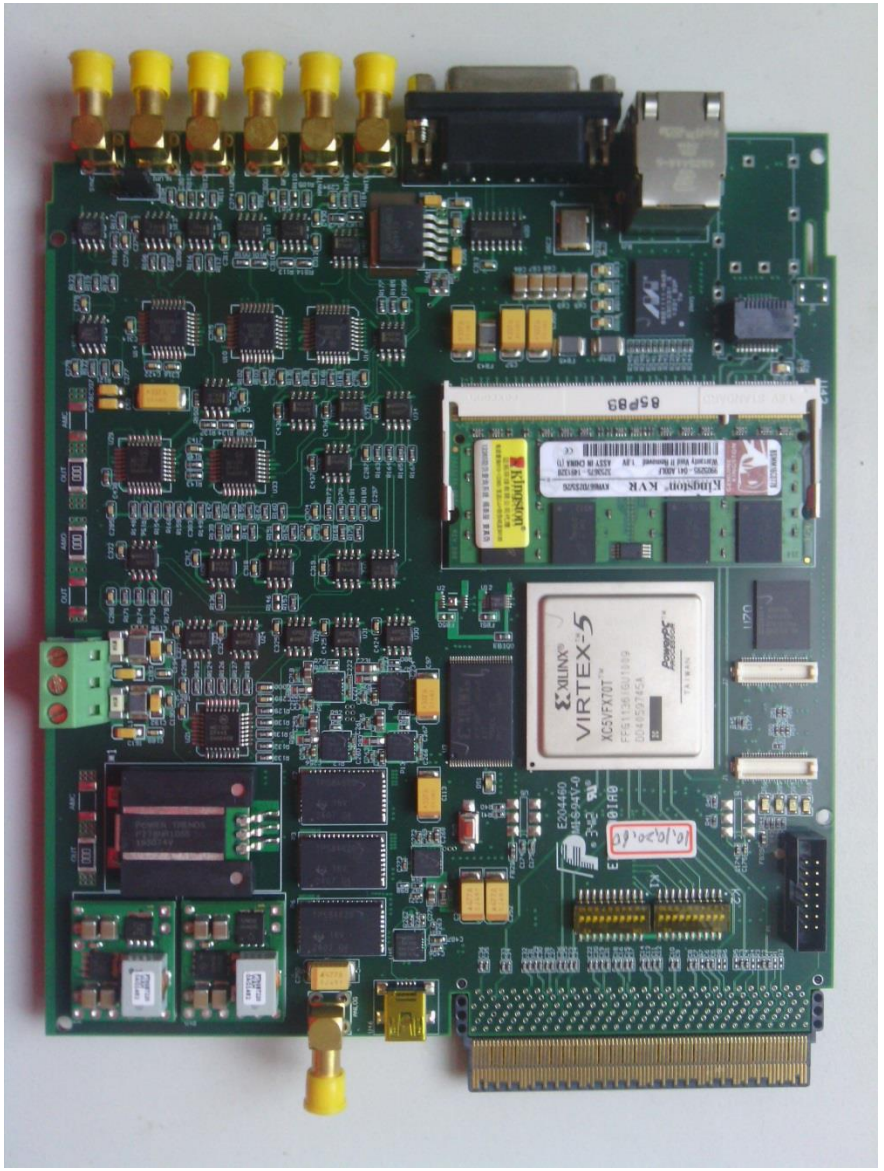
- Single Width AMC
  - Type 1 for trigger
    - Discriminators
  - Type 2 for CN
    - Virtex 5 XC5V50T
    - 4GB DDR2
    - 1 Ethernet
    - 2 SFP(3 Gbps)
  - Type 3 for DATCON
    - Virtex 5 XC5V70T
    - 4GB DDR2
    - 1 Ethernet
    - 4 SFP+(6.4 Gbps)





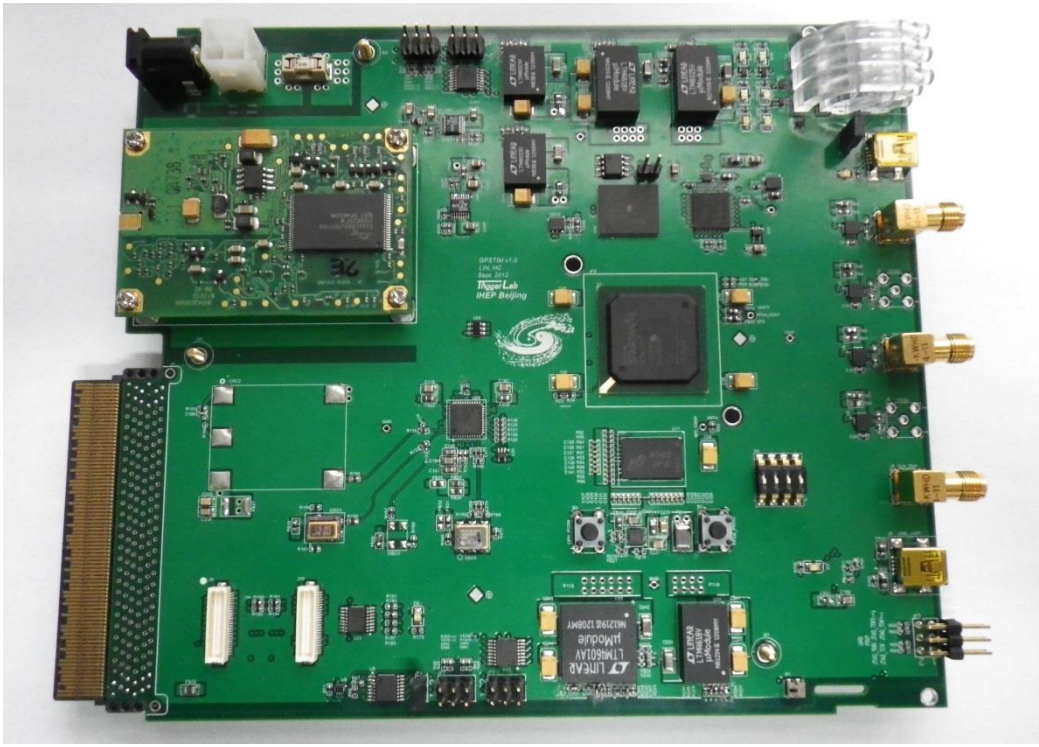
# Activities in IHEP/TrigLab-MicroTCA

- Double Width AMC
  - Type 1 for LumiMonitor
    - Up to 6 Signal inputs
    - 2 delayed signal/clock
    - Virtex 5 XC5V70T data processing
    - 2GB DDR2 data buffer
    - 1 Ethernet output
    - 1 SFP(3 Gbps)



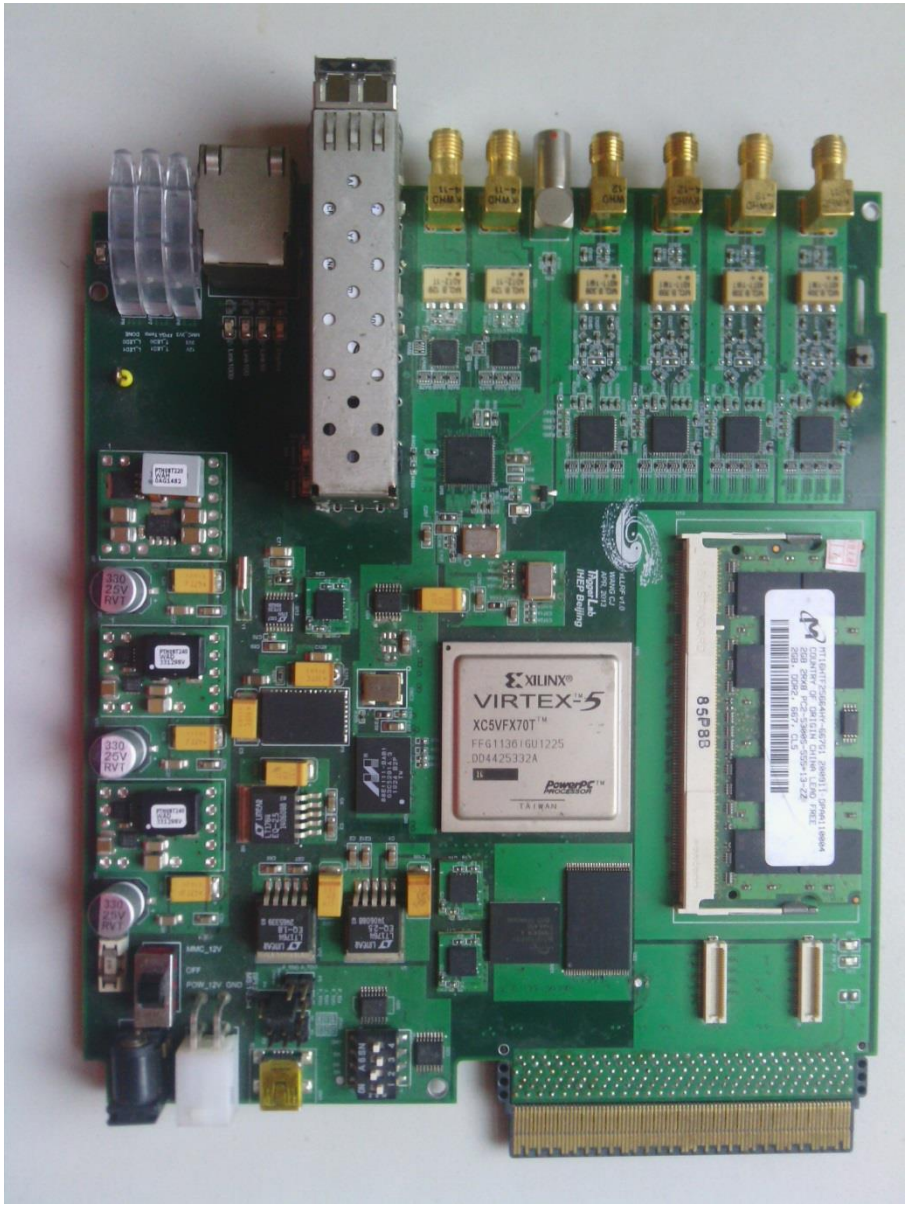
# Activities in IHEP/TrigLab-MicroTCA

- Double Width AMC
  - Type 2 for GPS timing
    - Add-on GPS daughter board
    - Fine timing for tagging
    - Spartan 6 processor
    - Trigger inputs
    - USB ports



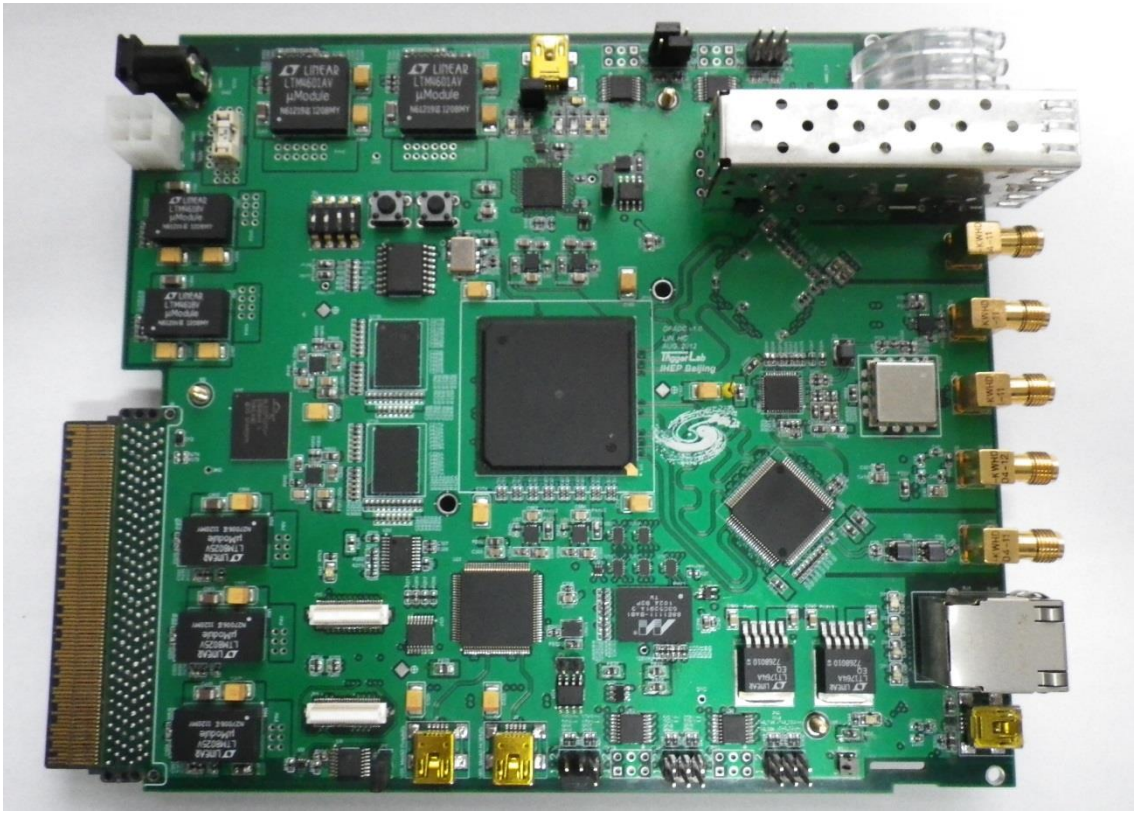
# Activities in IHEP/TrigLab-MicroTCA

- Double Width AMC
  - Type 3 for LLRF
    - 4 ADC inputs
      - 120Msps
    - 1 DAC output
    - Virtex 5 XC5V70T data processing
    - 2GB DDR2 data buffer
    - 1 Ethernet output
    - 1 SFP(3 Gbps)



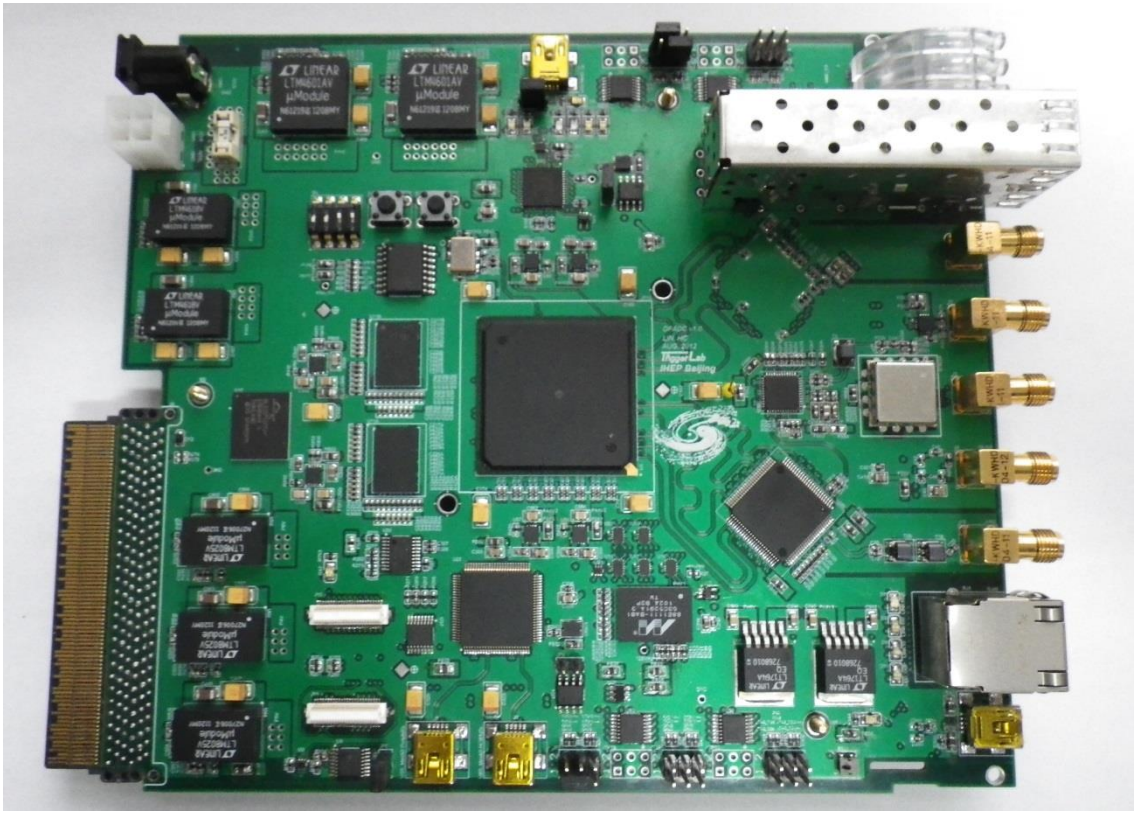
# Activities in IHEP/TrigLab-MicroTCA

- Double Width AMC
  - Type 4 for TREND
    - 2 ADC inputs for antennas
      - 250Msps
    - Virtex 5 XC5V70T data processing
    - 1 Ethernet output
    - 1 SFP(3 Gbps)
    - USB ports



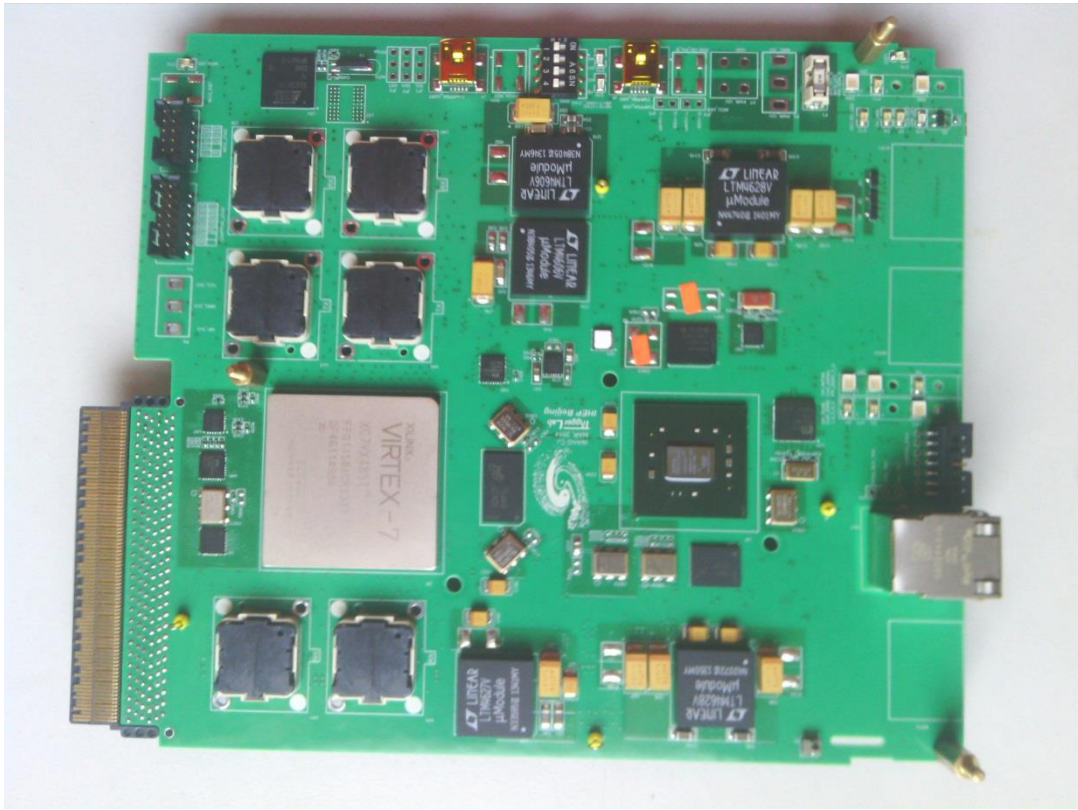
# Activities in IHEP/TrigLab-MicroTCA

- Double Width AMC
  - Type 5 for TREND upgrade/GRAND
    - 3 ADC inputs for antennas
      - 500Msps
    - 1 ADC for Sci.
    - Virtex 5 XC5V70T data processing
    - 1 Ethernet output
    - 1 SFP(3 Gbps)



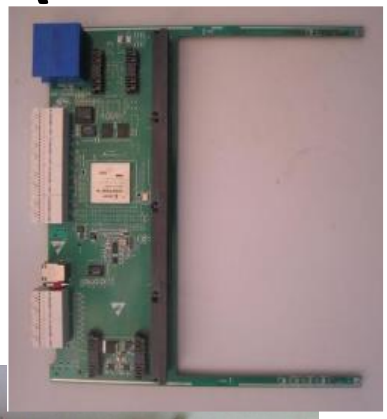
# Activities in IHEP/TrigLab-MicroTCA

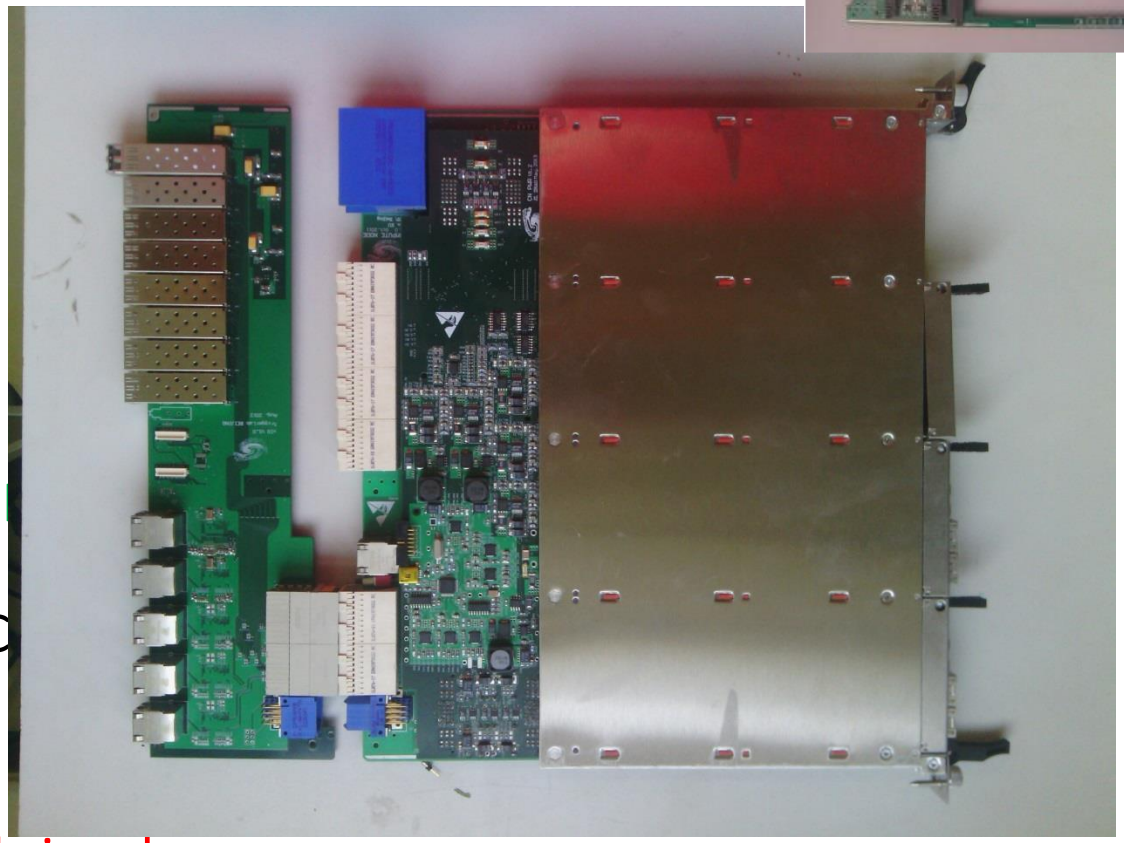
- Double Width AMC
  - Type 6 for CMS TRG upgrade
    - 48 1.6Gbps inputs
    - 24 9.6/10Gbps output
    - Virtex 7 XC7V485T data processing
    - Kintax 7 for control
    - 1 Ethernet output



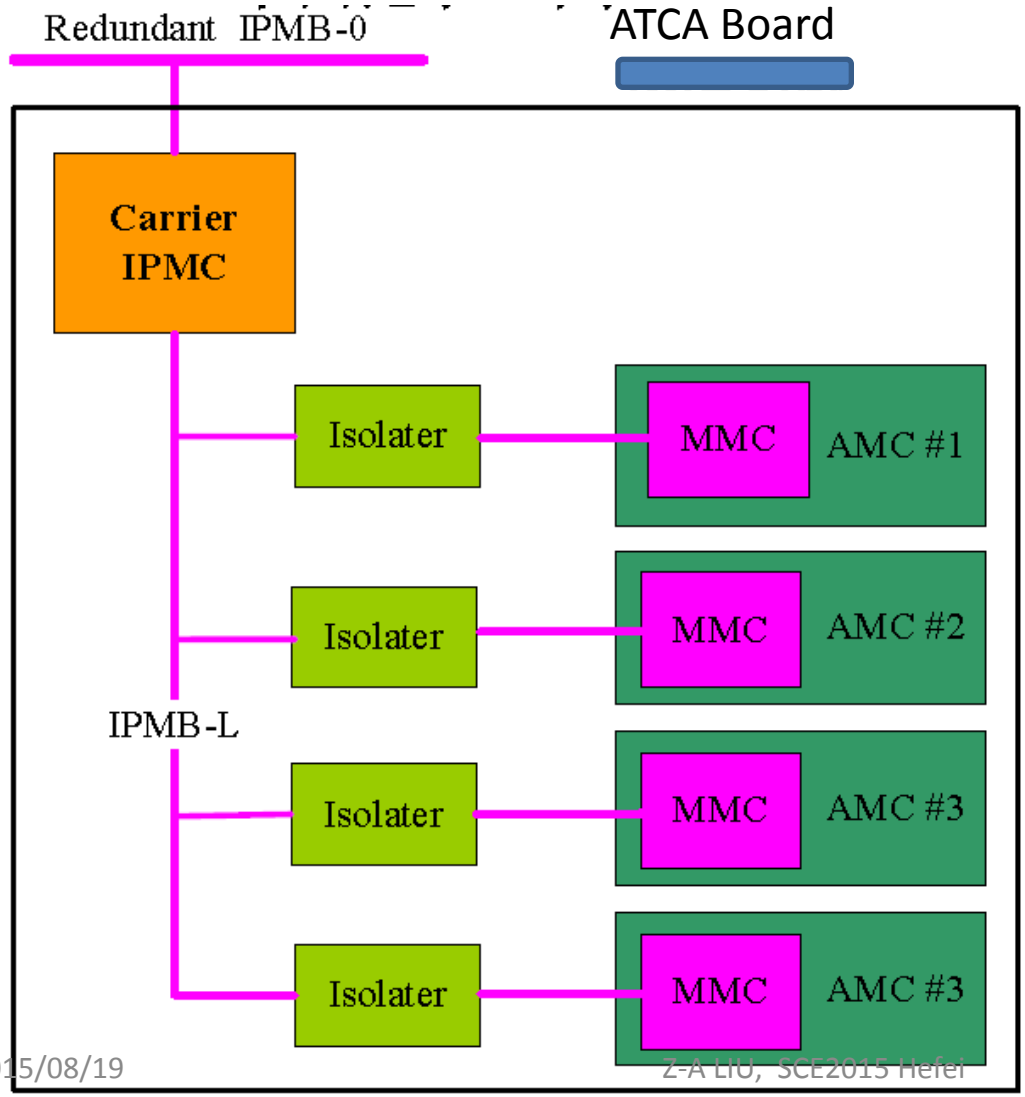
# Activities in IHEP/TrigLab-xTCA

- PICMG 3.8
- ATCA Carrier AMC Board
  - 1 Virtex-4 for Routing(13 backplain)
  - 2 GB DDR2
  - Host 4 AMCs
  - JTAG chain
- Add-on Power board
  - Power converters
  - Jtag Port
- AMC
  - 2x Optical Link (6.4Gb
  - 1 ethernet Panel
  - 2 Embedded PowerPC
  - Real time Linux
- RTM
  - Replacement of panel signals

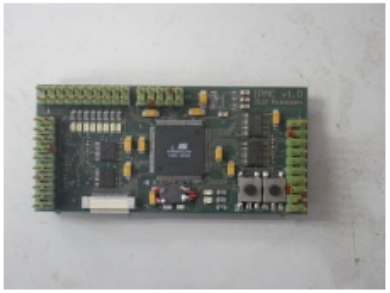




# IPMC/MMC design



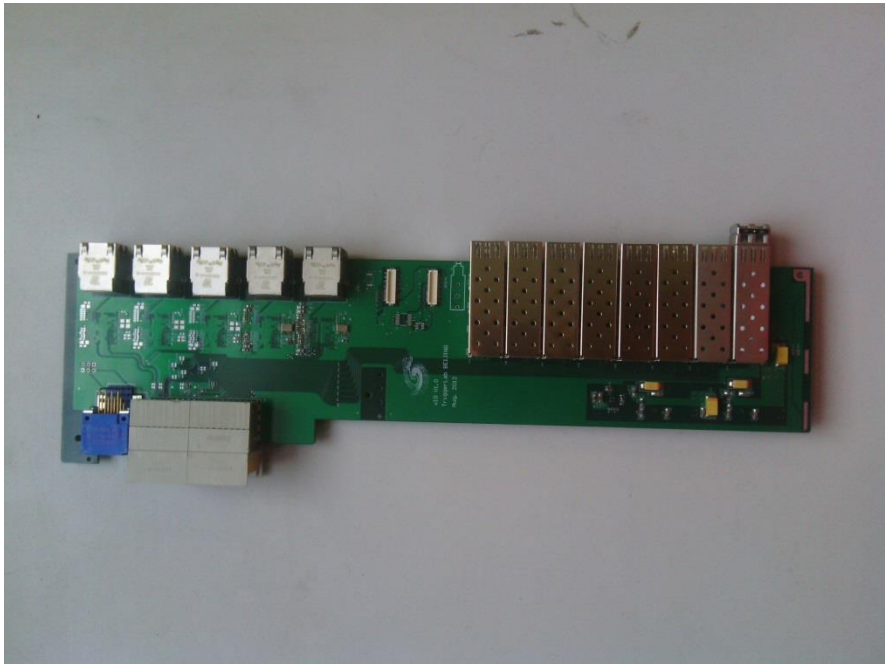

- ACBA: IPMC



- AMC:MMC

# Activities in IHEP/ RTM

- IPMC
  - Power management
  - Temperature monitoring
  - Voltage Monitoring
  - Communication with MMC
- MMC
  - Power management
  - Temperature monitoring
  - Voltage Monitoring
- RTM for PICMG 3.8



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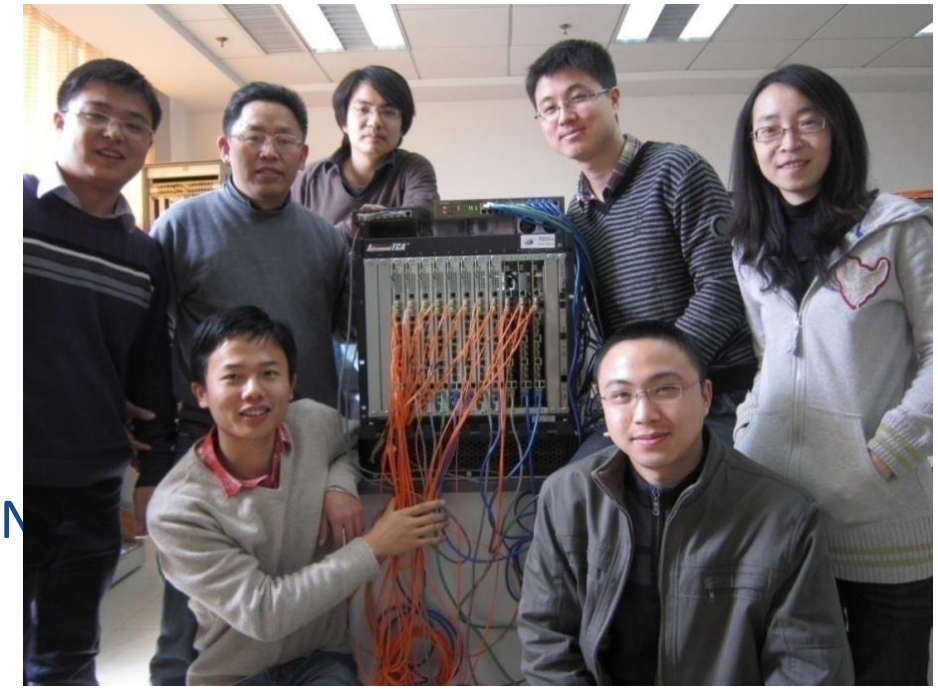
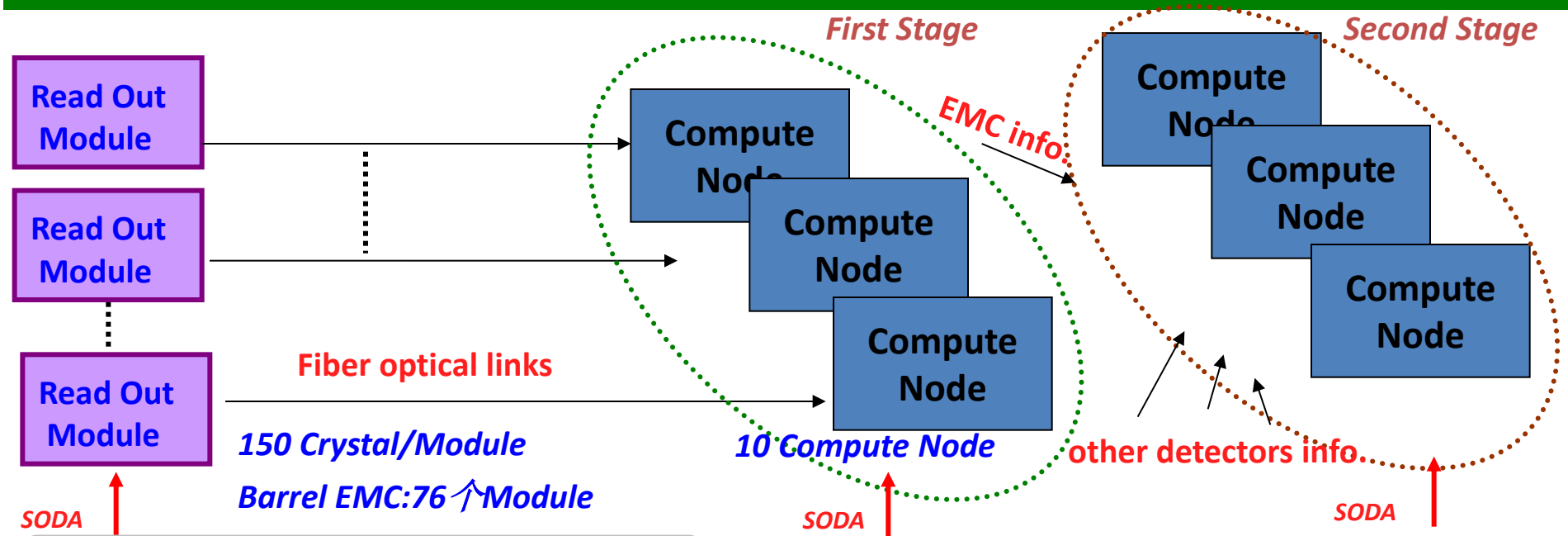


# PANDA EMC TDAQ development System in PANDA




**SODA: Synchronization Of Data Acquisition**

**Task**

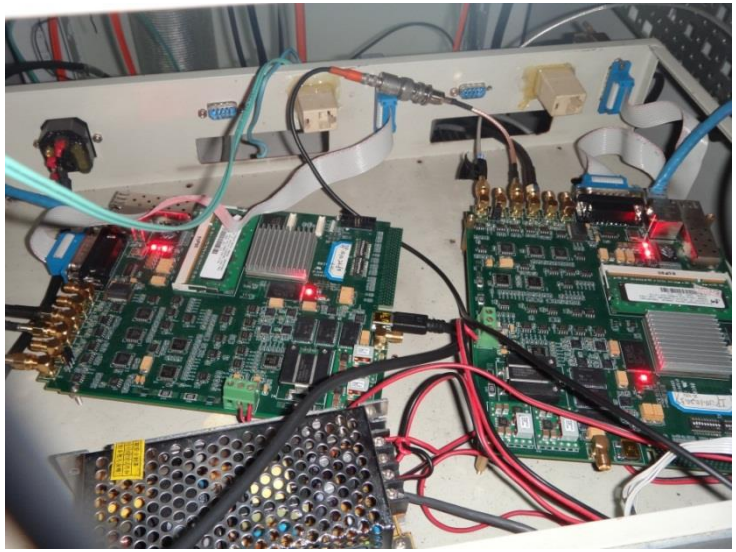
1. Signal Feature extraction (Time, Amplitude)
2. Data Zero suppression

1. Clustering
2. Cluster Properties extraction
3. Pattern recognition

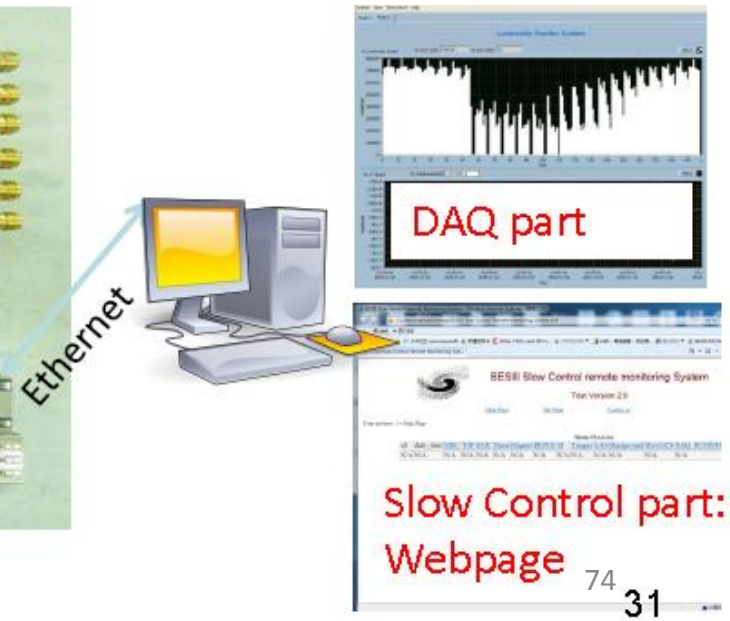
1. Correlation
2. Physical parameters calculation
3. Event building

# Application BESIII LUMI

- Successfully running for one year
  - Prototype of xFP card
  - A full-size, Double-width AMC module
  - Embedded system designed
  - Open source Linux system
  - Luminosity IP core
  - Web slow control
  - MTCA complaint

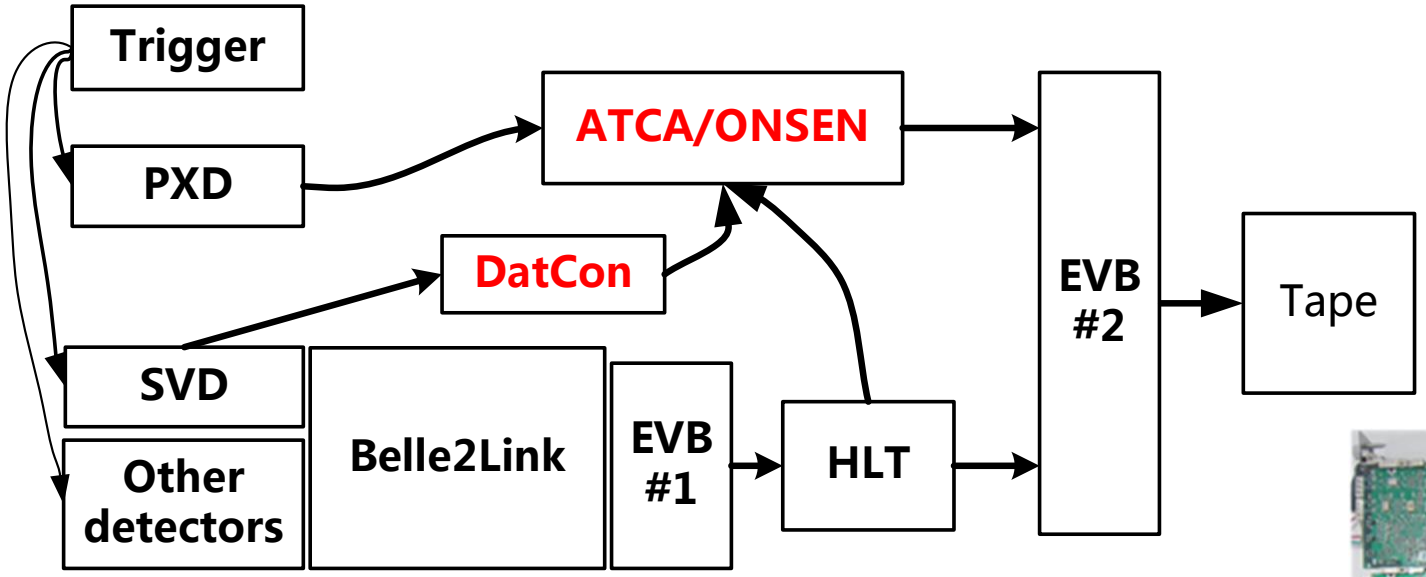



rocessing board
*ze, double-width AMC module*

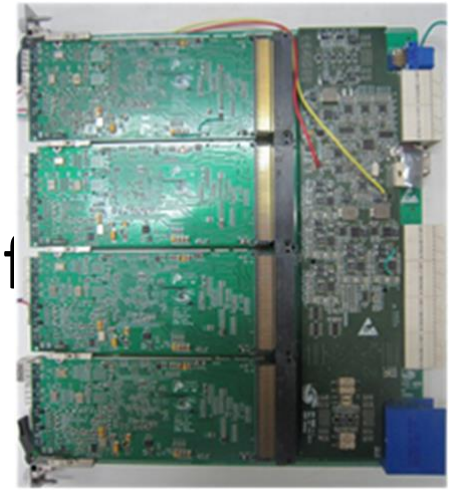


# Belle II PXD-DAQ/SVD-DATCON

- PXD/DAQ design in DEPFET Colaboration aimed for Belle II at KEK

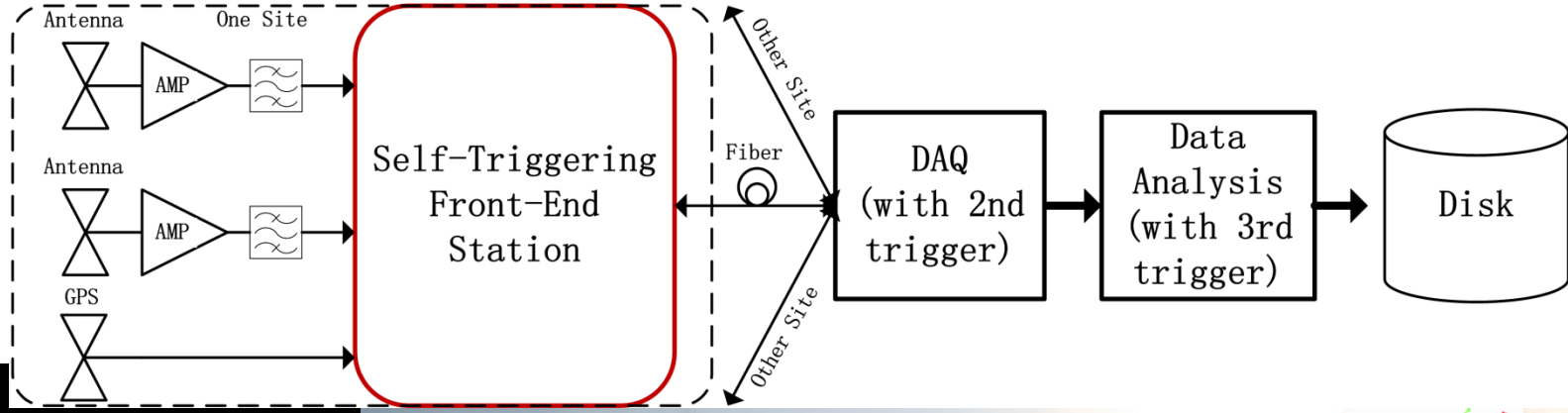


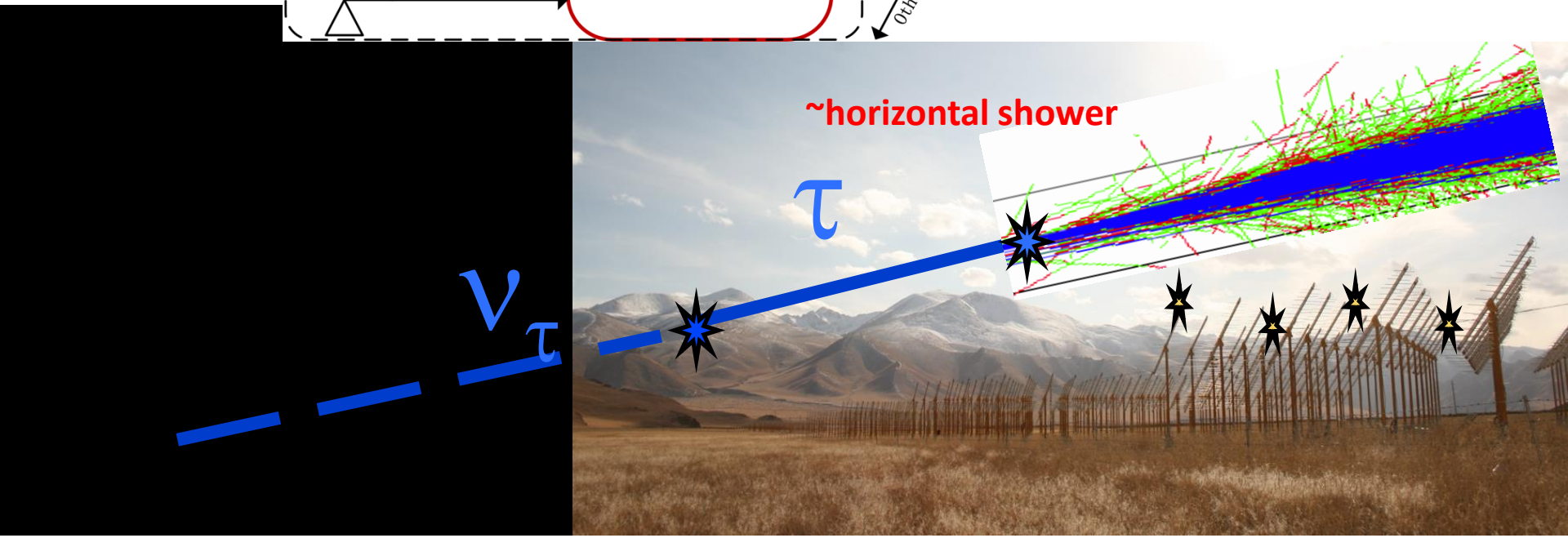

- ATCA/ONSEN and DatCon both consist of Computer Node compliant to xTCA specification in both MTCA and ATCA shelves.



# TREND

- All AMC/MTCA/ATCA composed system
- Site test successful



# What is xTCA?

- ATCA(Advanced Telecommunication Computer Architecture)
  - High speed IO interconnection up to 10Gbps
  - High availability HA~99.999%
  - System intelligence management
- MicroTCA(MTCA)
  - Have advantage of ATCA
  - Half hight of ATCA, compact system
- AdvancedMC(Advanced Mezzanine Card )
  - Filed Replace Unite module(FRU)
- **xTCA for physics:** new standard formed xTCA CCTS committee under PICMG which admits some of ATCA/MTCA/AMC
- **xTCA** for short

# xTCA features

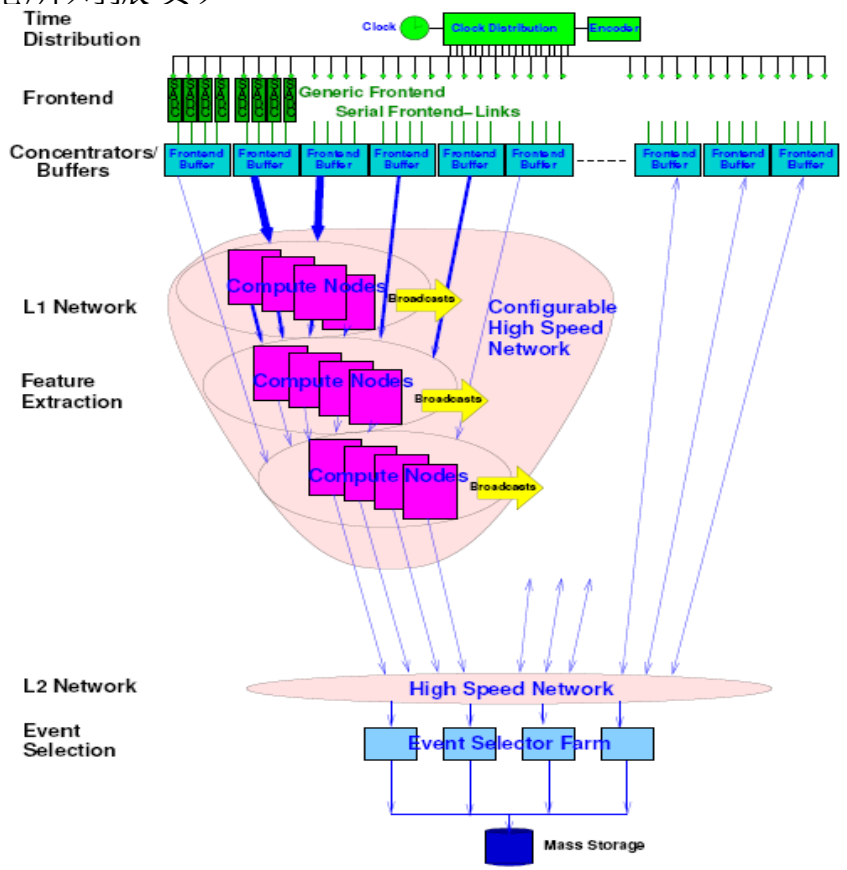
- ATCA & MicroTCA Unique Features
  - ATCA board, shelf is first modular computer architecture with completely serial multi-Gbps backplane
  - Serial ports are bidirectional pairs in star or mesh topology
  - Serial bit rate of one port at 2.5 Gbps exceeds data rate of parallel bus backplanes, e.g. VME 32/64 bit word at 10 MHz => 320/640 Mbps (*now 2.5G=>10G=> 40 G*)
  - Architecture based on FPGAs with imbedded SERDES Tx-Rx, LVDS balanced logic
  - High processing power of single ATCA card (Blade)
  - MCH enables module to any other module communication
  - Special low jitter switches for clocks
  - Dual redundancy MCH, Processor, Power Units - optional

# xTCA **Standards – Hardware Extensions**

- Rear Transition Modules
  - ATCA Card => PICMG 3.8
    - Zone 3 area defined but interface left to discretion of vendors
    - Severely limits interoperability of vendor modules
    - Physics developed ATCA Standard RTM Interface
    - Fabric, power, JTAG, IPMI, managed from ATCA
  - MicroTCA Double-Wide Card => MTCA.4
    - MTCA.0 defined double-wide AMC but not Zone 3 or RTM mechanics
    - MTCA.4 developed new crate, RTM, interface, cooling
    - Fabric, power, JTAG, IPMI, managed from AMC
    - RTM hot-swappable

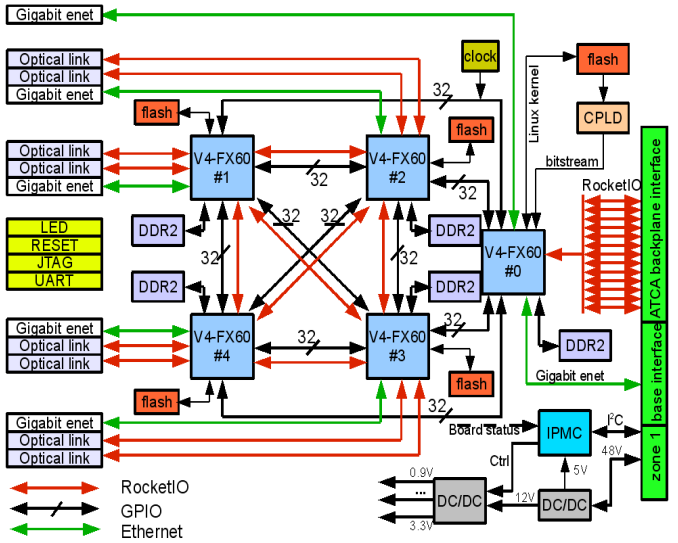
# 一.PANDA国际合作简介

- 973：自由电子激光和反质子加速器重大基础研究（高能所姜晓明）
  - FAIR有关的大型实验探测器关键技术问题研究（近物所徐瑚珊）
    - PANDA实验触发及数据获取系统（高能所刘振安）
- 实验室间长期合作
  - 高能所实验物理中心触发实验室
  - 德国吉森大学第二物理所
  - 2006年起长期合作
    - PANDA实验
    - DEPFET硅像素探测器应用研究
- 研究内容
  - 新型触发与数据获取系统构架（TDA
    可行性研究
  - 高性能计算节点的研制硬件设计
  - 基于FPGA的嵌入式片上数据获取系
- 高能所的作用
  - 负责硬件设计，调试
  - 负责系统平台的建立
  - 参加软件触发功能的开发
  - 承担EMC 高级触发算法研究



# 一. PANDA完成情况（1）

- 完成情况: 全面完成了计划预定的任务
  1. 成功研制2版实用计算节点原型样机
  2. 完全实现了预定的功能
     - 高数据传输带宽（6 个千兆网口，8 个光纤口(到3.125Gbps)，13个RocketIOs板板点对点的互联
     - 大容量数据处理能力（5个V4 FPGA + 2GB DDR2）
     - 嵌入式设计方式（通用的系统+专用的数据处理模块
     - 智能平台管理（基于板上IPMC子板与机箱控制器的通信来实现系统监测及管理功能）

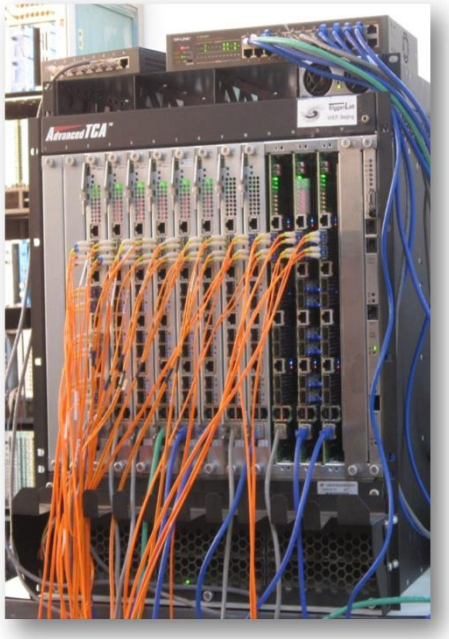


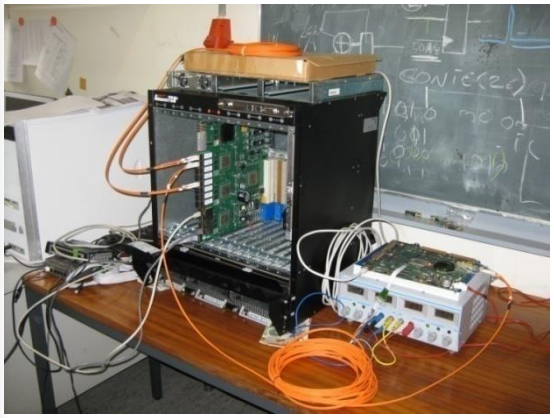

计算节点原理方框图

高能所研制的第二版计算节点

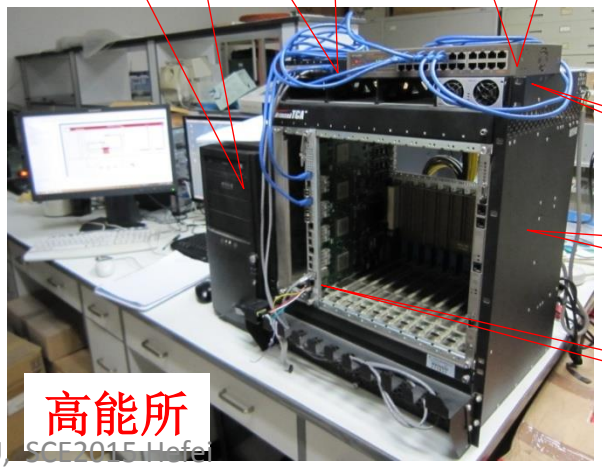
# 一. 计划任务完成情况（2）

- 完成情况: 全面完成了计划预定的任务(续）
  3. 小批量生产了计算节点
  4. 搭建了5套样机验证系统(高能所一套，吉森大学2套，波恩大学一套，荷兰KVI一套)
  5. 实现了PANDA EMC电磁量能器在线事例特征提取、触发与事例预选择和事例组建的样机系统
- 973项目结题
- 后续研究（xTCA相关)?



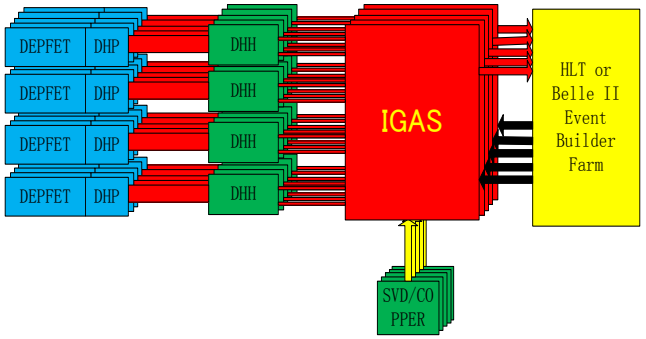


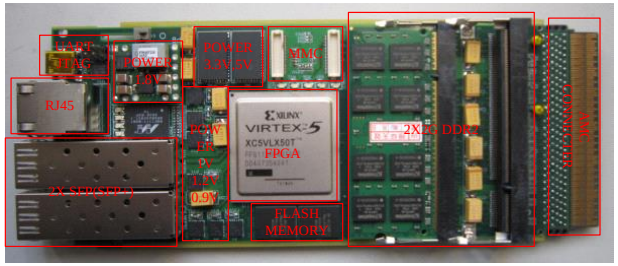
德国吉森大学

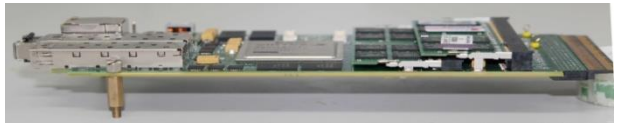


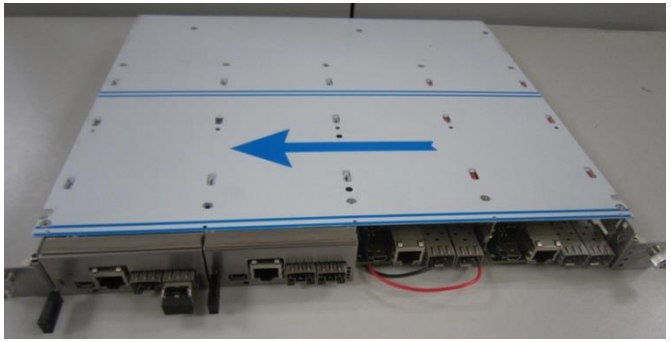
# DEPFET/PXD硅像素探测器国际合作

- **DEPFET：** 欧洲硅像素探测器国际合作之一
- 触发实验室2010年4月底受邀正式加入合作
- 任务：
  - 海量数据快速读出与预处理系统的设计
  - 高能所与德国吉森大学合作承担
  - 取名 **ONSEN** 系统
  - 应用目标：**BelleII**实验
- IGAS有以下特点：
  - 基于**xTCA**新标准（高能所特殊贡献）
  - 实现单通道光纤数据带宽**6Gb/**秒
  - 实现数据缓冲内存**200GB**
  - 事例的局部判选
  - 实现数据事例率**1/10**的压缩
- **2012**年进展
  - 完成了关键部件的第一版样机，包括载板、电源板、子板、后插板等，已完成调试
  - 功能调试在德国吉森大学进行
  - 建立了开发平台

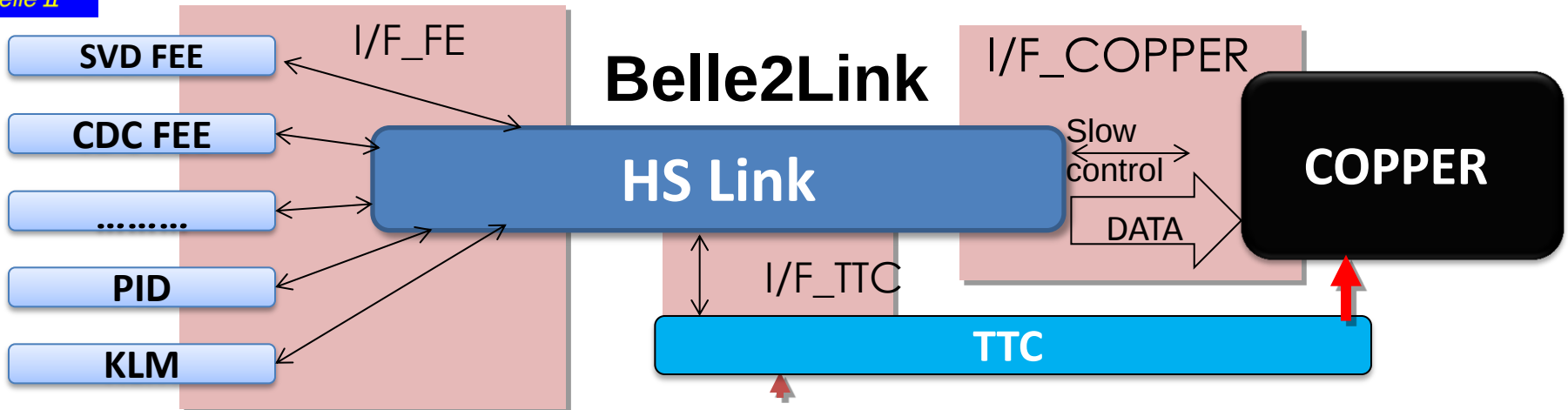




# BelleII高速读出与数据传输系统




2009底我们决定受邀参加

触发实验室负责（命名为Belle2Link ）

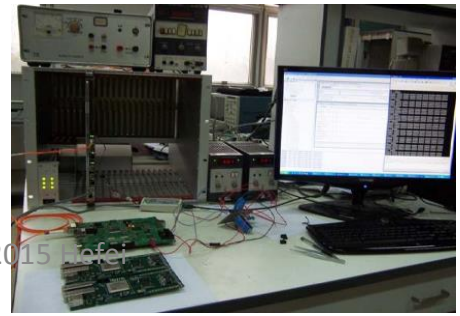
- 整体方案设计、TDR撰写
- 样机研制、系统调试
- Belle II 联调

主要特性有

- 国际上率先实现告诉通路数据和慢控命令的共享传输
- 各探测器统一的硬件设计
- 各探测器统一的固件设计
- 实现了电隔离
- 3.125Gb/秒的高速率数据和信号传输
- 可以兼容不同系统的不同数据输入速率
- 自主研发的传输协议

2012年进展

- 基于CDC的样机系统得到合作组认定，并进行了评估鉴定
- 成立了Belle II推广工作组，刘振安任组长，开展所有探测器的读出改进及联调
- 开始了硬件的批量生产
- 期待获得经费支持

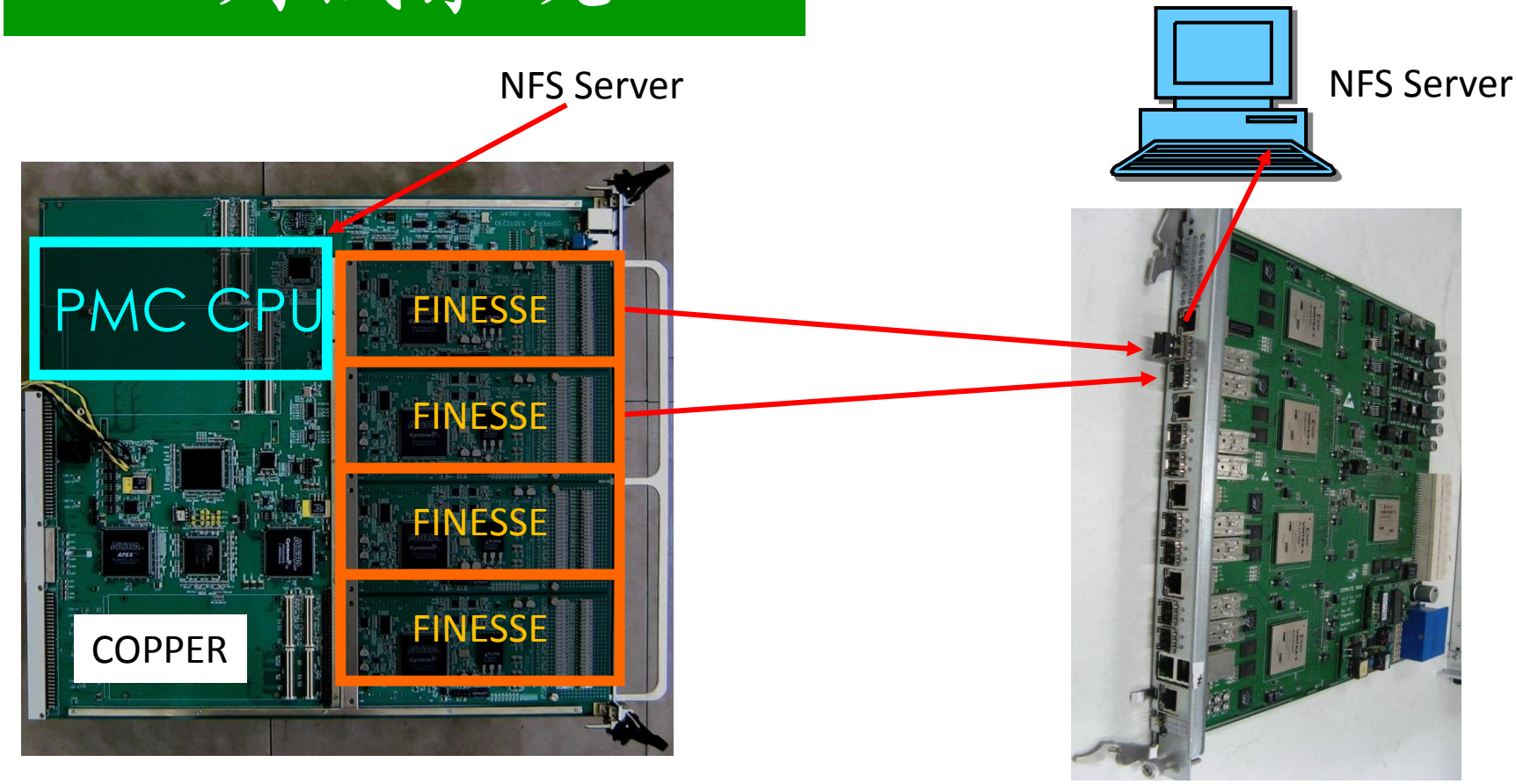


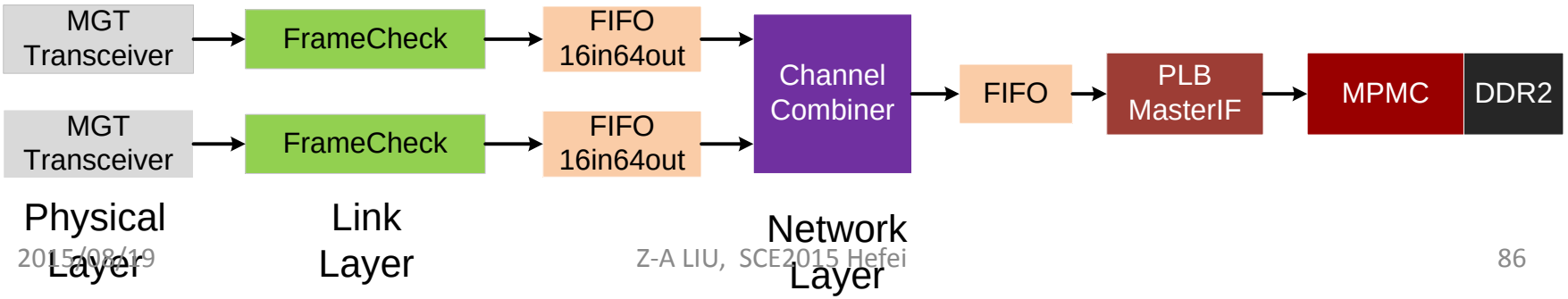
# xTCA标准制定及相关研究
# -下一代核仪器及设备标准XTCA进展


刘振安
中国科学院高能物理研究所快触发实验室

核探测与核电子学国家重点实验室揭牌仪式
北京 2012年3月7日

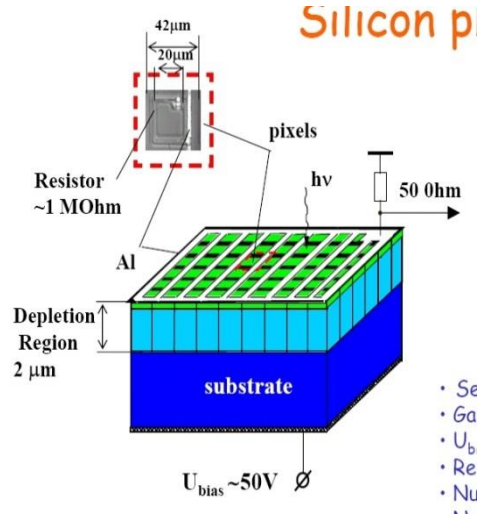
# 测试系统

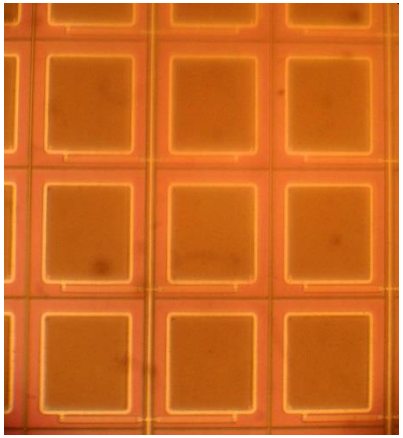

NFS Server
NFS Server
PMC CPU
FINESSE
FINESSE
FINESSE
FINESSE
COPPER

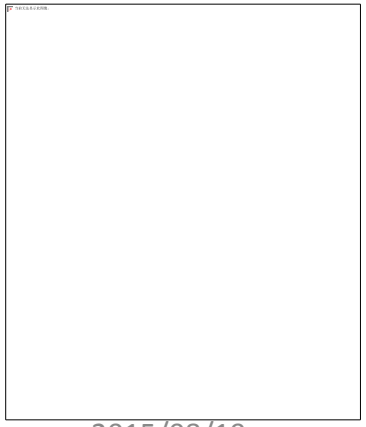

MGT Transceiver
MGT Transceiver
FrameCheck
FrameCheck
FIFO 16in64out
FIFO 16in64out
Channel Combiner
FIFO
PLB MasterIF
MPMC
DDR2
Physical Layer
Link Layer
Network Layer

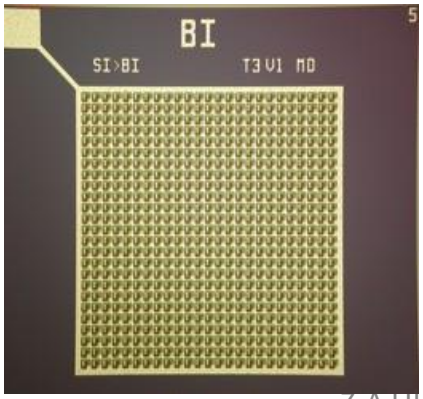
# PET phodetectors promizing technologies

- SiPM/MPPC-DSiPM

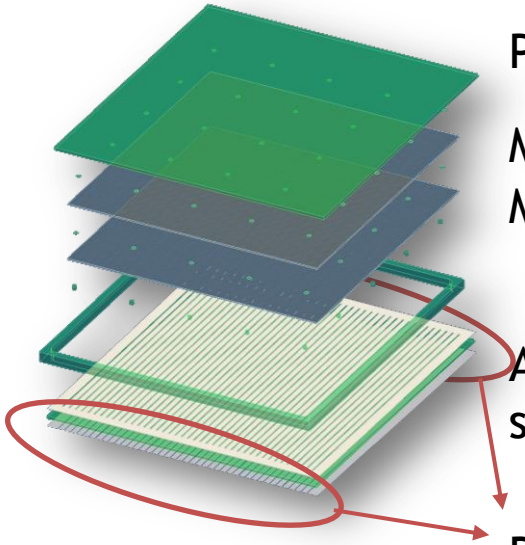







## Large Area MCP's

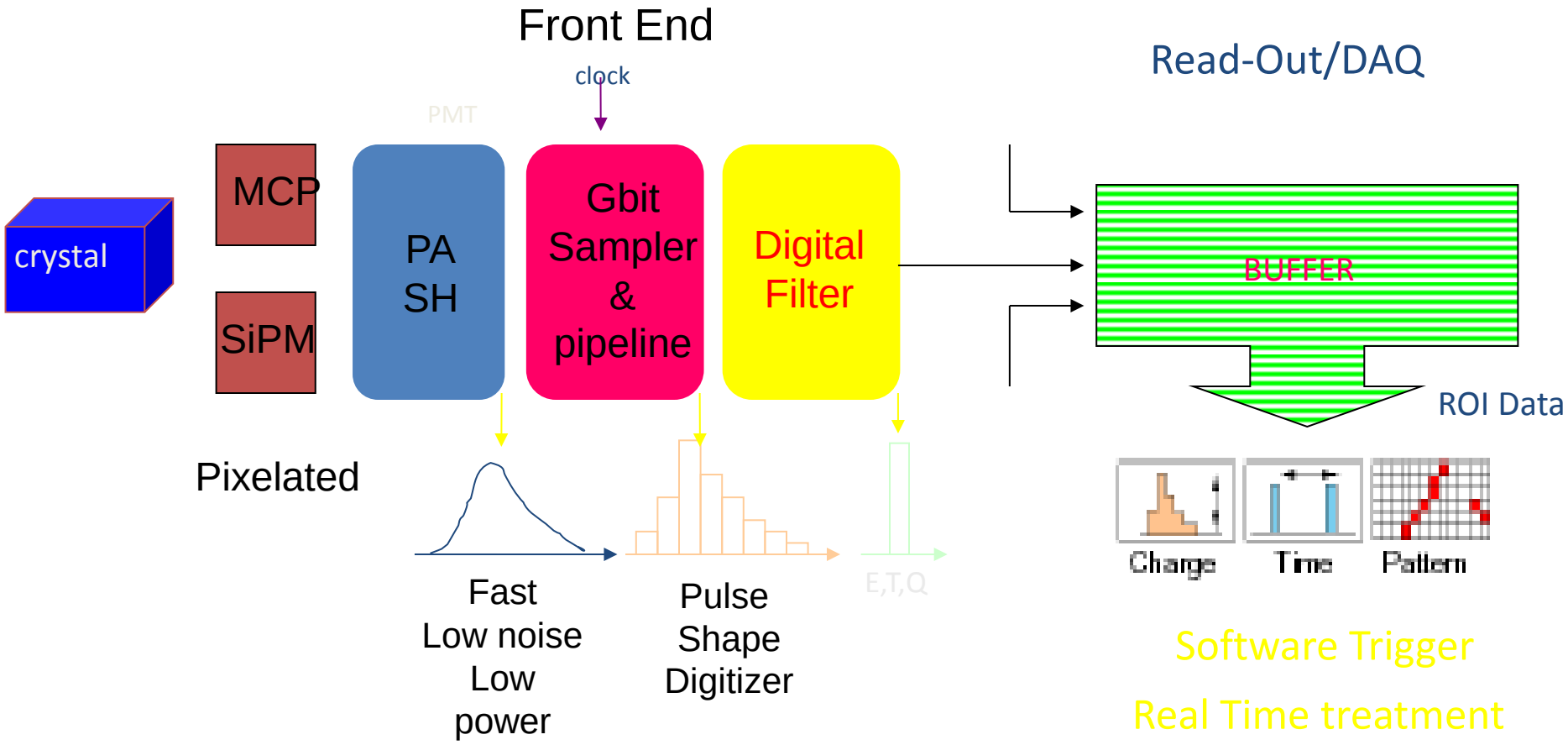



LAPPD Collaboration

(U Chicago ANL)

Cheap for large area

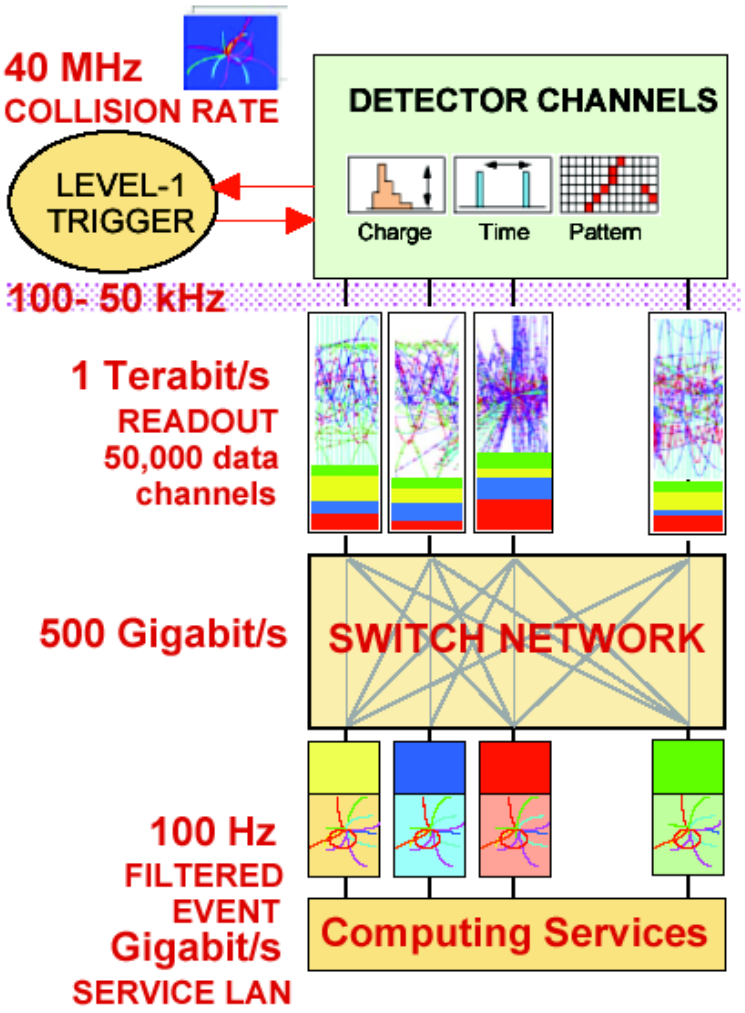
# Exemple of Conceptual TOF-PET architecture model




- Free-running analog waveform sampling and digitizer (SCA)
- Digital filter used to extract pulse amplitude and high resolution timing (FPGA)
- Pipelined processing architecture to avoid deadtimes
- Parallel digital read out
- Terabit network for communication and processing (xTCA)

# TDAQ = Pipeline Architectures

**LHC**




**Digitisation**

**Pipeline**

**Event builder**

**Future PET**