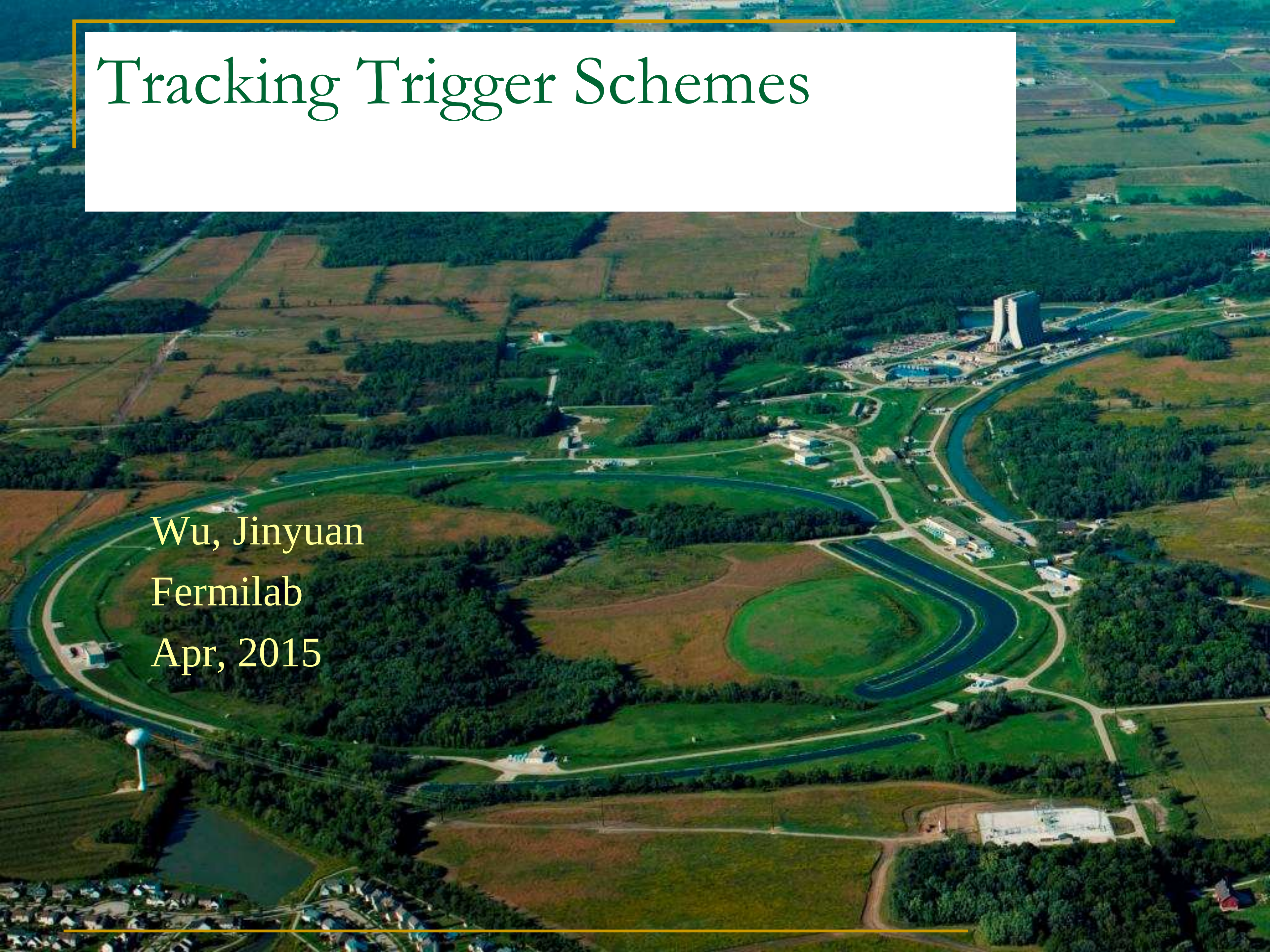
Tracking Trigger Schemes



Wu, Jinyuan
Fermilab
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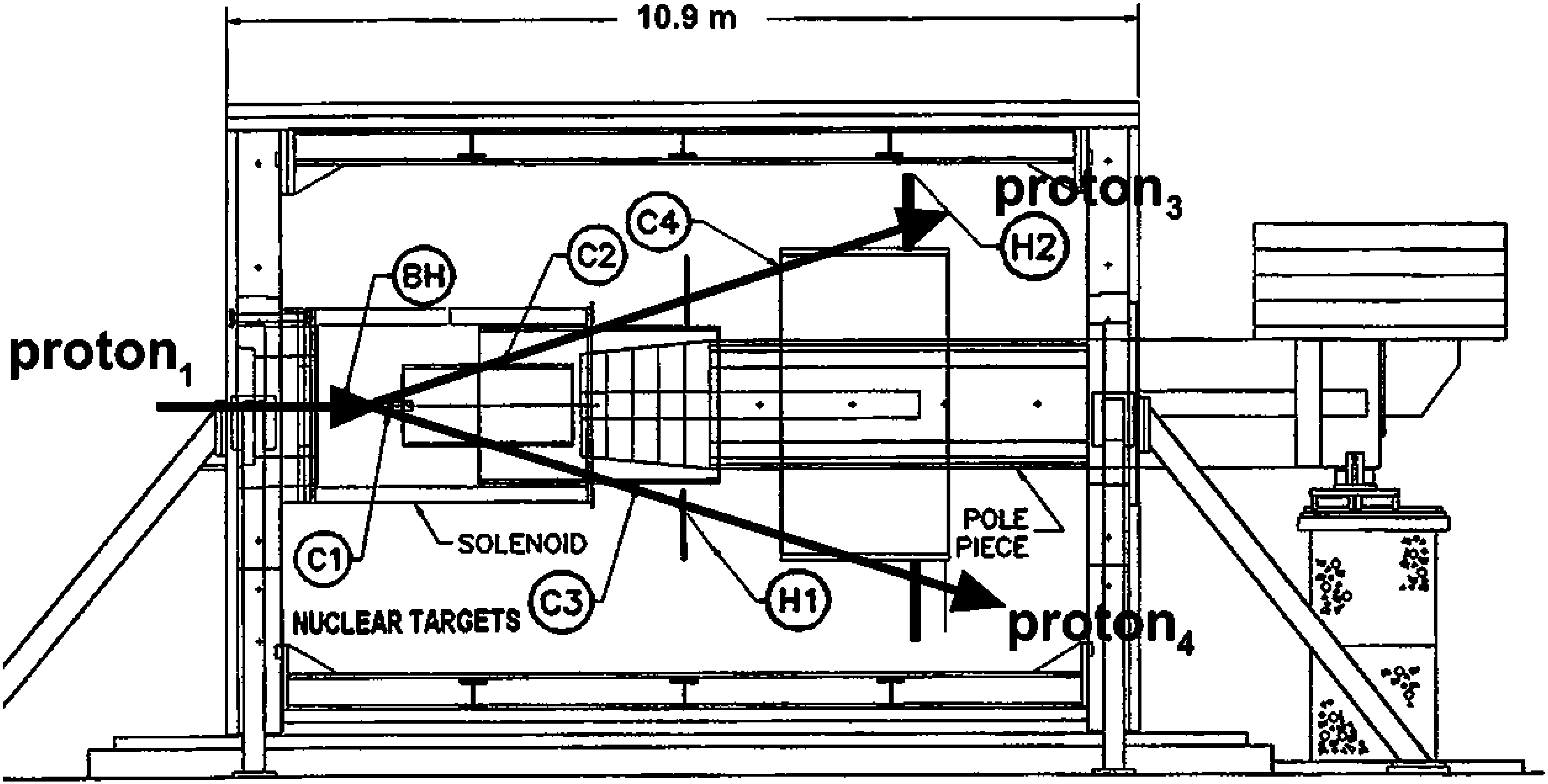
Introduction

- Charged track parameters such as momentum and angles have been important event selection primitives since the early age of experimental high energy physics.
- LHC see very high hit rate with possible pile up of 200 interactions in each beam bunch crossing.
- The outline of this talk:
  - Tracking Trigger in the Old Days
  - Contemporary Tracking Trigger Challenges
  - Double-Layer Detectors
  - Track Finding
  - Track Fitting

Tracking Trigger in the Old Days

BNL E850 (EVA), Color Transparency Measurements

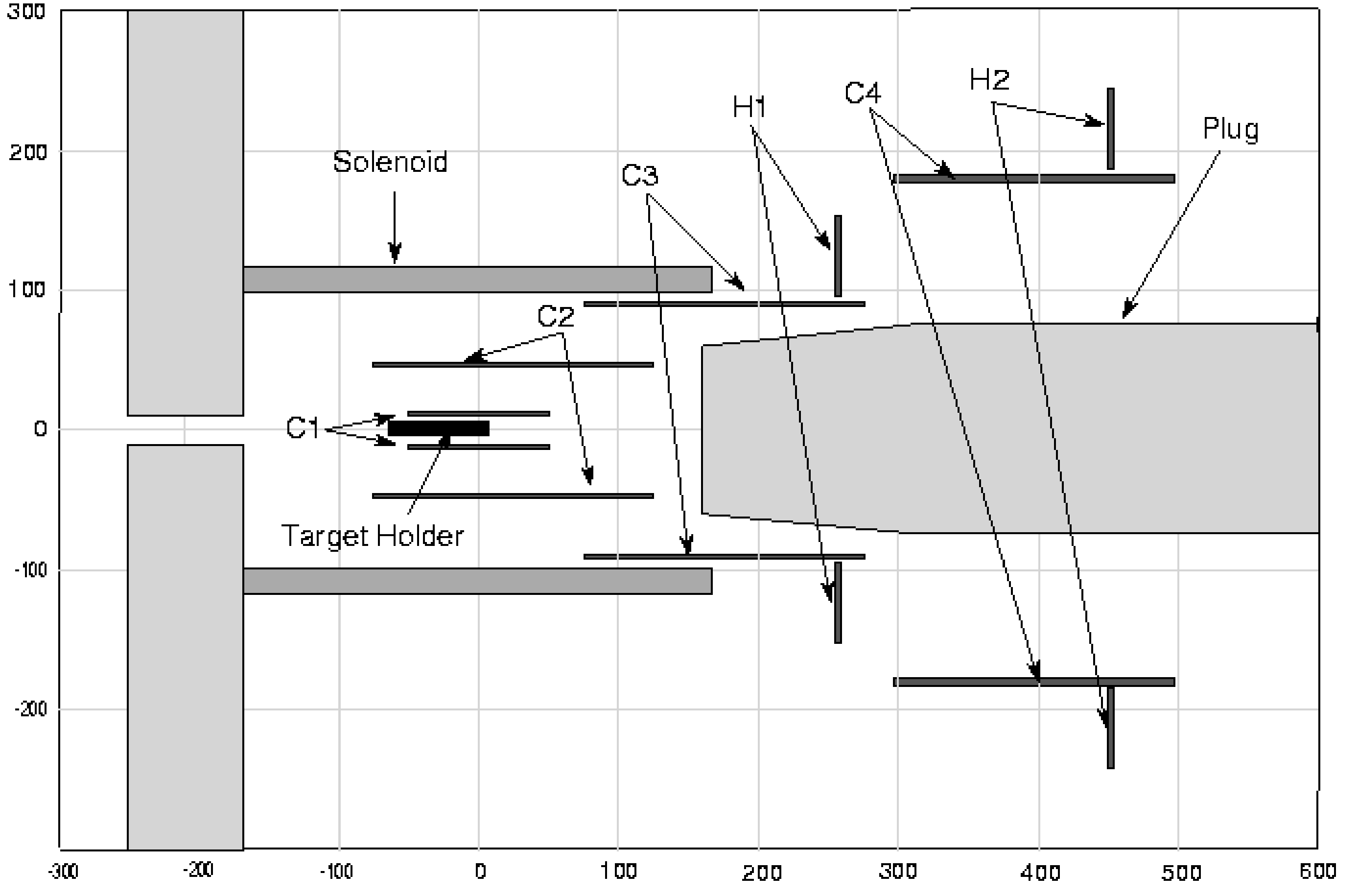


- Scintillation counters H1 & H2.
- Straw tube cylinders C1, C2, C3 & C4.
- Measuring the two high PT protons.

BNL E850 (EVA), Decommissioning

- 2004 ☹

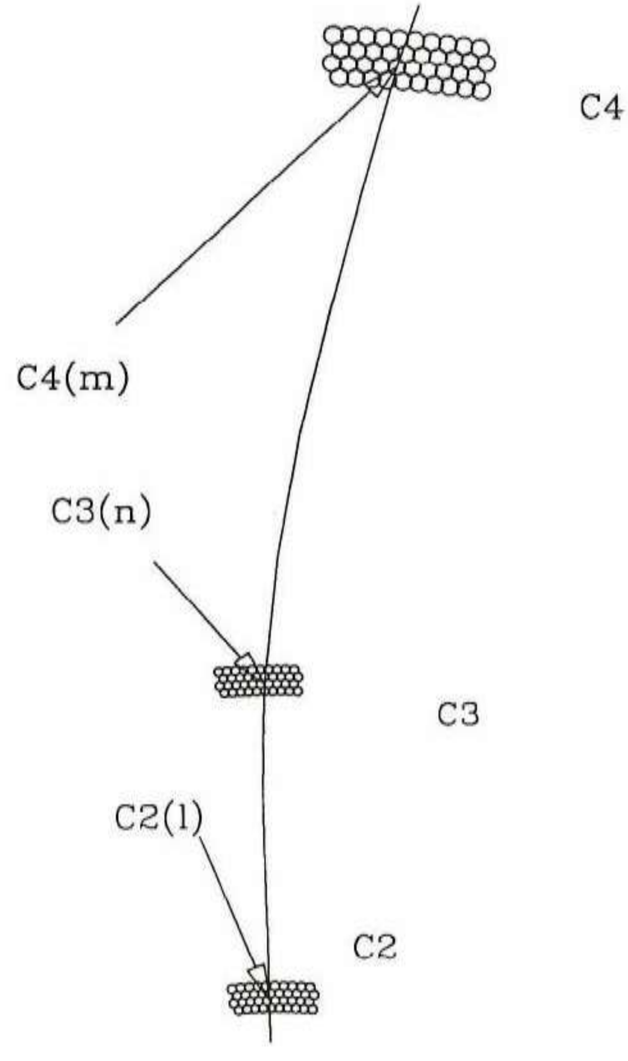
Detector



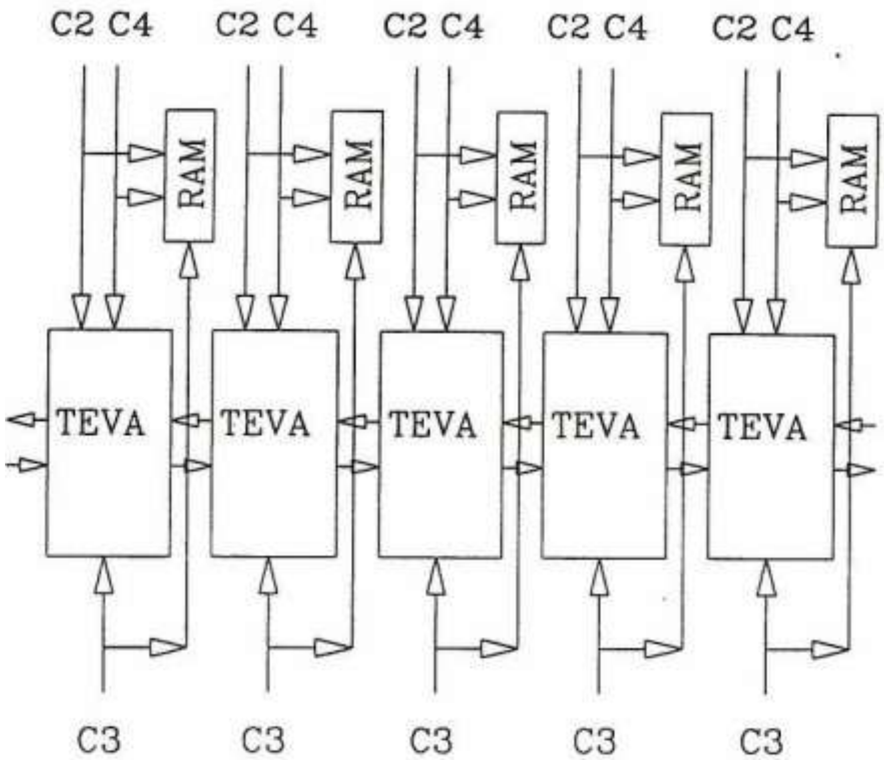
- Level 1 trigger: (H1, H2)
- Level 2 trigger: high PT proton tracks in (C2, C3, C4).

High PT Tracking Trigger

- High PT tracks are bent in magnetic field and hit detector cylinders C2, C3 and C4.
- Middle two layers in each chamber are used for the trigger.
- The position differences (l-n) and (m-n) provide PT information.

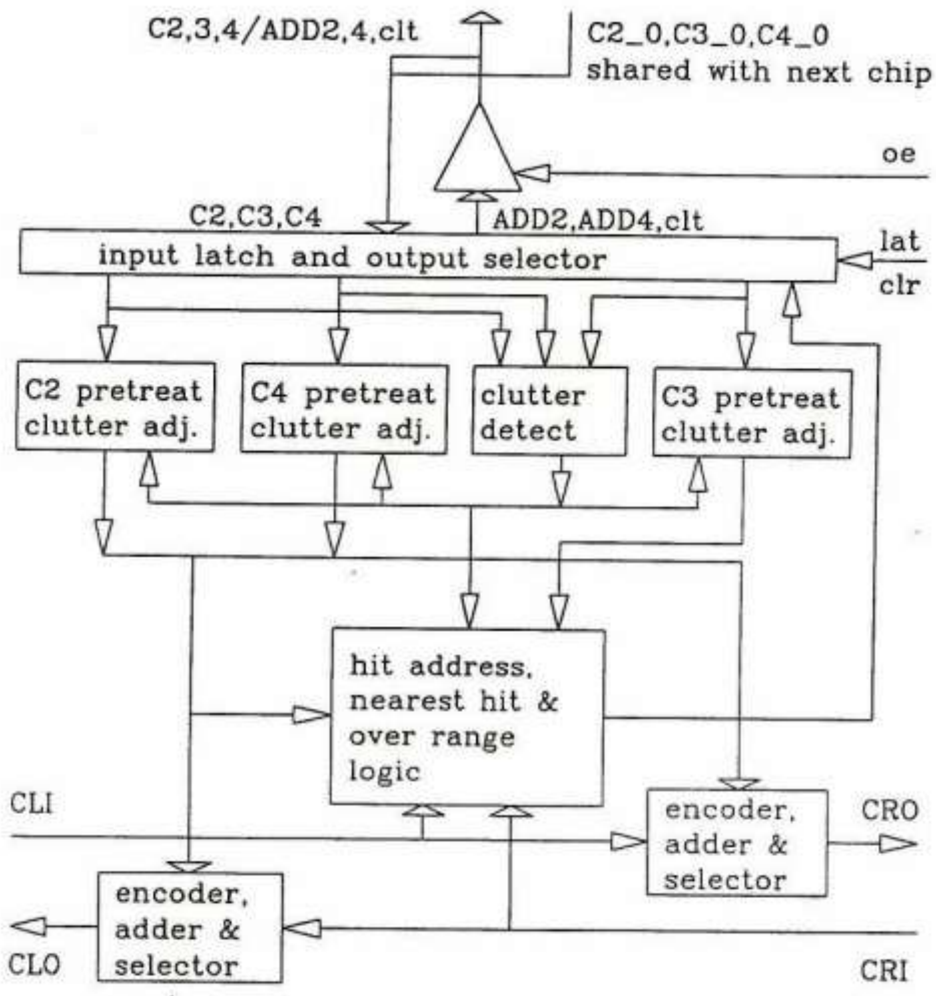


TEVA ASIC Array



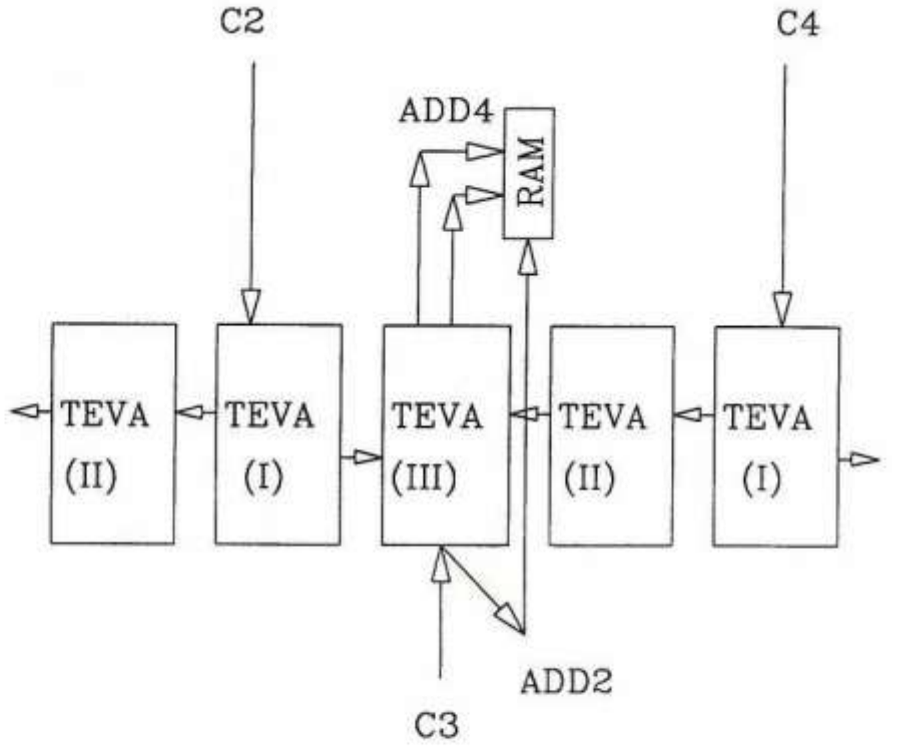
- Hits from C2, C3 and C4 are sent into the TEVA ASIC.
- Each chip processes 4 inputs from each layer.
- Hit locations on C2 and C4 are encoded and sent to left and right.
- When the codes from C2 and C4 meet C3 hit, the distances of the hits are calculated.
- The hit distances are used to address the external RAM and the outputs of the RAM are combined as level 2 decision.

Logic Block Diagram of the TEVA Chip



- Any hit in C2 or C4 is encoded and sent to left and right.
- When there is no hit in C2 or C4, any code from left side is passed to right side and added by 4.
- Same for right to left passing.
- Codes are passed up to 4 chips, i.e., 16 straw tubes.
- When any C3 hit exists, hit distances are calculated.

Trigger Example



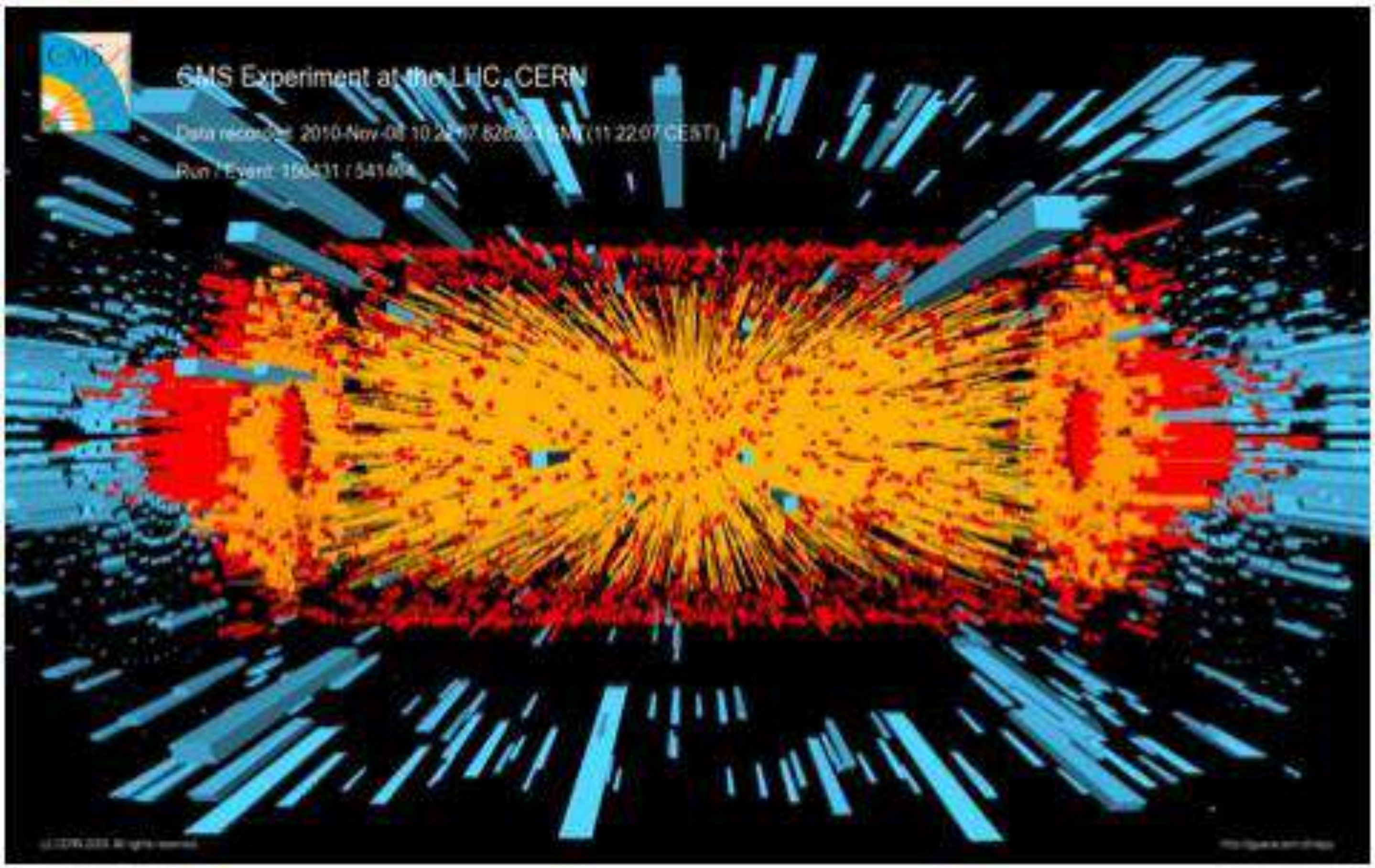
- The hit locations of C2 and C4 are sent to the chip (III) containing a C3 hit.
- Hit distances ADD2 and ADD4 are calculated and used to address the RAM.
- Trigger acceptance map are preloaded in the RAM and the outputs of the RAM make trigger decision.

Tracking Trigger

- Hit Data Transmission.
- Hit Data Matching (Pattern Recognition, Track Finding)
- Tracking Parameter Calculation (Track Fitting)
- Trigger Decision.

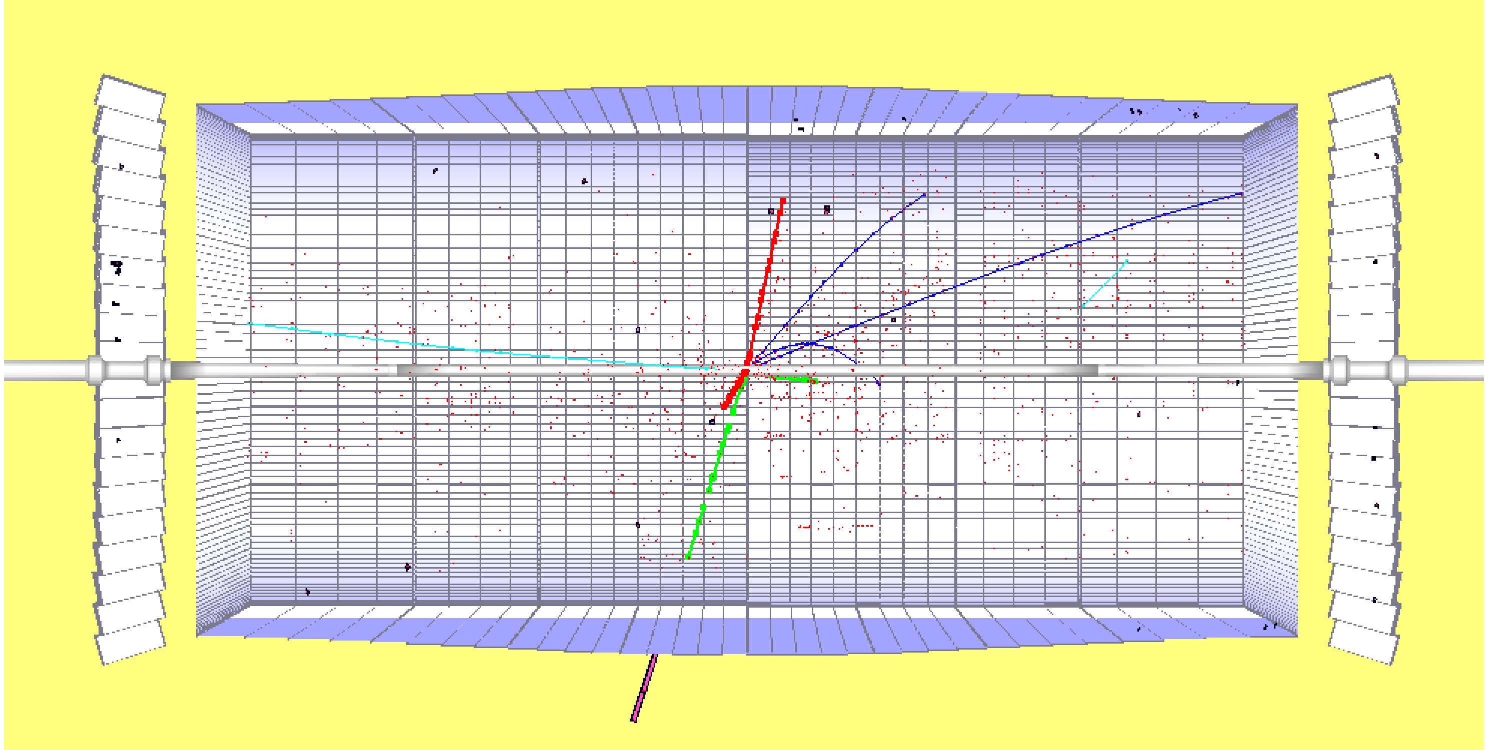
Contemporary Tracking Trigger Challenges

Very Messy Detector Hits in Every Beam Crossing



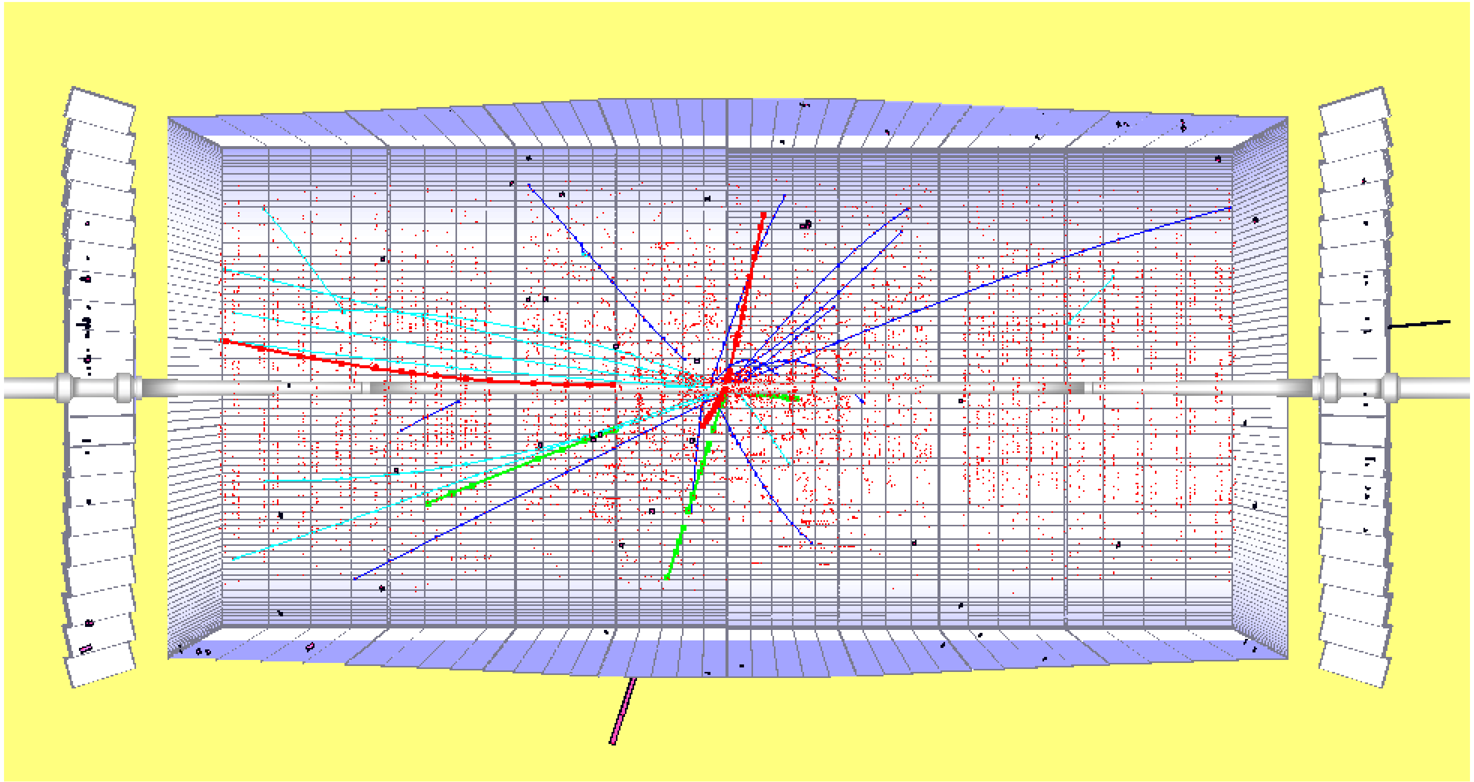
- CMS Detector

PP Collisions at 10^32



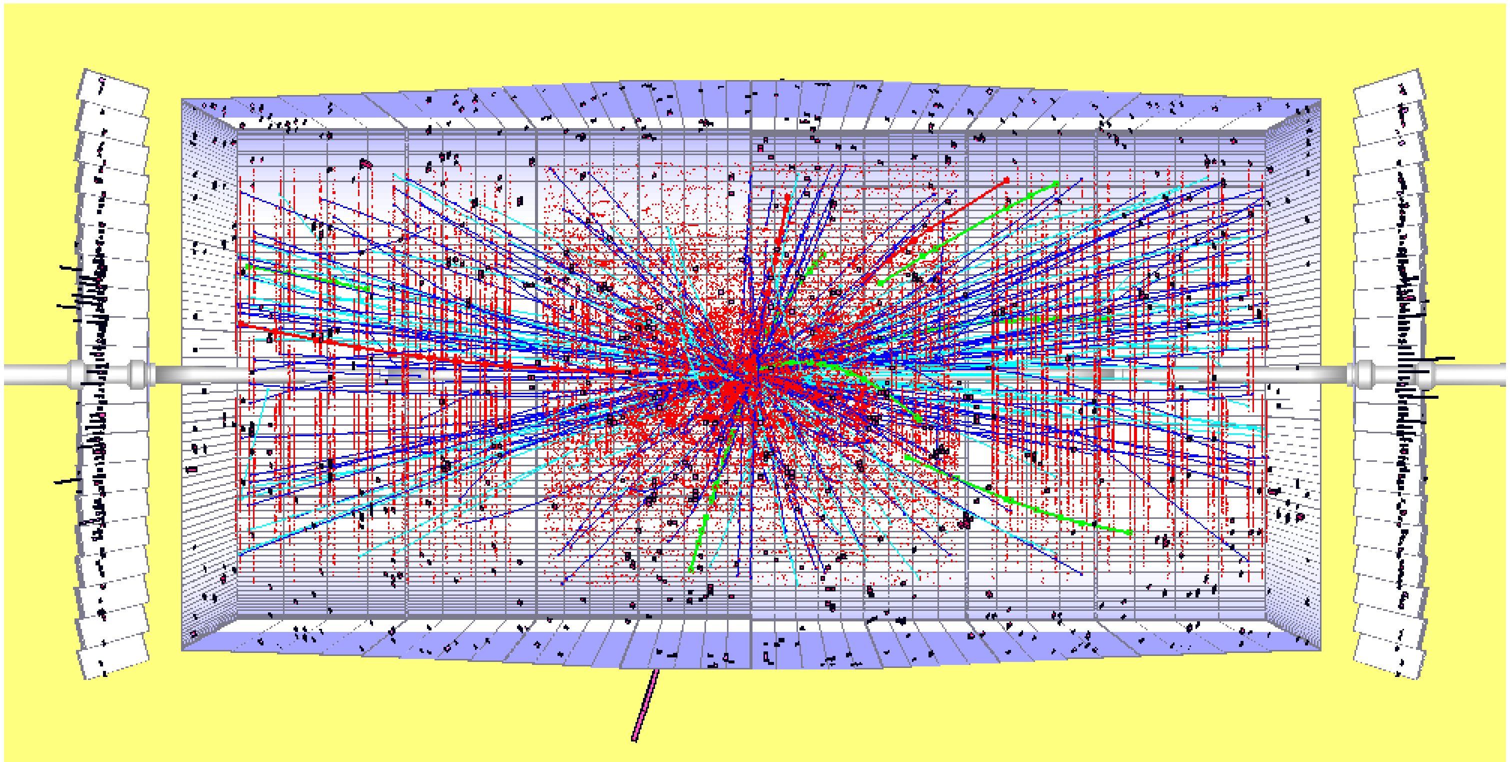
- Most beam crossings (BX) look empty.
- A few tracks are seen in triggered physics events.

10^33



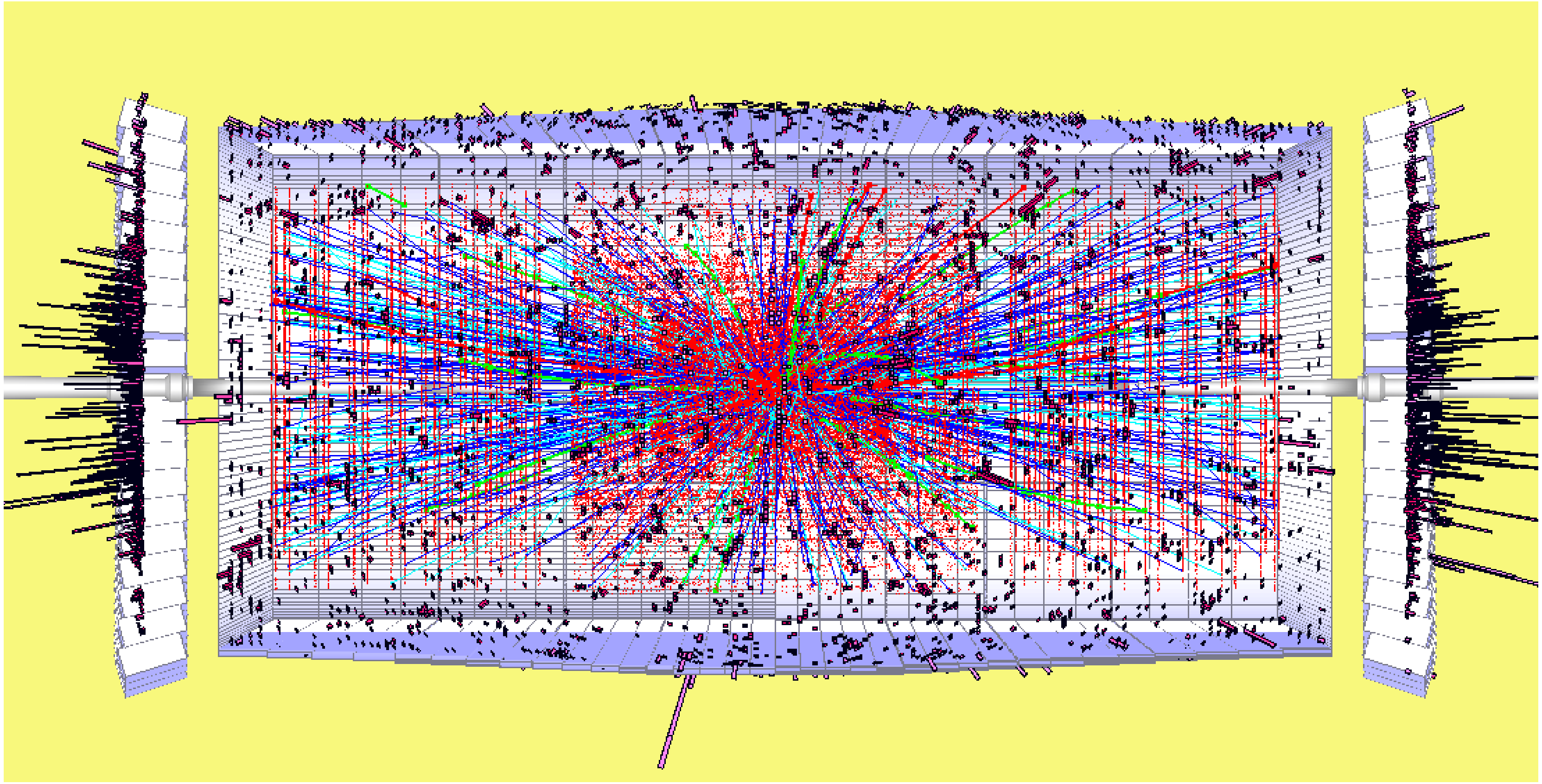
- Several minimum bias collisions are seen in each BX.

10^34



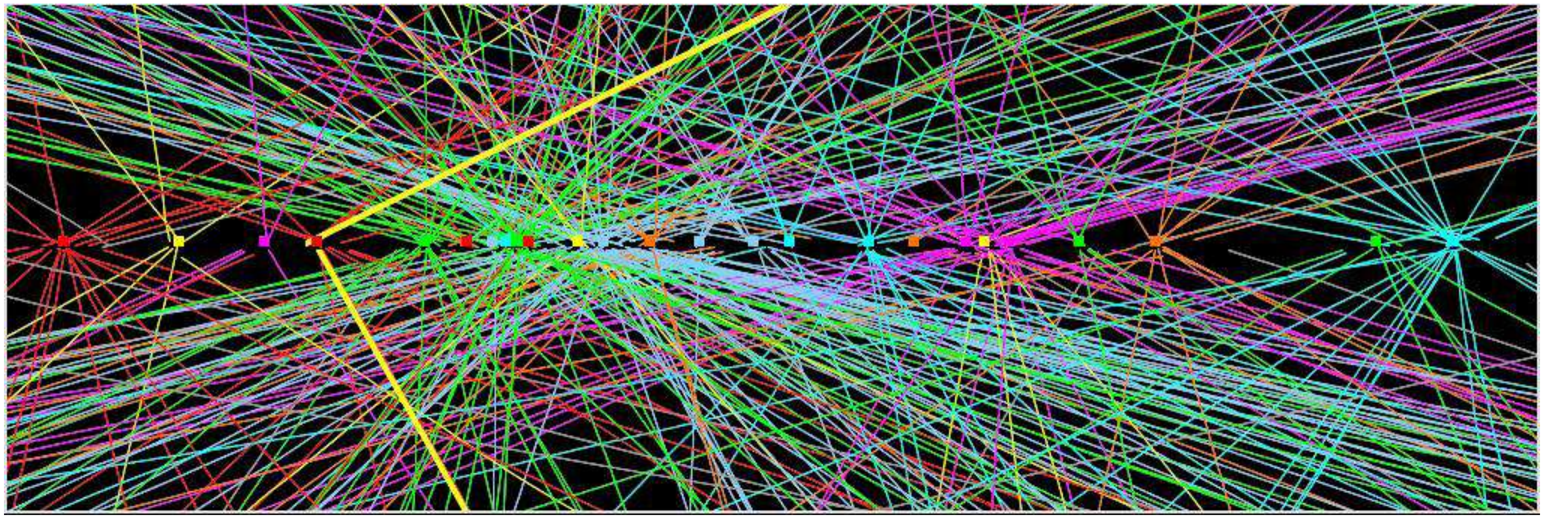
- Many minimum bias events are seen in each BX.

10^35



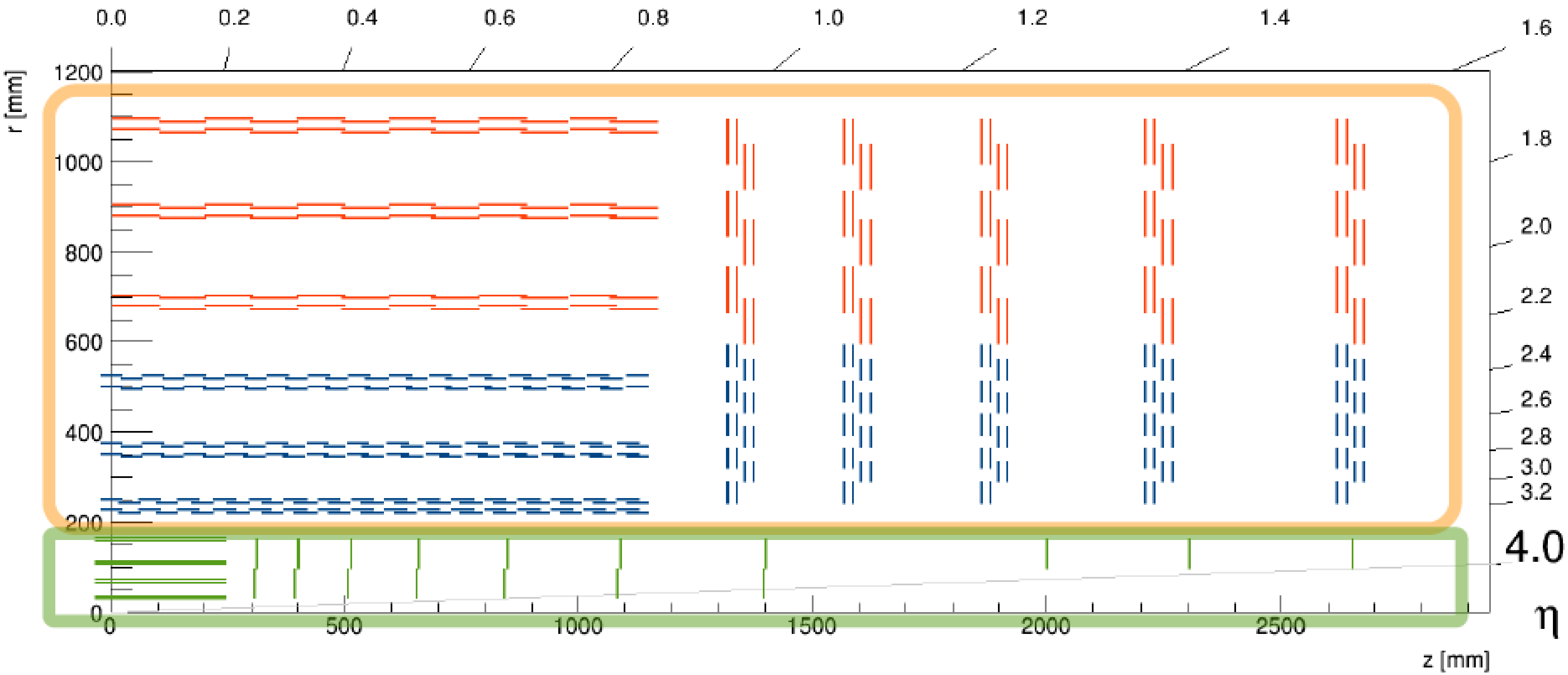
- Hundreds minimum bias events are seen in each BX.

Pileup



- In each beam crossing (BX), there could be up to 200 pileups in LHC detectors.
- All BX look similar, with or without physics events.

Very Large Channel Count

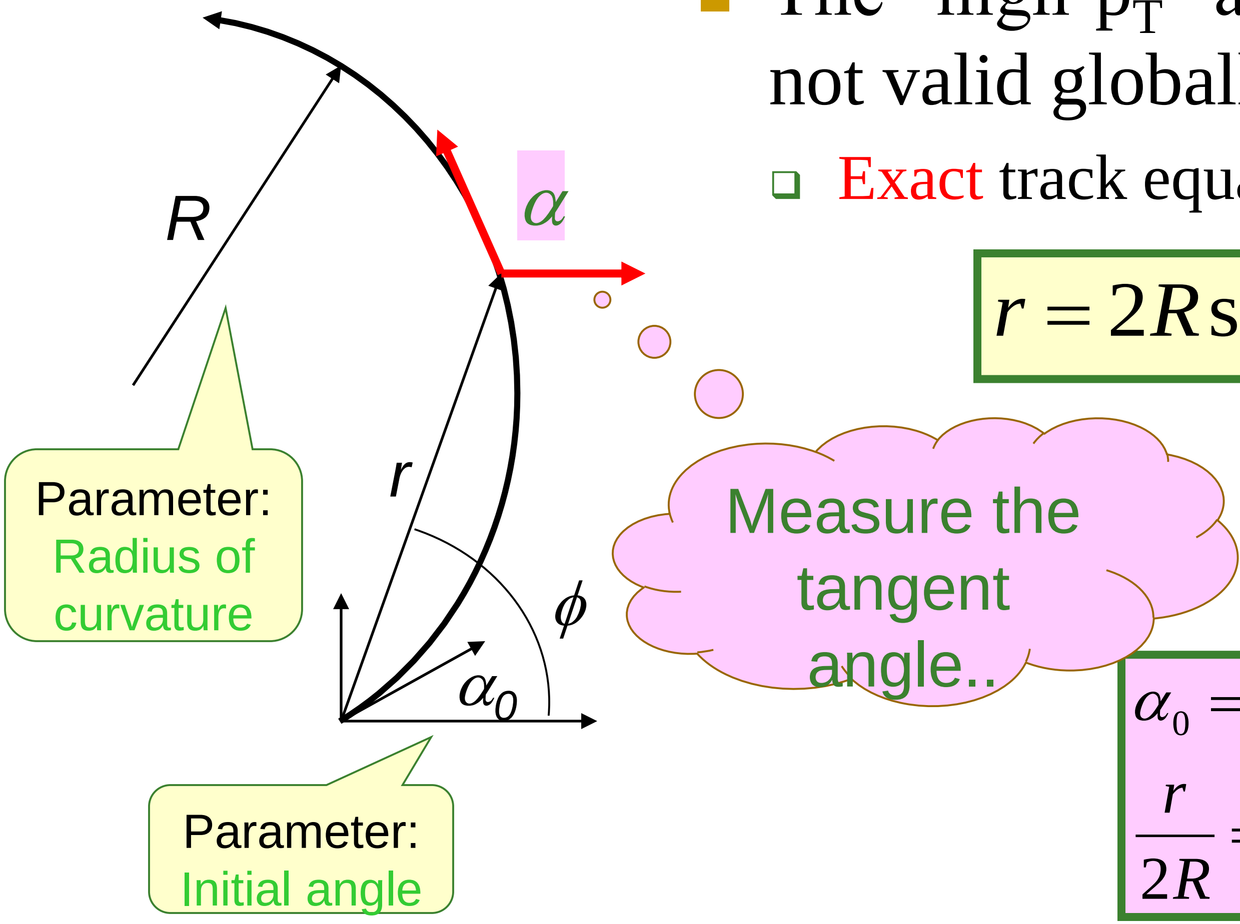


- In high rate tracking detector, silicon pixel or strip detectors are used.
- The detector pitch is fine => large channel counts.

Double-Layer Detectors

A Large Curvature Track

- A soft track hits large φ region.
- The "high-p_T" approximation is not valid globally.
  - Exact track equation is needed.



$$r = 2R\sin(\phi - \alpha_0)$$

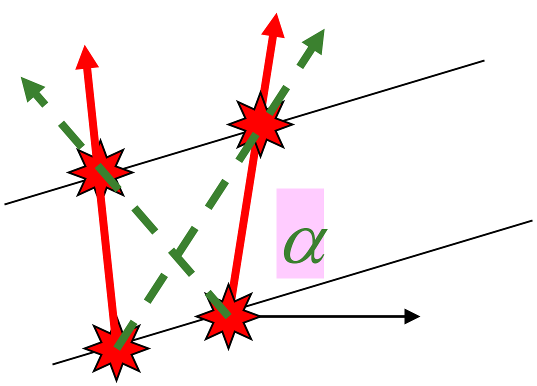
~~$r = 2R(\phi - \alpha_0)$~~

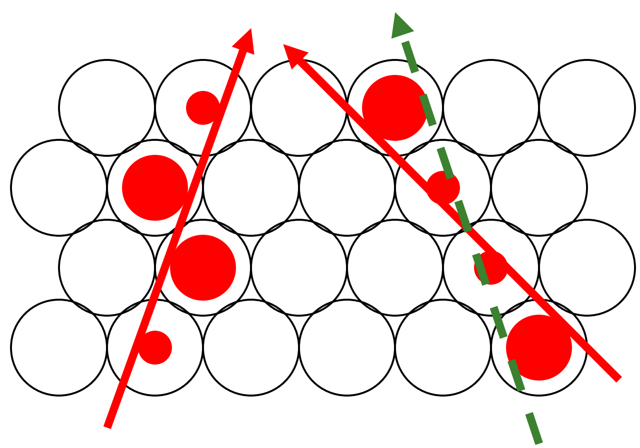
$$\alpha_0 = 2\phi - \alpha$$

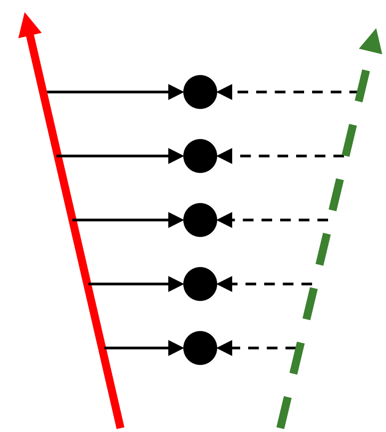
$$\frac{r}{2R} = \sin(\alpha - \phi)$$

Tangent Angle Measurements

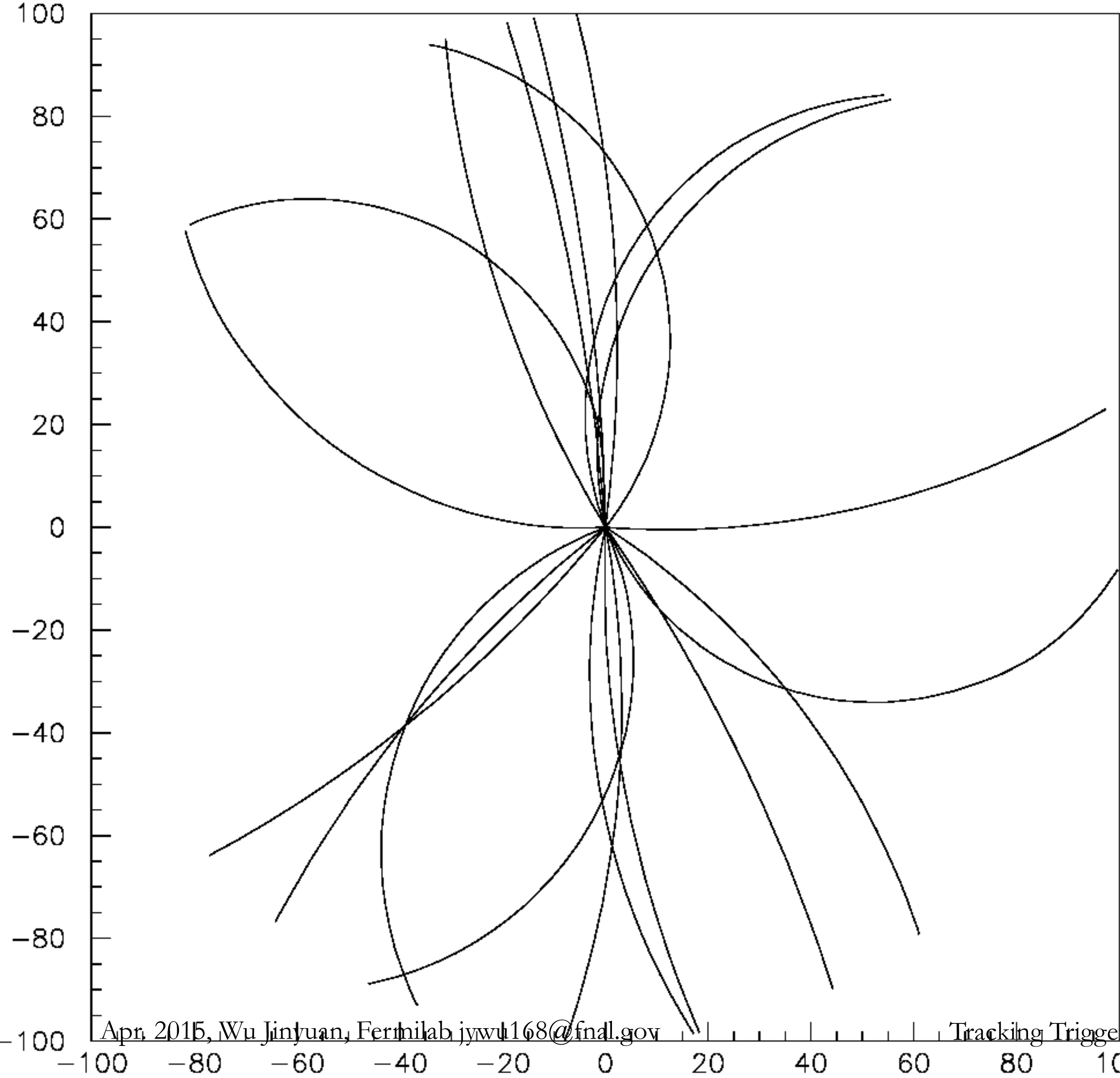
- There are various techniques to measure the tangent angle of the track segment (or "doublet", or "stub").
- Sometimes extra "ghost" segments may exist.
- The ghost segments may be resolved in track recognition process later.





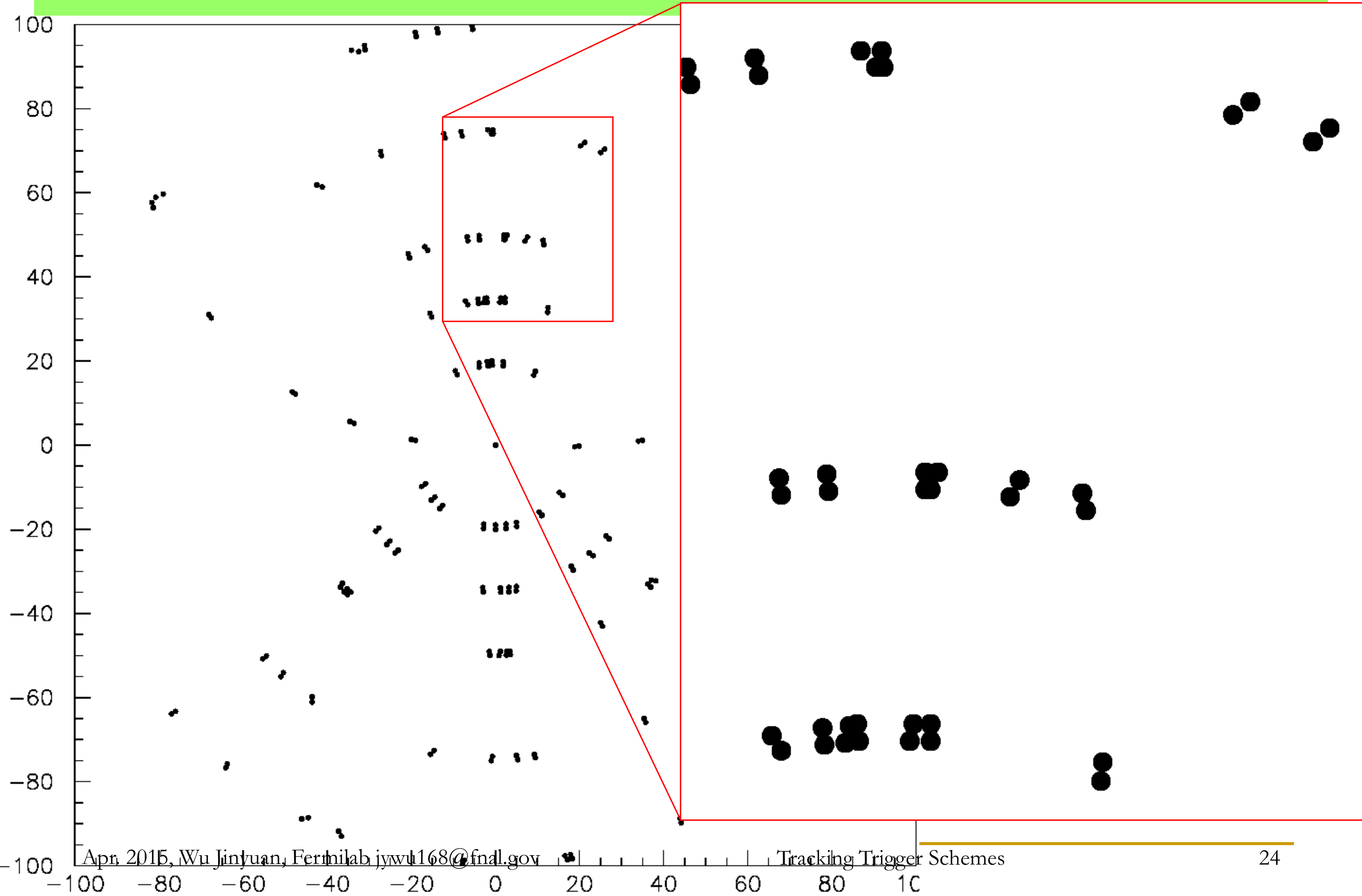


An Example of Track Recognition: *Event*

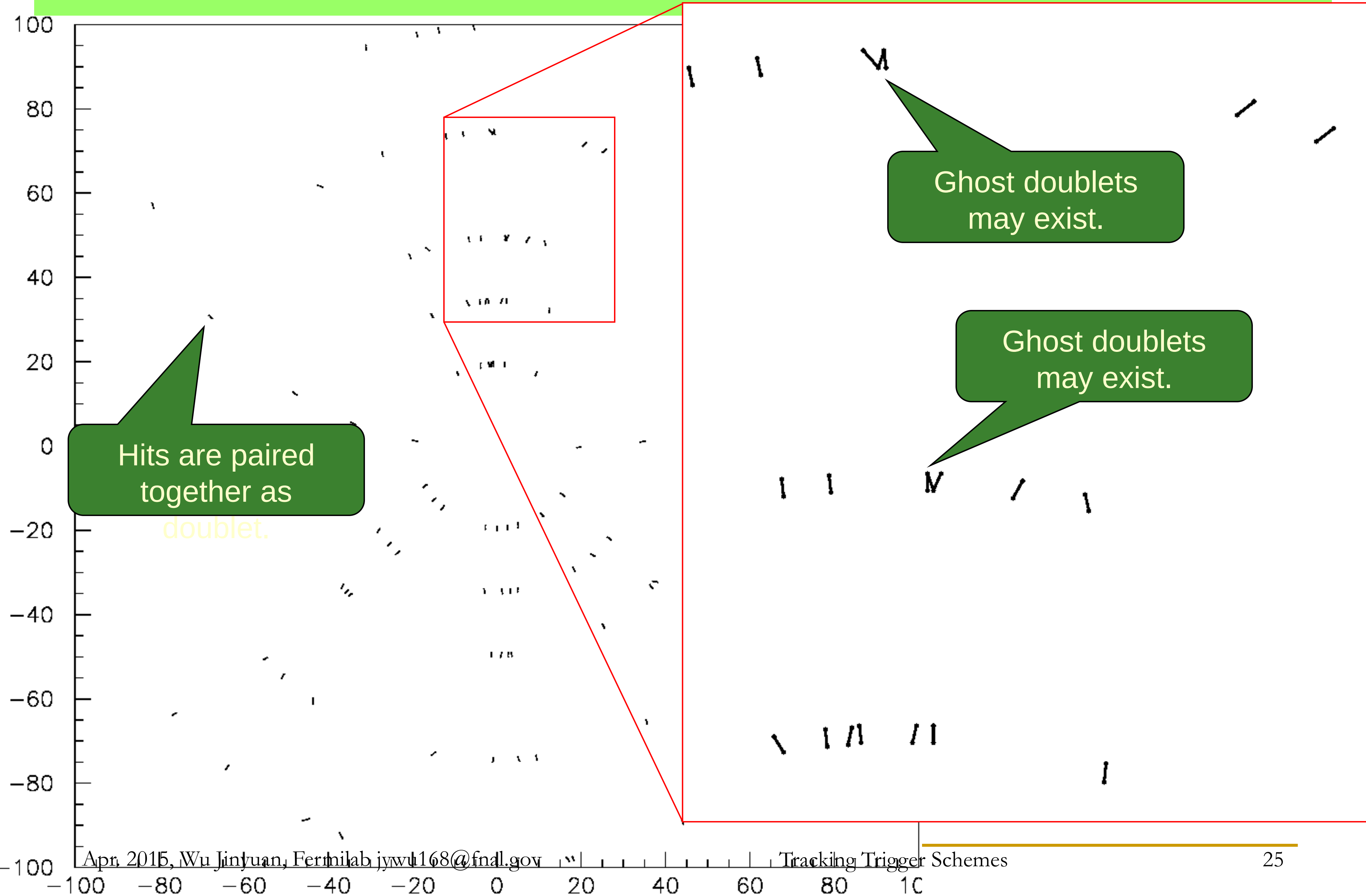


We explain the track recognition process using this 20-track example.

An Example of Track Recognition: *Hits*



An Example of Track Recognition: *Doublets*



An Example of Track Recognition: *Histogram*

$$\alpha_0 = 2\phi - \alpha$$

$$c_0 = \frac{25cm}{R} = \frac{50cm}{r}\sin(\alpha - \phi)$$

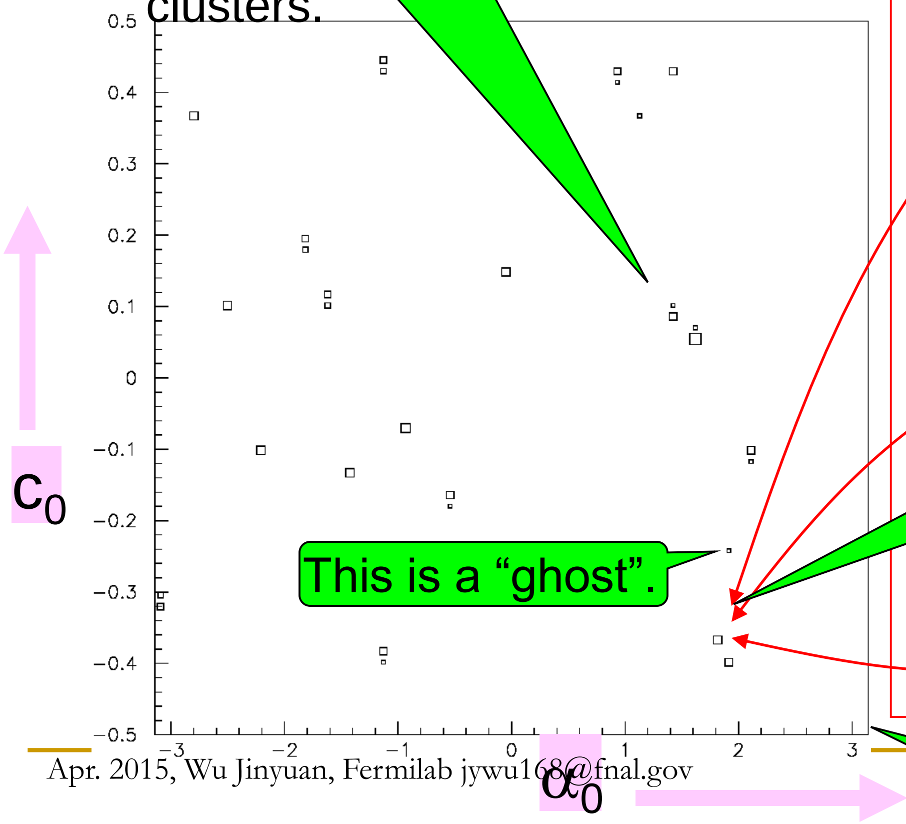
Two track parameters can be calculated for each doublet.

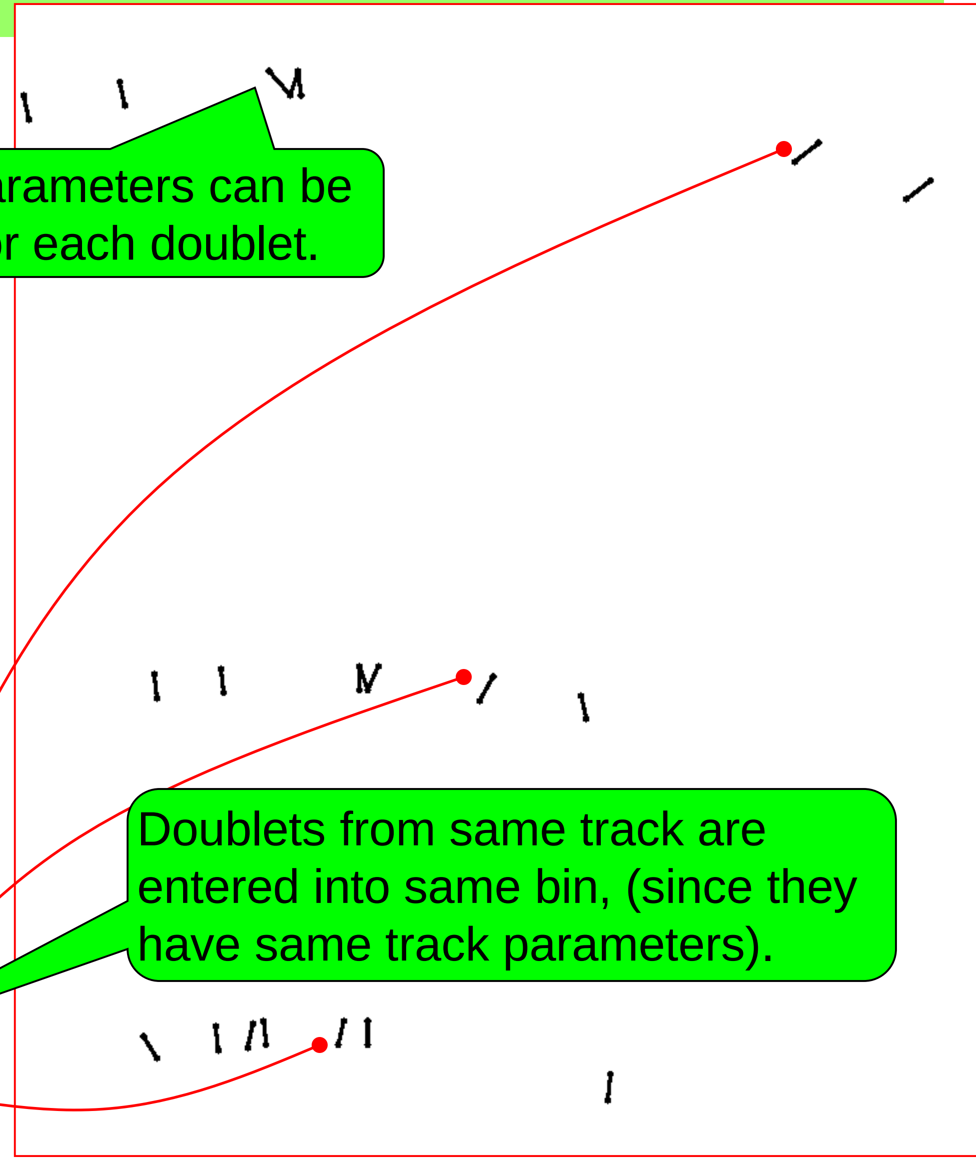
Sometimes they are stored in clusters.

Doublets from same track are entered into same bin, (since they have same track parameters).

This is a "ghost".

A 2-D histogram is booked.



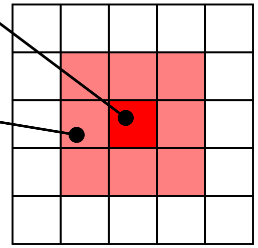


An Example of Track Recognition: *Clustering*

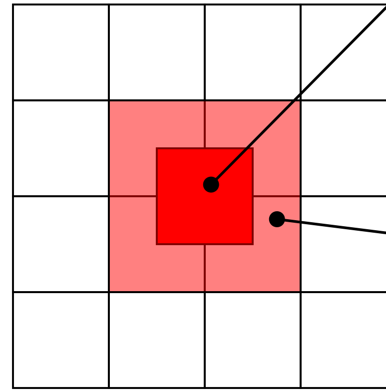
For doublets on the seeding super layer in

search for coincident in these

The 9-bin scheme



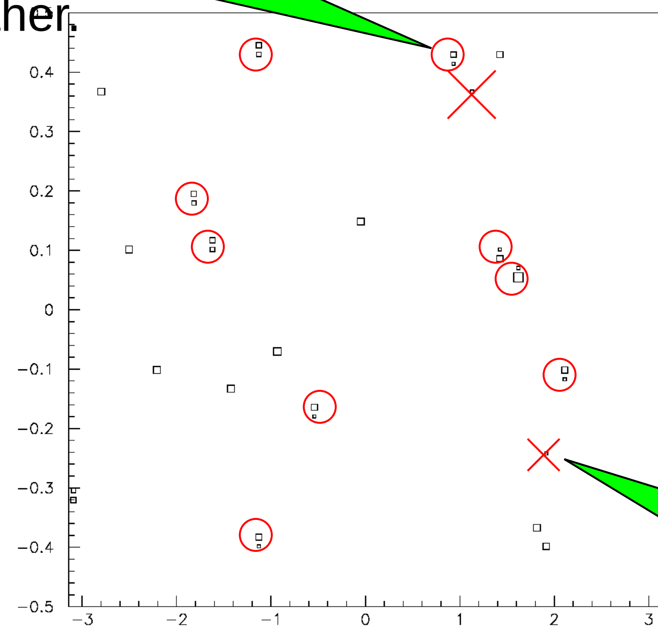
The 4-bin scheme



For doublets on the seeding super layer in

search for coincident in these

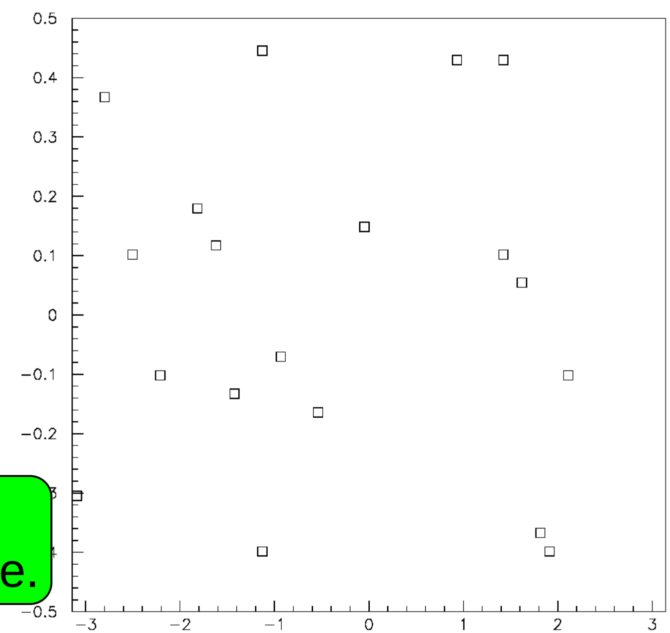
The doublets in clusters are grouped together.



c_0

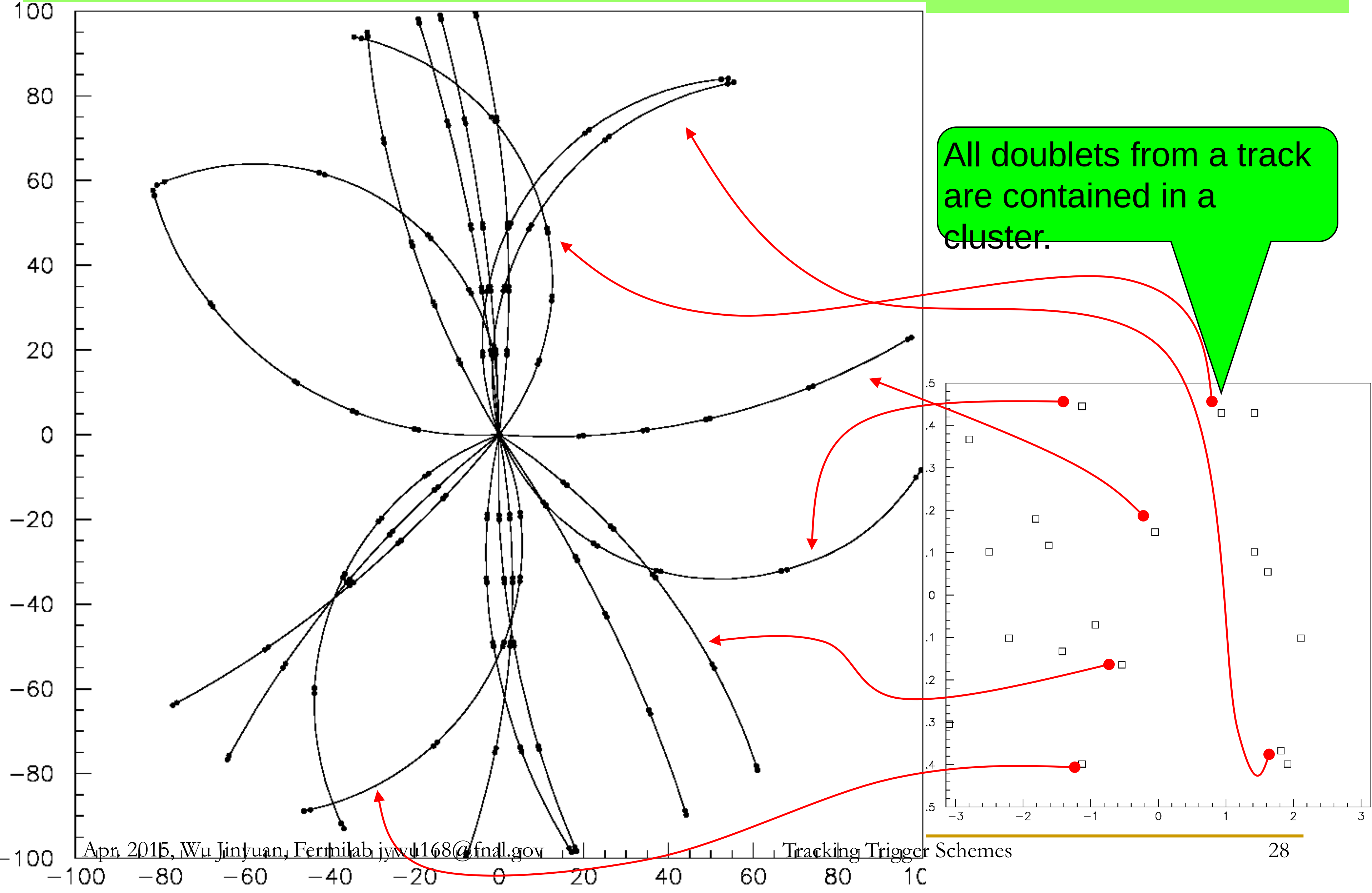
α_0

clustering



The "ghost" doublets are gone.

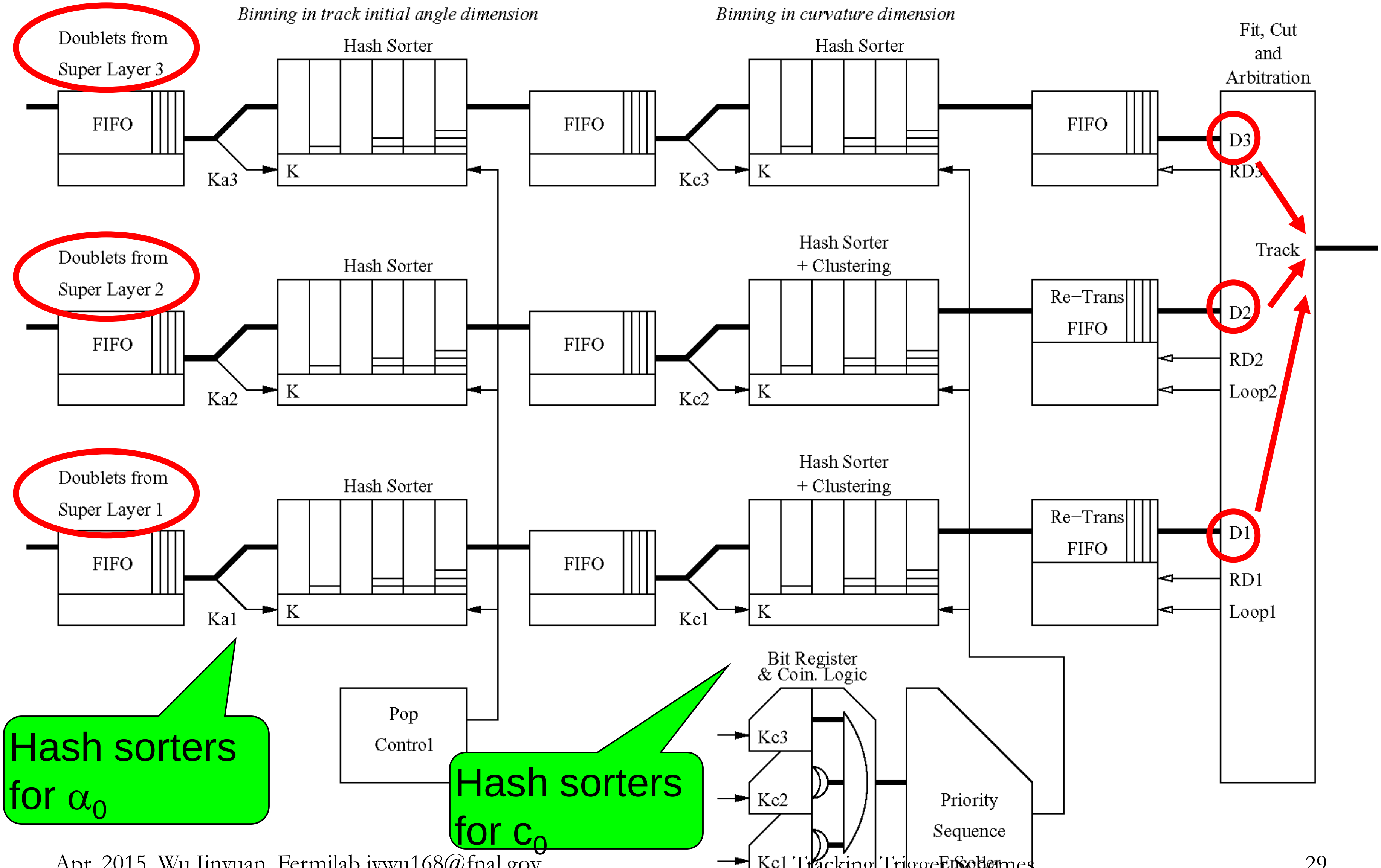
An Example of Track Recognition: *Tracks*



$$\alpha_0 = 2\phi - \alpha$$

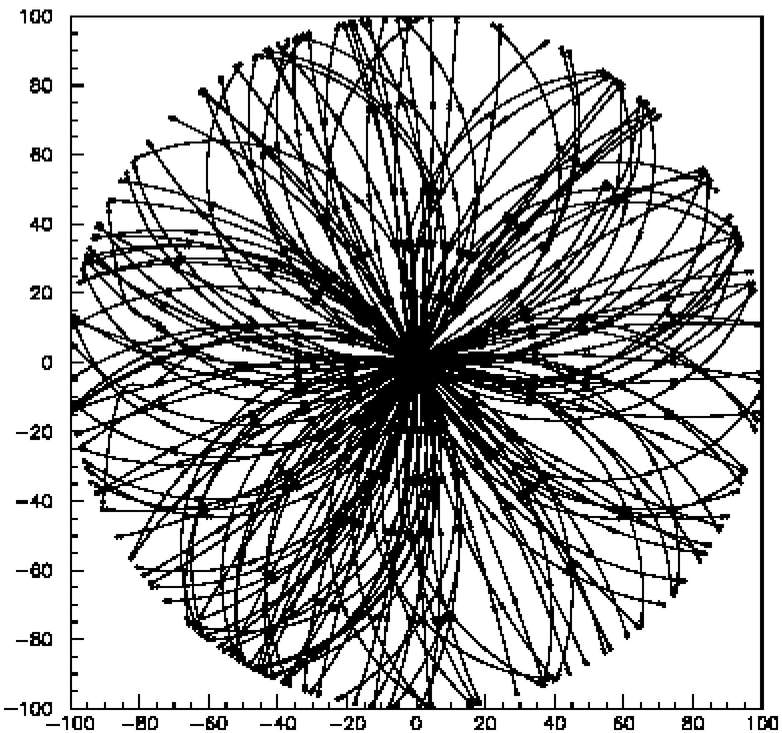
$$c_0 = \frac{25cm}{R} = \frac{50cm}{r}\sin(\alpha - \phi)$$

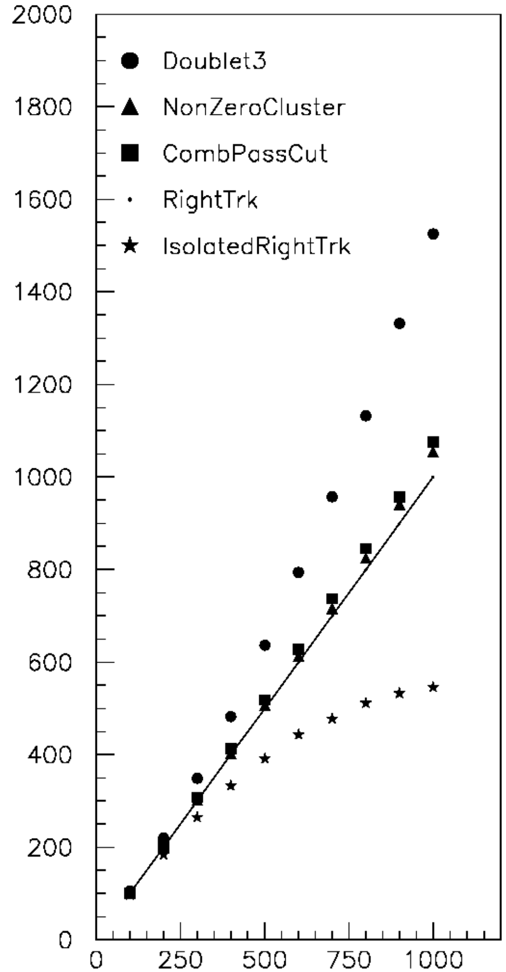
FPGA Block Diagram

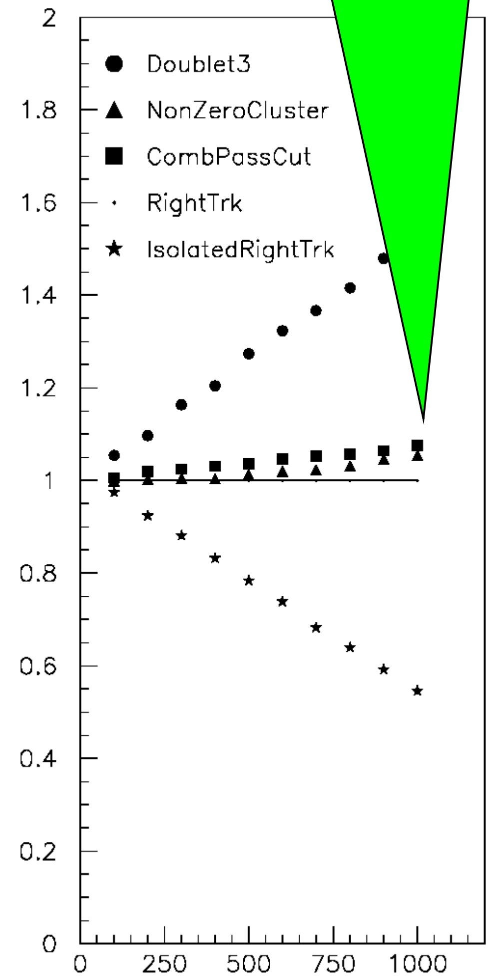


Simulation Results

It still works at 1000 tracks/event







An event with 200 tracks

Without Full Track Recognition

$$\alpha_0 = 2\phi - \alpha$$

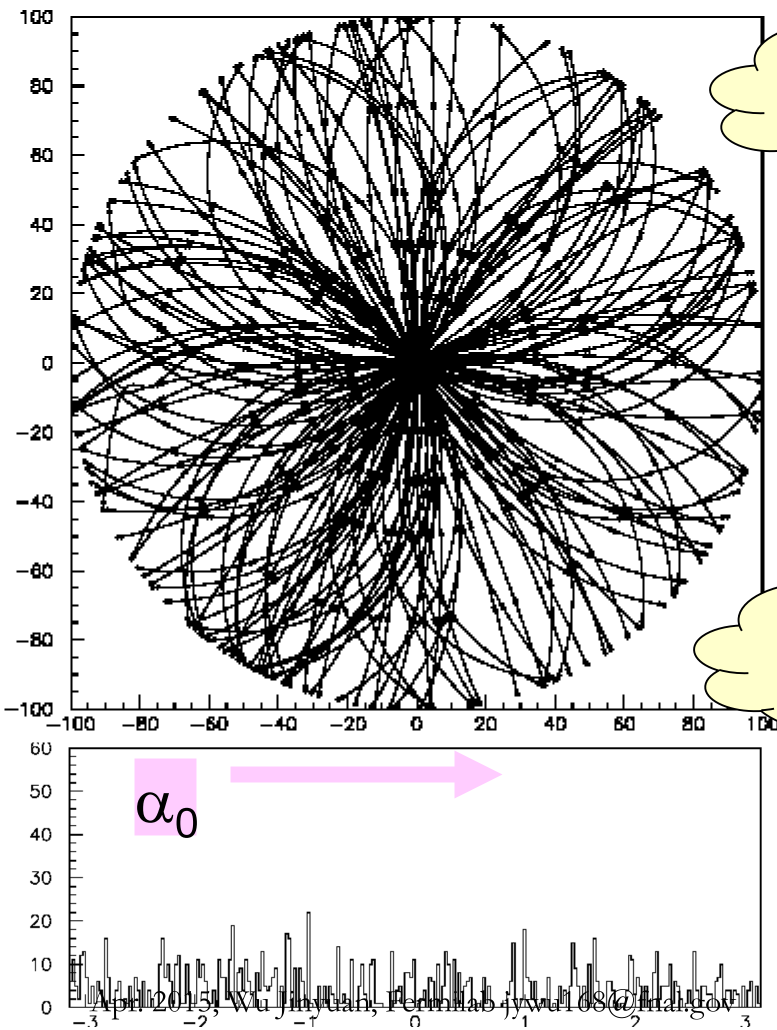
$$c_0 = \frac{25cm}{R} = \frac{50cm}{r}\sin(\alpha - \phi)$$

- Two track parameters can be calculated for each doublet.
- Useful trigger primitives can be found without full track recognition.
- For example…

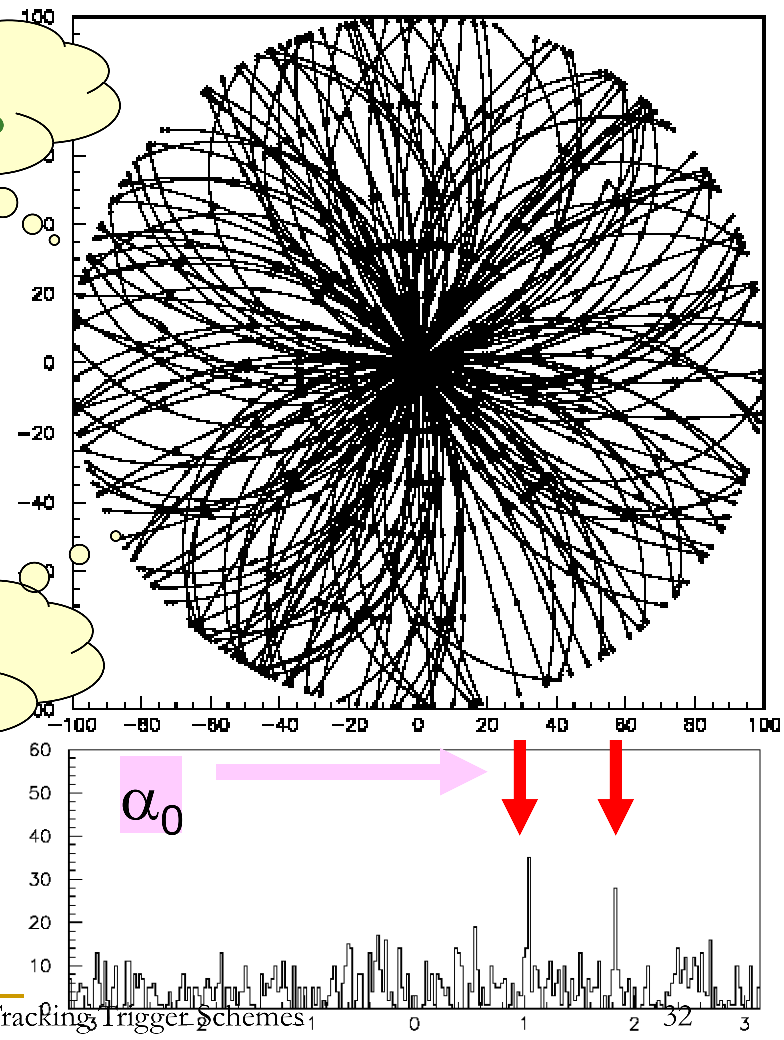
Example: Finding “Soft Jets”

A simulated event with 200 tracks.
Flat distributions.
Min. R = 55 cm

16 soft tracks are added.
They are grouped in 2 small initial angle regions, i.e., 2 “soft jets”.

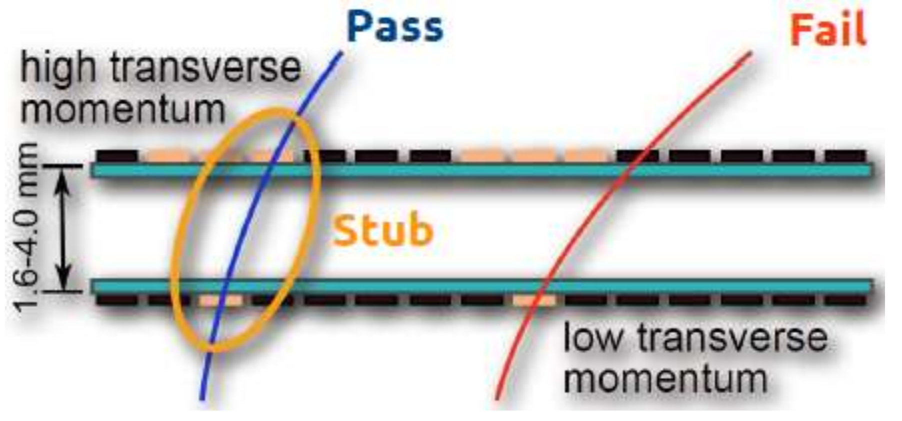


Can you see the “soft jets”?



Can you see the “soft jets” now?

CMS Double-Layer Silicon Tracking Detector

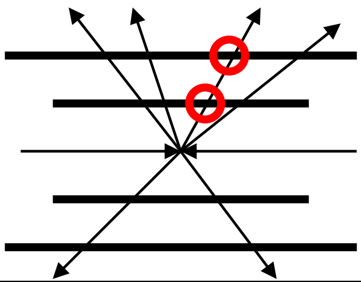


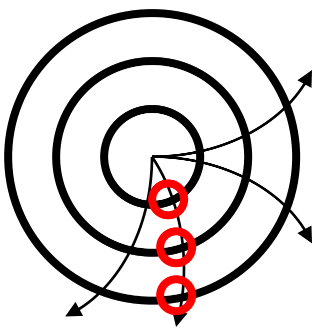
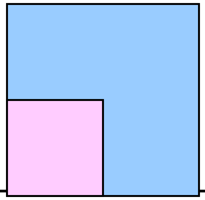
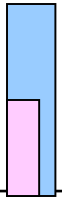
- Two layers of silicon detector.
- Send only High PT stubs to the readout system.

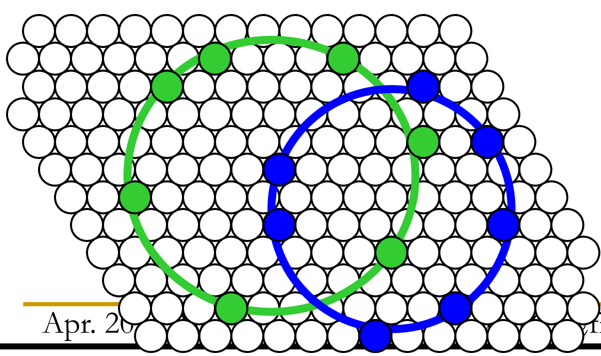
Track Finding

Hit Matching

	Software	FPGA Typical	FPGA Resource Saving Approaches

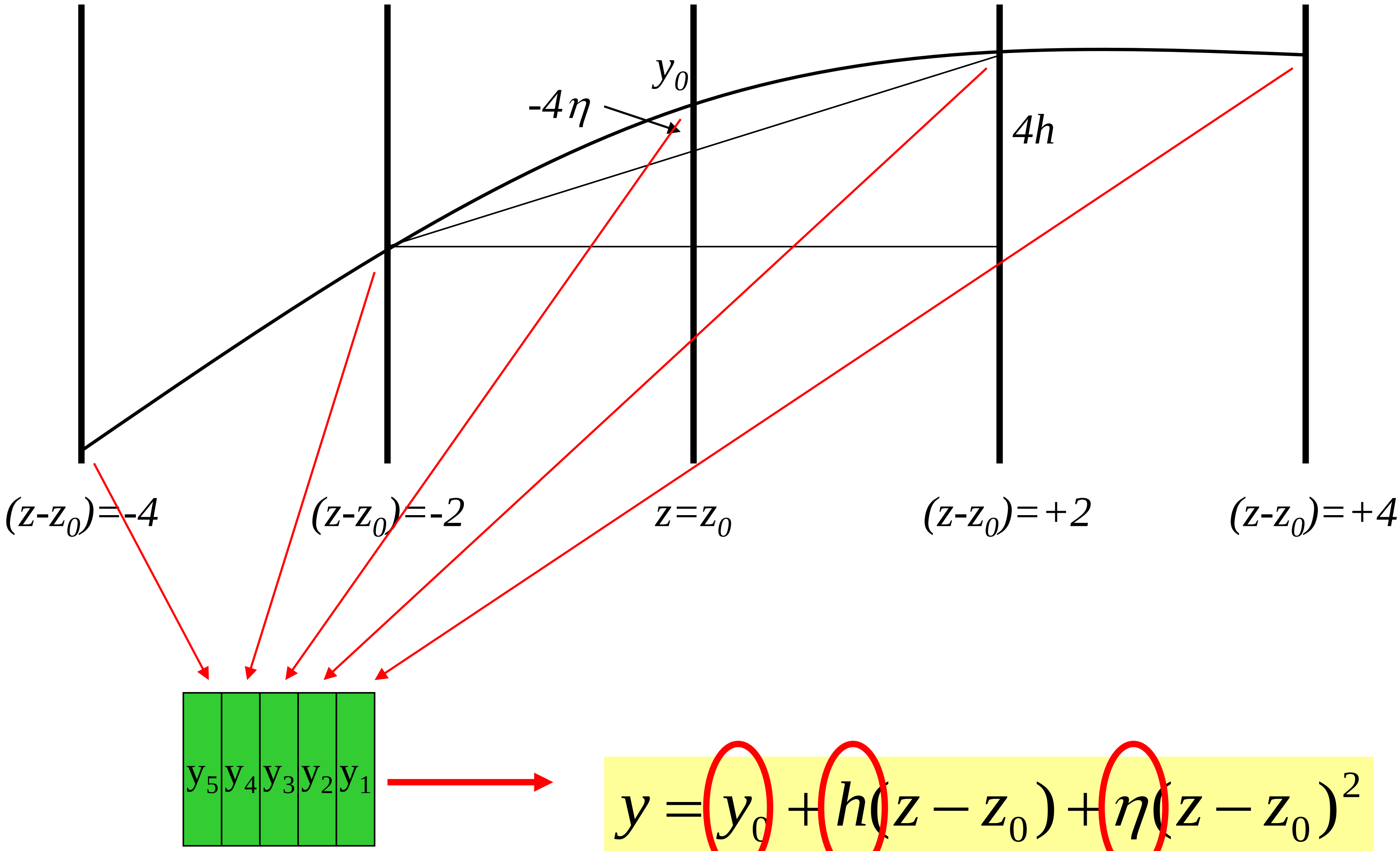
	$O(n^2)$
	for(){
	for(){…}
	}
		$O(n)*O(N)$
		Comparator Array
			Hash Sorter
			$O(n)*O(N)$: in RAM

	$O(n^3)$
	for(){
	for(){
	for(){…}
	}
	}
		$O(n)*O(N^2)$
		CAM, AM
		Hugh Trans.
		
			Tiny Triplet Finder
			$O(n)*O(N*logN)$
			

	$O(n^4)$
	for(){ for(){
	for(){ for()
	{…}
	}}}		

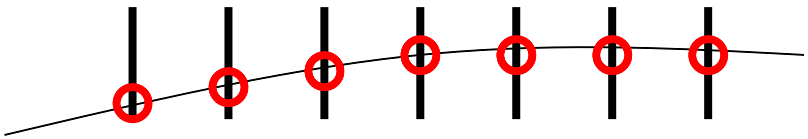
Track Fitting

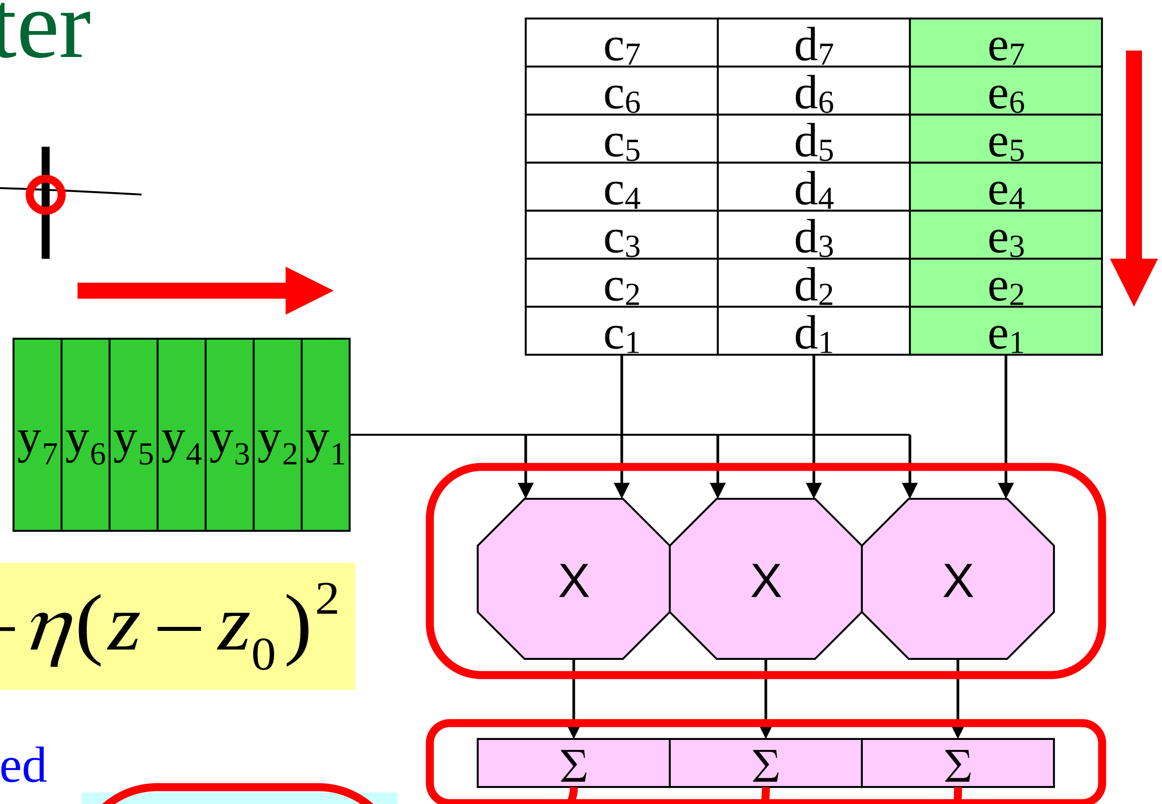
Track Fitting



$$y = y_0 + h(z - z_0) + \eta(z - z_0)^2$$

Least Square Fitter





$$y = y_0 + h(z - z_0) + \eta(z - z_0)^2$$

- The parameters can be described as inner-products.
- Hit coordinates and coefficients are fed simultaneously.
- The inner-products can be calculated with multiplier-accumulator structures.

$$y_0 = \sum_i c_i y_i$$

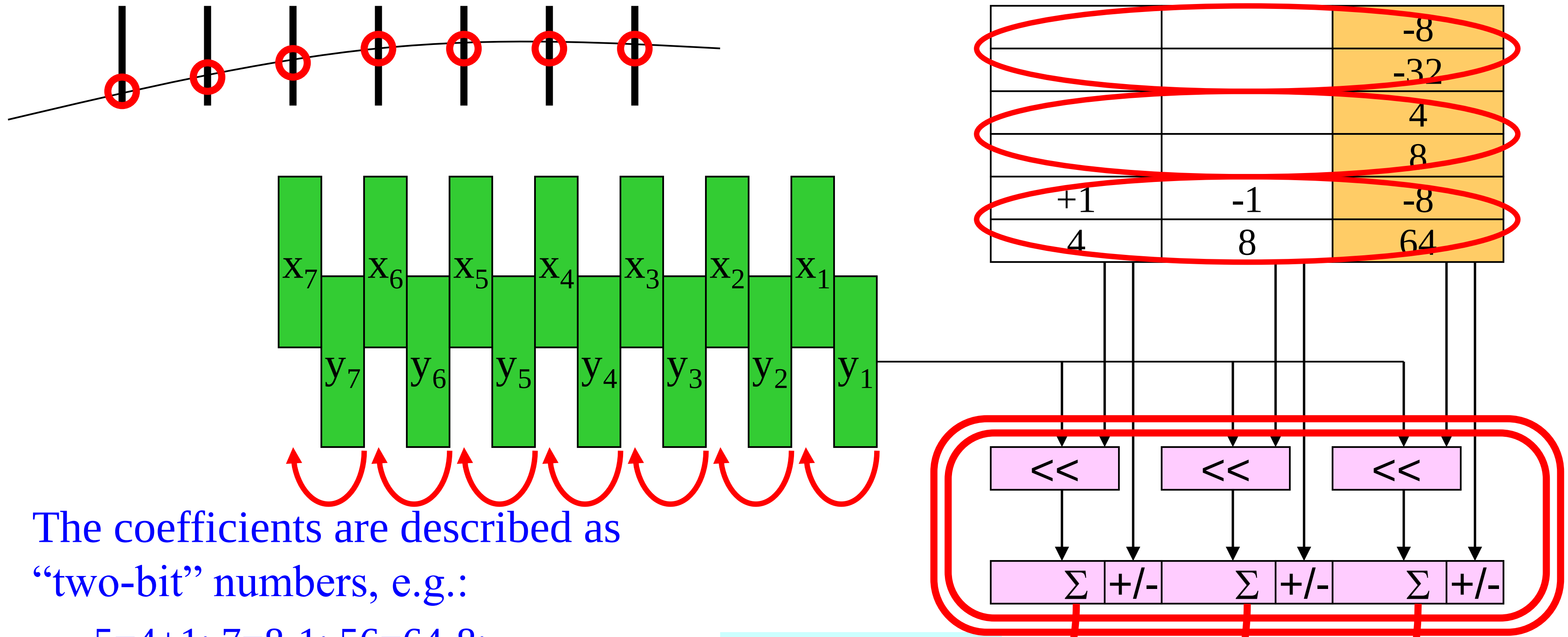
$$h = \sum_i d_i y_i$$

$$\eta = \sum_i e_i y_i$$

Coefficient Table, Least Square Fitter

	Half-length of the Track													
	16		14		12		10		8		6		4	
$z\text{-}z_0$	e_i	e[i]	e_i	e[i]	e_i	e[i]	e_i	e[i]	e_i	e[i]	e_i	e[i]	e_i	e[i]
-16	5.3	6												
-14	3.3	2	7.5	8										
-12	1.6	2	4.3	4	11.3	12								
-10	0.1	0	1.6	2	5.6	5	17.9	18						
-8	-1.1	0	-0.7	-2	1.0	1	7.2	7	31.0	31				
-6	-2.0	-3	-2.4	-2	-2.6	-4	-1.2	-1	7.8	8	61.0	56		
-4	-2.6	-3	-3.6	-5	-5.1	-5	-7.2	-8	-8.9	-9	0.0	12	146.3	144
-2	-3.0	-3	-4.4	-4	-6.6	-5	-10.7	-9	-18.8	-20	-36.6	-40	-73.1	-64
0	-3.2	-2	-4.6	-2	-7.2	-8	-11.9	-14	-22.2	-20	-48.8	-56	-146.3	-160
2	-3.0	-3	-4.4	-4	-6.6	-5	-10.7	-9	-18.8	-20	-36.6	-40	-73.1	-64
4	-2.6	-3	-3.6	-5	-5.1	-5	-7.2	-8	-8.9	-9	0.0	12	146.3	144
6	-2.0	-3	-2.4	-2	-2.6	-4	-1.2	-1	7.8	8	61.0	56		
8	-1.1	0	-0.7	-2	1.0	1	7.2	7	31.0	31				
10	0.1	0	1.6	2	5.6	5	17.9	18						
12	1.6	2	4.3	4	11.3	12								
14	3.3	2	7.5	8										
16	5.3	6												
Error	2.91	3.02	3.05	3.15	3.22	3.26	3.41	3.43	3.65	3.65	3.93	3.99	4.28	4.29
Ratio		1.04		1.03		1.01		1.00		1.00		1.02		1.00

Multiplier-less (ML) Quasi-Least Square Fitter



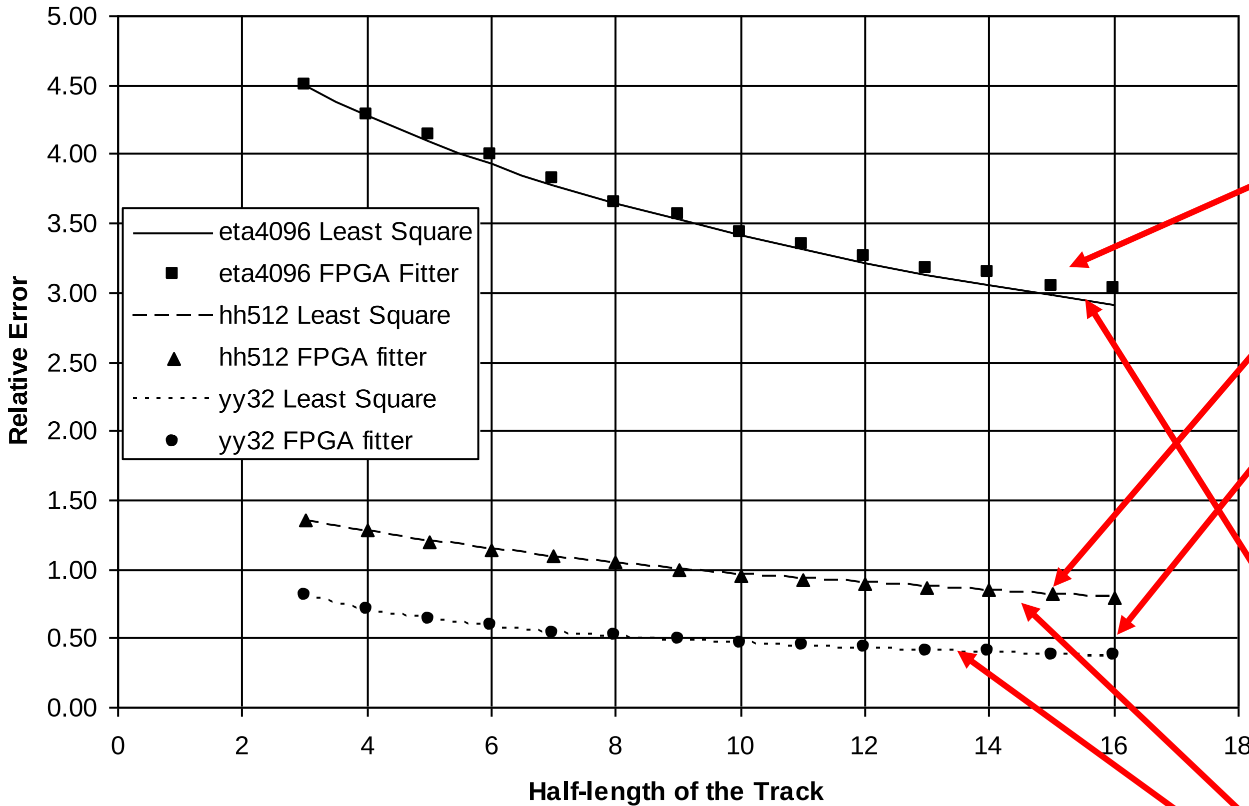
- The coefficients are described as “two-bit” numbers, e.g.:
  - 5=4+1; 7=8-1; 56=64-8;
- The multiplication is replaced with two shift & add/sub operations.
- There are two clock cycles to fetch a measurement point (i.e., y_1, y_2, etc.) allowing two shift & add/sub operations

$$y_0 = \sum_i c_i y_i$$

$$h = \sum_i d_i y_i$$

$$\eta = \sum_i e_i y_i$$

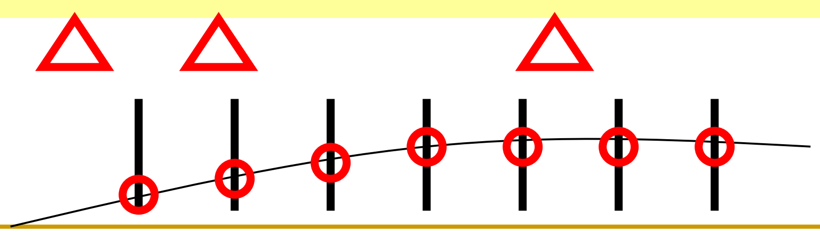
Inaccuracy Doesn't Matter, A Lot of Time



Multiplier-less Quasi-Least Square FPGA Fitter

Least Square Fitter

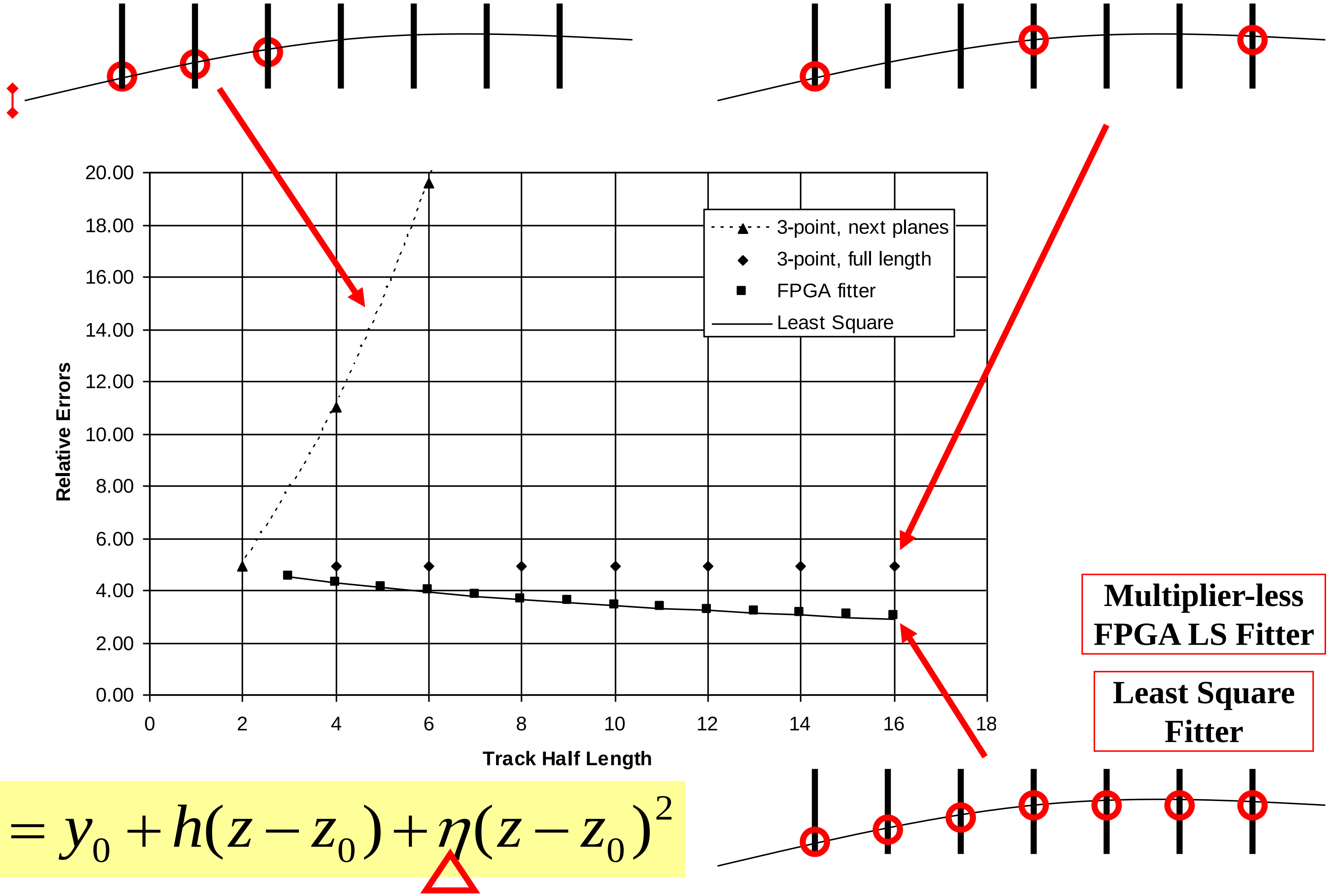
$$y = y_0 + h(z - z_0) + \eta(z - z_0)^2$$



Coefficient Table, ML Fitter

	Half-length of the Track													
	16		14		12		10		8		6		4	
z-z_0	e_i	e[i]	e_i	e[i]	e_i	e[i]	e_i	e[i]	e_i	e[i]	e_i	e[i]	e_i	e[i]
-16	5.3	6												
-14	3.3	2	7.5	8										
-12	1.6	2	4.3	4	11.3	12								
-10	0.1	0	1.6	2	5.6	5	17.9	18						
-8	-1.1	0	-0.7	-2	1.0	1	7.2	7	31.0	31				
-6	-2.0	-3	-2.4	-2	-2.6	-4	-1.2	-1	7.8	8	61.0	56		
-4	-2.6	-3	-3.6	-5	-5.1	-5	-7.2	-8	-8.9	-9	0.0	12	146.3	144
-2	-3.0	-3	-4.4	-4	-6.6	-5	-10.7	-9	-18.8	-20	-36.6	-40	-73.1	-64
0	-3.2	-2	-4.6	-2	-7.2	-8	-11.9	-14	-22.2	-20	-48.8	-56	-146.3	-160
2	-3.0	-3	-4.4	-4	-6.6	-5	-10.7	-9	-18.8	-20	-36.6	-40	-73.1	-64
4	-2.6	-3	-3.6	-5	-5.1	-5	-7.2	-8	-8.9	-9	0.0	12	146.3	144
6	-2.0	-3	-2.4	-2	-2.6	-4	-1.2	-1	7.8	8	61.0	56		
8	-1.1	0	-0.7	-2	1.0	1	7.2	7	31.0	31				
10	0.1	0	1.6	2	5.6	5	17.9	18						
12	1.6	2	4.3	4	11.3	12								
14	3.3	2	7.5	8										
16	5.3	6												
Error	2.91	3.02	3.05	3.15	3.22	3.26	3.41	3.43	3.65	3.65	3.93	3.99	4.28	4.29
Ratio		1.04		1.03		1.01		1.00		1.00		1.02		1.00

Relative Errors of Several Track Fitter Schemes

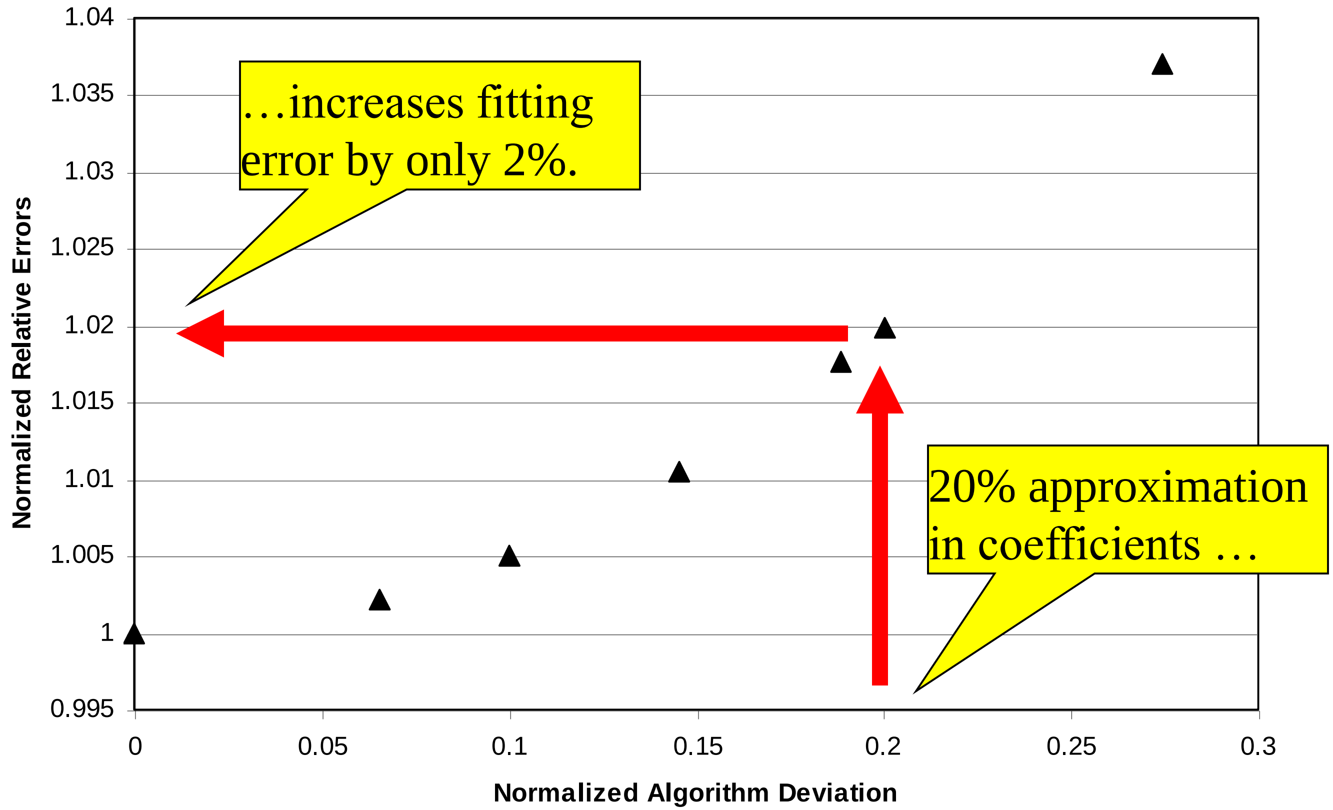


Multiplier-less FPGA LS Fitter

Least Square Fitter

$$y = y_0 + h(z - z_0) + \eta(z - z_0)^2$$

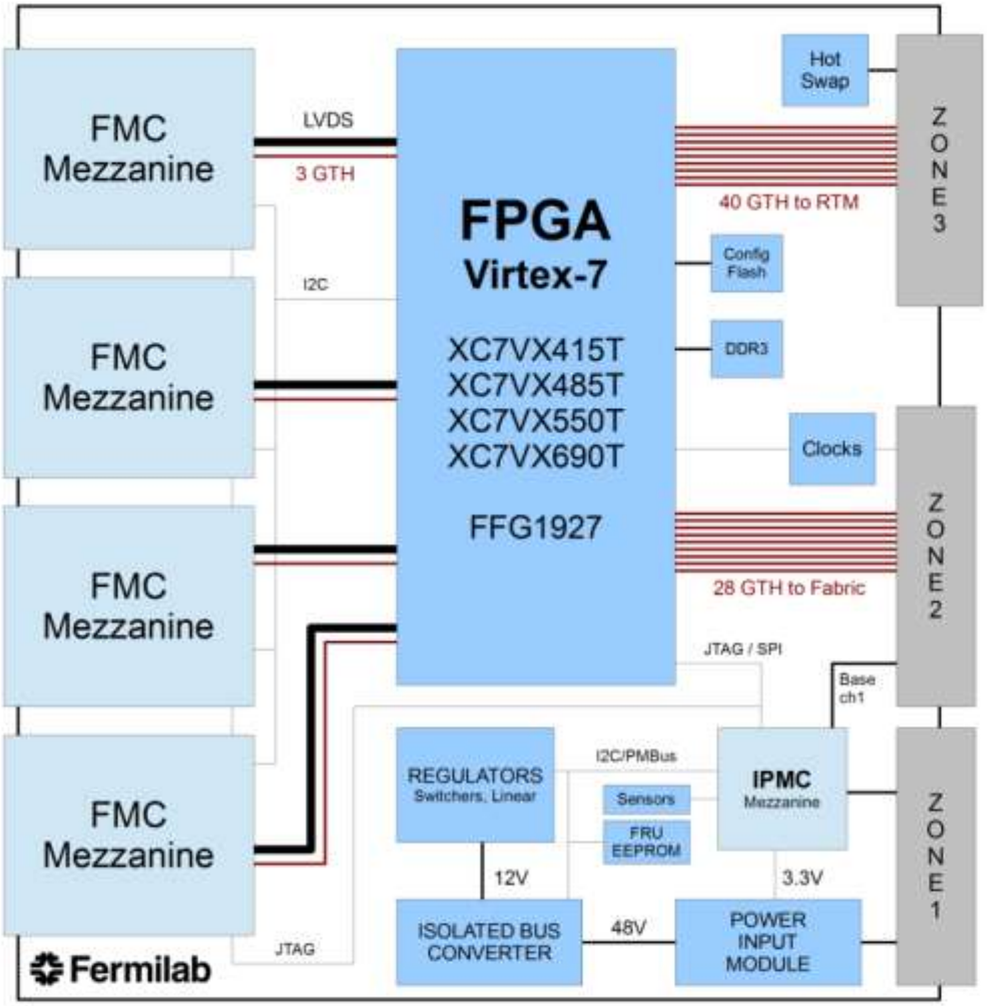
Fitting Errors From Approximations



$$(\delta a_j)^2 = (\delta y)^2 \sum_{i=1}^{n} (G_{ji})^2 + (\delta y)^2 \sum_{i=1}^{n} (\Delta g_{ji})^2$$

Some Efforts in FNAL

Next Generation: Pulsar IIb



The Pulsar IIb represents a big increase in I/O bandwidth, FPGA logic, and power. It was designed with the CMS L1 tracking trigger in mind.

Xilinx Virtex 7 FPGA
- XC7VX415T – XC7VX690T

Up to 80 GTH transceivers
- 40 for RTM
- 28 for Fabric
- 12 for Mezzanines

Four FMC Mezzanines
- Up to 35W each
- LVDS up to 34 Gbps unidirectional
- 3 x GTH up to 30 Gbps bidirectional

IPMC Mezzanine Card

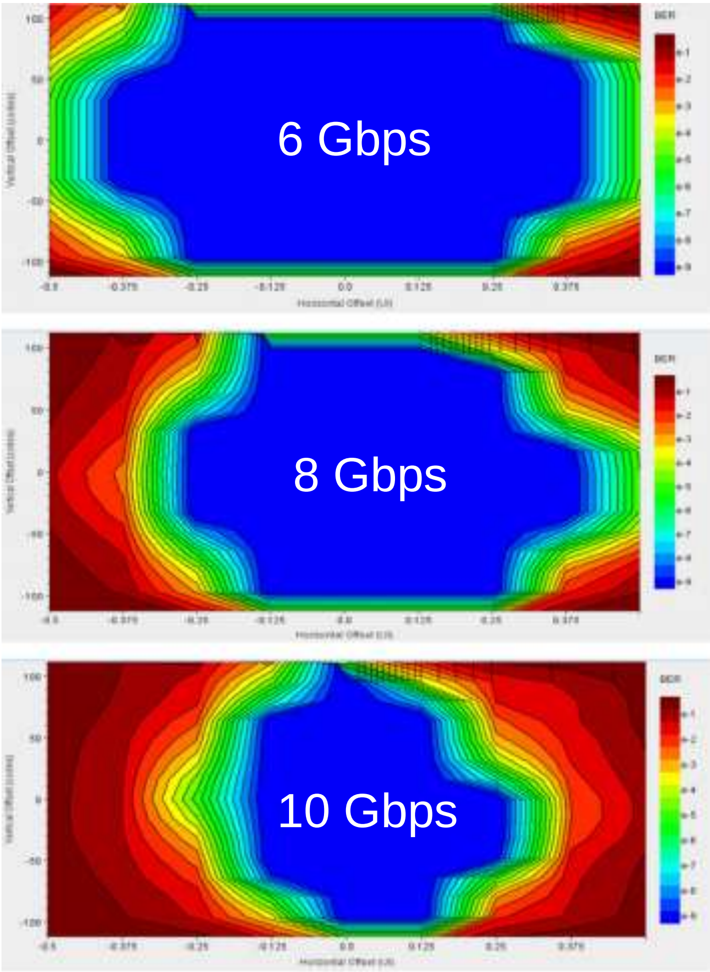
Backplane clock distribution
- M-LVDS on CLK3A and CLK3B

Pulsar IIb and RTM

First Boards Received May 2014

GTH Transceiver Tuning

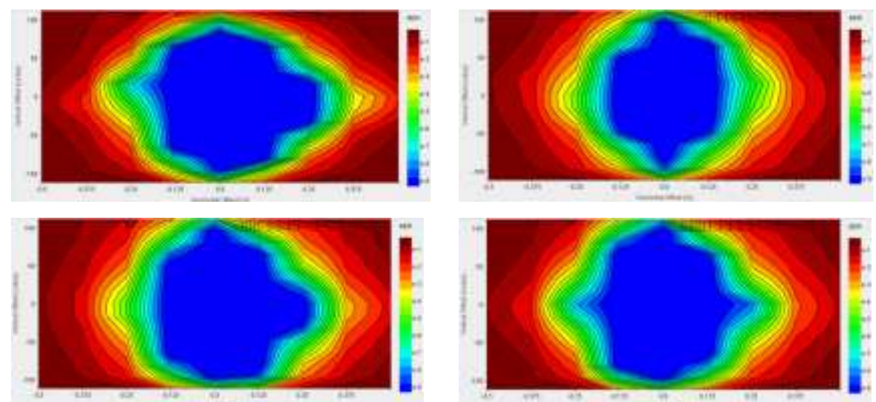
- The quality of all 80 GTH transceiver channels tested with the Xilinx IBERT tool
- Statistical “eye diagrams” based on BER measurements determine RX margins
- GTH transceiver tuning parameters
  - TX_DIFF_SWING
  - TX Pre/Post Cursor
  - RX termination
  - RX LPM/DFE
- IBERT-like functionality built into user firmware using MicroBlaze processor (Northwestern U.)
- Remotely tuning individual transceivers is possible, but not anticipated.



Example RTM channel with 0dB QSFP+ loopback adapter, after tuning transceiver parameters

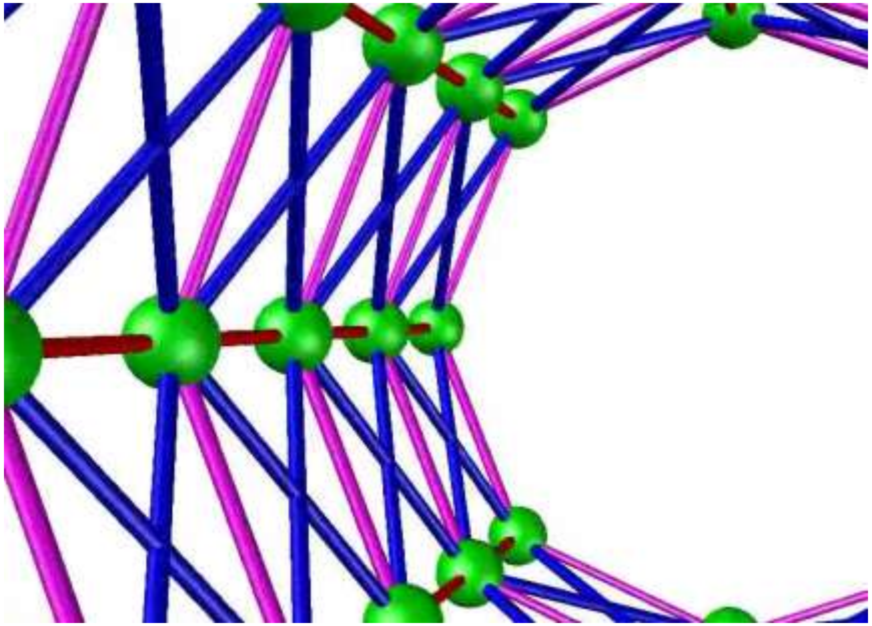
Pulsar IIb Backplane Fabric Channel Testing

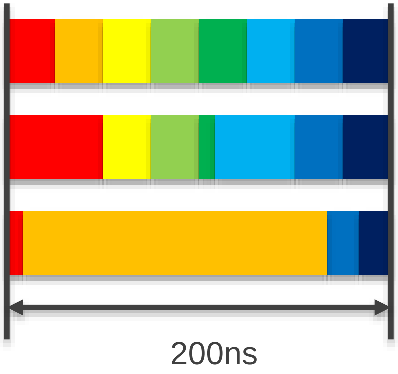
- Full shelf tests with all lanes running at 10 Gbps
  - No bit errors after several days
  - BER = 2×10^{-16}
- We are currently evaluating the latest high performance 40G+ full mesh backplanes from ASIS-PRO, COMTEL, and Pentair/Schroff
- No apparent signal degradation across the width of the backplane



Next Steps: CMS L1 Tracking Trigger Vertical Slice Demo

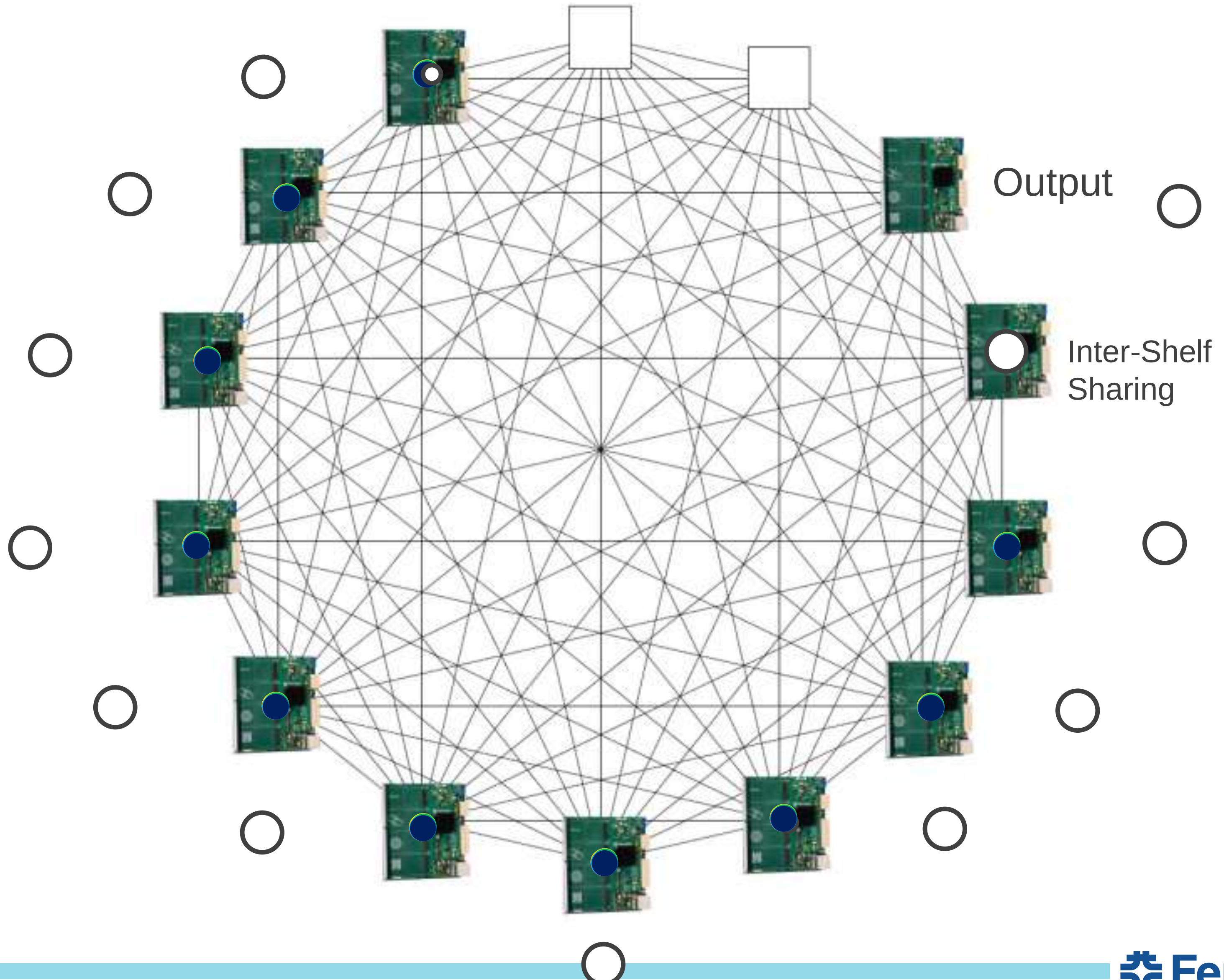
- 6 x 8 towers
- Nearest neighbor sharing
- 1 tower = 1 ATCA shelf
- ~350 input links/tower
- Parallel track finder engines on Mezzanine cards
  - AM / VIPRAM Based
- Use the full mesh backplane to maximum effect…





Input links use a fixed length 8 BX frame. The number of stubs per BX is variable, up to a maximum of 12 stubs.

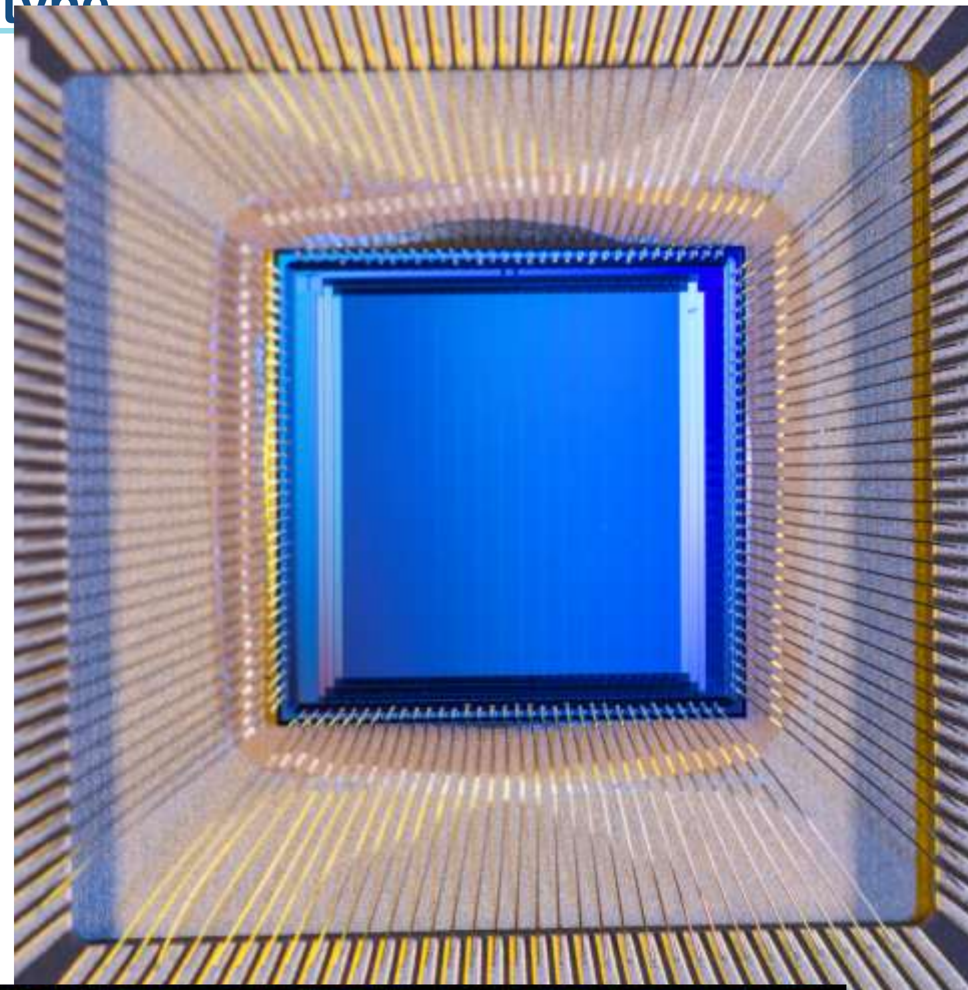
Mesh Transfer

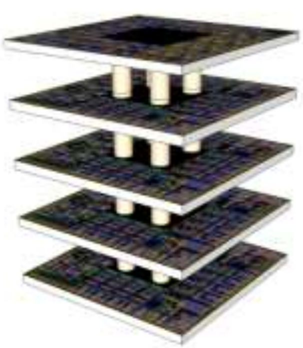


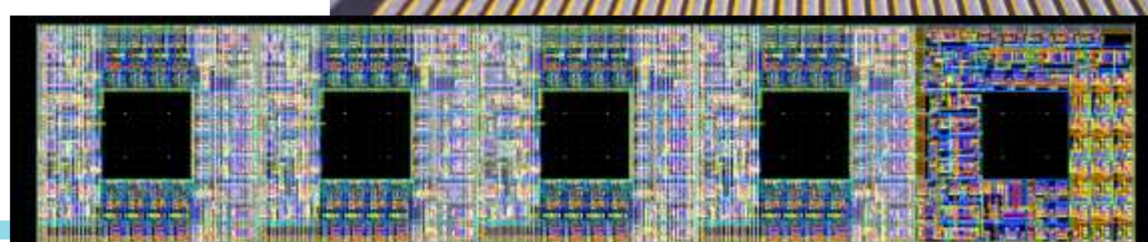
Fermilab

protoVIPRAM – our first prototype

A Tested, Functioning Chip

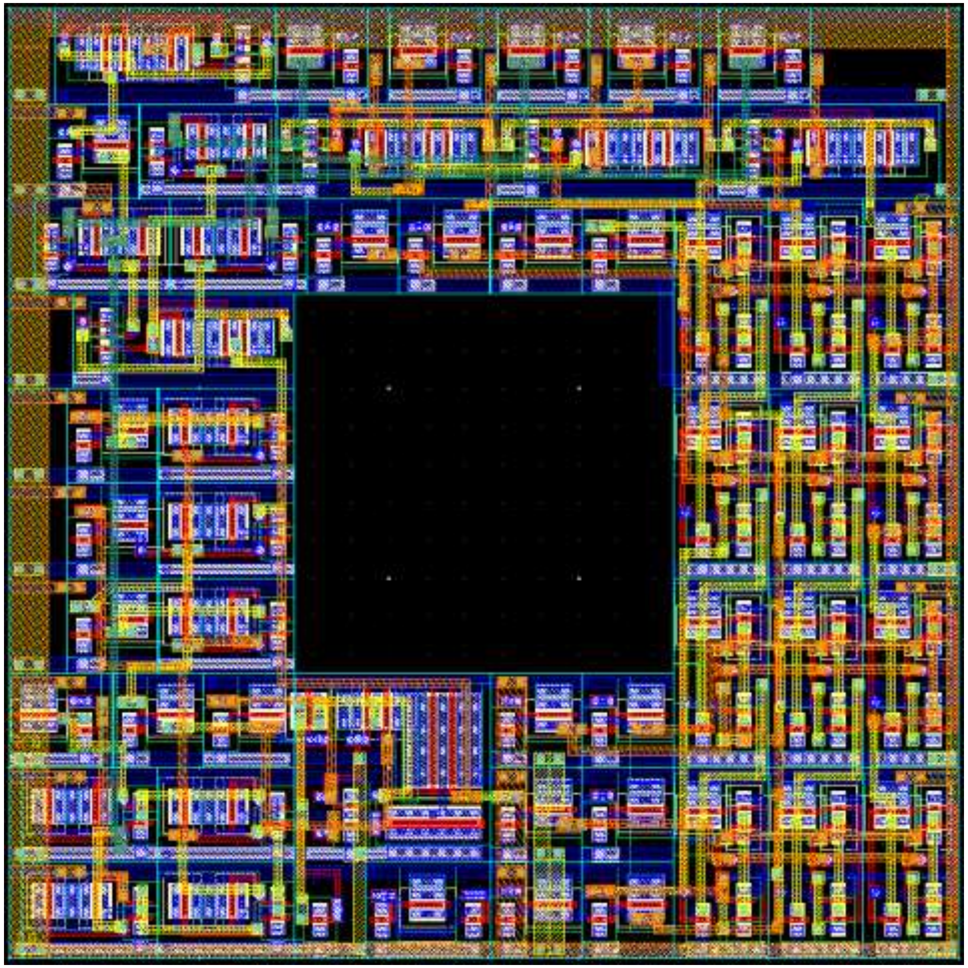






The Existing 2D protoVIPRAM

The Control Cell



The Existing 2D protoVIPRAM

- 4-Layer Road Cell

The Road Cell

- 4 CAM Cells with one Control Cell
- The layout of the cells themselves requires an area 25x125 μm²
- An area 10x125 μm² was added to allow for routing *within* the Road Ce
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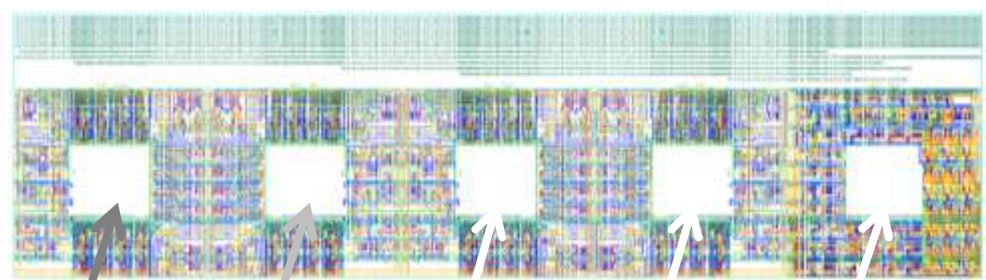

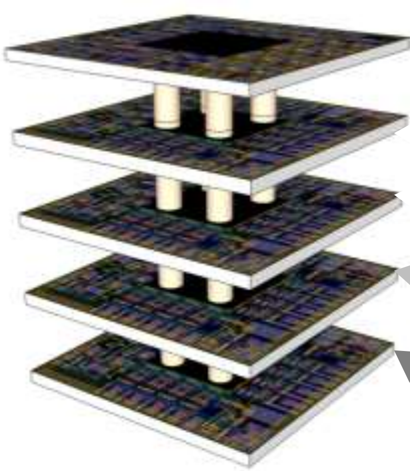

Summary

- Tracking Trigger Processes:
  - Hit Data Transmission.
  - Hit Data Matching (Pattern Recognition, Track Finding)
  - Tracking Parameter Calculation (Track Fitting)
  - Trigger Decision.
- High rate causes challenges to all stages.
- There exist many resource saving schemes for each stage.

The End

Thanks