Status of Silicon

Yunpeng Lu (IHEP)

On behalf of Vertex detector sub-group
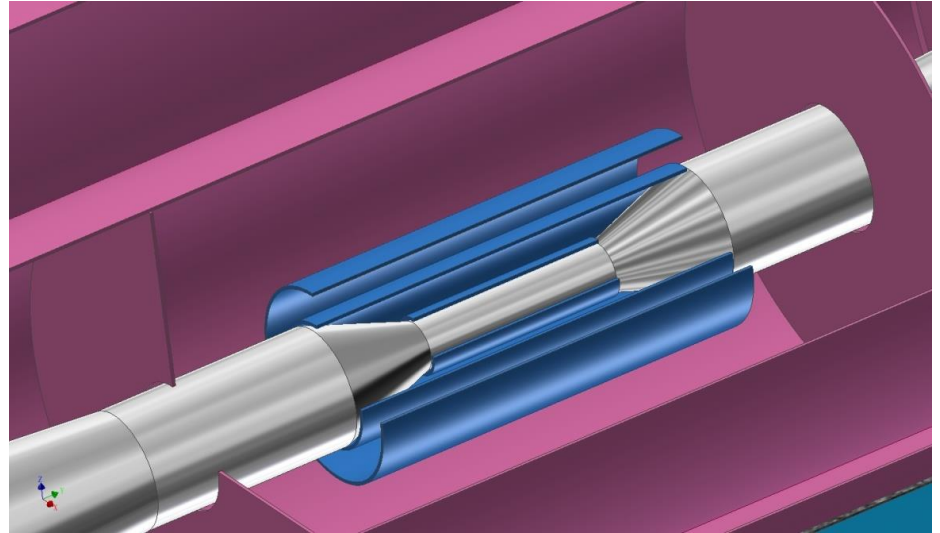
2016-4-8

Outline

- Introduction to the Vertex and Strip
  - Unprecedented challenges in Vertex
- R&D thread #1: Fine pitch and Low power
  - First set of specifications
  - R&D on CMOS
  - R&D on SOI
- R&D thread #2: Towards ~1µs time resolution
  - Second set of specifications
- Summary

Detector concept
Baseline design for the pre-CDR

Vertex detector：

- 3 layers of double-sided pixels
- σ_{SP}=2.8μm, inner most layer
- readout time <20μs

VXD Geometry

|	R (mm)	|z| (mm)	|cos θ|	σ_{SP} (μm)	Readout time (μs)
Layer 1	16	62.5	0.97	2.8	20
Layer 2	18	62.5	0.96	2.8	20
Layer 3	37	125.0	0.96	4	20
Layer 4	39	125.0	0.95	4	20
Layer 5	58	125.0	0.91	4	20
Layer 6	60	125.0	0.90	4	20

Detector concept (Cont.)

Si-tracker:

• Silicon Internal Tracker (SIT) – 2 inner layers strip detectors

• Forward Tracking Detector (FTD) – 5 disks (2 with pixels and 3 with Si strip sensor), comparing to 7 disks on ILD, due to smaller L*

• Silicon External Tracker (SET) – 1 outer layer Si strip detector

• End-cap Tracking Detector (ETD) – 1 end-cap Si strip detector on each side

Layout of strips (SET and ETD not shown)
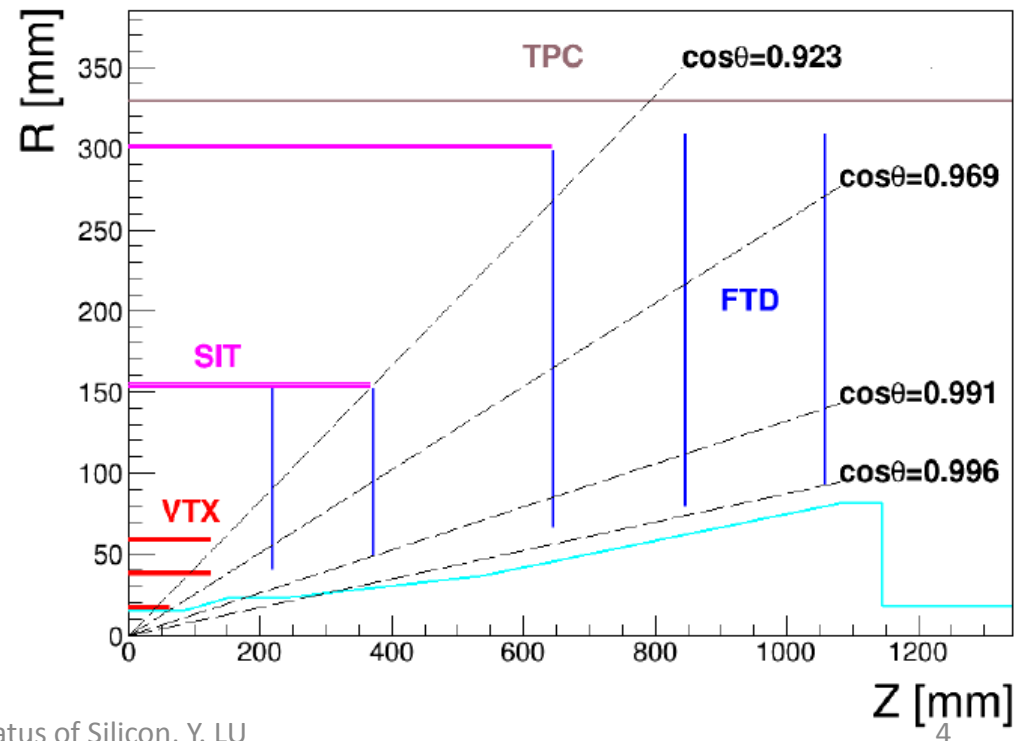
Detector requirements

B=3.5T

> momentum resolution

> impact parameter resolution

$$\sigma_{1/p_T} = 2 \times 10^{-5} \oplus 1 \times 10^{-3} / (p_T \sin\theta)$$

$$\sigma_{r\phi} = 5\,\mu m \oplus \frac{10}{p(GeV)\sin^{3/2}\theta}\,\mu m$$

Vertex detector specifications:

- σ_{SP} near the IP: *≤3 µm*
  - → small pixels 16×16µm² or below, digital readout
- material budget: *≤ 0.15%X$_0$/layer*
  - → low power circuits, air cooling
- pixel occupancy: *≤ 1 %*
- radiation tolerance: Ionising dose *≤100 krad/ year*
              Non-ionising fluences *≤10^{11}n$_{eq}$/ (cm² year)*
- first layer located at a radius: *~1.6 cm*

Silicon tracker specifications:

- σ_{SP} : *≤ 7 µm* → small pitch (50 µm)
- material budget: *≤ 0.65%X$_0$/layer*

Critical R&D

- Pixel sensors with low power consumption and high readout speed
  - Starting design with HR-CMOS process
  - Exploring possibility with SOI process, especially for smaller pixel size
- Light weight mechanical design and cooling
  - 0.05%(0.1%) material budget without(with) cabling
  - Air cooling technology with acceptable vibration due to air flow
- Pixel sensor thinning to 50μm
- Slim edge silicon microstrip sensor
- Low noise, low power consumption front-end electronics for silicon microstrip

Unprecedented challenges in vertex—
Single point resolution

(Source of the plots: Y. Voutsinas, 2012)
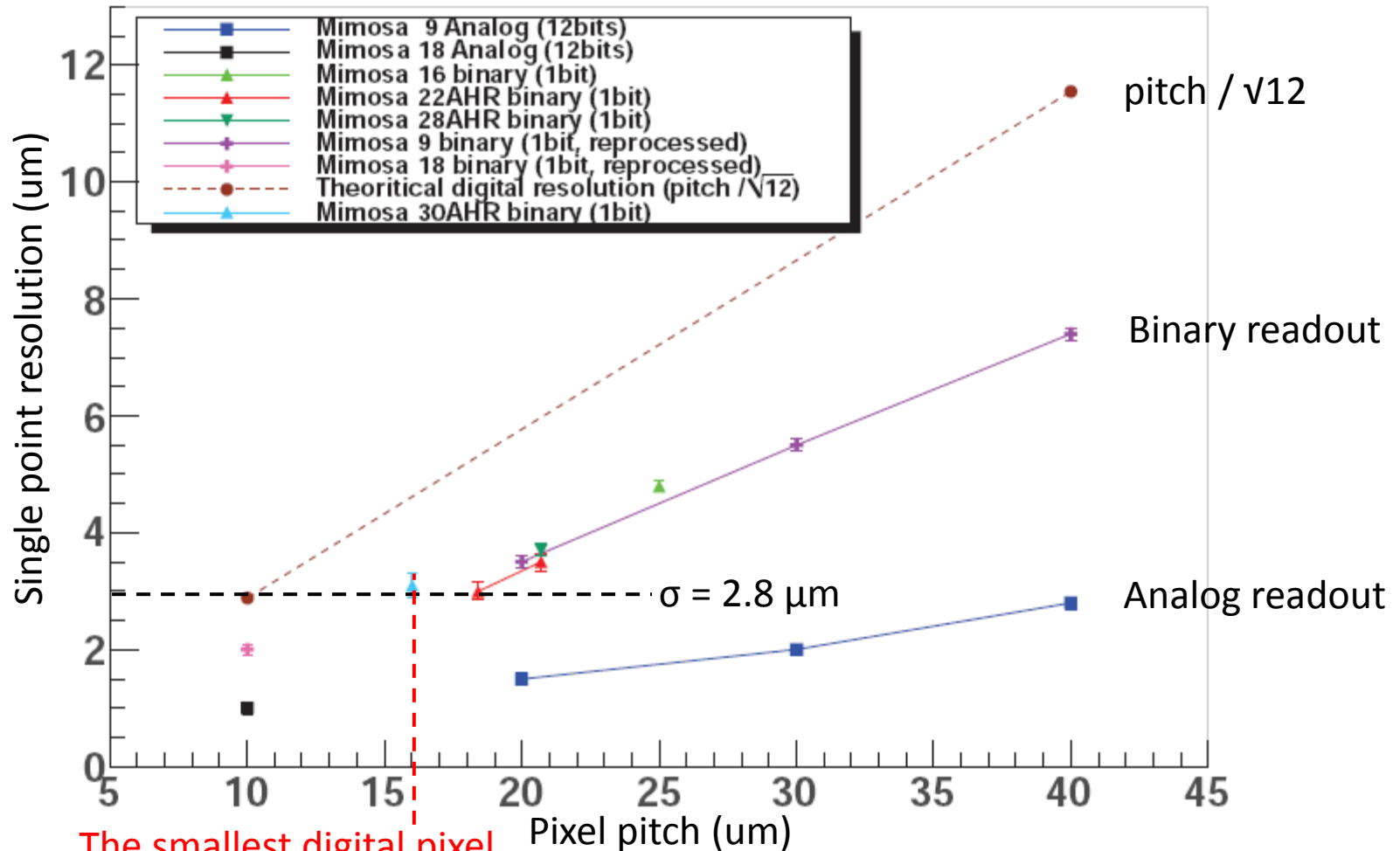
The smallest digital pixel
for particle physcis

# Unprecedented challenges in vertex—
Low power consumption

- Power pulsing, an ingredient missing for CEPC
  - Instantaneous power ~600W@ILC
  - Average power ~20W@ILC by applying power cycling
- The maximum heat load of 150W imposed by air cooling
  - CEPC has to cut down the power by a factor of 4
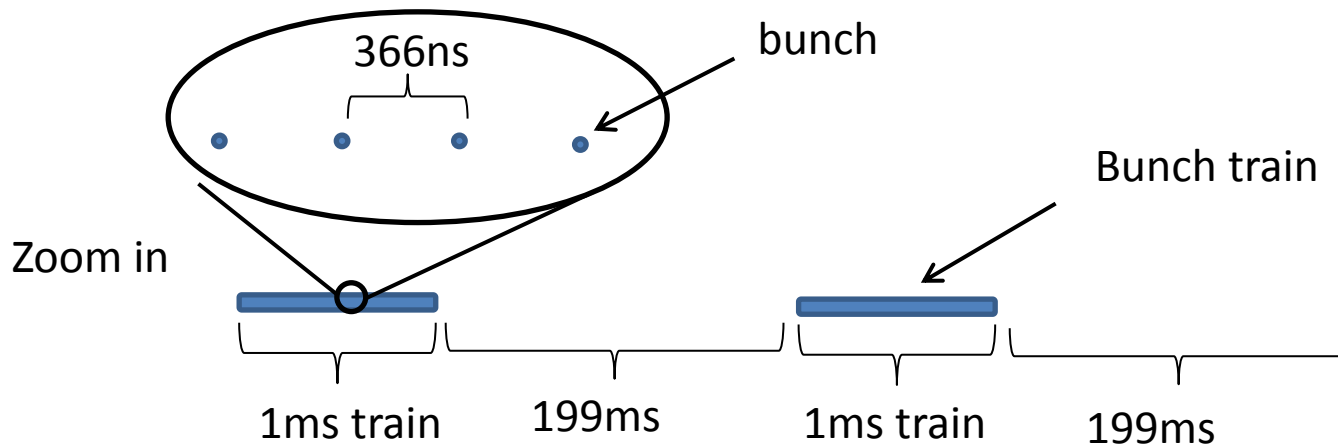
ILC beam timing structure

Unprecedented challenges in vertex— Fast readout speed

- Readout intervals of ~1µs will be required if the Local Double-ring Scheme is to increase the hit density dramatically.
  - One magnitude lower than the-state-of-art design
  - Background estimates are still in early stage

Pretzel Scheme
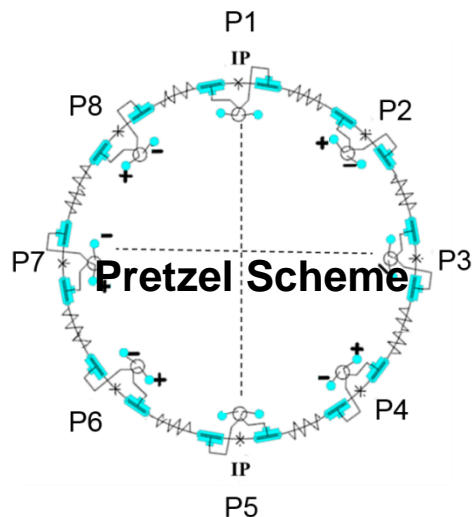
- Baseline design in pre-CDR
- Colliding every 3.6µs, continuously

Local Double-ring Scheme
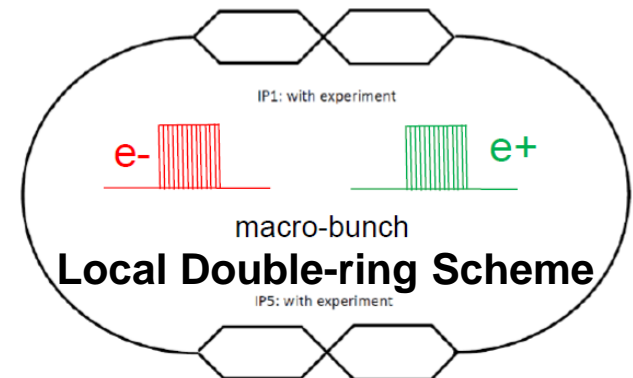
- to reduce beam and AC power
- to increase the flexibility and luminosity
- 196ns bunch spacing
- Duty cycle: 9.4µs / 181µs

Reference: CEPC/SppC with ILC (FCC), J. Gao, LCWS 2015

R&D thread #1: Fine pitch and low power

- Strategies:
    - Fine pitch to achieve <3µm SP resolution for the inner most layer
    - Low power compatible with air cooling
    - Relaxed requirement on readout speed (flexible)
- Specifications:
    - 16 µm pitch
    - 50 mW/cm^2
    - 10-100 µs readout speed

1st CMOS prototype

由高能所创新经费支持

- Goals: sensor optimization and radiation hardness study

- Floorplan overview:

  - Two independent matrices: Matrix-1 with 33 × 33 μm² pixels (except one sector SFA20 with 16 × 16 μm² pixels), Matrix-2 with 16 × 16 μm² pixels.

  - Matrix-1: 20 sectors, each sector includes 48 rows and 16 columns

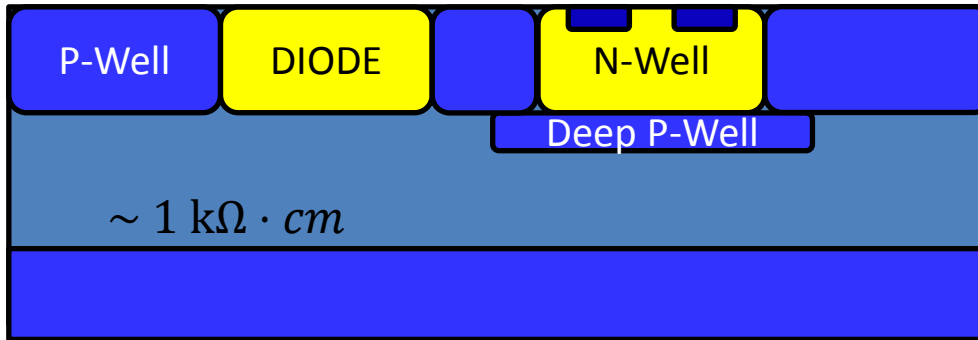 - Matrix-2: 16 sectors, each sector includes 96 rows and 16 columns
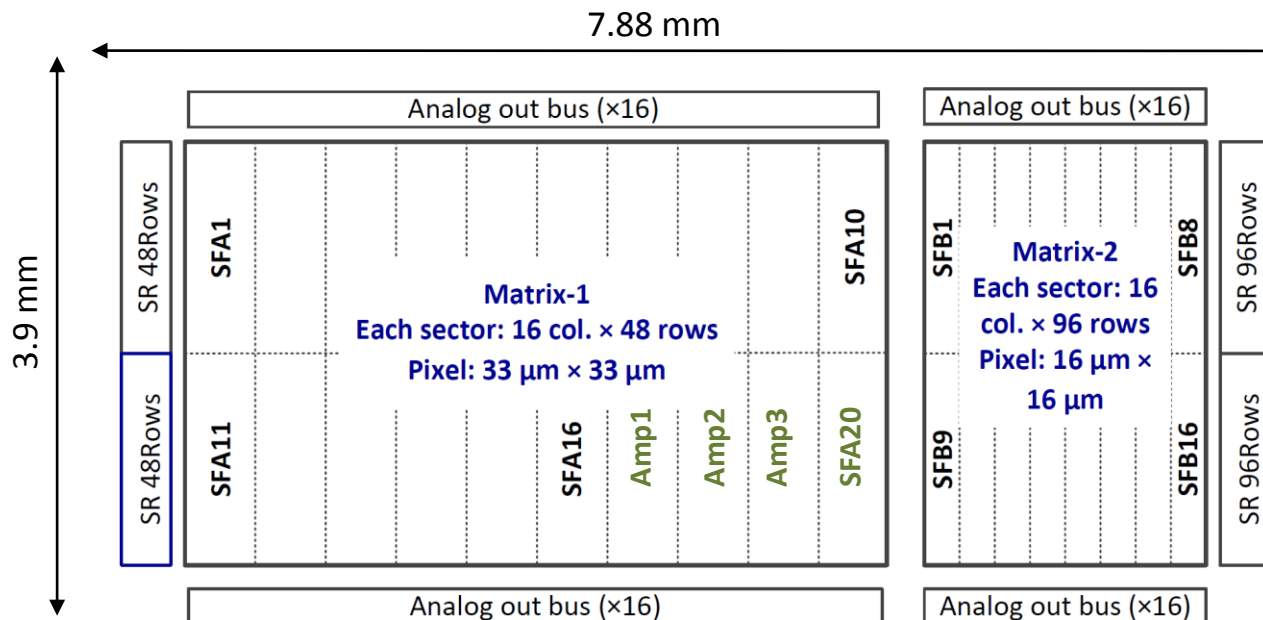
TowerJazz CIS 0.18 μm November 2015 submission

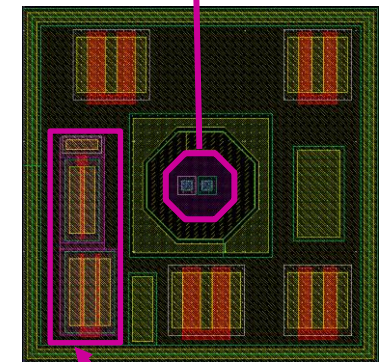# 1st CMOS prototype: Deep P-well shielding

Y. ZHANG, M. FU, L. ZHANG, H. ZHU

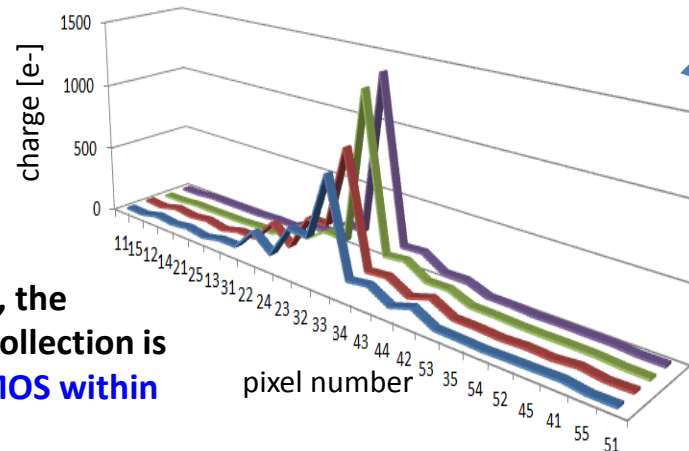- To look at the effectiveness of deep P-well shielding

charge collection N-well

Nwell for PMOS

| Sector	Diode area	Footprint area	Structure
SFB3	8 μm^2	20 μm^2	2T_nmos
SFB13	8 μm^2	20 μm^2	2T_pmos
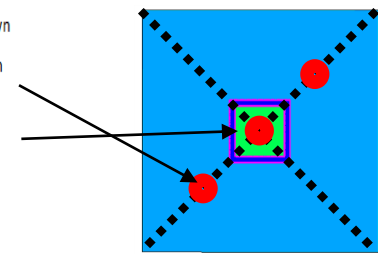
hit position on the central pixel

With the shielding of deep P-well, the competition of PMOS on charge collection is almost negligible ➜ allow full CMOS within the pixel

1st CMOS prototype: Cluster size

Y. ZHANG, M. FU, L. ZHANG, H. ZHU

- Pixel cluster with four different epitaxial layers
 - 18μm/1KΩ, 20μm/2KΩ, 25μm/2KΩ, 30μm/8KΩ
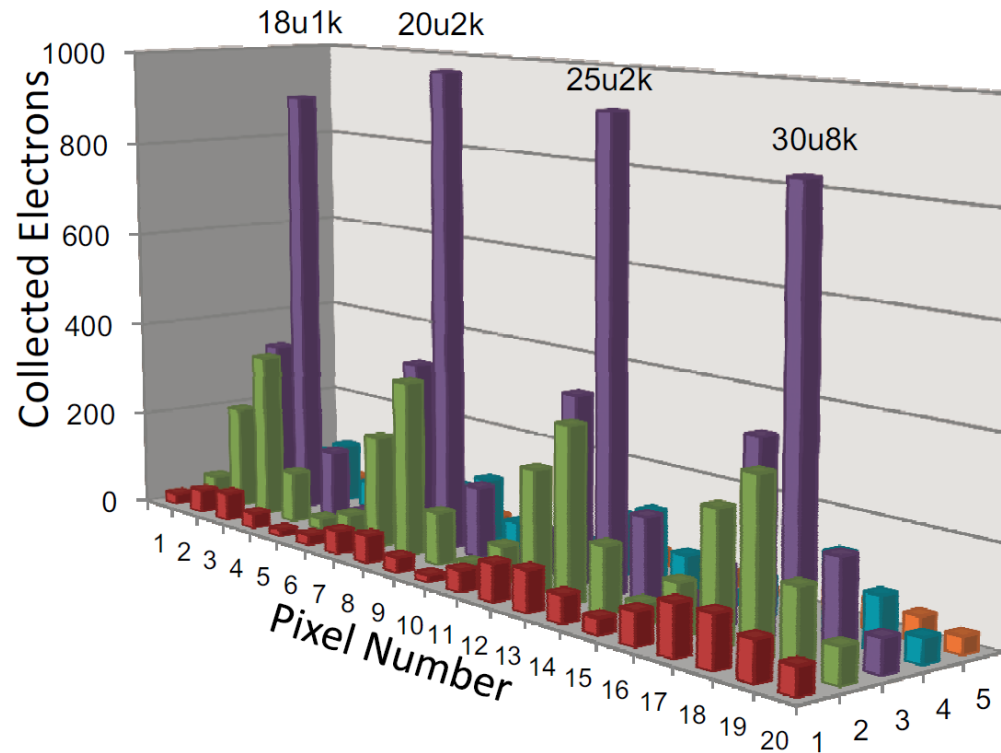
Total charge increases with the thickness and resistivity of the epi-layer, so does the charge sharing → **the 20 μm thick epitaxial layer could allow optimal charge collection**

1st CMOS prototype: Radiation damage

Y. ZHANG, M. FU, L. ZHANG, H. ZHU

- Charge collection efficiency decreased by radiation fluence
 - Signals remain ~80% and ~60% respectively at CEPC annual fluence

Seed pixel
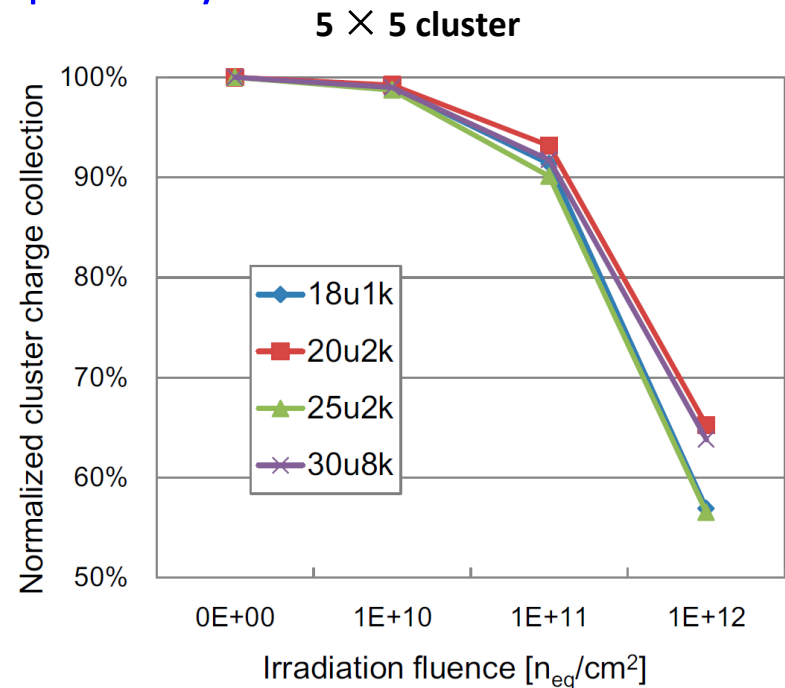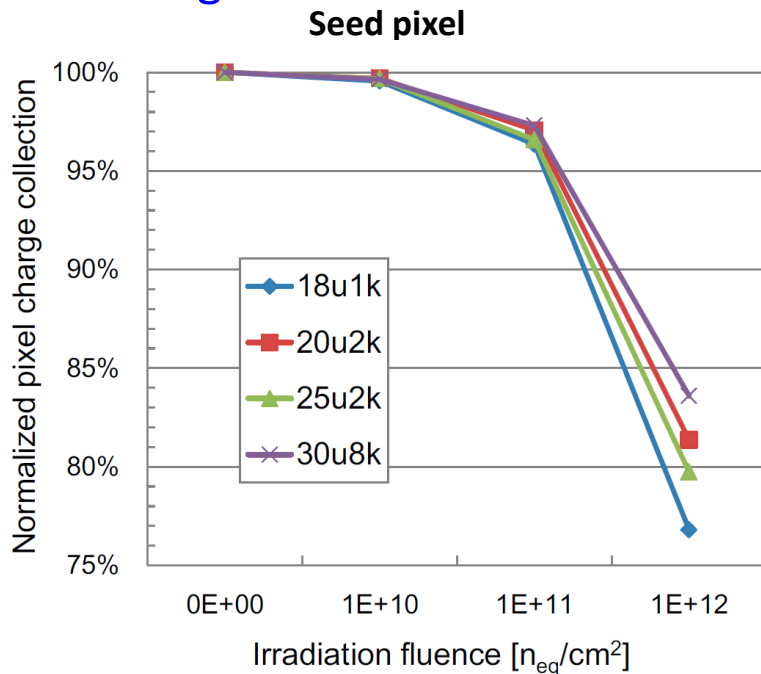
5 × 5 cluster

> Seed pixel: higher resistivity → better radiation tolerance
> Pixel cluster:
>   - 25 μm thick epi-layer worse than 20 μm (same resistivity) → charge sharing and radiation-caused-traps in a thicker epi-layer may degrade the performance
>   - 30 μm thick one similar to the 20 μm → advantage of high resistivity can be partly neutralized by thicker epi-layer
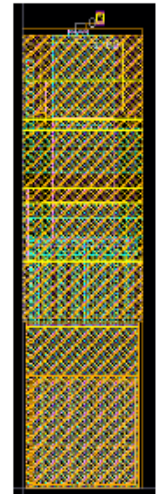
1st CMOS prototype: Biased diode

Y. Zhou, Y. LU, C. HU

- Bias voltage up to 10 V
  - To measure seed/cluster signal versus V_{bias}
  - To measure the cluster multiplicity
- Optimization of Cc, V_cal, SF and noise
- Layout
  - 16 µm*16 µm
  - Direct PAD for V_diode

Structure
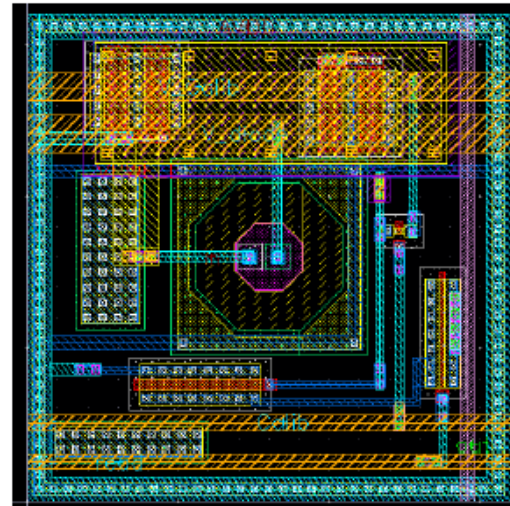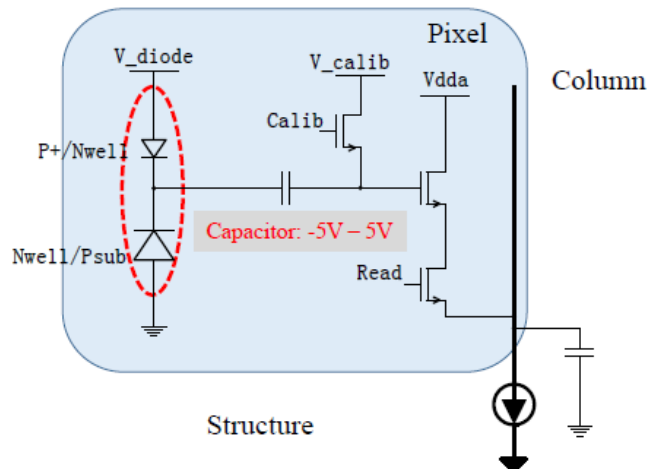
Pixel Layout

- $16 \times 16 \ \mu m^2$;
- with transistors under
  MIM capacitor

Direct PAD layout: for V_diode
- $250 \times 65 \ \mu m^2$
- Without ESD
- Both sizes & power lines
  match with other PADs
  provided by foundry

Choice of technology roadmap

C. Hu, Q. OUYANG, Y. Lu, Y. Zhou, M. Dong

- For the long run, a technology roadmap is essential.

- In-Pixel-Discrimination is selected.

  – Signal digitized in pixel, enabled by the new generation of process

  – Reduction of power consumption

  – Pixel size needs to be minimized, however
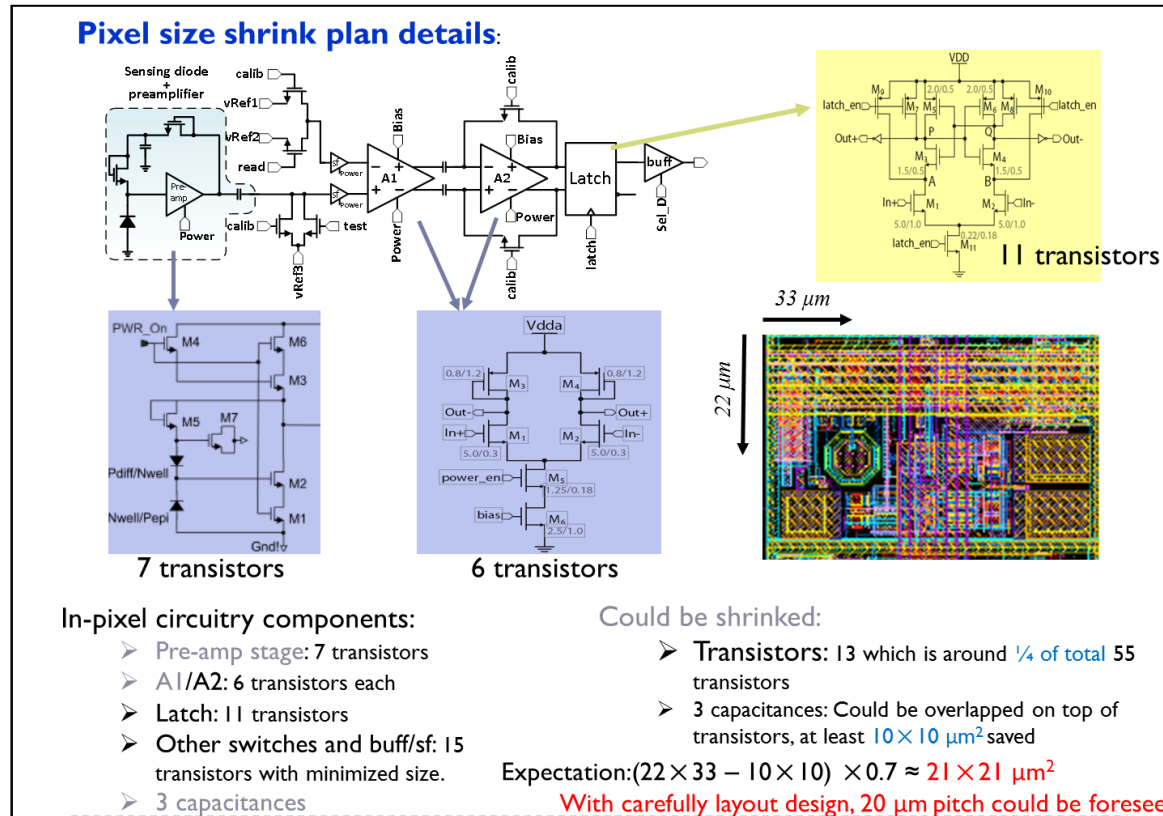
Chips designed for ALICE-ITS upgrade

Name	Architecture Discriminator, read-out	Pitch ($r\phi \times z$) (μm^2)	Integ. time (μs)	Power (mW/cm^2)
MISTRAL(IPHC)	end-of-column, rolling shutter	22 × 33 (66)	30	200 (100)
ASTRAL(IPHC)	in-pixel, rolling shutter	24 × 31(IB) 36 x 31 (OB)	20	85 60
ALPIDE (CERN,INFN,CCNU, YONSEI)	in-pixel, in-matrix sparsification	28 x 28	4	< 50

* CCNU has contributed to the design and test of ALPIDE chips

A preliminary plan to shrink the pixel size

Y. Zhou, Y. LU, C. HU

- Target on 20*20 µm² with in-pixel-discrimination
  - Depleted diode to improve S/N
  - To reduce the number of transistors and improve layout
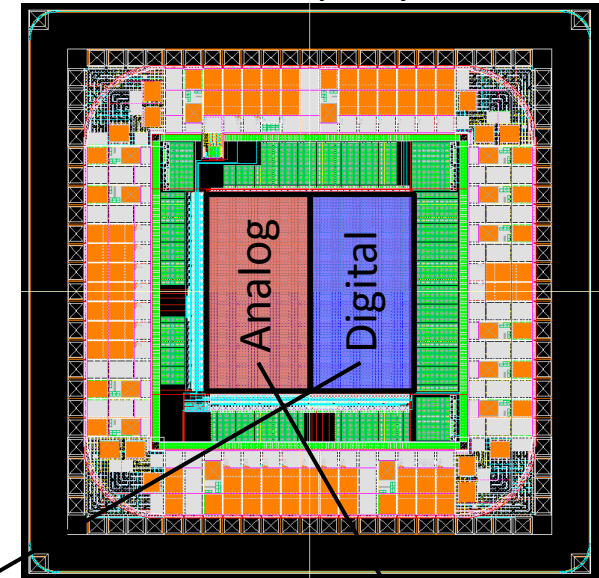 - Preparing design for the 2nd CMOS prototype (presumably end of 2016)

Pixel size shrink plan details:

7 transistors

6 transistors

11 transistors

33 µm

22 µm

In-pixel circuitry components:
- Pre-amp stage: 7 transistors
- A1/A2: 6 transistors each
- Latch: 11 transistors
- Other switches and buff/sf: 15 transistors with minimized size.
- 3 capacitances

Could be shrinked:
- Transistors: 13 which is around ¼ of total 55 transistors
- 3 capacitances: Could be overlapped on top of transistors, at least 10×10 µm² saved

Expectation:$(22 \times 33 - 10 \times 10) \times 0.7 \approx 21 \times 21$ µm²
With carefully layout design, 20 µm pitch could be foreseen
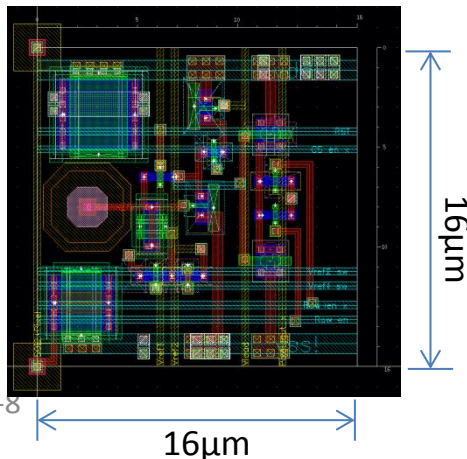
1st SOI prototype

- ## Compact Pixel for Vertex (CPV1)

    Y. Lu, J. DONG

  - Designed in line with the technology roadmap
  - 16*16 μm with in-pixel-discrimination
  - Based on the measurement of full depletion*
  - Pixel array: 64*32 (digital) + 64*32 (analog)
  - Double-SOI process for shielding and radiation

  Enhancement

  - Submitted June, 2015

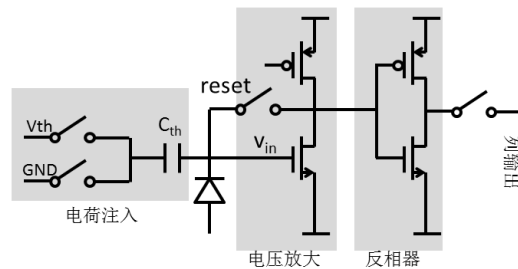 * Y. LIU, Y. LU, X. JU, Q. OUYANG, Chinese Physics C, Vol.40, No. 1 (2016)
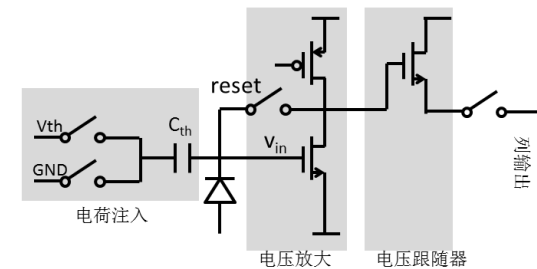
CPV1 chip Layout

CPV1 digital pixel layout

16μm

16μm

64row*32col. digital pixel   64row*32col. analog pixel

reset

Vth
GND
C_{th}
v_{in}

电荷注入

电压放大   反相器

列输出

（a）数字像素

reset

Vth
GND
C_{th}
v_{in}

电荷注入

电压放大   电压跟随器

列输出

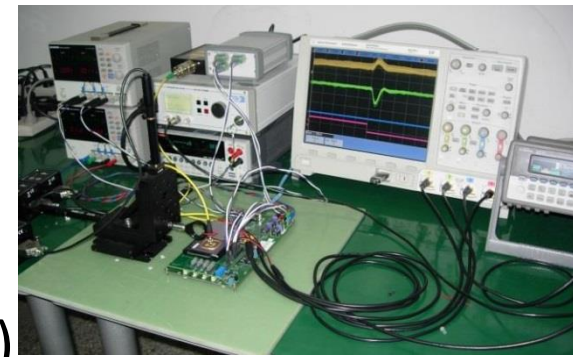（b）模拟像素

CPV1 test setup

- Chip delivered in Feb. 2016
- Mounted in a Pin Grid Array package (176 pins)
- Sub-board PCB prepared
- Fit in the SEABAS* DAQ system
- FPGA firmware and PC software partly ready, modified from the existing system for other chips

Bare chip

Chip & Package   FPGA   Ethernet

Sub-board
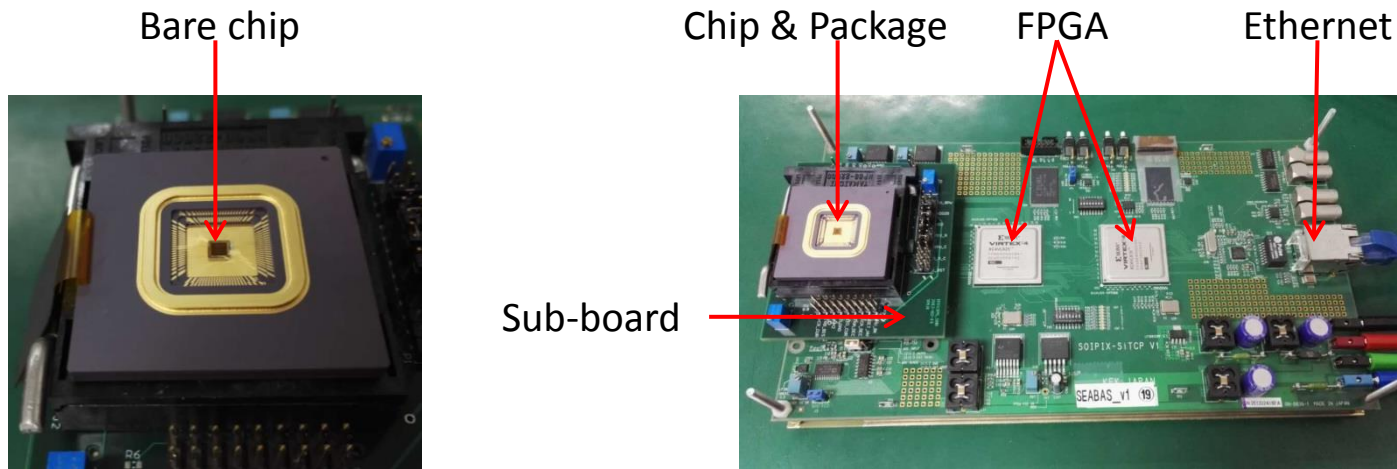
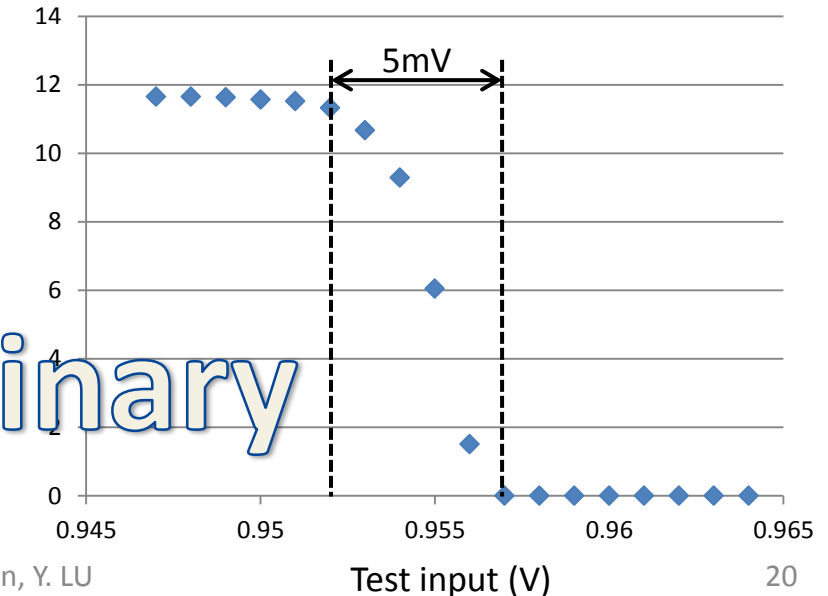*A DAQ system developed by KEK, mainly for pixel chip readout

Preliminary results of CPV1

- ## Gain of amplifier measured on analog pixels
  - Measured 10.2 agrees with the design value 10

- ## Transfer curve measured on digital pixels
  - Transition region ~5mV, equivalent to 120e[-]
  - A decent ENC noise ~ 17e[-]

- ## Radiative source test is in preparation
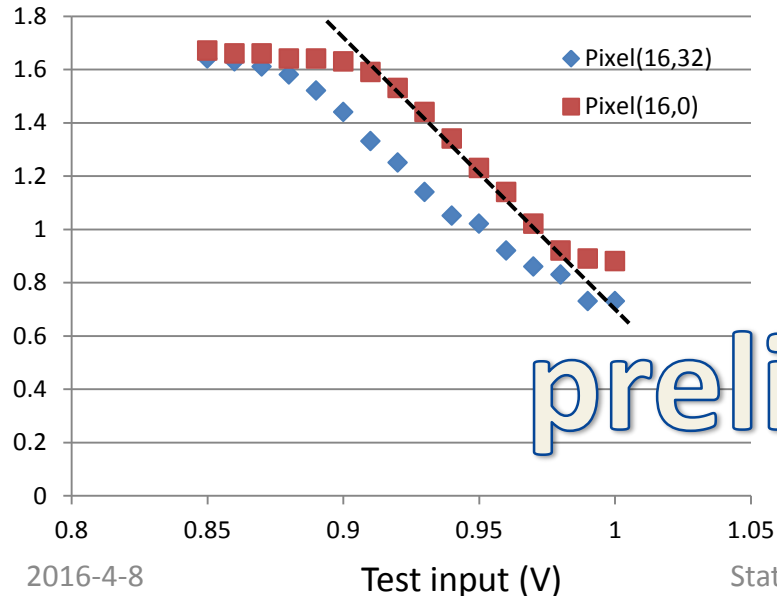
R&D thread #2: towards ~1 us time resolution

- Strategies:
  - Relaxed requirement on SP resolution
  - Low power compatible with air cooling
  - Enhanced readout speed by a factor of 10
- Specifications:
  - 20-30 um pitch to achieve $\sigma \sim 5um$
  - 50 mW/cm^2
  - ~1us readout intervals
- Technology roadmap
  - Continuous signal discrimination (and low power)
 - Asynchronous encoding of hit position

Summary

- Pixel sensor was identified as the core of R&D activities in the past half year.
- To address the challenges from the inner layers of Vertex, 2 threads of RD efforts are proceeding in parallel.
  - 16um pitch, 50mW/cm^2, 10-100us
  - 20-30um pitch, 50mW/cm^2, ~1us
- Two chips consist of 16 um pixel array have been submitted
  - TowerJazz 180nm CMOS process and HR wafer will be characterized shortly in terms of sensor optimization and radiation hardness.
  - First prototype chip using Lapis 200nm SOI process has shown encouraging results.
- More test results is to come in the second half of 2016.

Backup slides

A study on the depletion and cluster size

Y. LIU, Y. LU, Q. OUYANG

- SOI offers a good chance to look into depletion
  - Pixel size 19*19um^2
  - Analog readout
  - Central window of 5*9um^2
- 1064nm focused to 3.2um, simulating MIPs
  - Pass through the central window of seed pixel
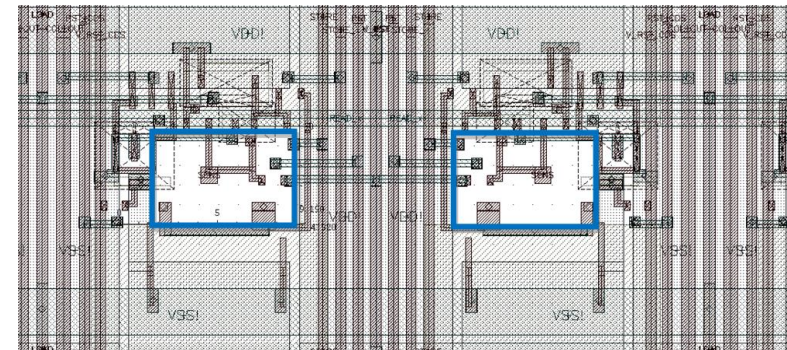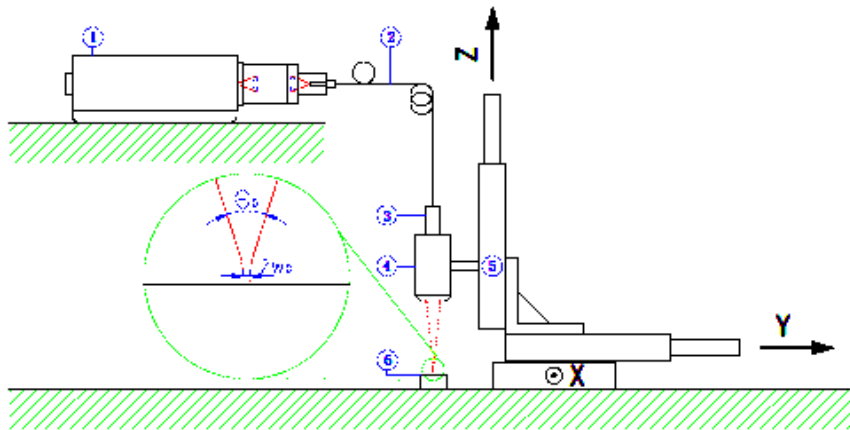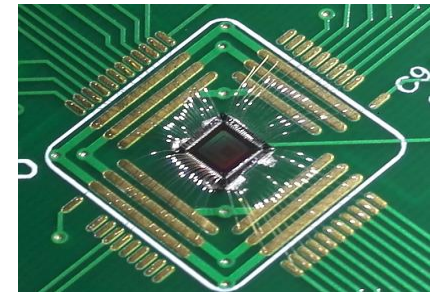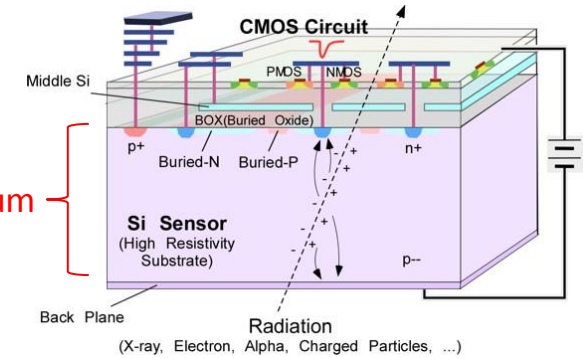
Layout of 2 pixels with only metal shown

Measurement results

Y. LIU, Y. LU, Q. OUYANG

- 70% of charge collected by the seed pixel
  - V_{bias} = 20V, expect to deplete 80um
  - Unable to scan across the border of pixel
- Signal increases with V_{bias}
  - Fully depleted around 190V
  - Seed / cluster ratio decreases with V_{bias}

Single pulse response

response_voltage

Cluster signal

Seed signal

Seed / cluster ratio