



A monolithic pixel sensor with fine space-time resolution based on SOI technology for the ILC vertex detector

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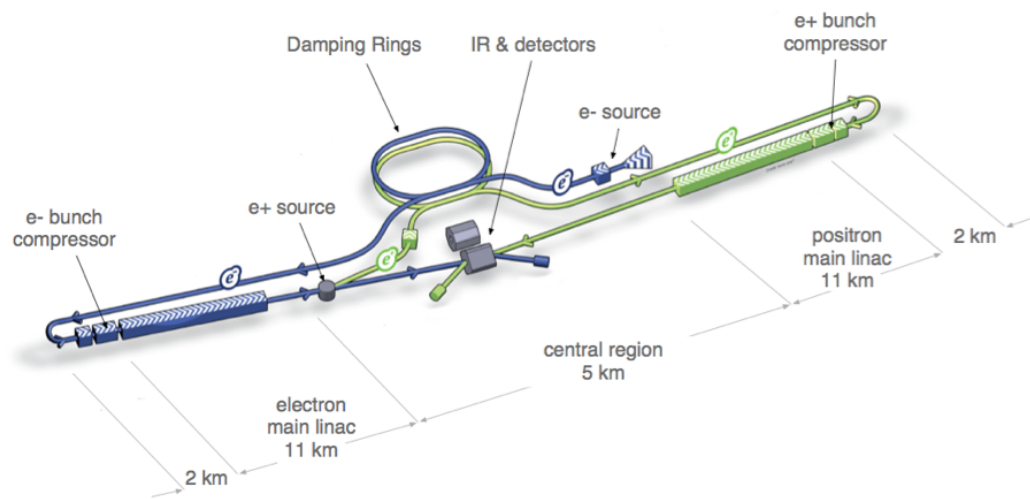
Manabu Togawa, Teppei Mori(Osaka-Univ.)

Kazuhiko Hara, Daisuke Sekigawa, Shun Endo(Tsukuba Univ.)

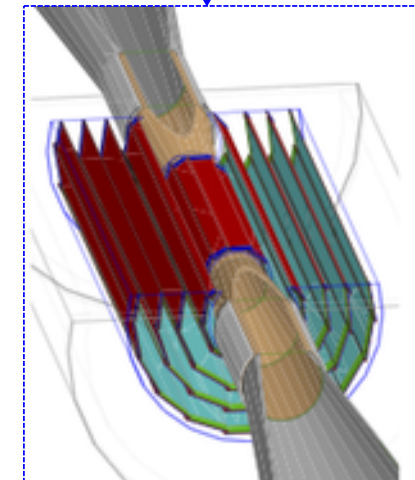
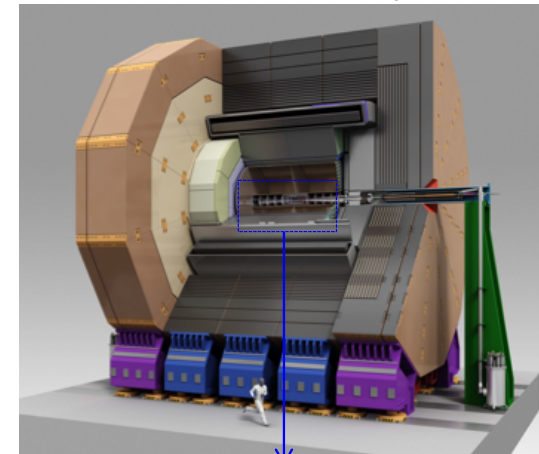
Akimasa Isikawa(Tohoku Univ.)

International Linear Collider

- ILC Experiment: e^+e^- linear collider
 - Precise measurement of the Higgs boson
 - Search for physics beyond the Standard Model

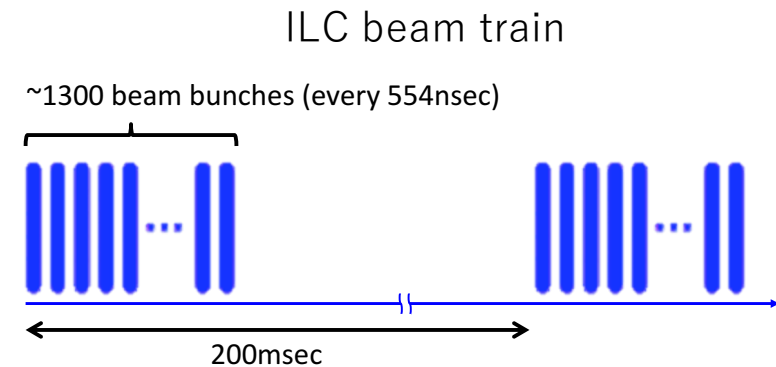


ILC detector concept (ILD)



ILC Vertex Detector

- Detector requirements
 1. Sensor position resolution: $3 \mu\text{m}$
 - Pixel size: $\sim 20 \times 20 \mu\text{m}^2$
 - Low material budget: $\sim 0.1\%/X_0$
 - corresponds to $\sim 100 \mu\text{m Si}$
 2. Time resolution
 - Bunch identification during beam train: 554ns interval



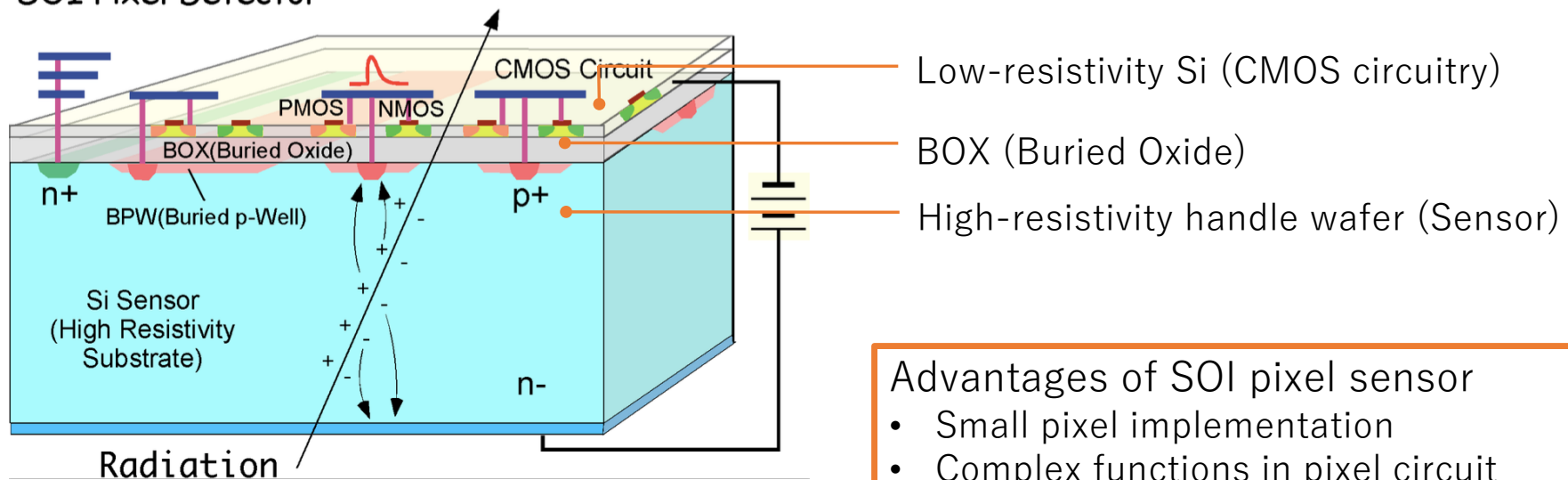
SOI pixel sensor for the ILC vertex detector

- Storing both the hit position and timing of charged particle

SOIPIX (SOI Pixel Detector)

- Monolithic pixel detector with SOI technology

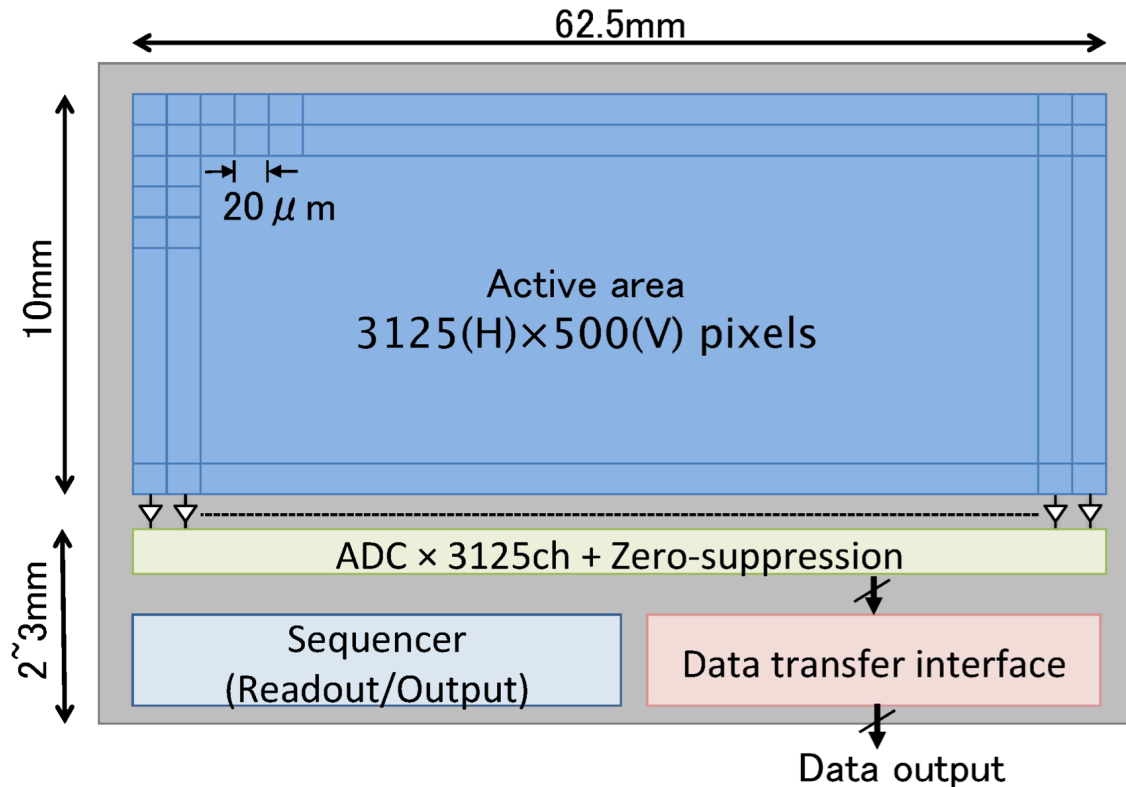
SOI Pixel Detector



- Advantages of SOI pixel sensor
 - Small pixel implementation
 - Complex functions in pixel circuit
 - Low material budget
 - Radiation hardness: > 100kGy(TID)

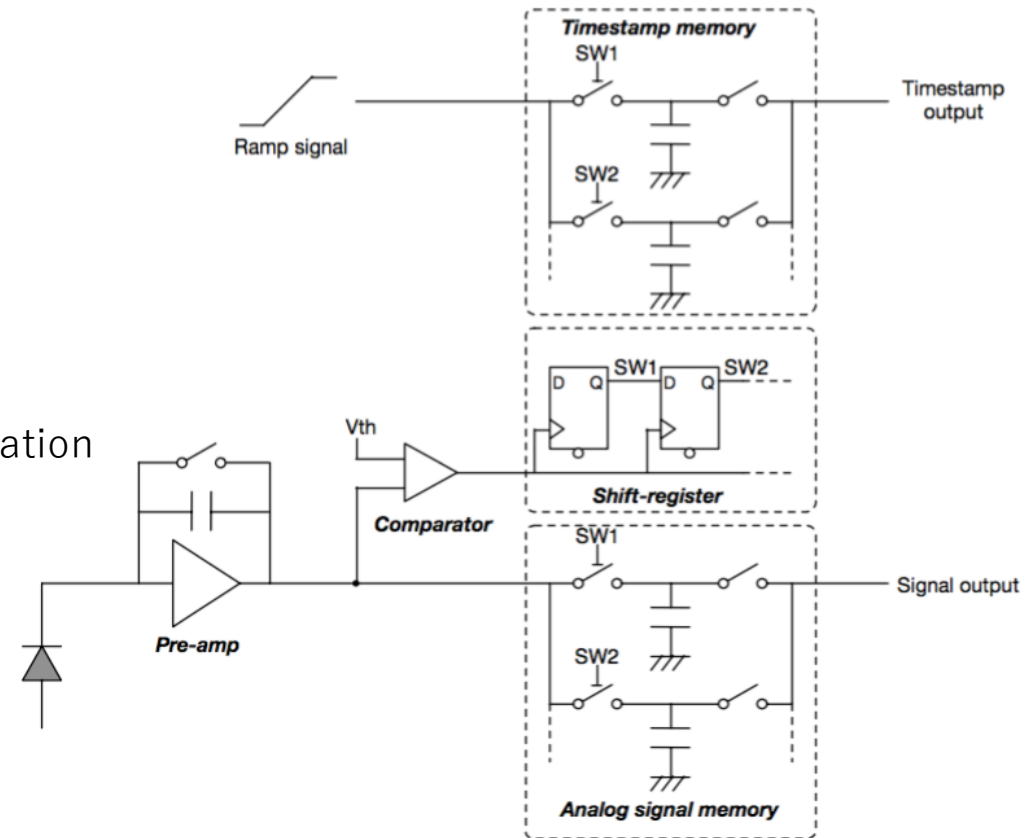
SOI sensor for ILC: SOFIST

- SOI sensor for Fine measurement of Space and Time
 - Conceptual design of SOI pixel sensor for the ILC vertex detector



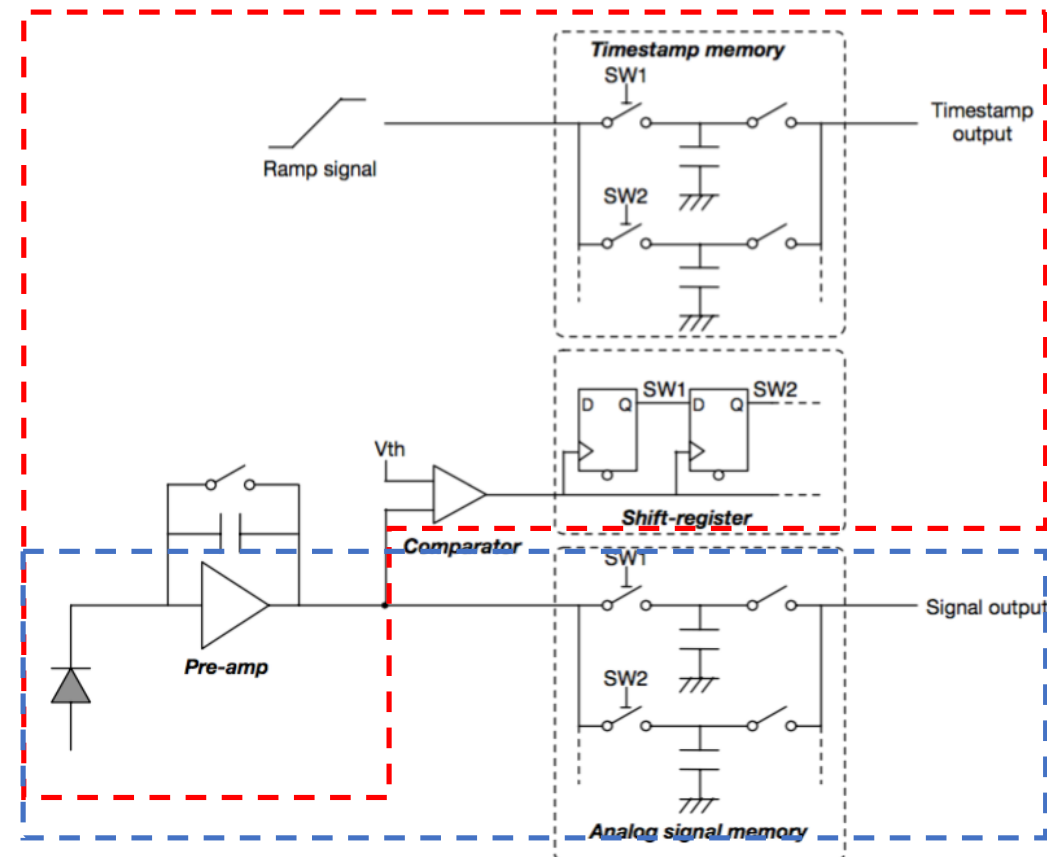
SOFIST Pixel architecture

- Pixel circuit
 - Pre-amplifier
 - Comparator
 - Signal discrimination
 - Shift register
 - Record hit events.
 - Analog signal memory
 - Store charge signal for hit position calculation
 - Timestamp memory
 - Store hit timing for event separation
- Multiple memories in one pixel

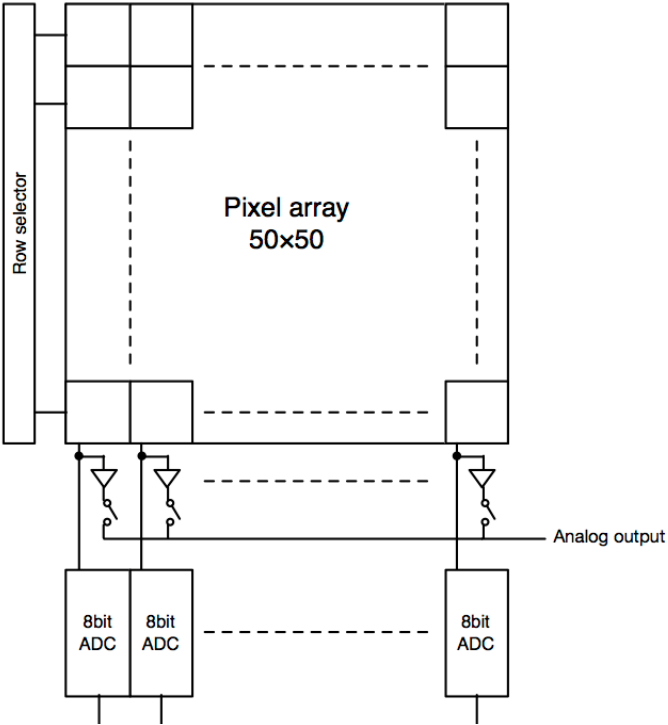
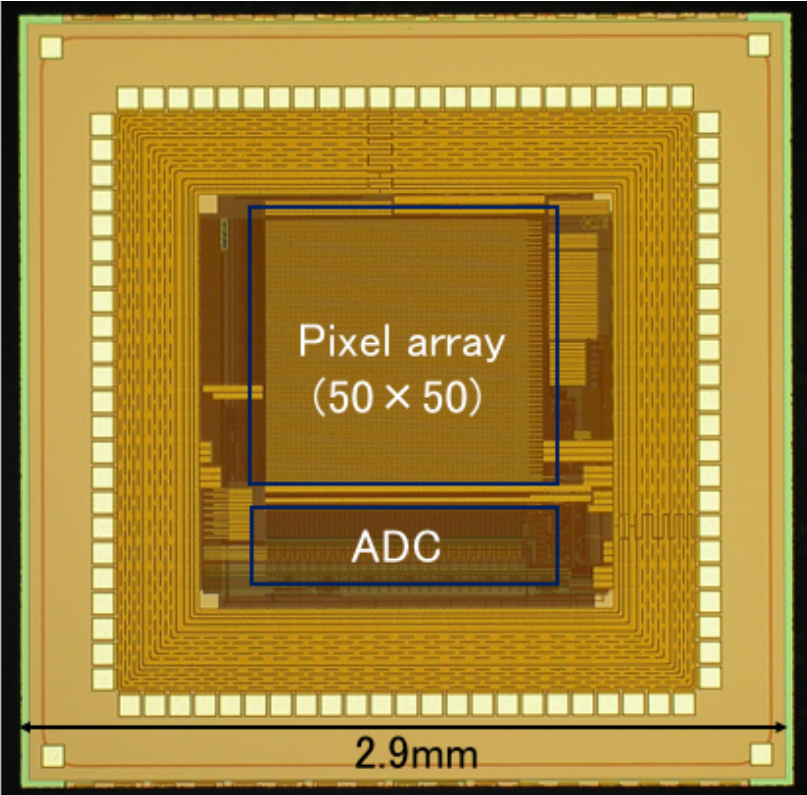


SOFIST Prototype sensors

- SOFIST prototype chips
 - **SOFIST Ver.1**
 - Pixel with analog signal readout
 - Delivered in Dec. 2015
 - SOFIST Ver.2
 - Pixel with time stamp readout
 - Delivered in Dec. 2016
 - SOFIST Ver.3 ~
 - Pixel integration of Ver.1 and Ver.2
 - Under designing



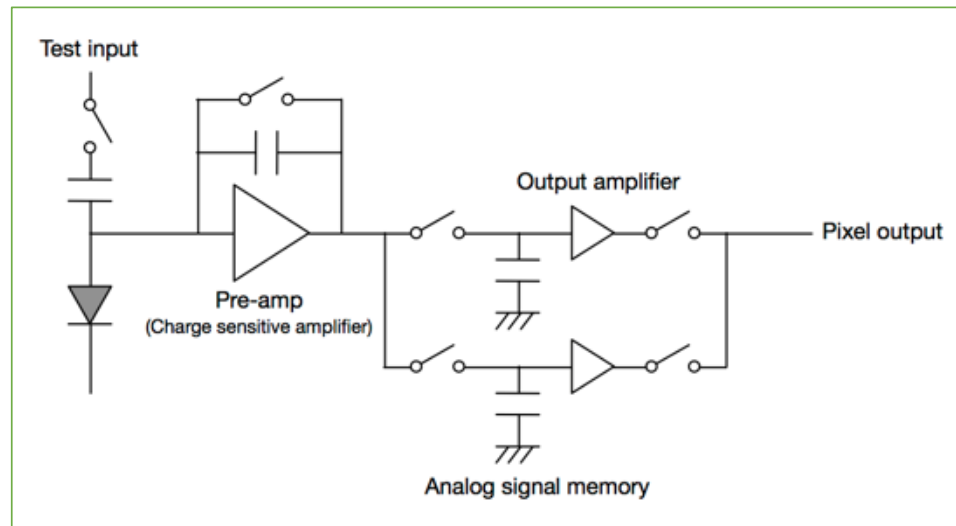
SOFIST Ver.1 chip



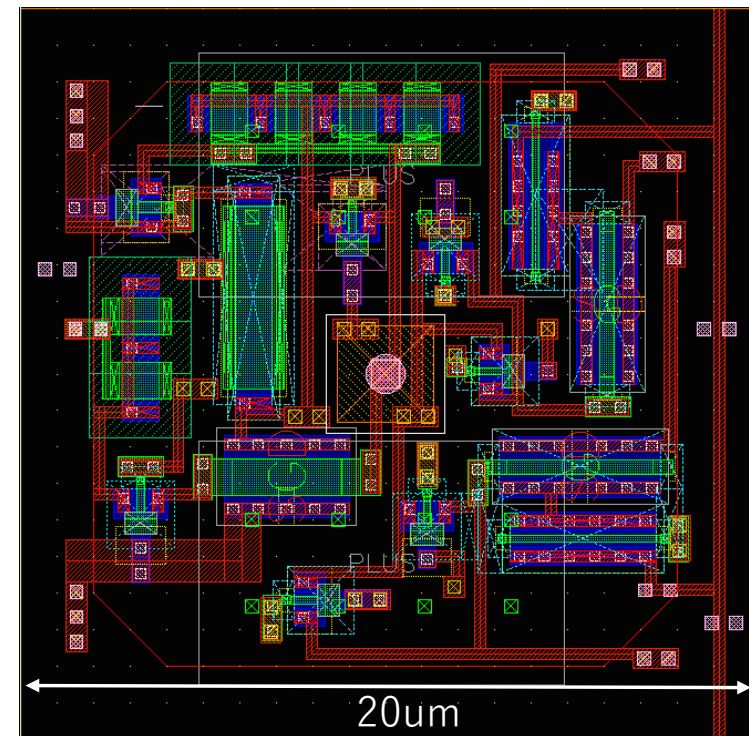
Parameter	
Pixel size	20x20 μm^2
Pixel array	50x50 (Active area: 1x1mm ²)
Sensor size	2.9x2.9 mm ²
Sensor thickness	500 μm

SOFIST Ver.1 chip

- Pixel circuit
 - Pixel size: $20 \times 20 \mu\text{m}^2$
 - Pre-amp gain: $32 \mu\text{V}/e^-$

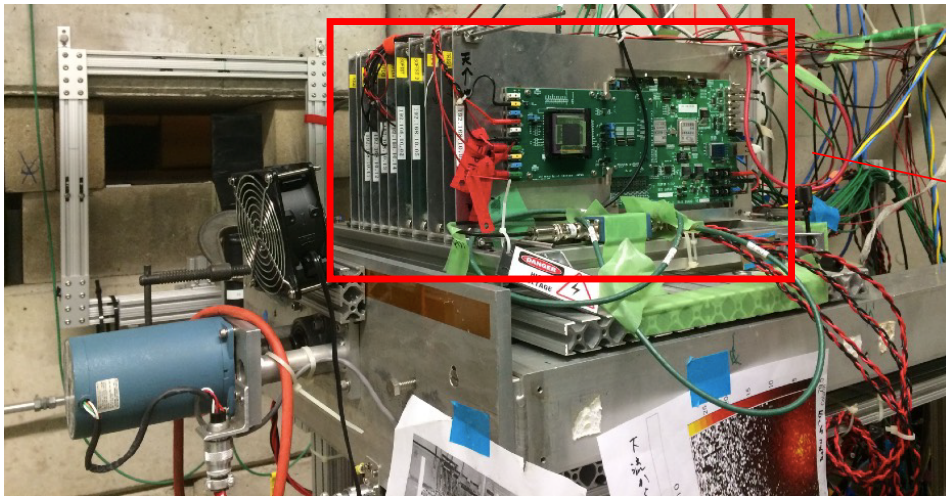


Pixel layout



SOFIST Ver.1 chip evaluation: Beam test

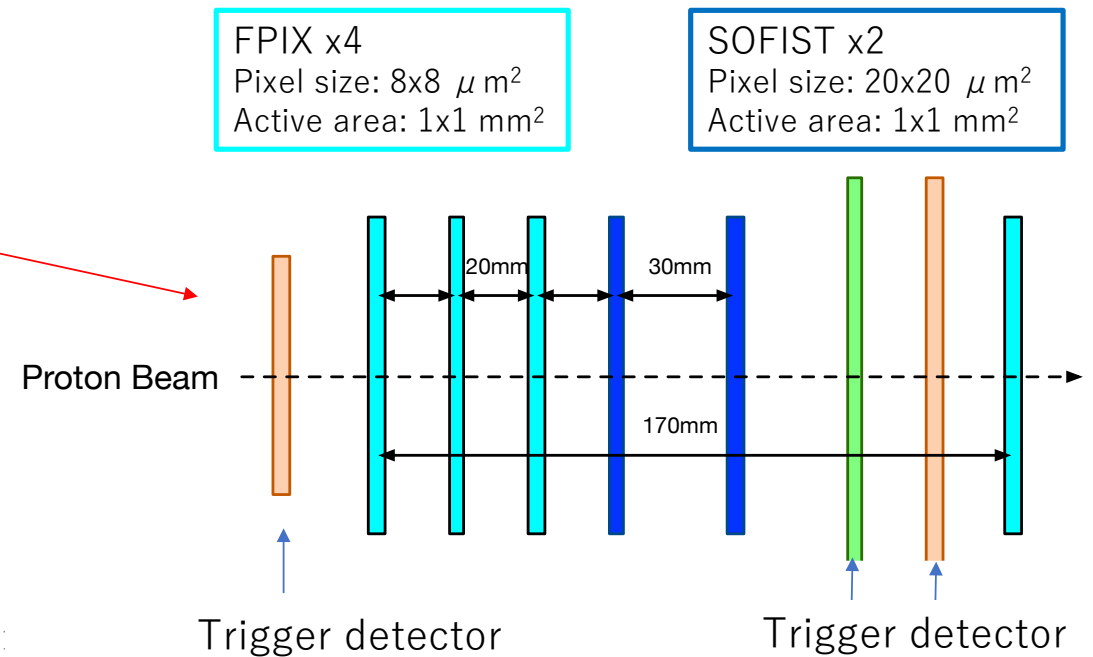
- Beam test @ Fermi national laboratory
 - Beam: 120GeV Proton
 - Evaluation of SOFIST Ver.1 and FPIX



2017/5/25

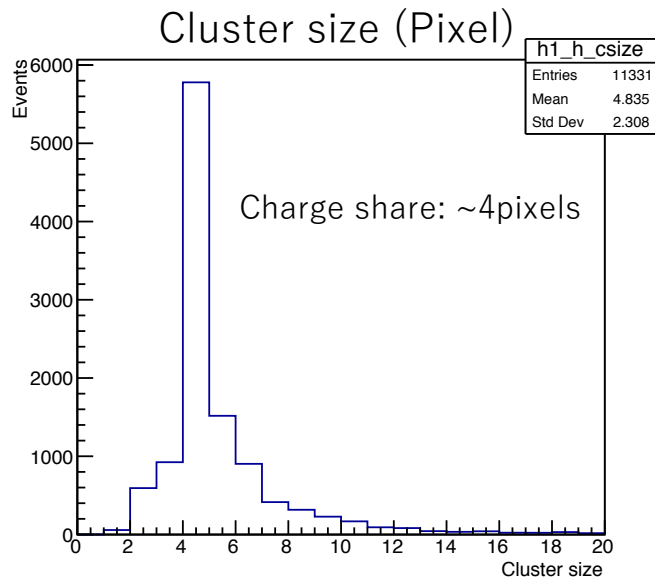
TIPP20:

Detector system with SOFIST

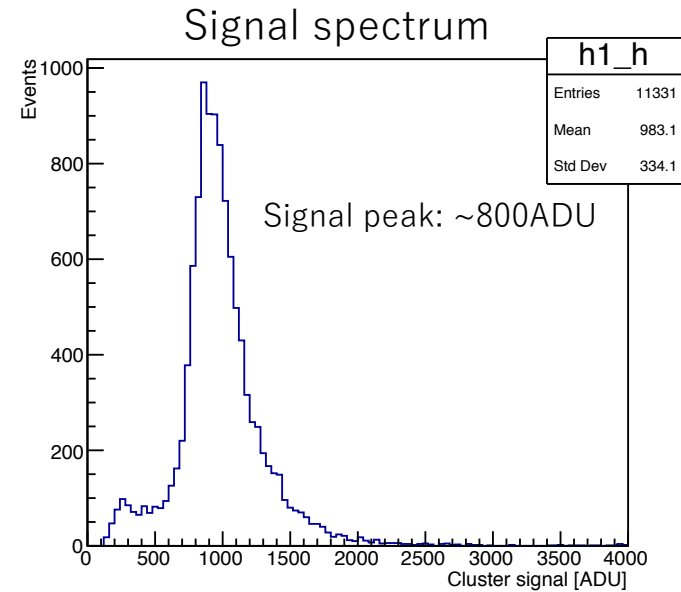


Cluster signal, S/N

- Sensor setup
 - Depletion width: ~500 [um] (HV=130V)
 - Readout by External ADC (12bit)



- Cluster signal reconstruction
 - Finding hit pixel over threshold
 - Summing 6x6 pixels around hit



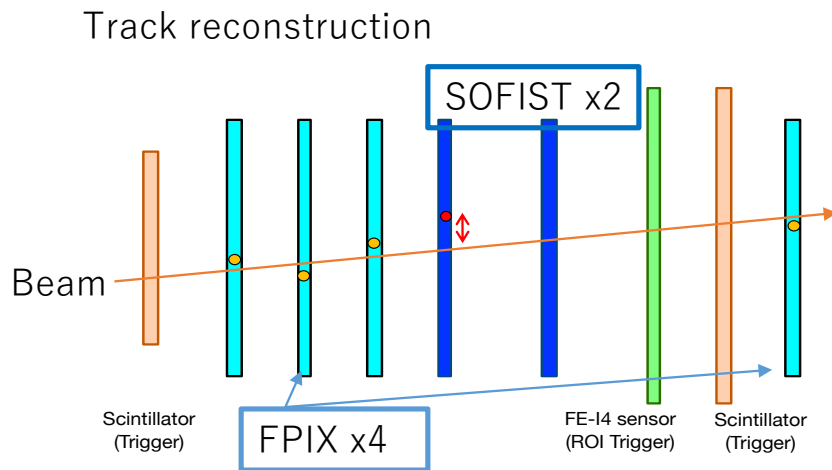
Signal peak: ~800 [ADU]
Pixel noise: 2.2 [ADU/pixel]



$S_{\text{peak}}/N_{\text{pixel}} \sim 360$ (@500um thickness)

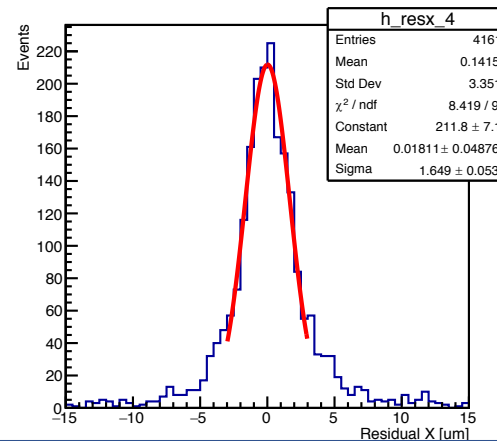
Chip evaluation: Position resolution

- **Track reconstruction**
 - Find track candidates from FPIX.
- **Residual calculation**
 - Difference between reconstructed track and detected hit on the SOFIST.



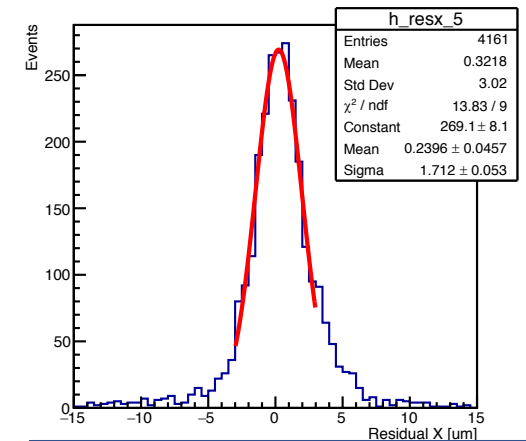
Residual analysis result @500um sensor thickness

SOFIST sensor 1



Sigma: $1.65 \pm 0.05 \mu\text{m}$

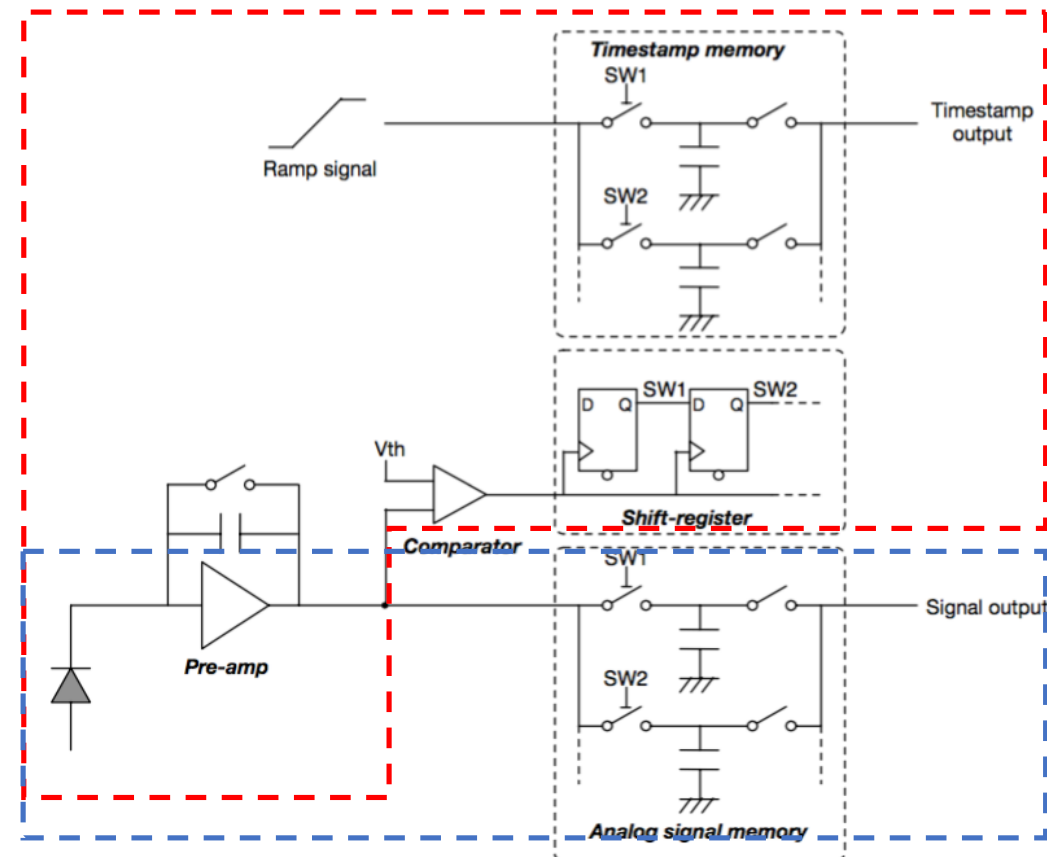
SOFIST sensor 2



Sigma: $1.71 \pm 0.05 \mu\text{m}$

SOFIST Prototype sensors

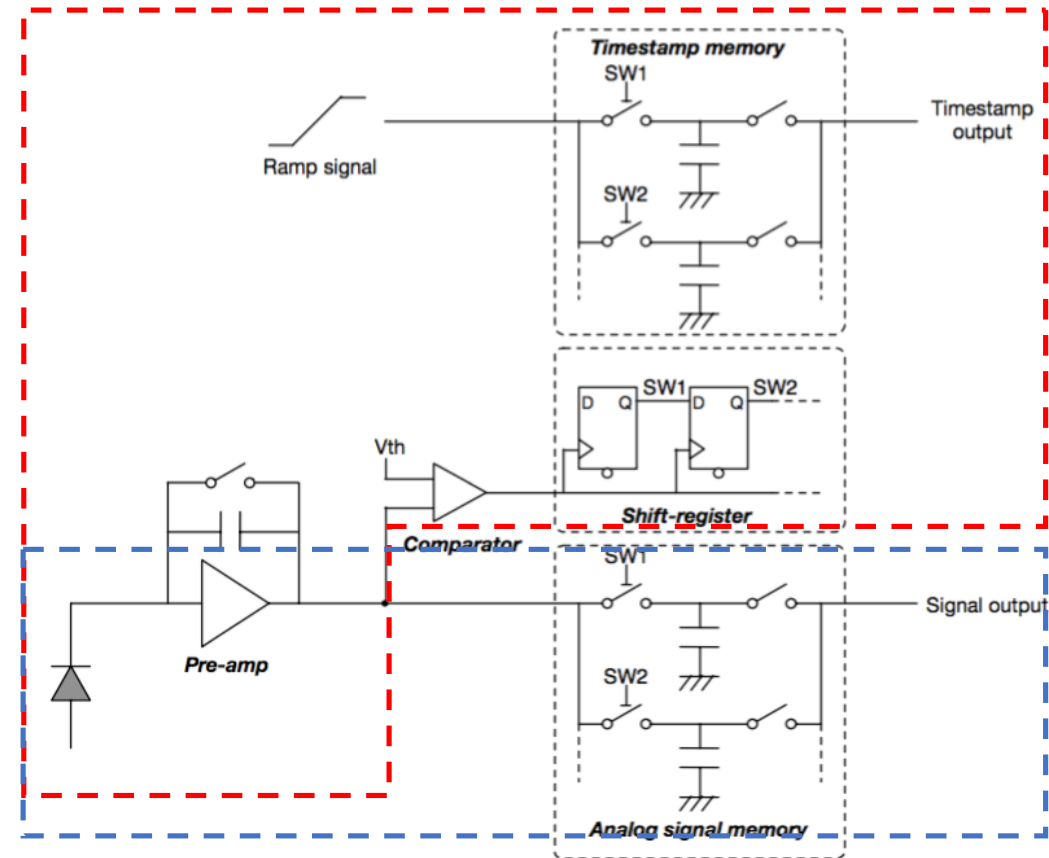
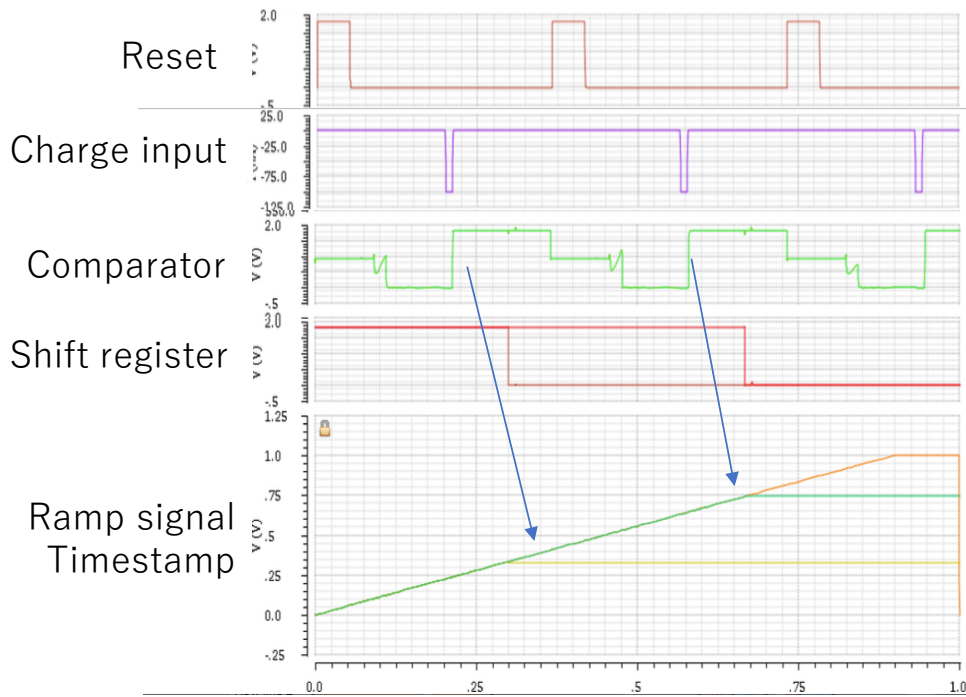
- SOFIST prototype chips
 - **SOFIST Ver.1**
 - Pixel with analog signal readout
 - Delivered in Dec. 2015
 - **SOFIST Ver.2**
 - **Pixel with time stamp readout**
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- SOFIST Ver.3 ~
 - Pixel integration of Ver.1 and Ver.2
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SOFIST Ver.2 pixel

- SOFIST Ver.2: In-pixel timestamp.

Pixel simulation

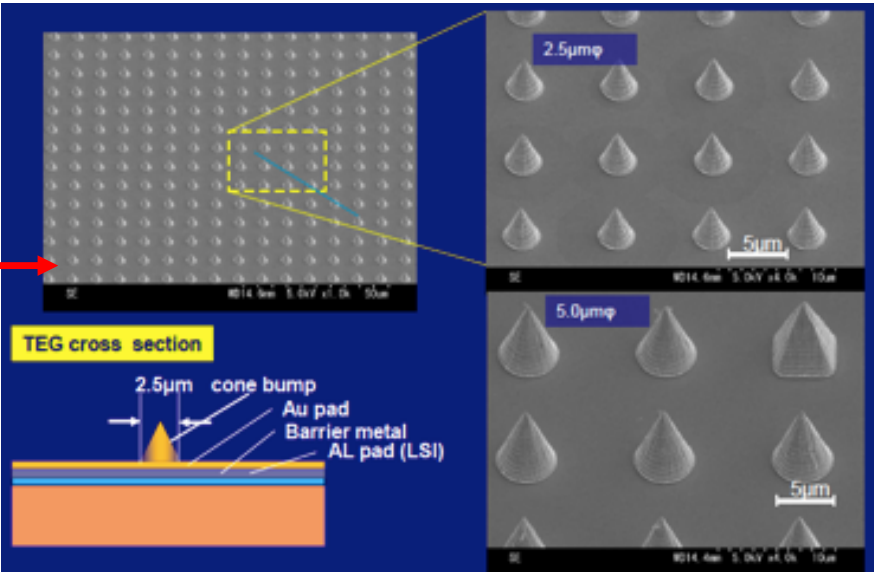
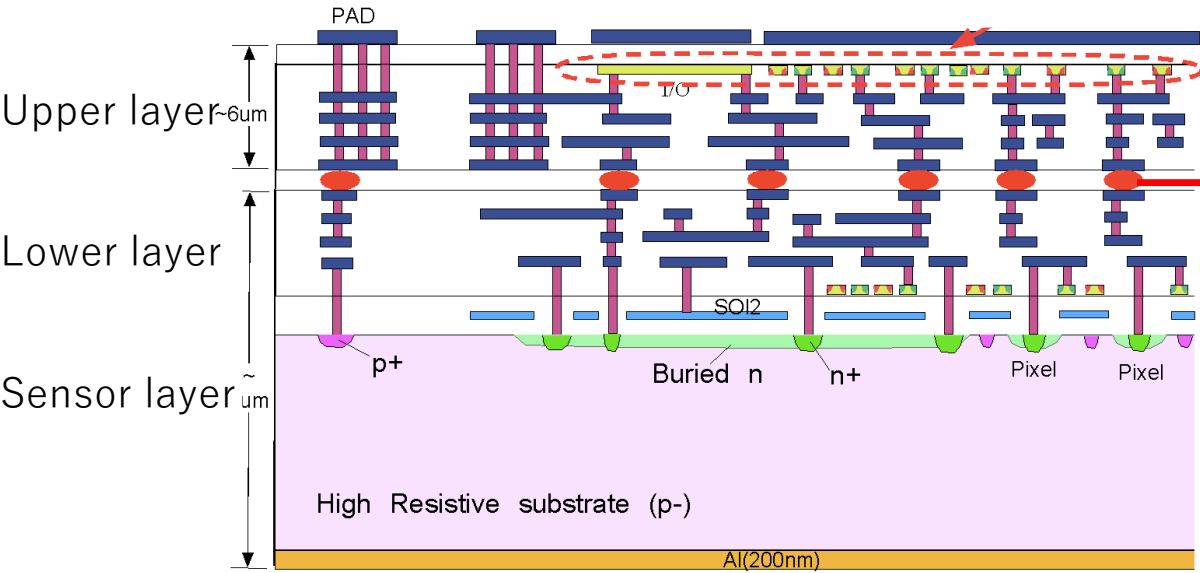


SOFIST Ver.3/Ver.4

- Design of next prototype chips
 - SOFIST Ver.3; Pixel size: **30x30um²**
 - Pixel circuit integration of both Ver.1 and Ver.2
 - 3 analog signal memories and 3 timestamps
 - SOFIST Ver.4; Pixel size: **20x20um²**
 - SOI sensor with 3D stacking technology
 - Reduction of the pixel size from Ver.3

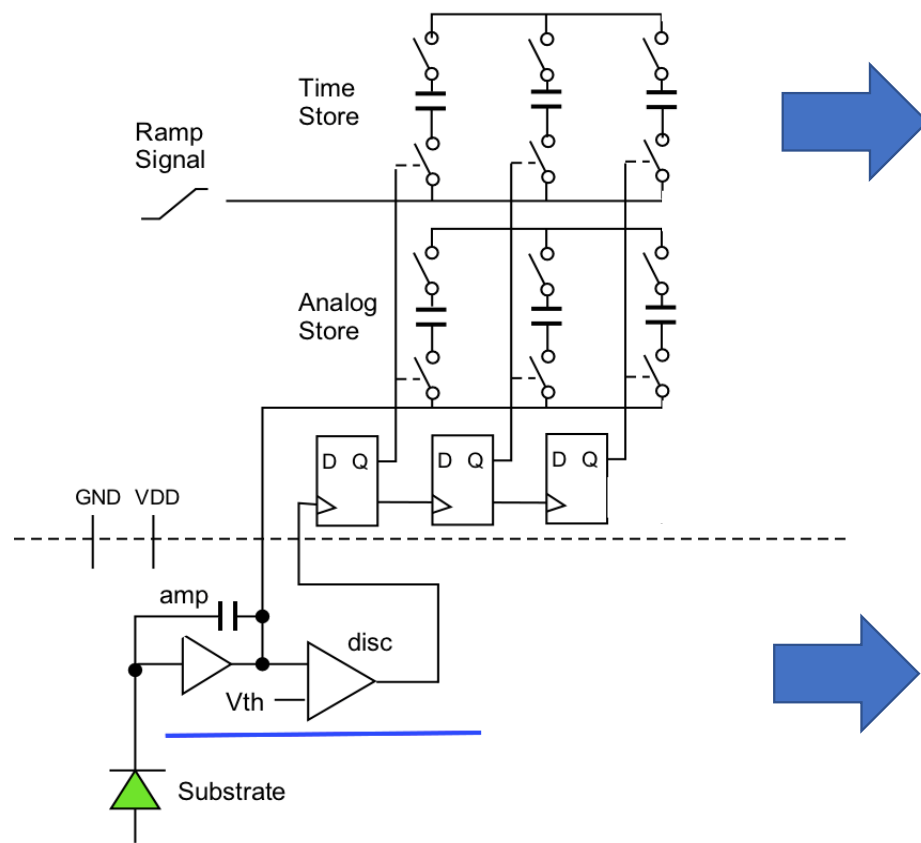
SOI-3D stacking sensor

- Stacking circuit chip on SOI sensor
 - Connecting upper and lower chip by Au cone bump with 5um pitch

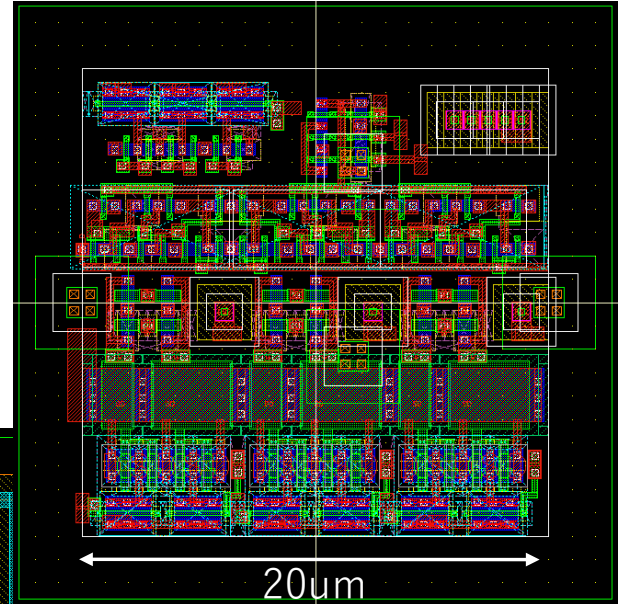
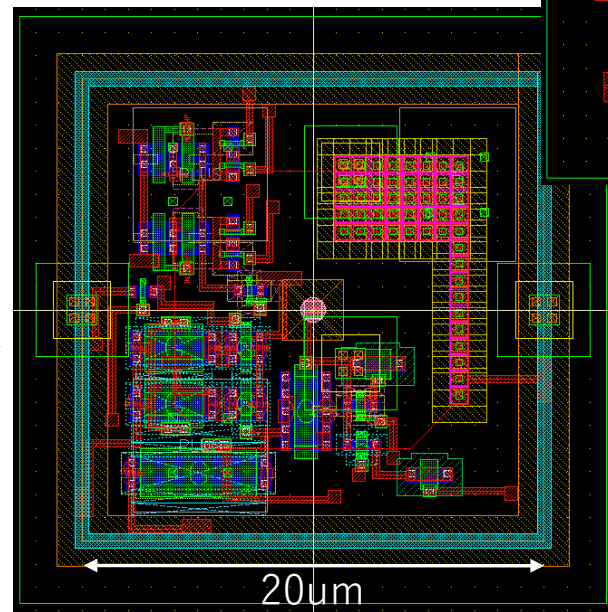


Tohoku MicroTec Co., Ltd.

SOI-3D stacking sensor



- Upper pixel
- Shift-register
 - Analog memory x3
 - Timestamp x3



- Lower pixel
- Pre-amp
 - Comparator

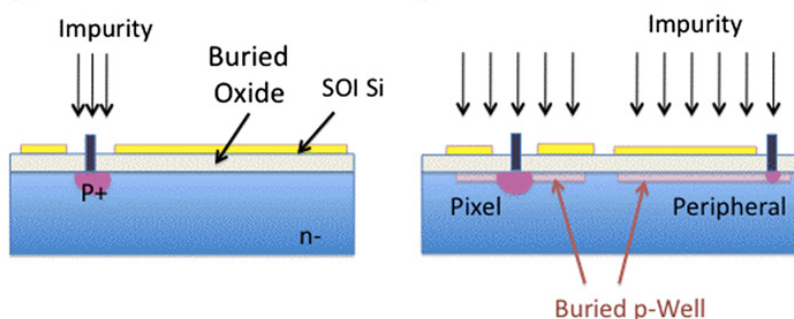
Summary

- Development SOI pixel sensor for the ILC experiment : SOFIST
 - SOFIST Ver.1: Analog signal readout
 - Beam test at Fermilab Test beam line.
 - Position resolution $\sim 1.7 \mu\text{m}$ @ 500um sensor thickness
 - SOFIST Ver.2: In-pixel timestamp circuit
 - Production was done.
 - SOFIST Ver.3/4: Pixel integration
 - Ver.4: Pixel implementation with 3D stacking technology
 - Under designing

Backup

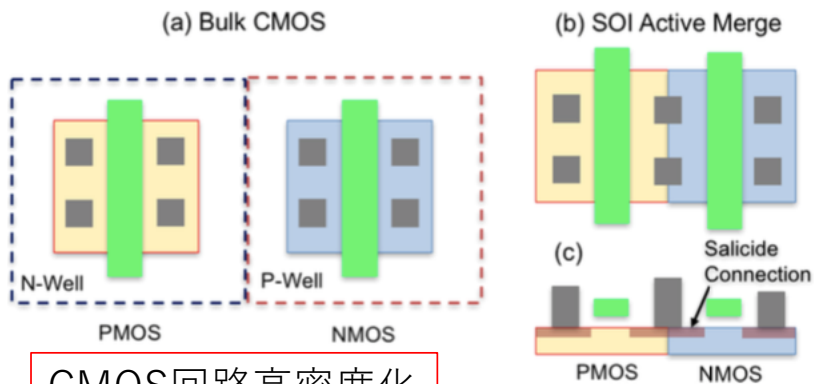
SOIピクセル検出器の特徴

- BPW (Buried p-well)



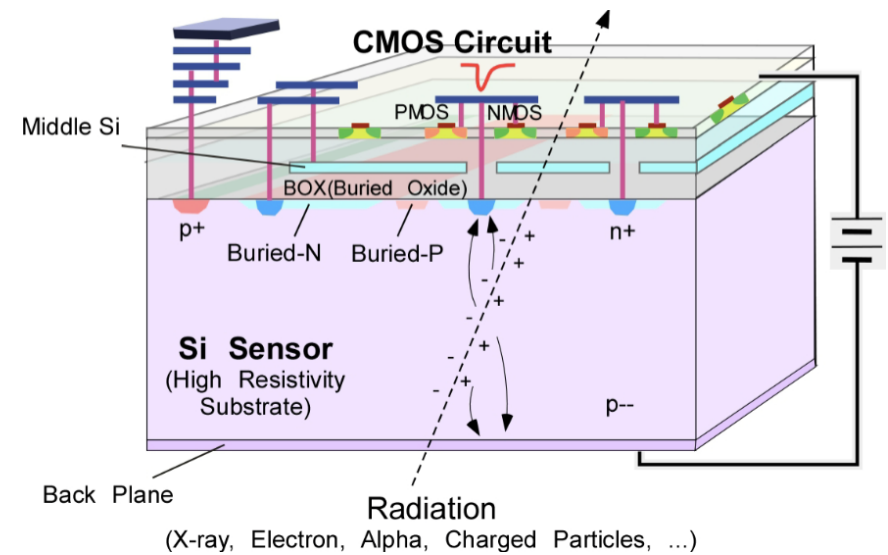
センサー部完全空乏化・電荷収集効率向上

- Active共有化



CMOS回路高密度化

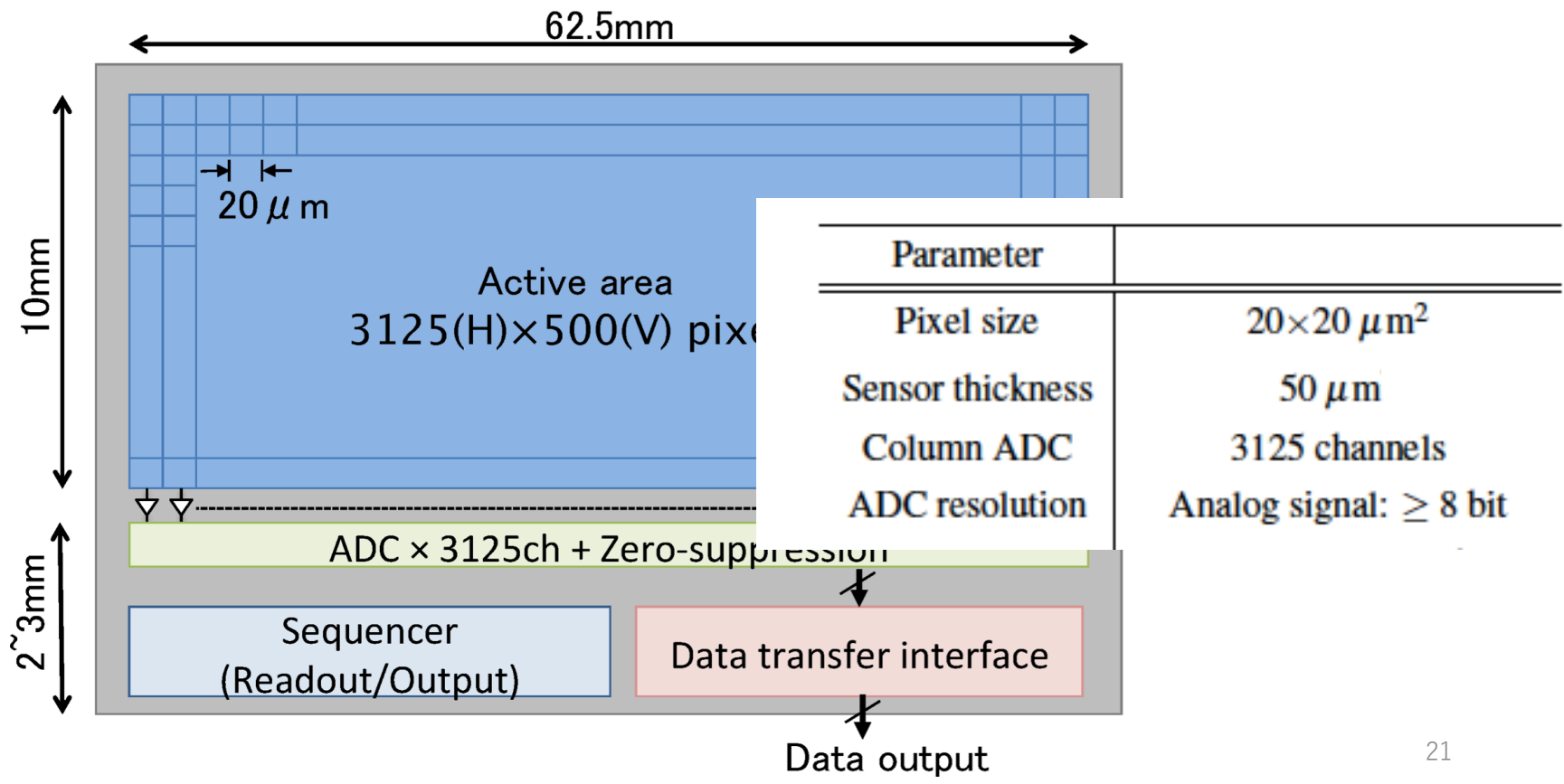
- Double-SOI



Middle Si層によるシールド
放射線耐性(TID)強化: > 1Mrad

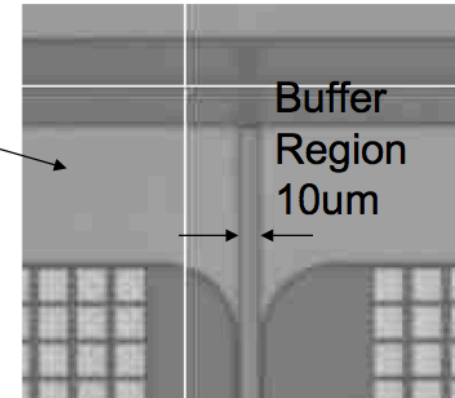
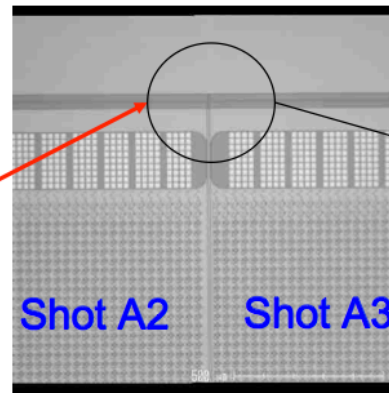
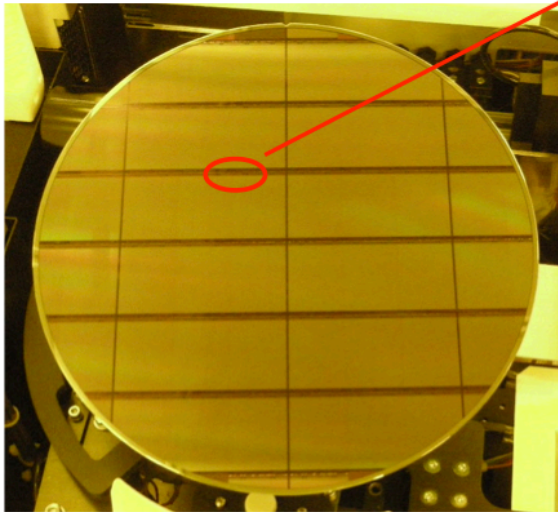
SOI sensor for ILC: SOFIST

- SOI sensor for Fine measurement of Space and Time



Stitching Exposure for Large Sensor

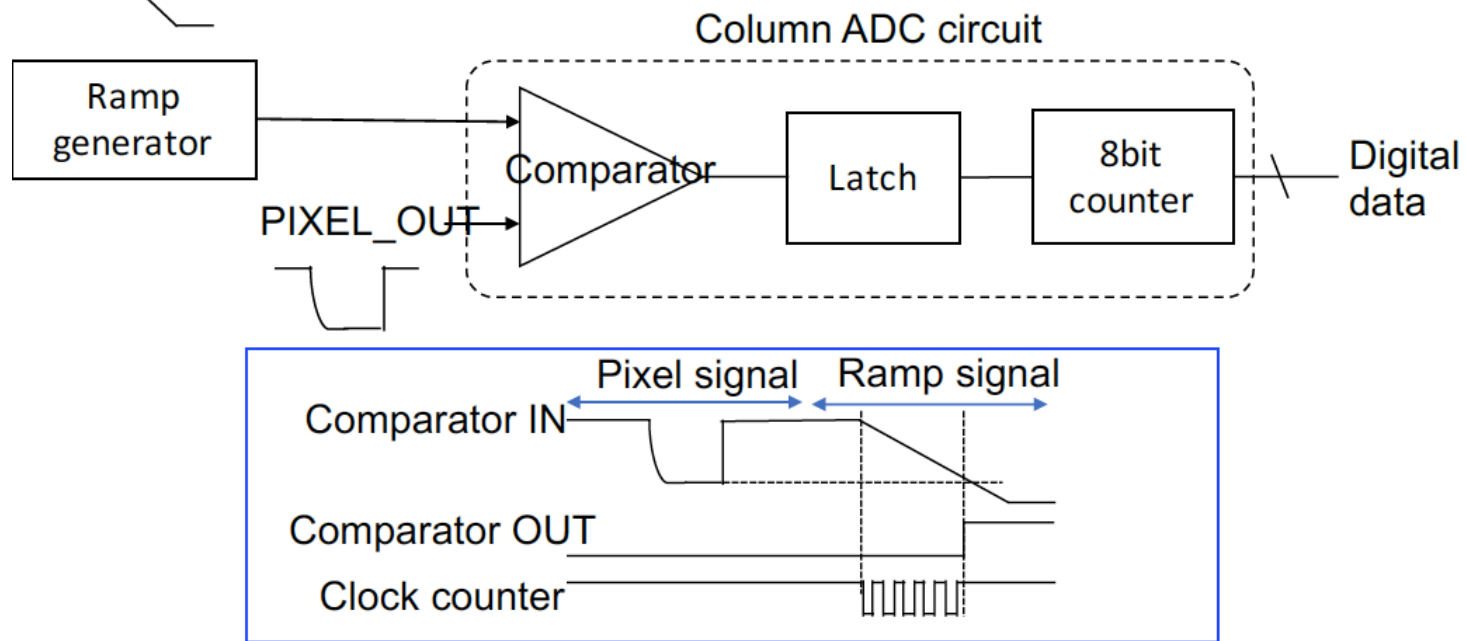
Produce 26.7 mm x 64 mm Sensing Area (3 Stitching).



- Width of the Buffer Region can be less than 10um.
- Accuracy of Overwrap is better than 0.025um.
- 1-direction stitching at present.

SOFIST Ver.1: Column ADC

- Colum ADC circuit
 - Wilkinson-Type ADC
 - Resolution: $8\text{bit} / 1\text{V} = 3.9\text{mV/bit}$, Conversion time: $2.56\mu\text{sec}$



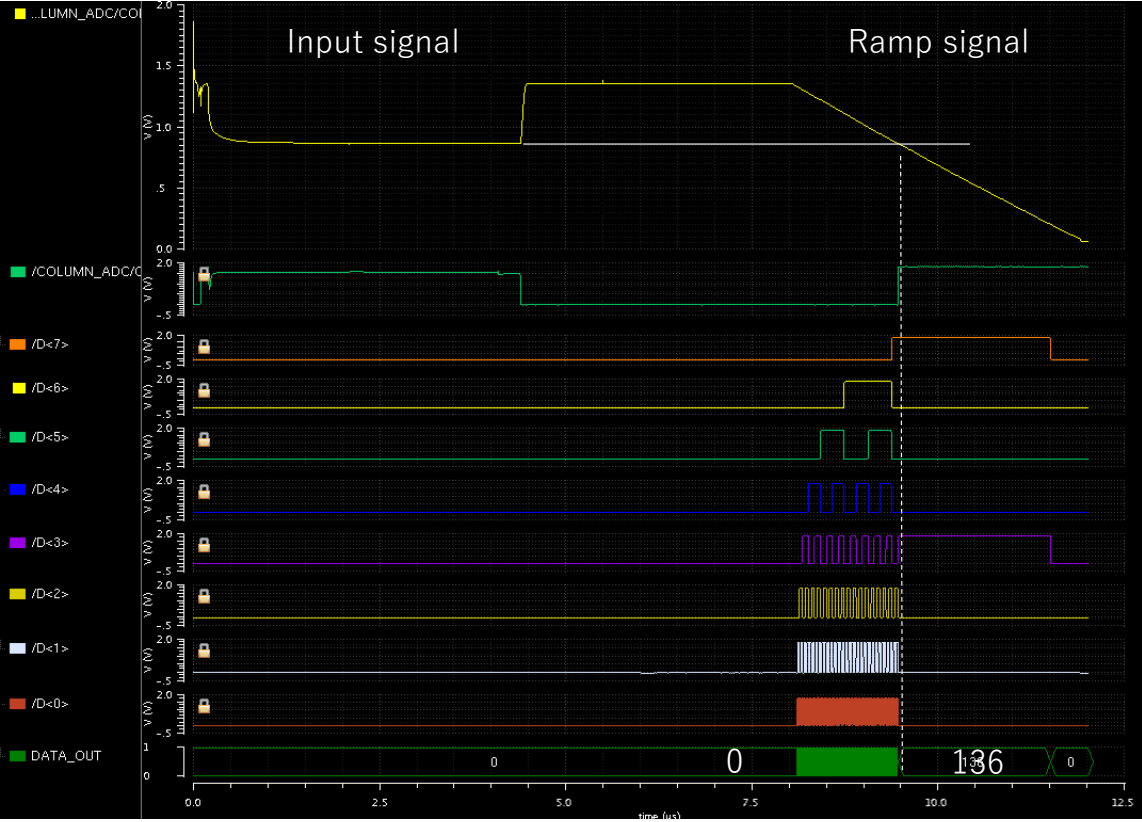
SOFIST Ver.1: Column ADC

- ADC SPICE simulation

Signal/Ramp input

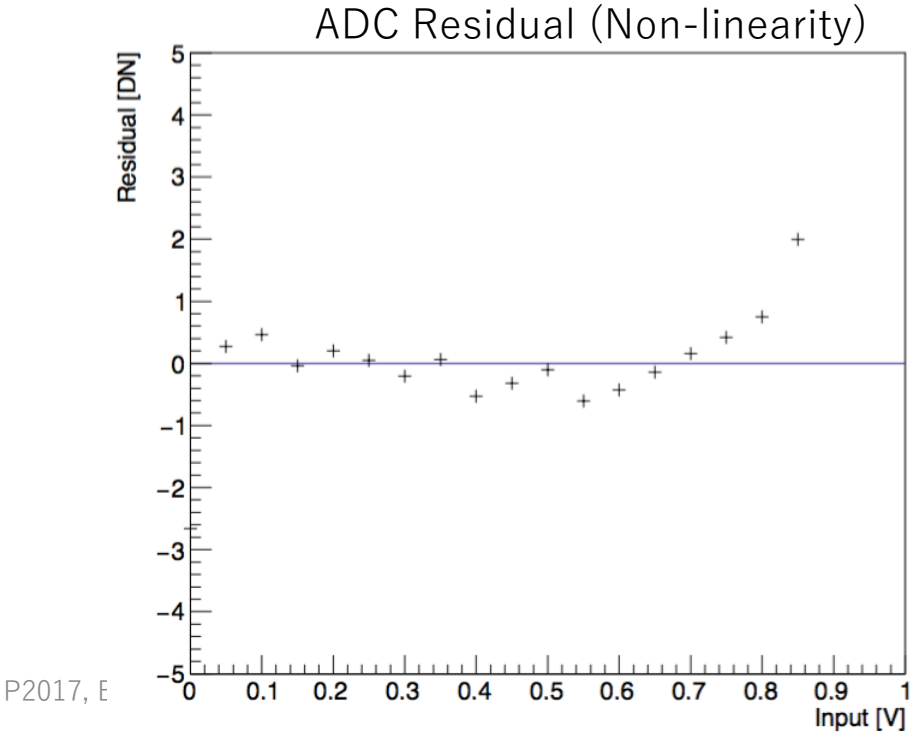
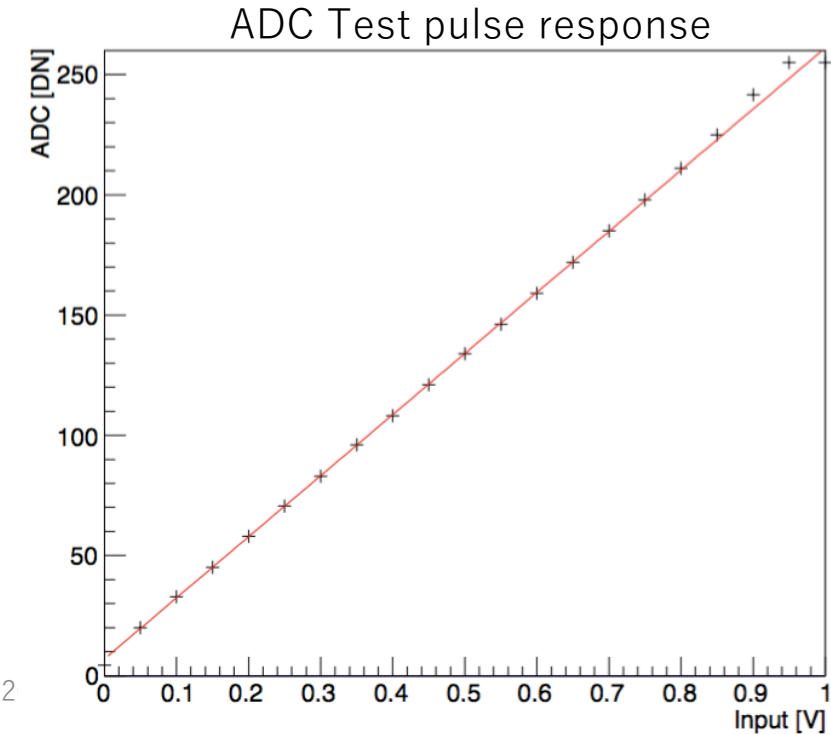
Comparator

Output (8bit)



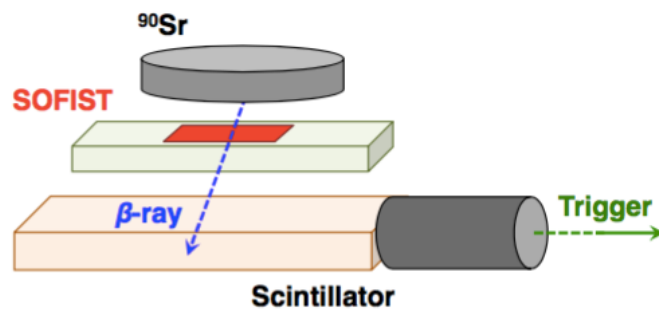
SOFIST Ver.1:

- Column ADC: output linearity
 - ADC response by test pulse input.

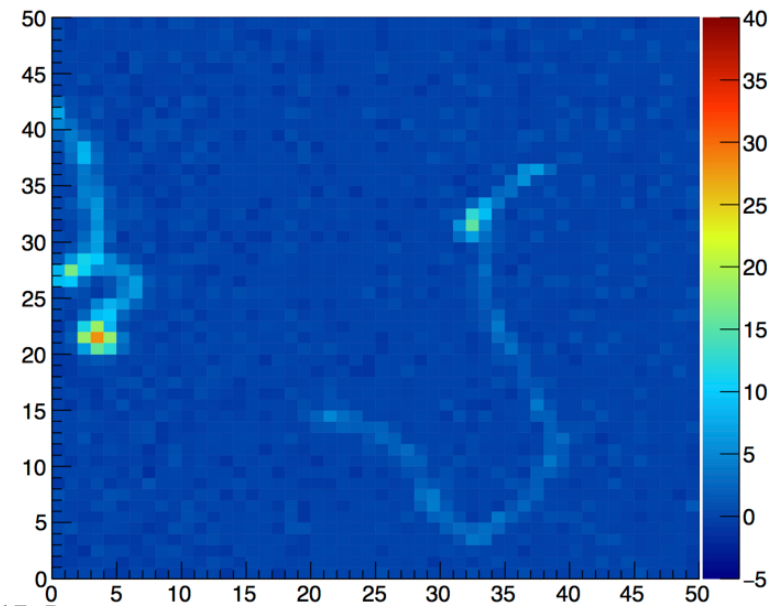


SOFIST Ver.1 chip

- Sr-90 irradiation
 - SOFIST setup: Bias voltage = 140V, Readout by On-chip ADC

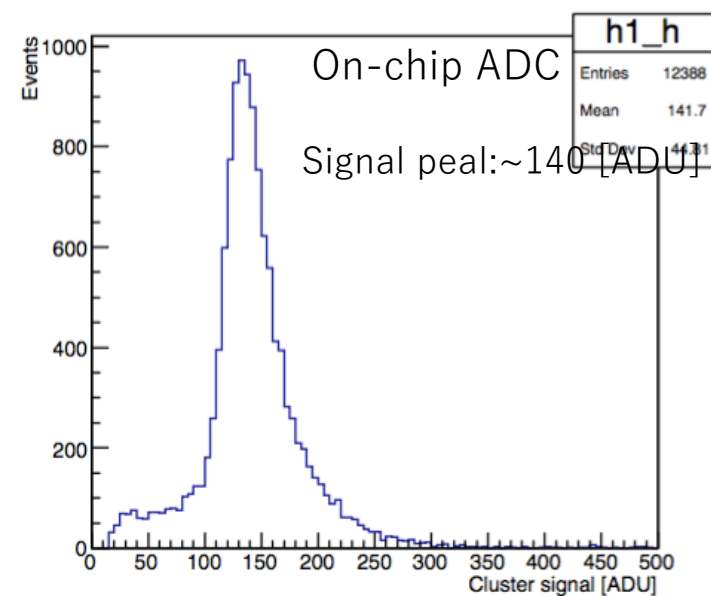
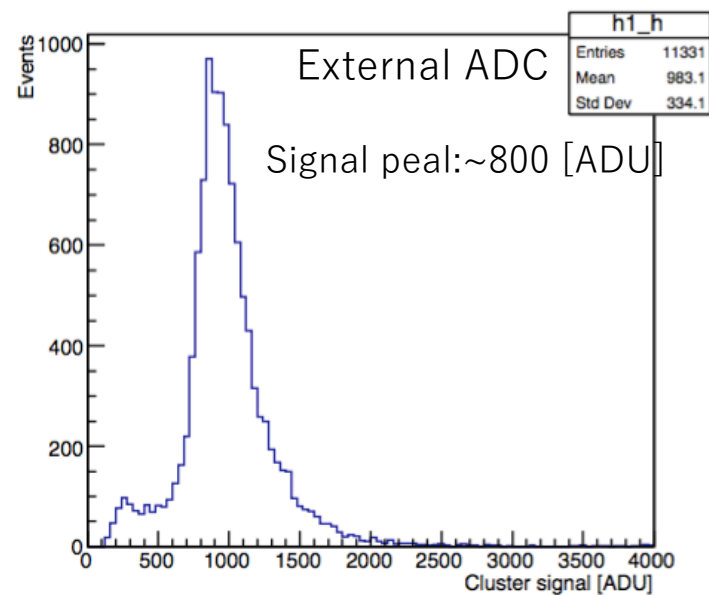


SOFIST output data



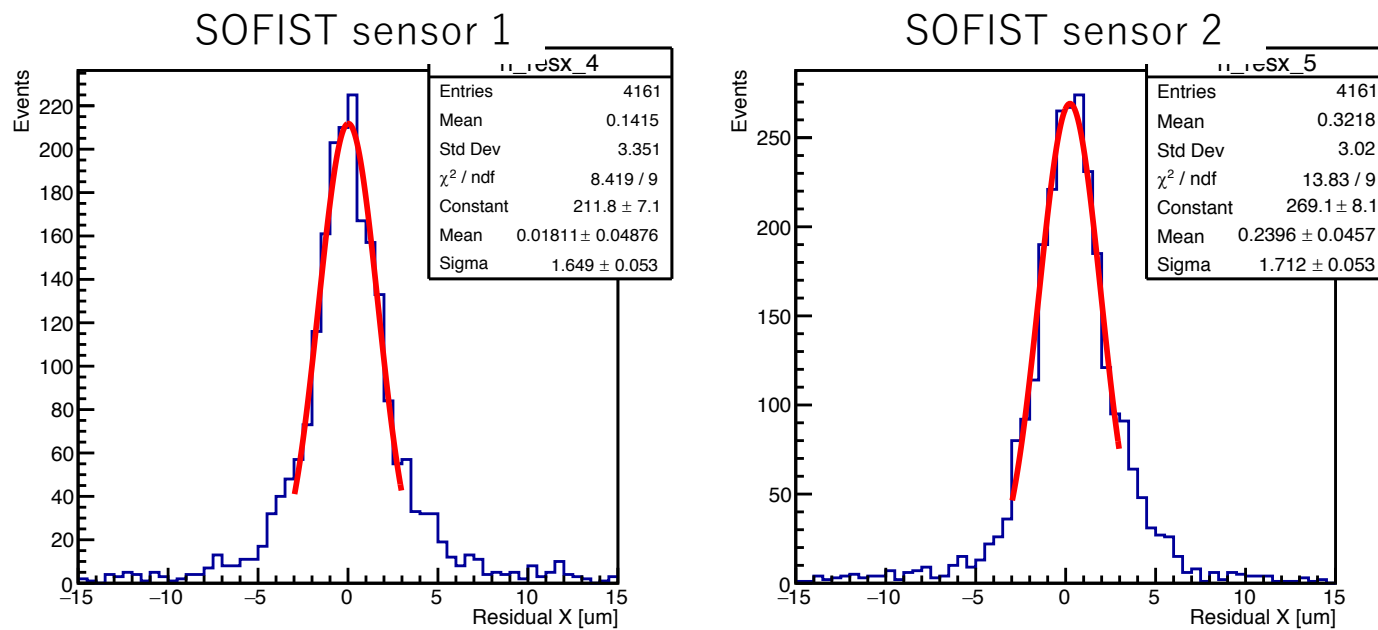
SOFIST Ver.1: Signal spectrum

- Cluster signal spectrum
 - SOFIST setup: External ADC (12 bit), On-chip ADC (8 bit)
 - Bias voltage: 130V (Full depletion), Clustering: 6x6 pixels



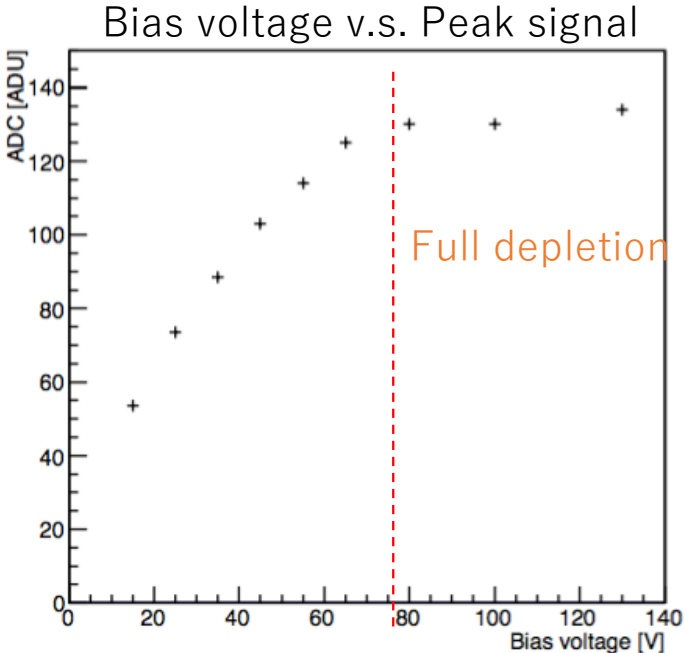
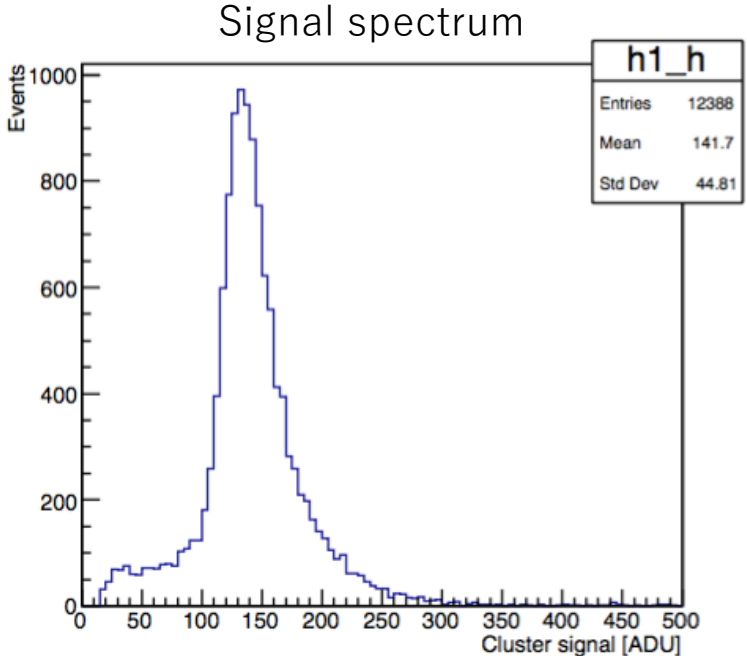
Chip evaluation: Position resolution

- Residual analysis result
 - Bias voltage = 130V Depletion width: ~500 [μm]



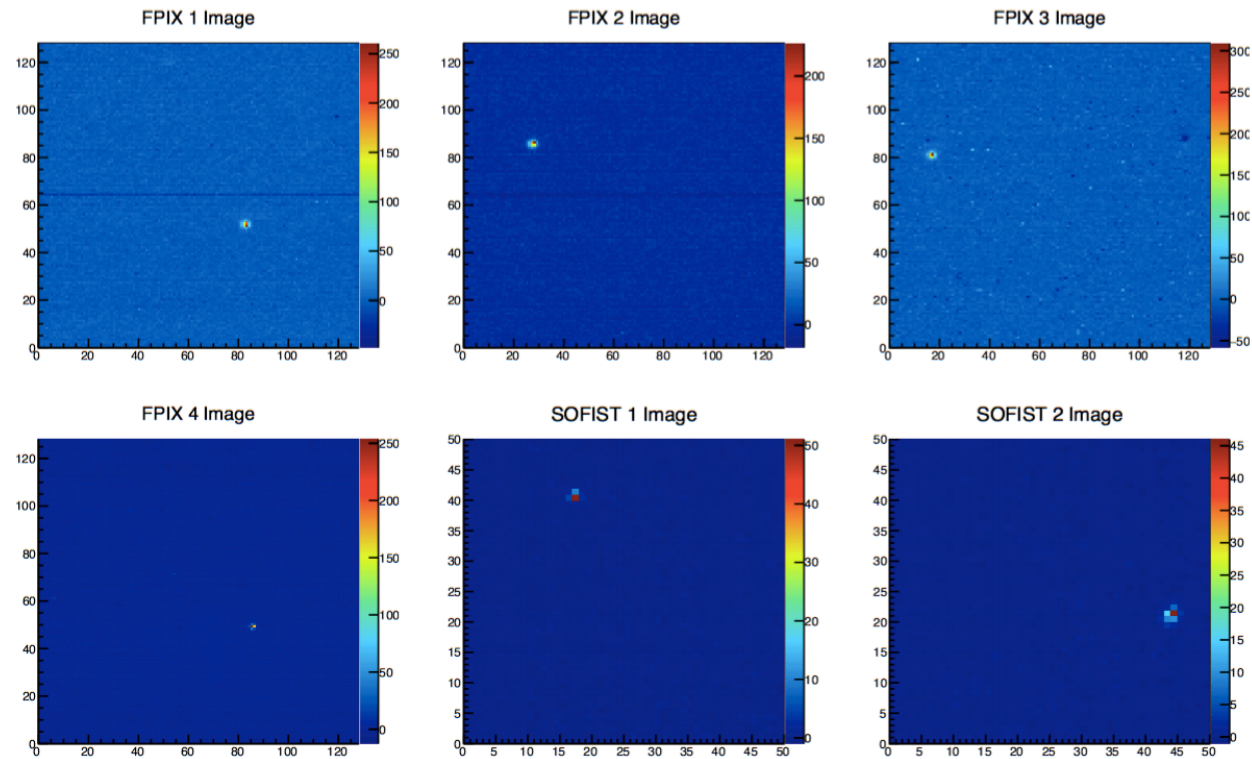
SOFIST Ver.1: HV scan

- Bias voltage dependence of Peak signal
 - Bias voltage: 15 ~ 130V



SOFIST Ver.1:Beamtest

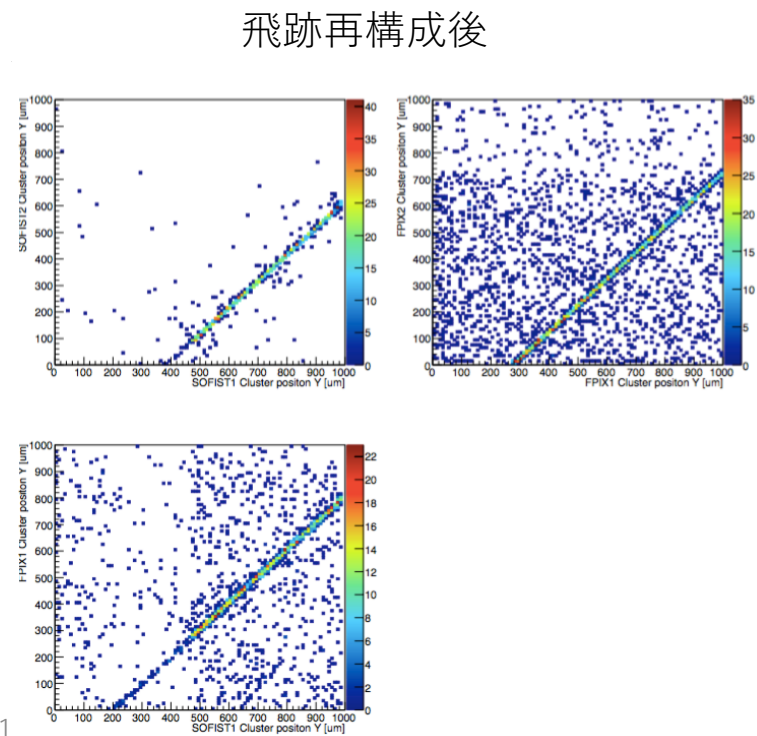
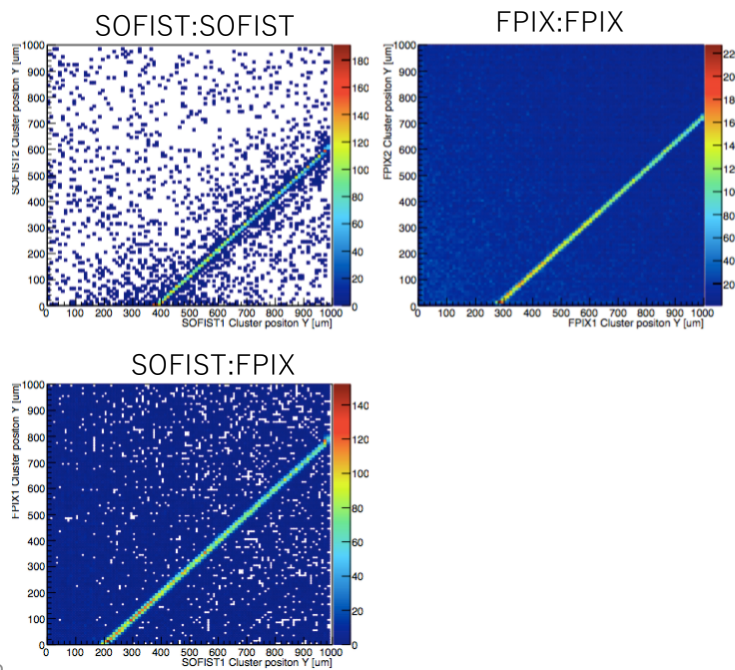
- Event display



2017/5/25

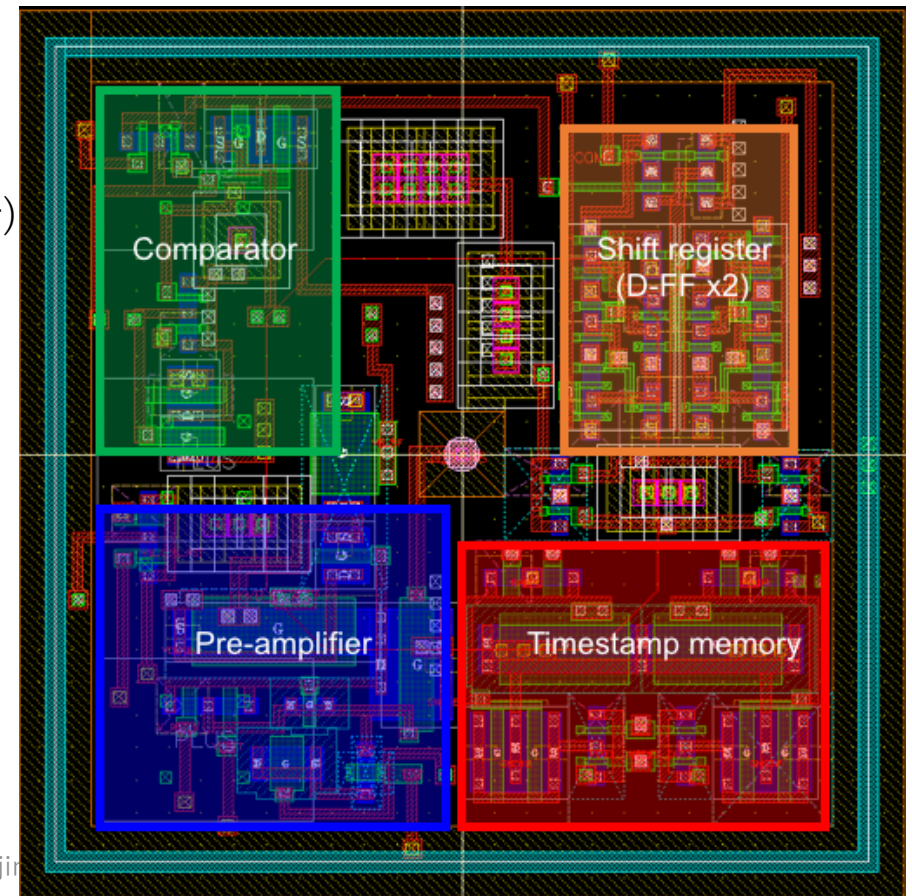
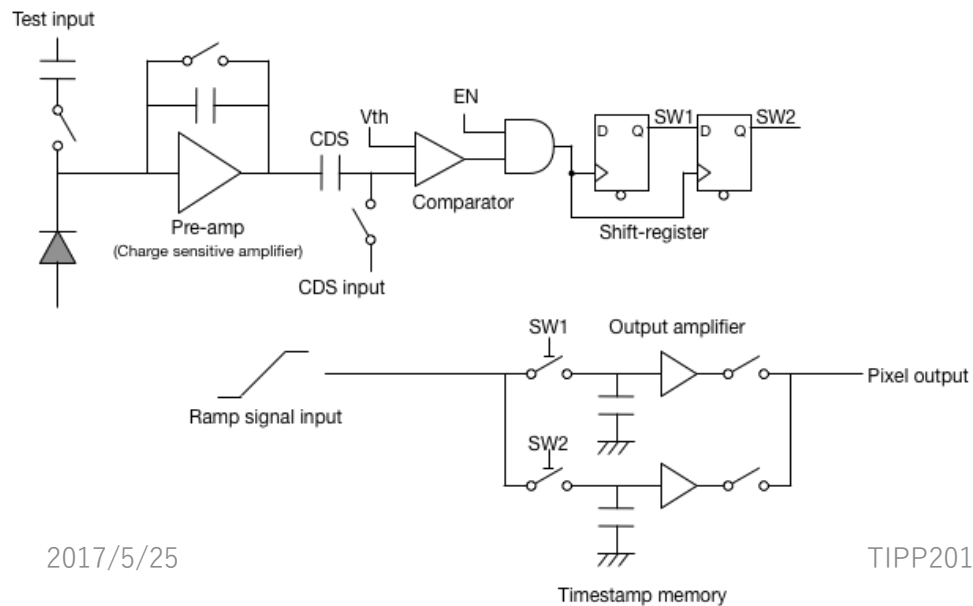
SOFIST Ver.1: 飛跡再構成

- 飛跡再構成によるイベントカット
 - 検出器間のヒット位置、相関



SOFIST Ver.2: Pixel circuit

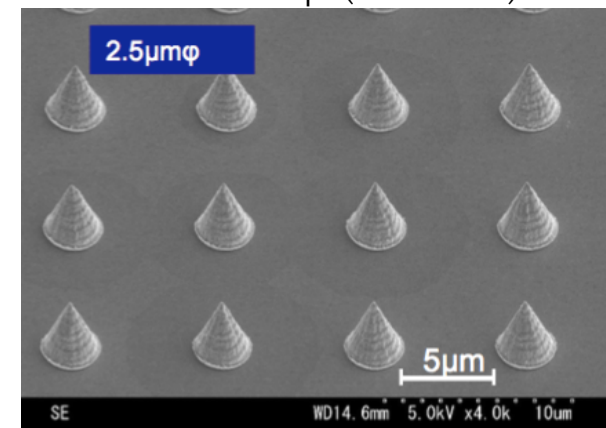
- Pixel circuit
 - Pixel size: $25 \times 25 \mu\text{m}^2$
 - Pre-amp: CSA (Cf: $\sim 3\text{fF}$)
 - Comparator: Chopper inverter (Cap. + Inverter)
 - Shift-register: D-FF x2



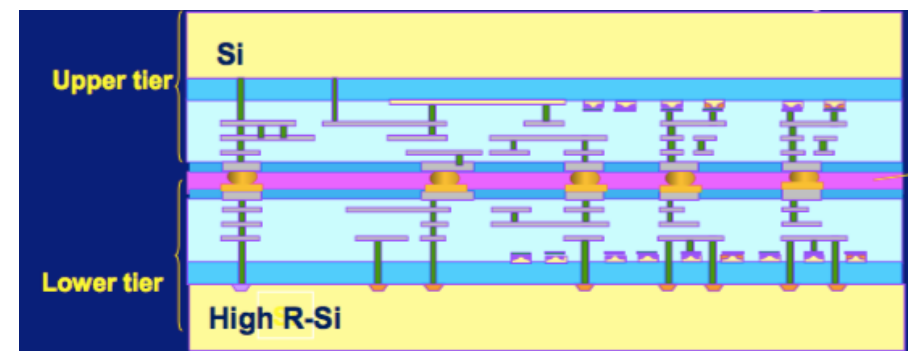
次期試作チップ開発

- SOFIST Ver.3
 - Pixel: **30x30 μm^2**
 - (Analog memory + Timestamp) x3
- SOFIST Ver.4 (3D)
 - SOI pixel sensor with 3D stacking
 - Cone bump connection
 - Pixel: **20x20 μm^2**
 - (Analog memory + Timestamp) x3

Cone bump (T-Micro)

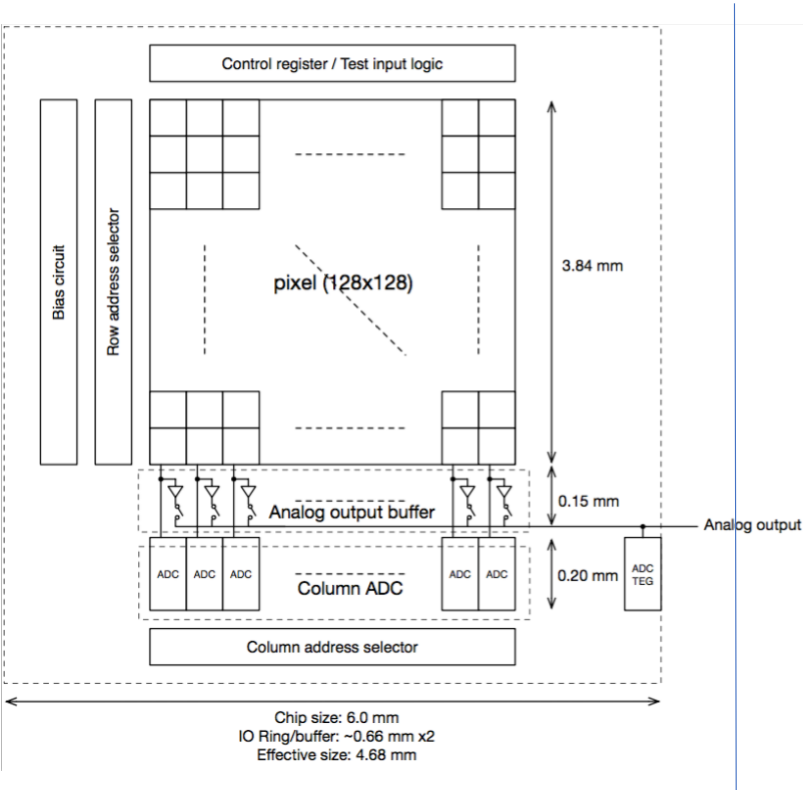


3D-stacking sensor (T-Micro)

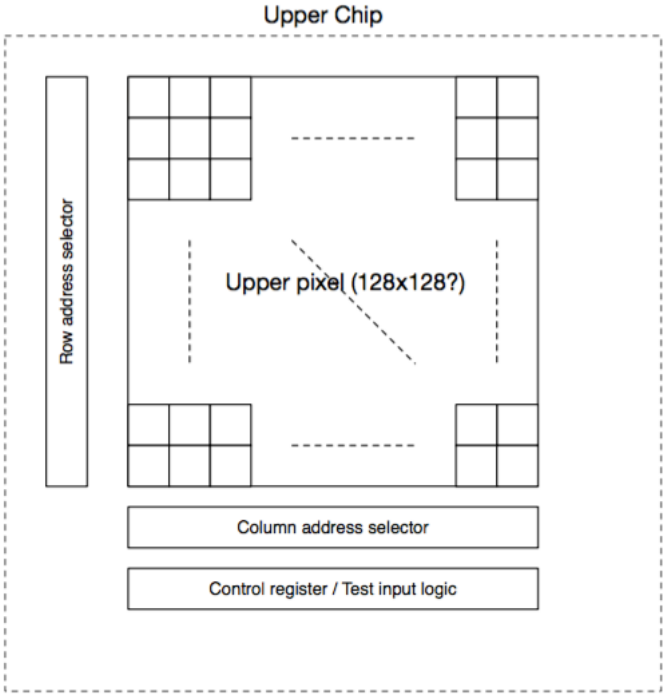
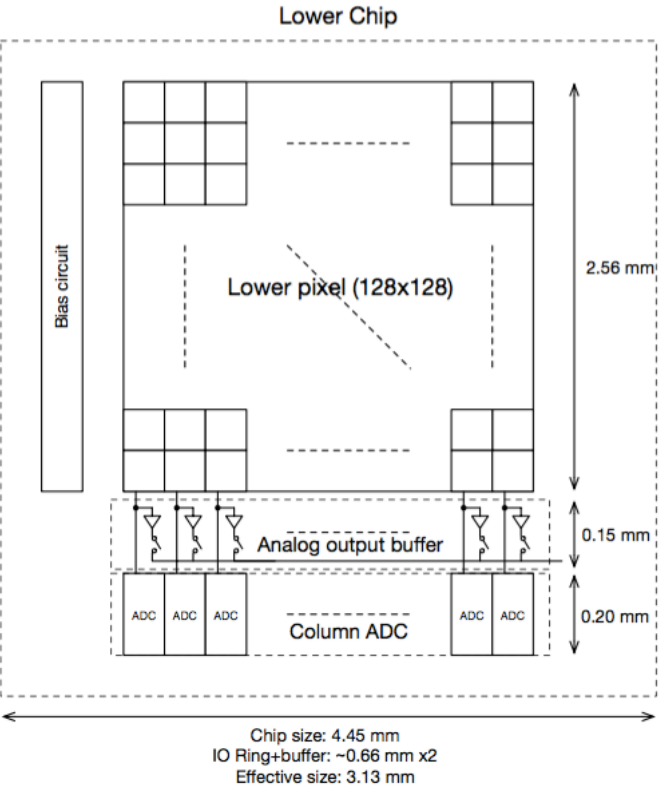


SOFIST Ver.3/Ver.4: Chip overview

Ver.3



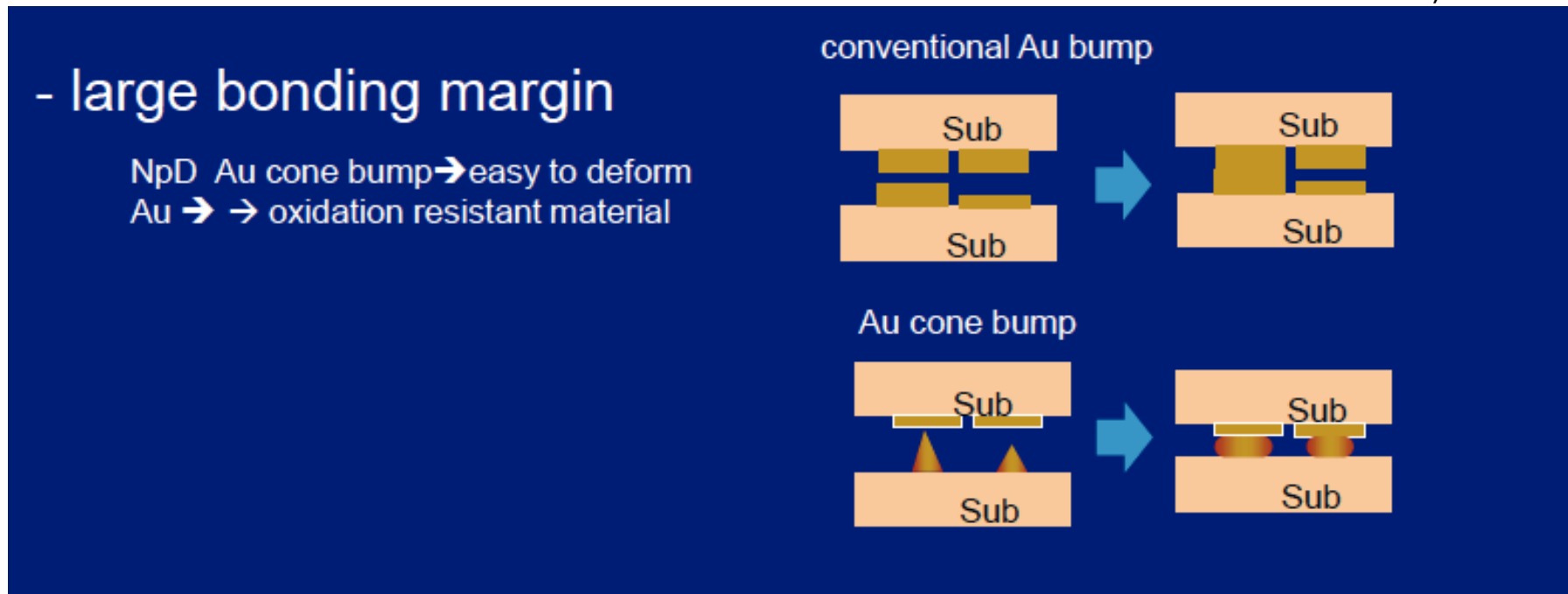
Ver.4(Upper, Lower chip)



Gold cone bump

- Merit of cone bump

Tohoku MicroTec Co., Ltd.



SOI-3D stacking sensor

- Stacking circuit chip on SOI sensor

