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CMOS pixel development for the ATLAS experiment at the HL-LHC

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To cope with the rate and radiation environment expected at the HL-LHC new approaches are being developed on CMOS pixel detectors, providing charge collection in a depleted layer.
They are based on: HV enabling technologies that allow to use high depletion voltages (HV-MAPS), high resistivity wafers for large depletion depths (HR-MAPS); radiation hard processed with multiple nested wells to allow CMOS electronics embedded with sufficient shielding into the sensor substrate and backside processing and thinning for material minimization and backside voltage application.
Since 2014, members of more than 20 groups in the ATLAS experiment are actively pursuing CMOS pixel R&D in an ATLAS Demonstrator program pursuing sensor design and characterizations.
The goal of this program is to demonstrate that depleted CMOS pixels, with monolithic or hybrid designs, are suited for high rate, fast timing and high radiation operation at LHC. For this a number of technologies have been explored and characterized. In this presentation the challenges for the usage of CMOS pixel detectors at HL-LHC are discussed such as fast read-out and low power consumption designs as well as fine pitch and large pixel matrices. Different designs of CMOS prototypes are presented with emphasis on
performance and radiation hardness results, and perspectives of application in the upgrade of the ATLAS tracker will be discussed.

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