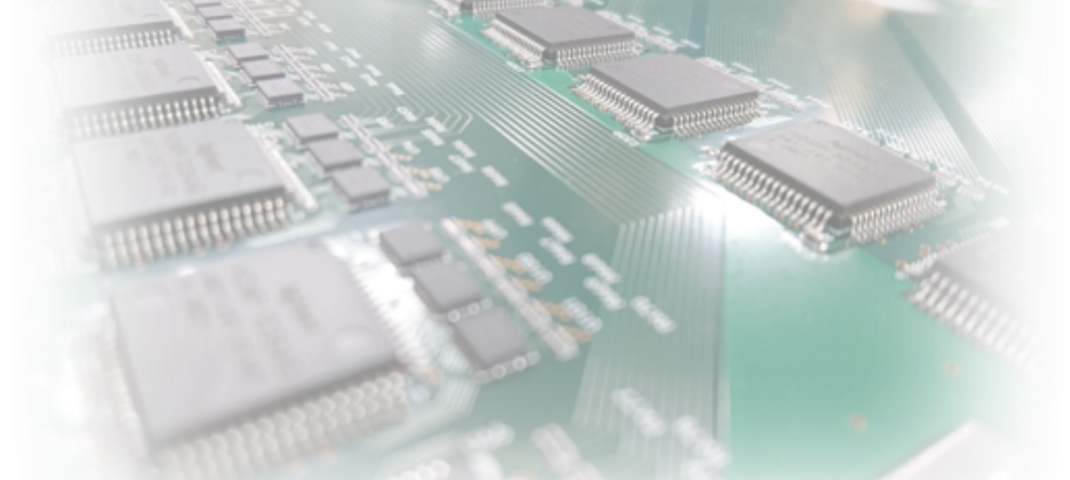
The Phase-1 Upgrade of the ATLAS Level-1 Endcap Muon Trigger

Shunichi Akatsuka (Kyoto University)
on behalf of the ATLAS Collaboration

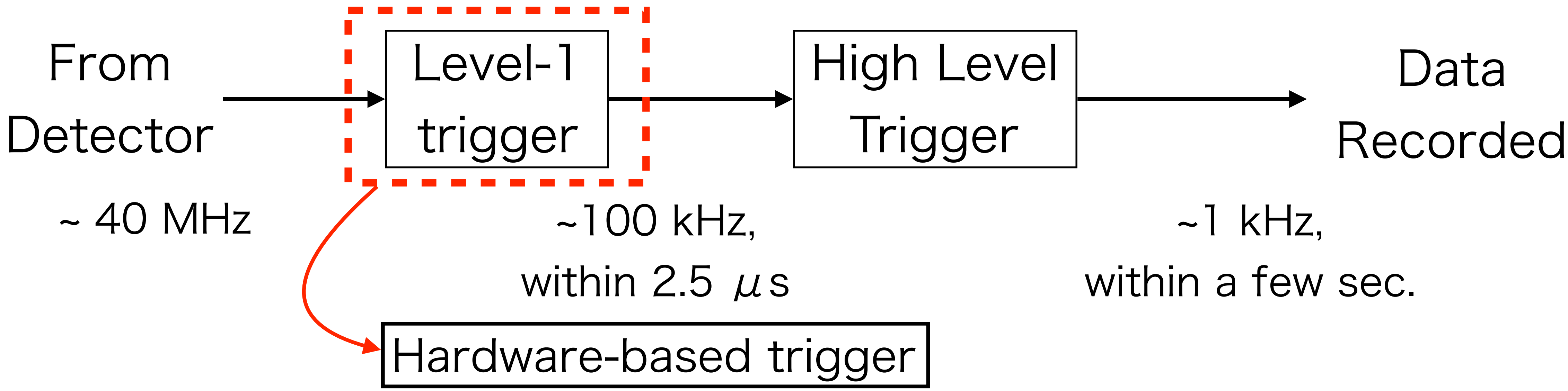


TIPP 2017 @Beijing 22-26 May, 2017

Introduction

- **LHC Run 3: 2021~ 2023**
  - Instantaneous luminosity will be 3×10^{34} cm^{-2}s^{-1}
  - More than twice the Run 2 luminosity

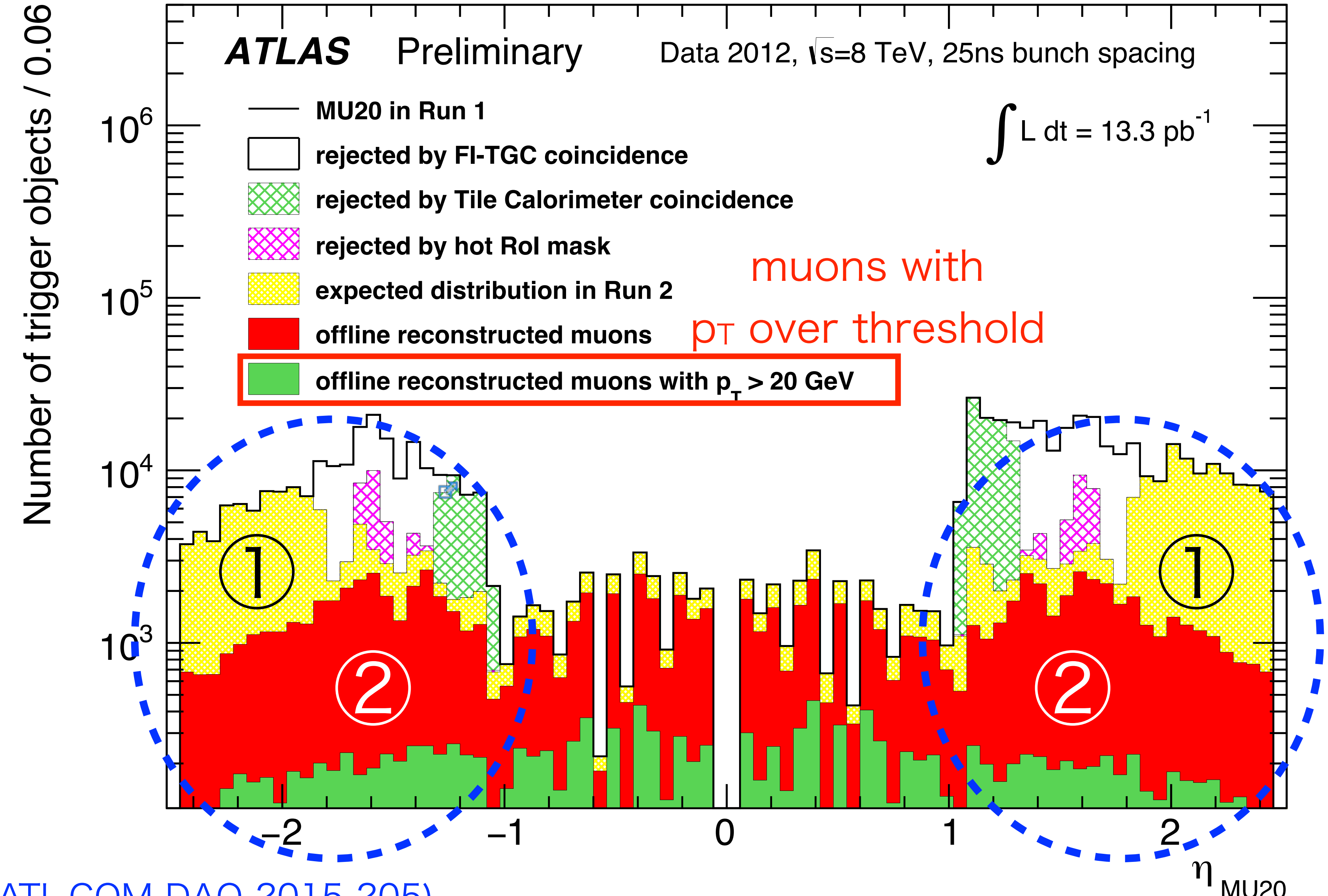
- **ATLAS Trigger System**



- **Phase-1 Upgrade for Level-1 Endcap Muon Trigger**
  - With Run 2 trigger system, the rate for muon trigger with p_T > 20 GeV will become **28 kHz** @ 3×10^{34} cm^{-2}s^{-1} (TDAQ TDR, ATLAS-TDR-023)
  - Run 3 requirement is **15 kHz** ← ~50% rate reduction is required
  - More powerful trigger strategy is needed to reduce the trigger rate, while keeping the trigger threshold and the efficiency

Level-1 muon trigger performance

- η distribution of the Level-1 Muon Trigger with p_T > 20 GeV



(ATL-COM-DAQ-2015-205)

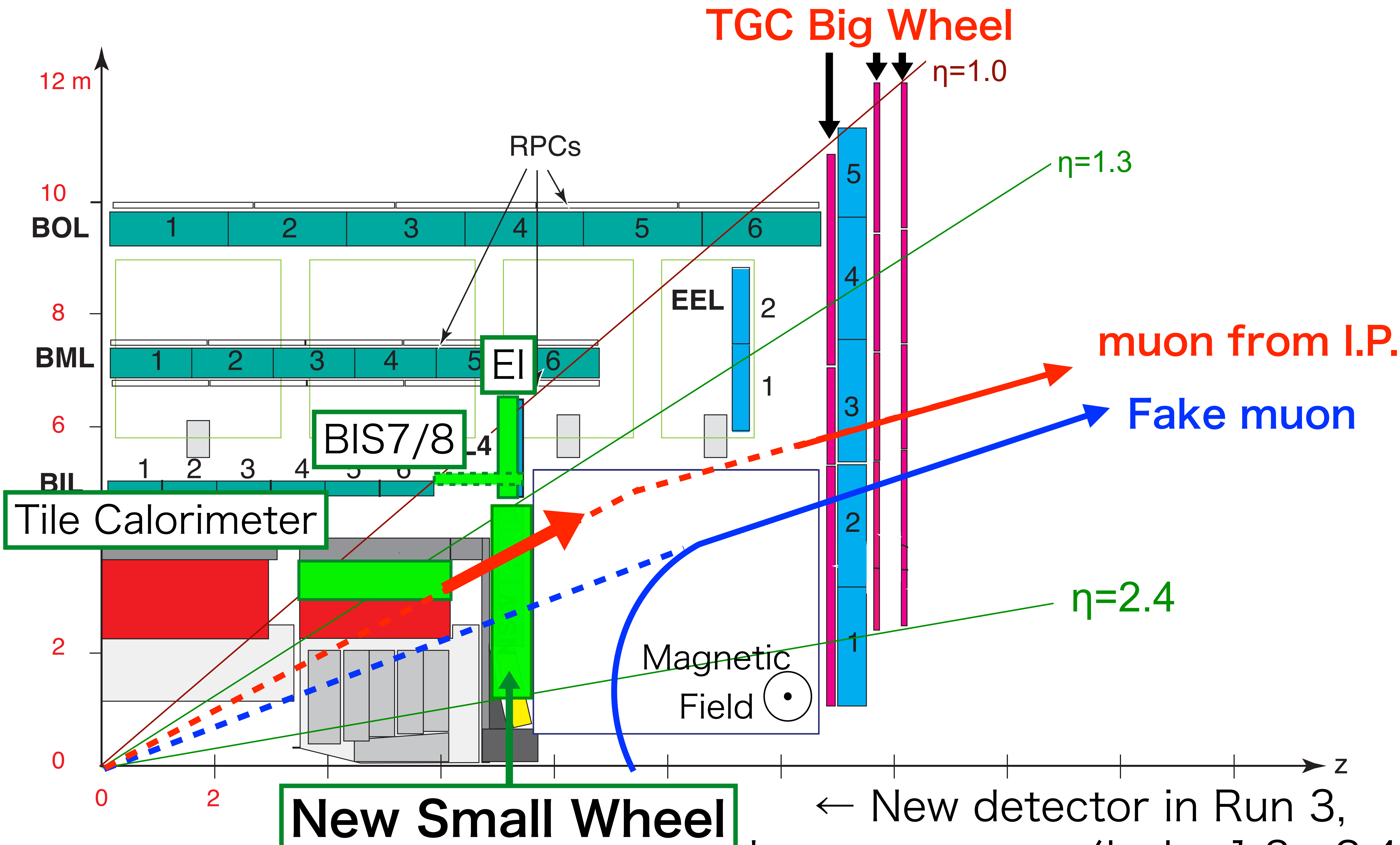
① Trigger with **no matching real muons (Fake muon)**

② Trigger by **Low p_T muons**

→ **Reject these triggers by introducing new coincidence logic!**

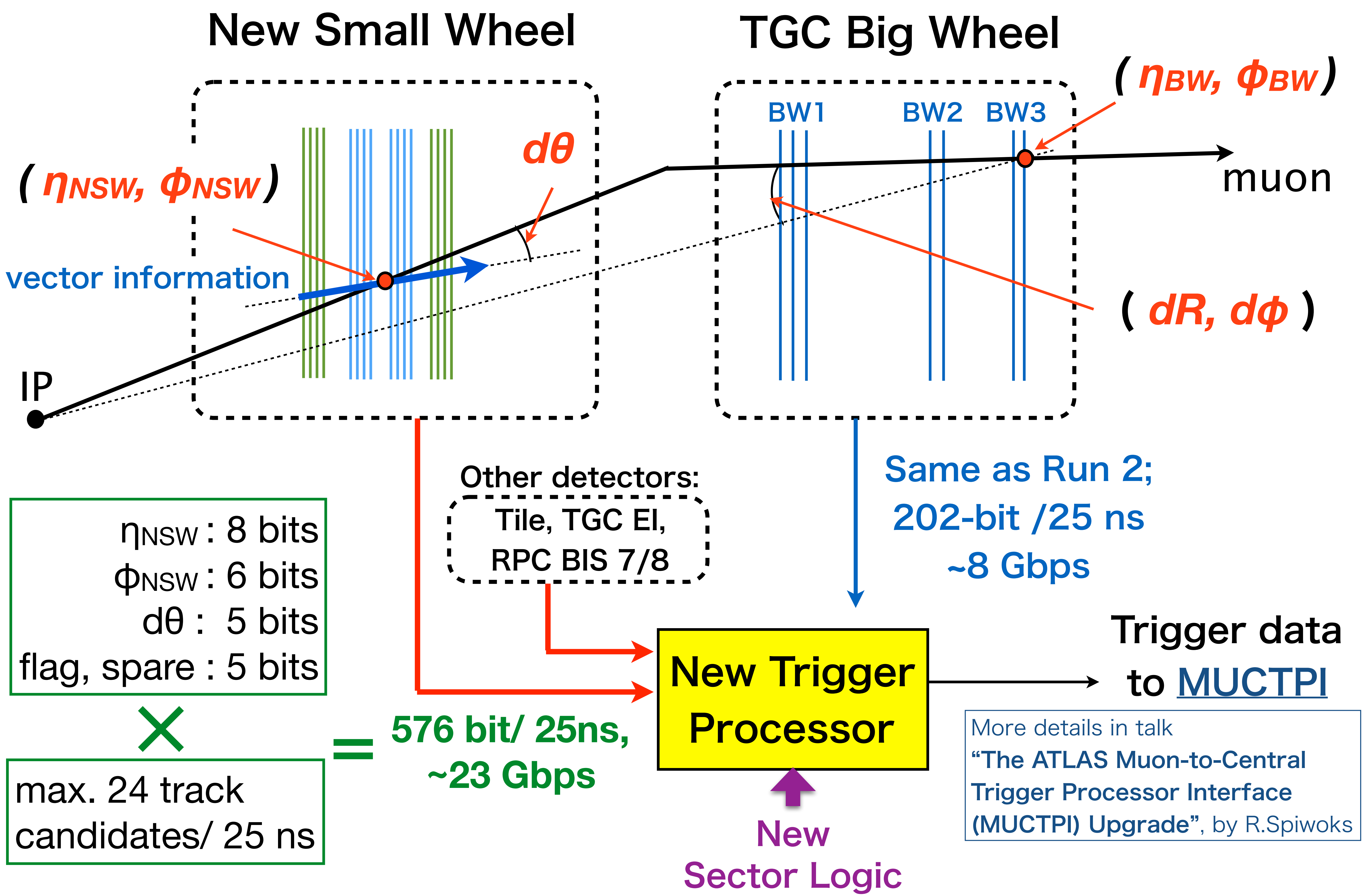
Level-1 Muon Trigger Strategy

- TGC Big Wheel + <u>Coincidence with detectors inside</u>
  → Reject fake muons



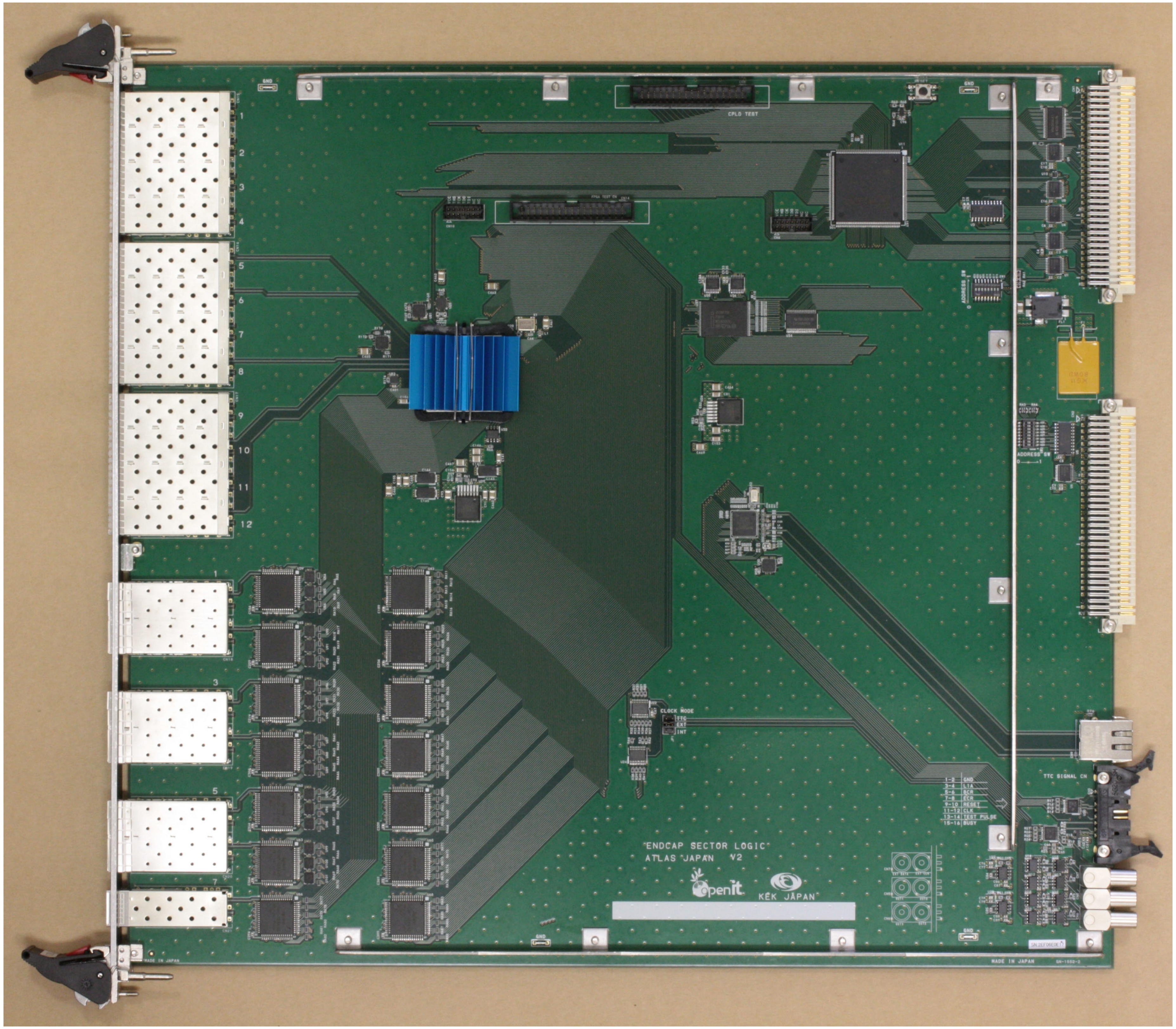
← New detector in Run 3, larger coverage (|η| ~ 1.3 - 2.4)

Run 3 Level-1 Endcap Muon Trigger

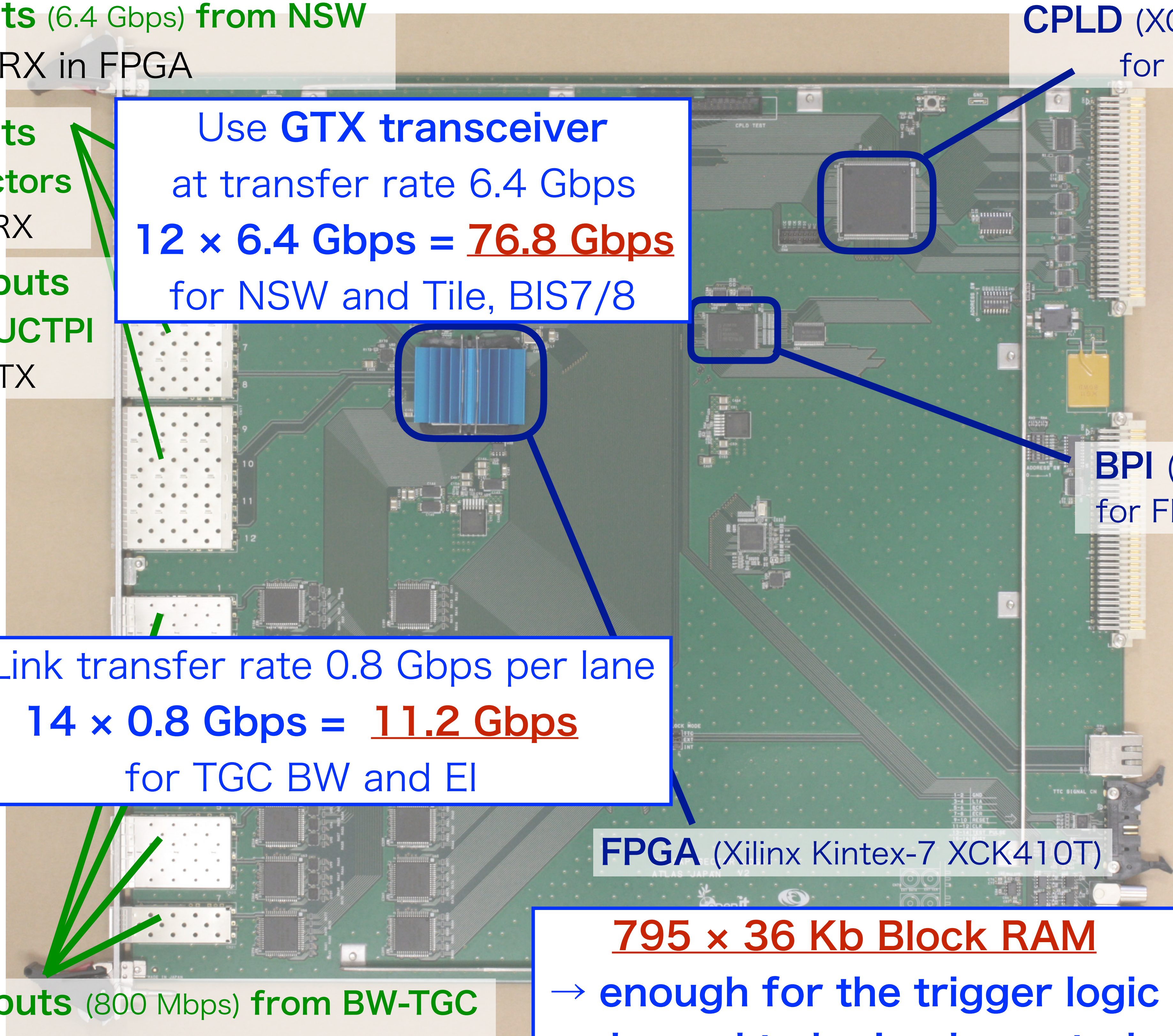


Hardware and Firmware Development

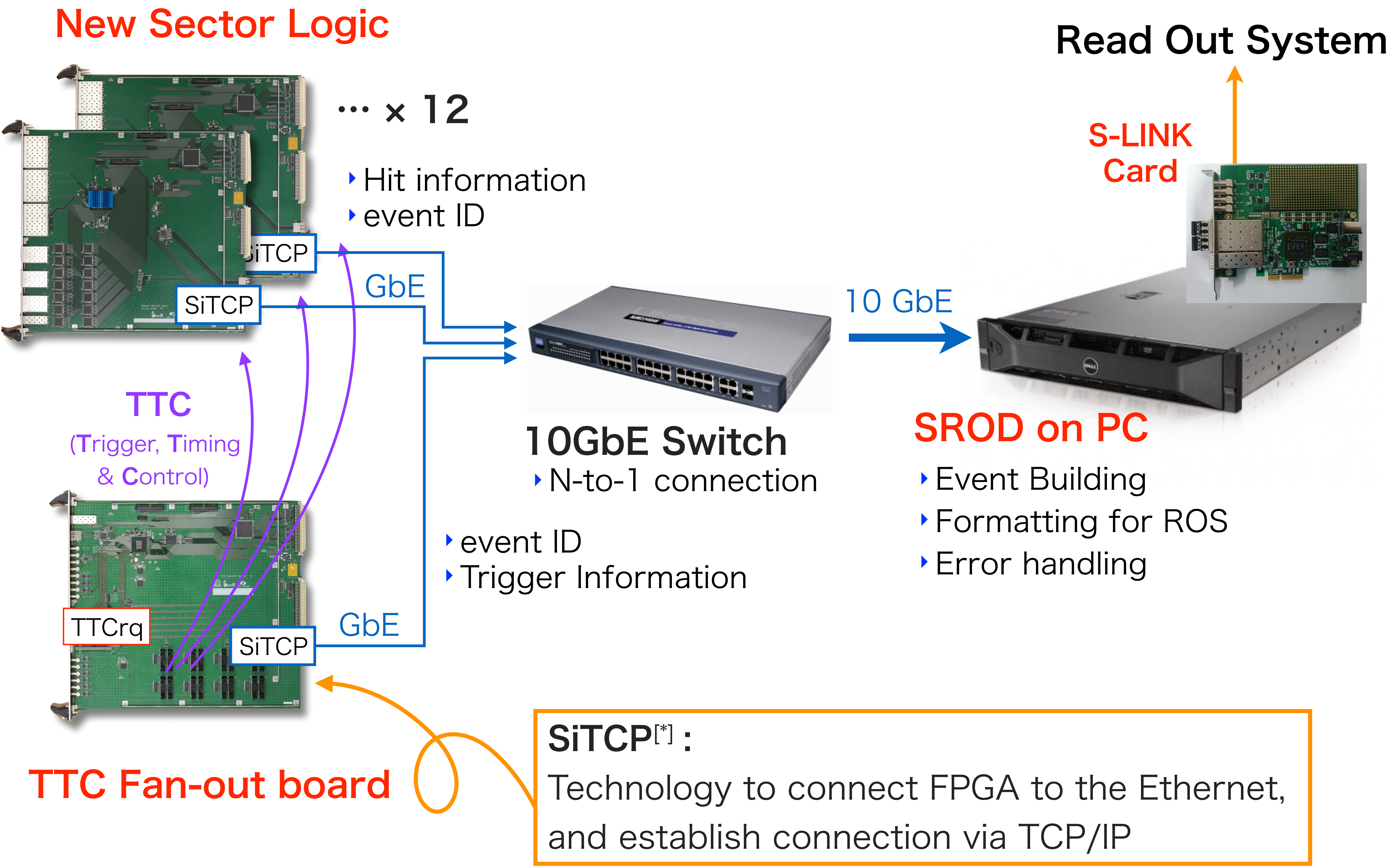
New Sector Logic Board design



New Sector Logic Board design

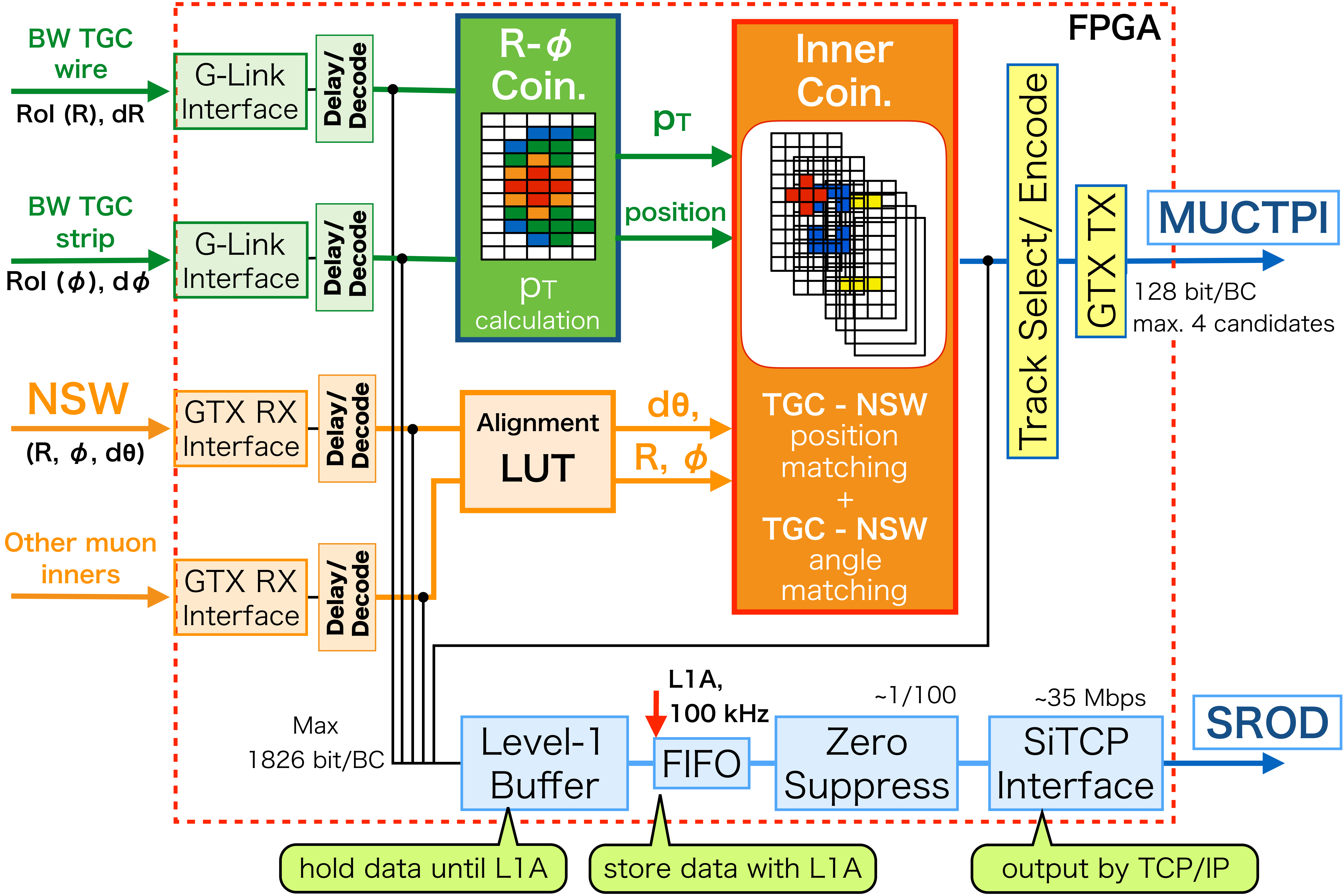


Run 3 Readout system



[*] Tomohisa Uchida, "Hardware-Based TCP Processor for Gigabit Ethernet", IEEE Trans. Nucl. Sci. Vol.55, No.3, June 2008, [LINK]

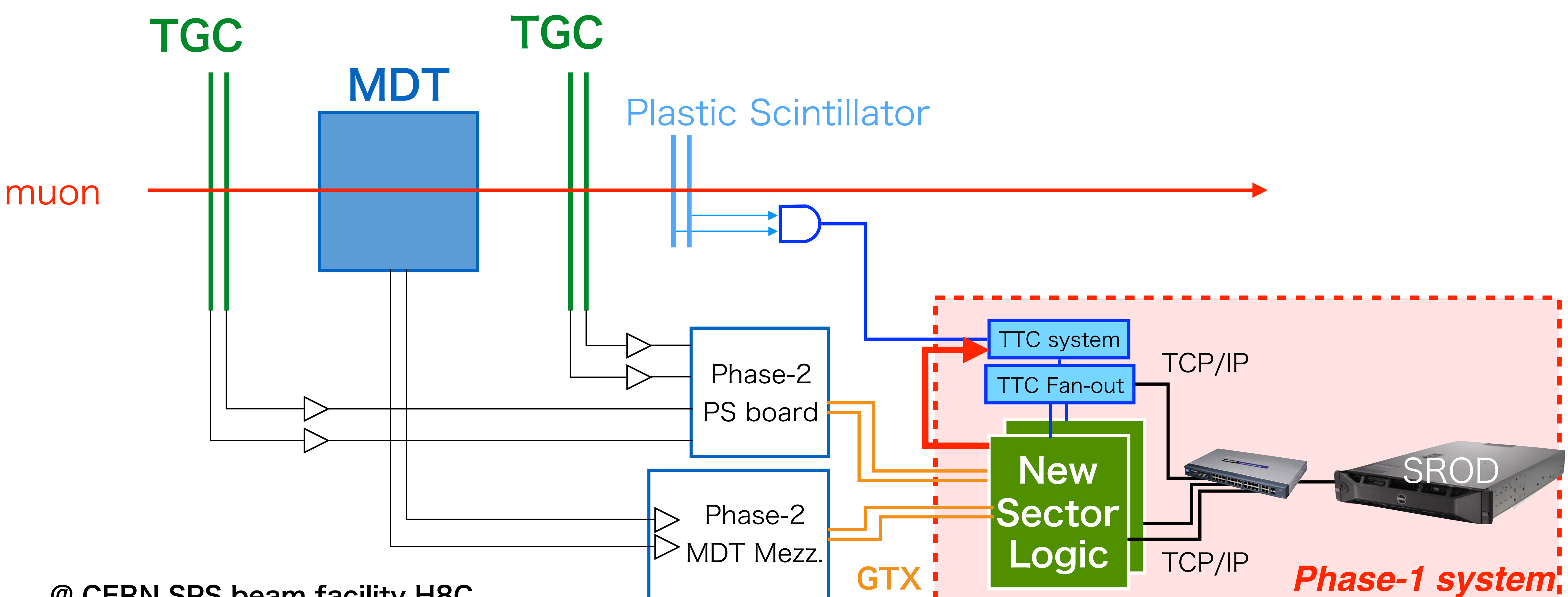
Firmware Design



Test Beam @SPS

- Aim of the test:
  - To test the phase-1 readout system and firmware
  - To confirm that TGC self-trigger using data received via GTX can be implemented on the New Sector Logic firmware.

- Test Beam Setup:



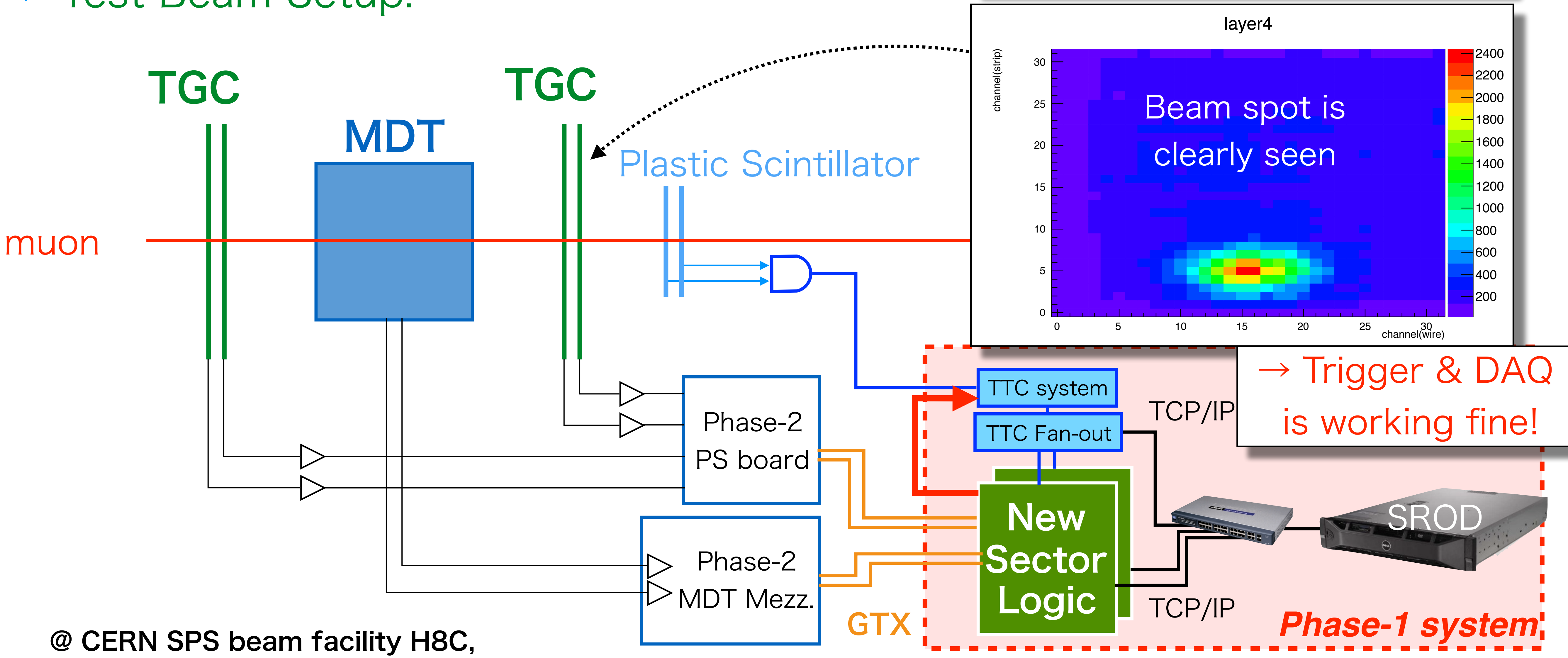
@ CERN SPS beam facility H8C,
19 Oct. ~ 14 Nov., 2016

Test Beam @SPS

- Aim of the test:
  - To test the phase-1 readout system and firmware
  - To confirm that TGC self-trigger using data received via GTX can be implemented on the New Sector Logic firmware.
- Result:

Data taken by TGC self-trigger

- Test Beam Setup:



→ Trigger & DAQ is working fine!

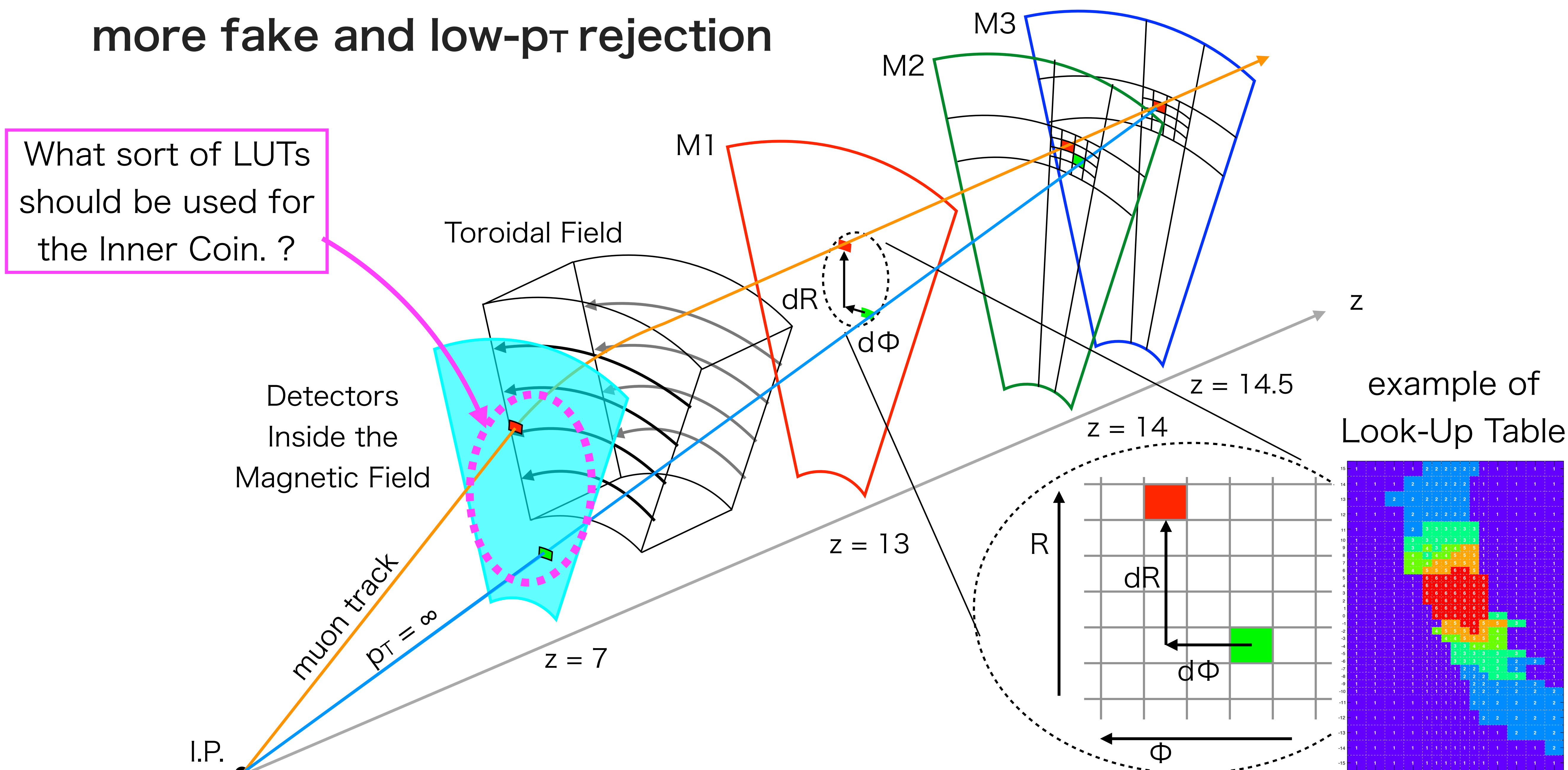
@ CERN SPS beam facility H8C,
19 Oct. ~ 14 Nov., 2016

Trigger Logic and Performance

BW dR-dϕ Coincidence

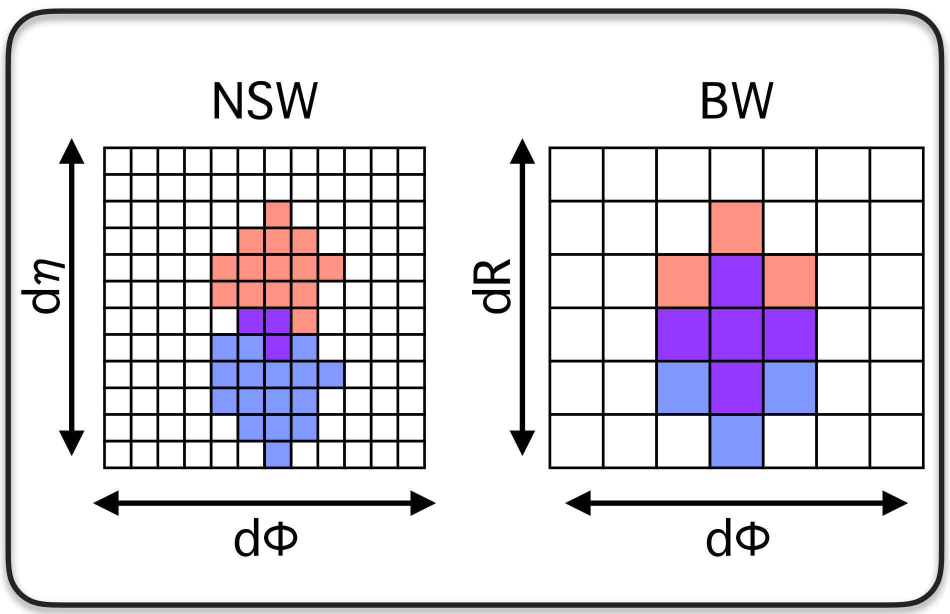
- Main idea of the trigger logic:
  - dR, dϕ defined as the hit position difference between M1and M3
  - dR, dϕ is combined, trigger decision is made using Look-Up Tables
  - Take coincidence with detectors inside to reject fake/low-p_T muons

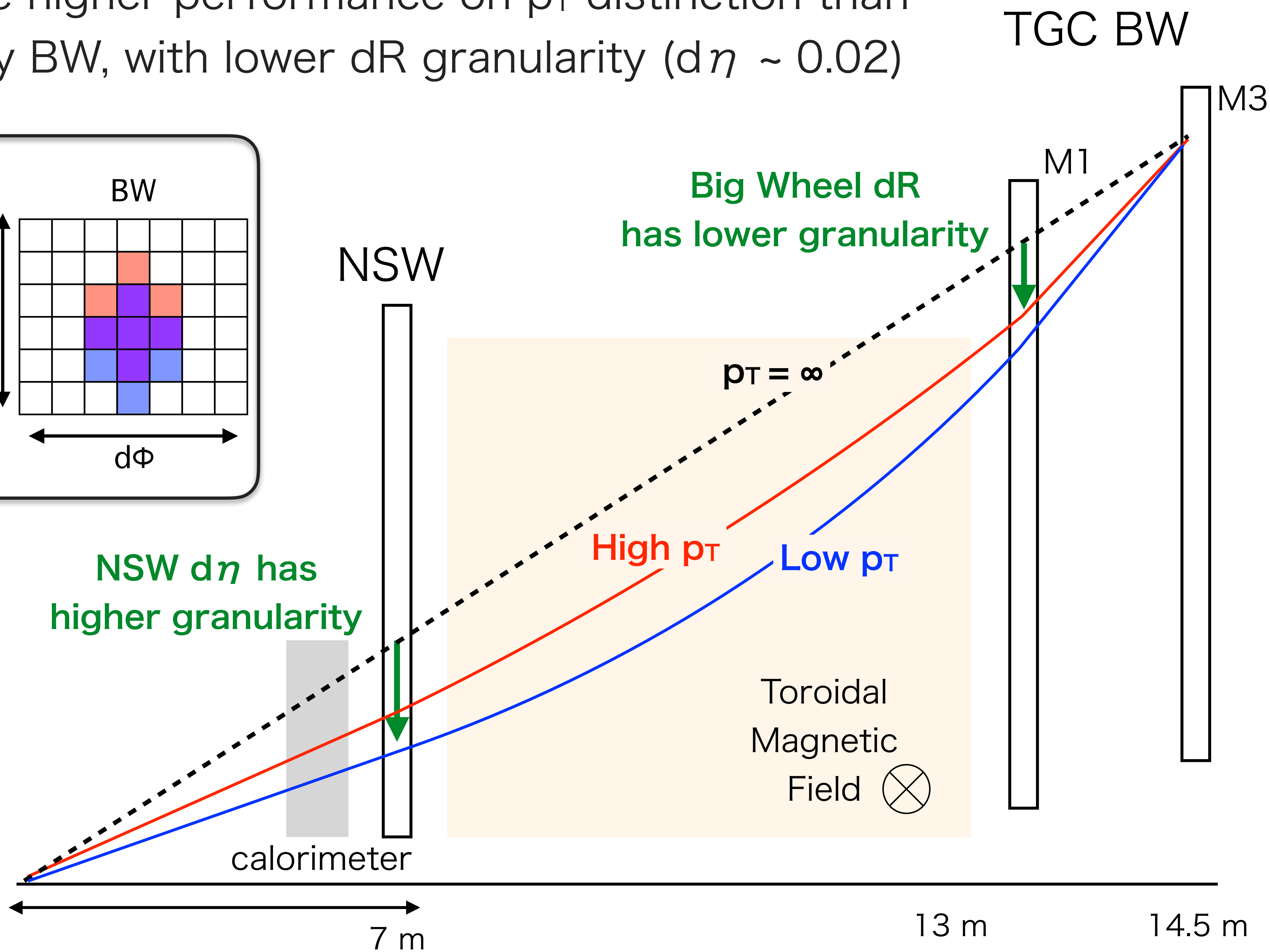
    → **New LUT for the Inner Coincidence gives more fake and low-p_T rejection**



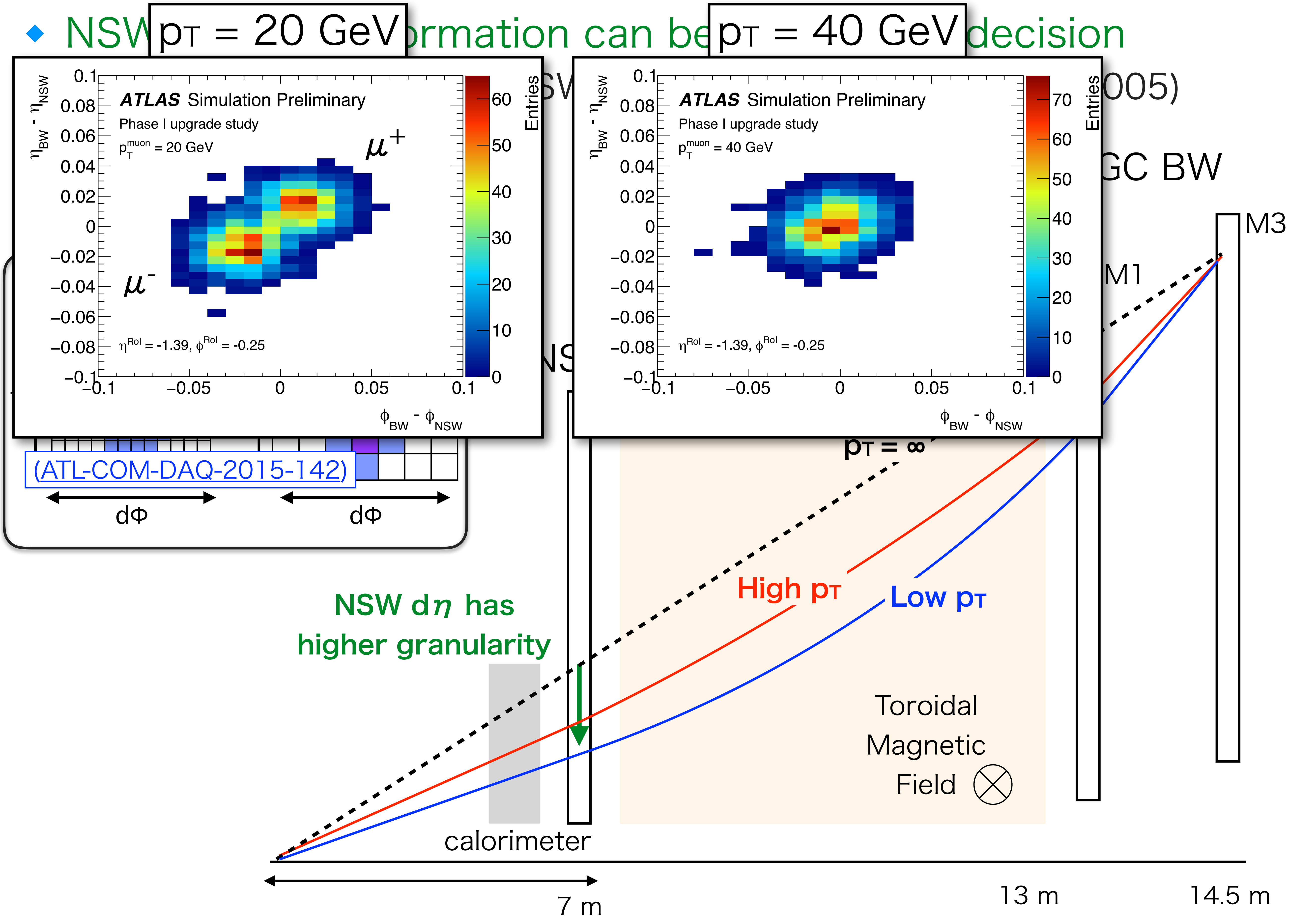
Position matching: BW - NSW

- NSW position information can be used for p_T decision
  - Using information from NSW with high granularity ($d\eta$ ~ 0.005) will realize higher performance on p_T distinction than using only BW, with lower dR granularity ($d\eta$ ~ 0.02)



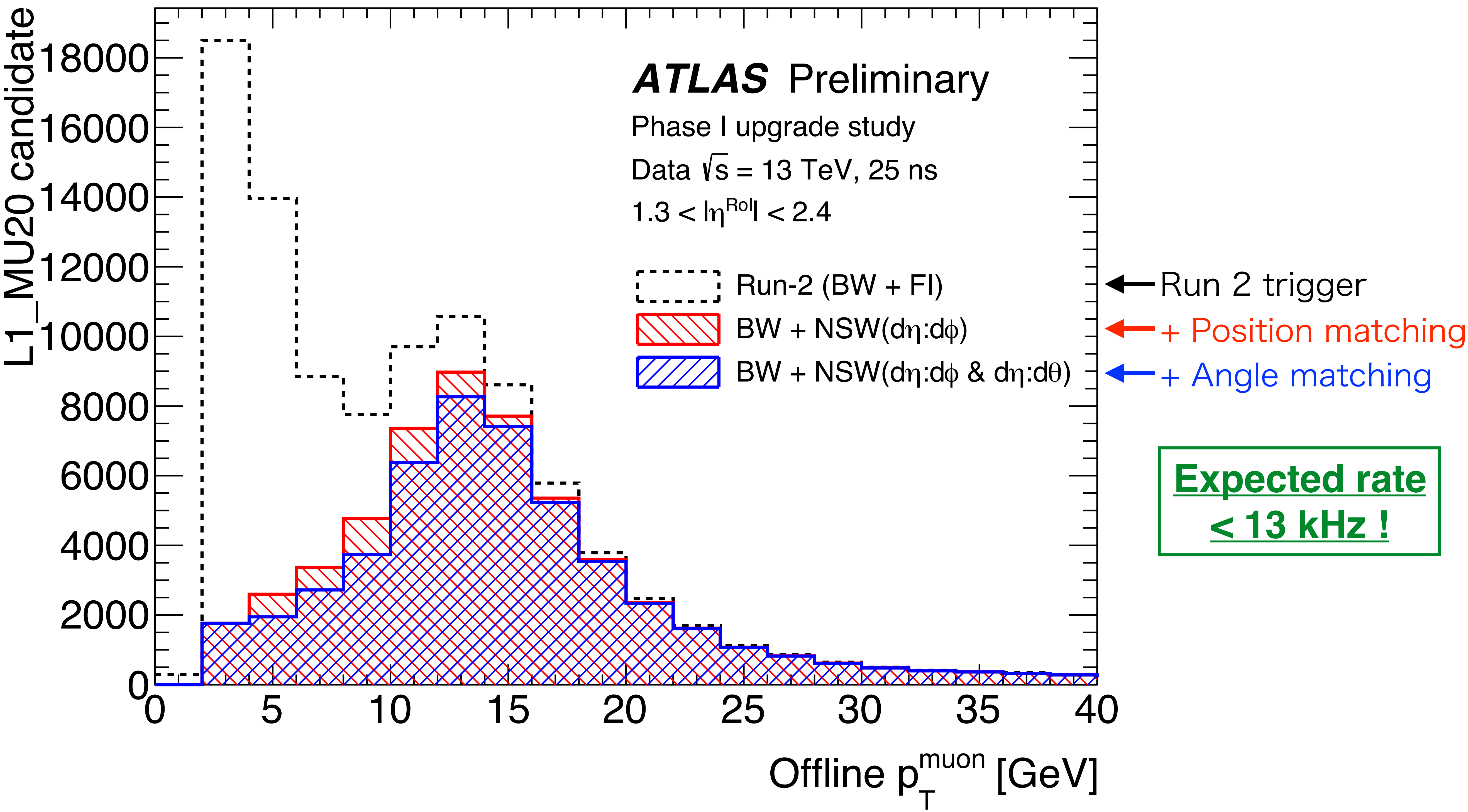


Position matching: BW - NSW



Rate Estimation

- p_T distribution of the muons that passed $p_T > 20$ GeV trigger
  - Low p_T muons are eliminated effectively, while keeping high p_T muons
  - Note: Fake triggers are rejected even more



Expected rate < 13 kHz !

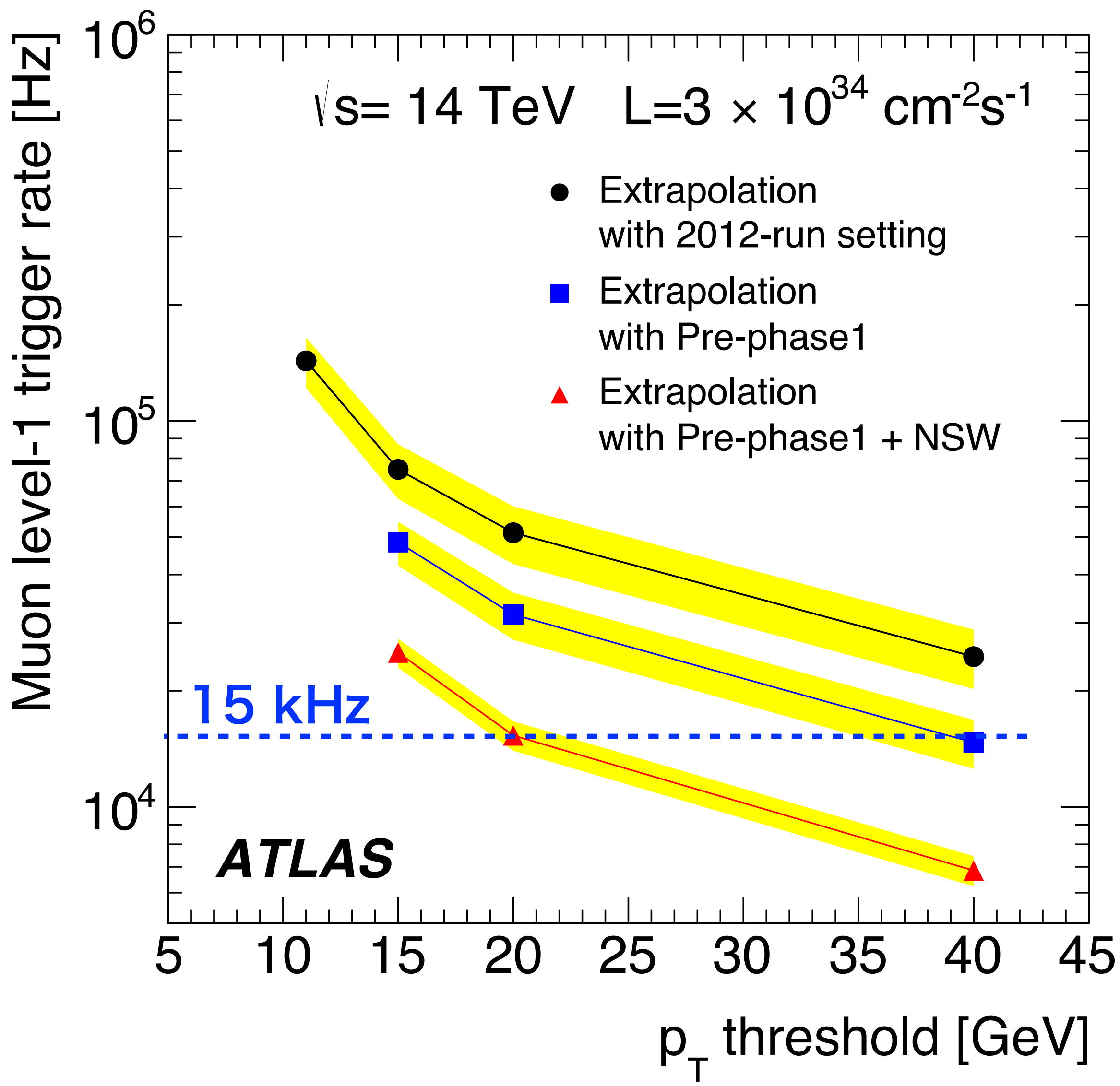
Summary

- Upgrade of the muon trigger system is required for Run 3:
  - Take coincidence with NSW to reject fake and low p_T muons.
  - New hardware is needed to combine data from current trigger chamber BW, NSW, and several other detectors.
- Hardware and Firmware development status
  - New trigger processor board, New Sector Logic, has been produced.
  - Other modules to read out the trigger data are also being developed.
  - Firmware design has been completed including the readout path.
  - Test beam has successfully been done using the new readout system.
- Trigger Logic and Performance
  - Taking position matching and angle matching between BW and NSW can reject low p_T muon candidates effectively.
  - The estimated rate < 13 kHz @ $L = 3\times10^{34}\ cm^{-2}s^{-1}$, which meets the phase-1 requirement of 15 kHz. (ATLAS-TDR-023)

backup slides

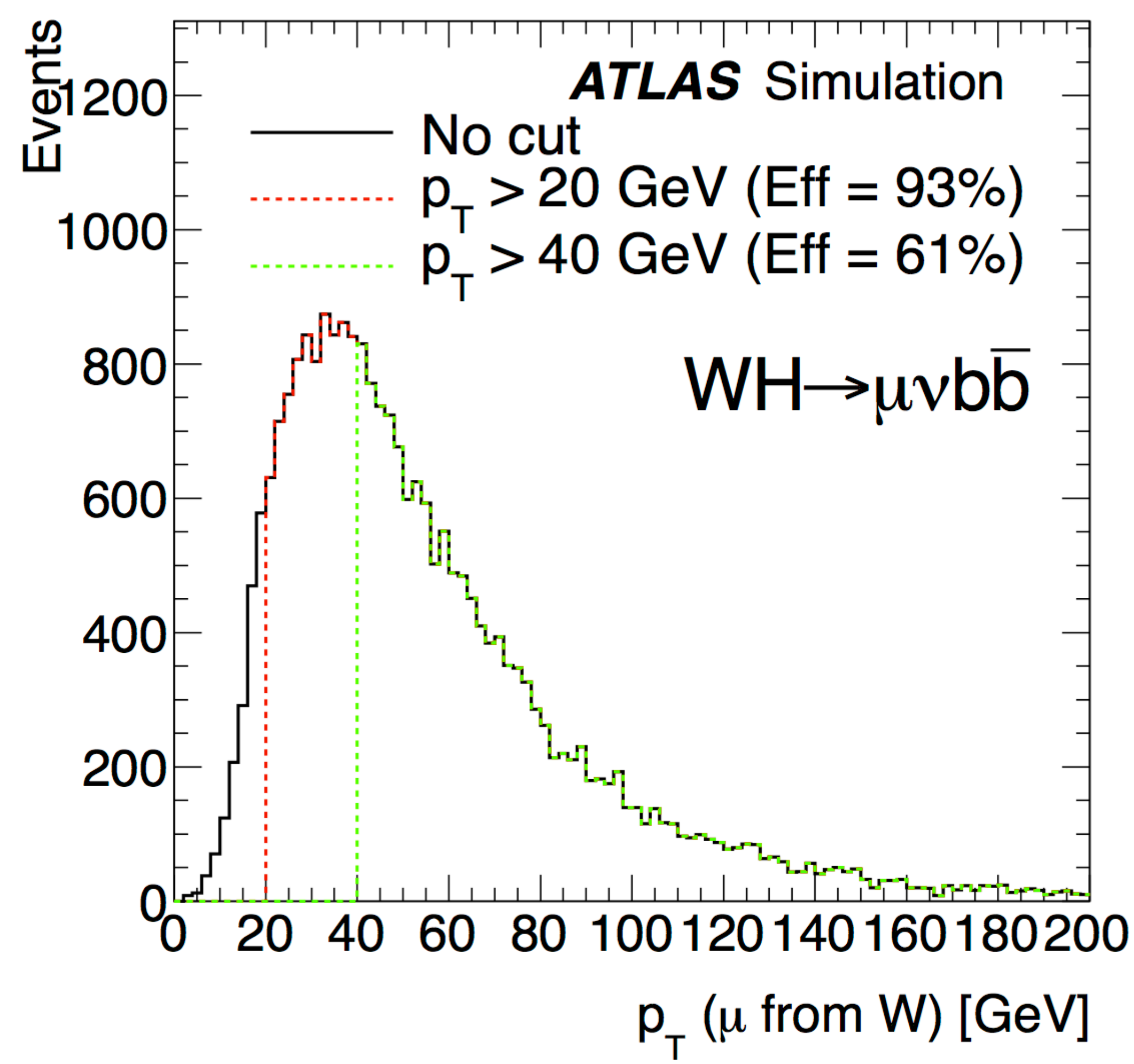
Physics Motivation

- Run 3 trigger rate estimation



- Without the phase-1 upgrade, to keep the trigger rate to the require level, the p_T threshold will need to be raised to ~40 GeV.

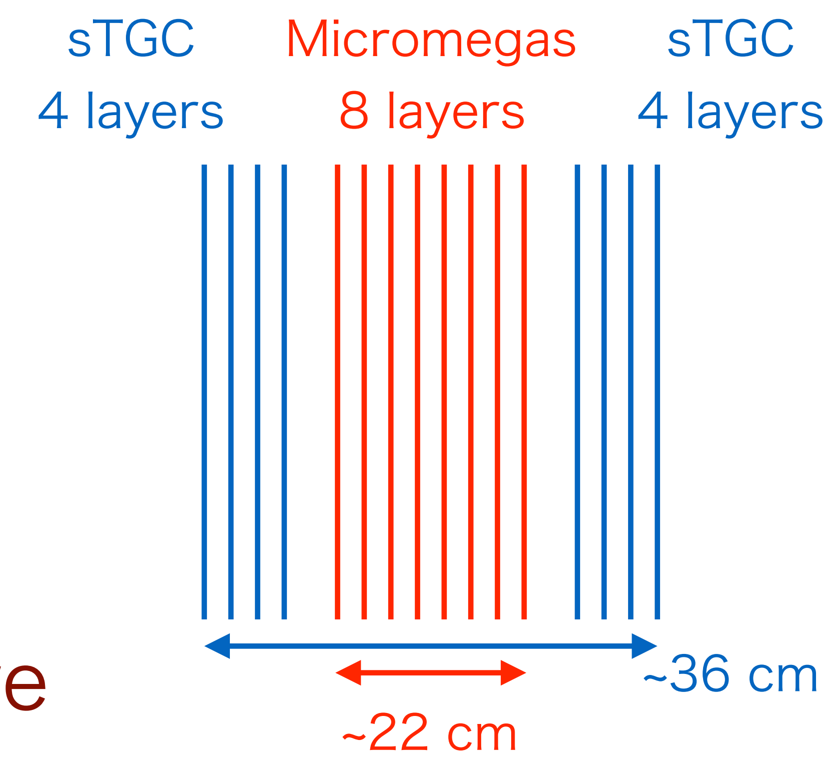
- Physics Acceptance



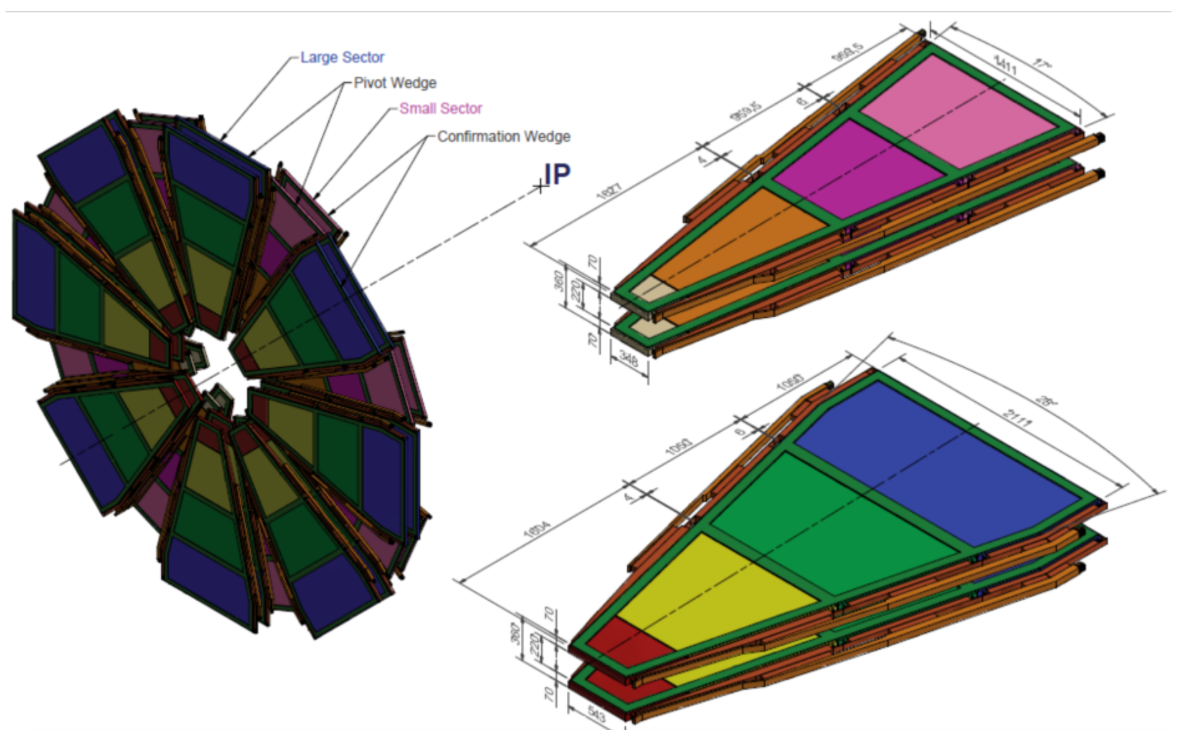
- If the threshold is raised to 40 GeV, the efficiency for muons from the decays of W boson produced in association with Higgs will be 61%.

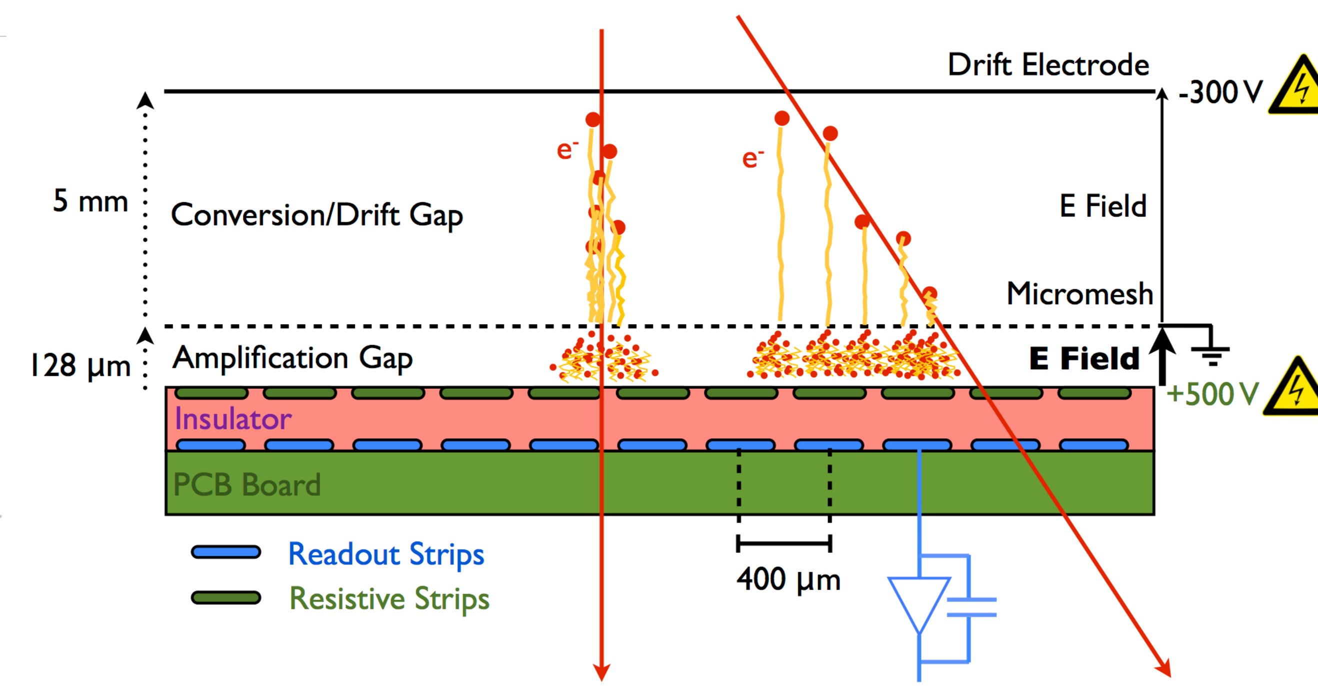
New Small Wheel

- Consists of sTGC and Micromegas
  - sTGC: small strip TGC
    - TGC chamber with strip width of 3.2mm, smaller than the strip width of current TGC (> 15 mm)
    - 4 wire-strip pairs are combined to make 1 module.
    - position resolution 60~150 μm
  - Micromegas: micro mesh gaseus structure
    - position resolution ~90 μm
    - 8 layers are sandwiched by sTGC 4-layer modules, to compose the New Small Wheel



Resolution: position ~30 μm
angle ~0.3 mrad.

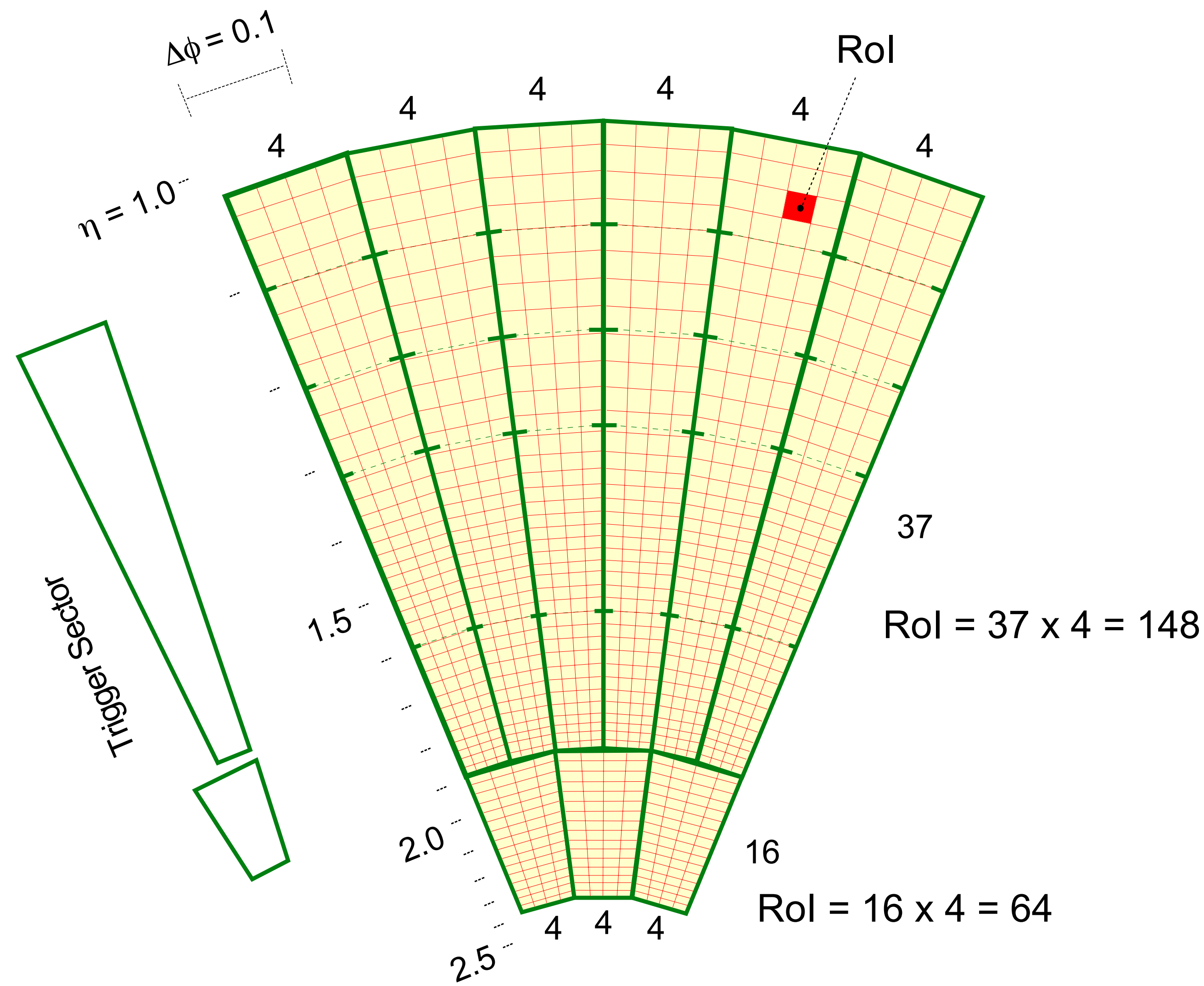




NSW Technical Design Report, [ATLAS-TDR-020]

Region of Interest

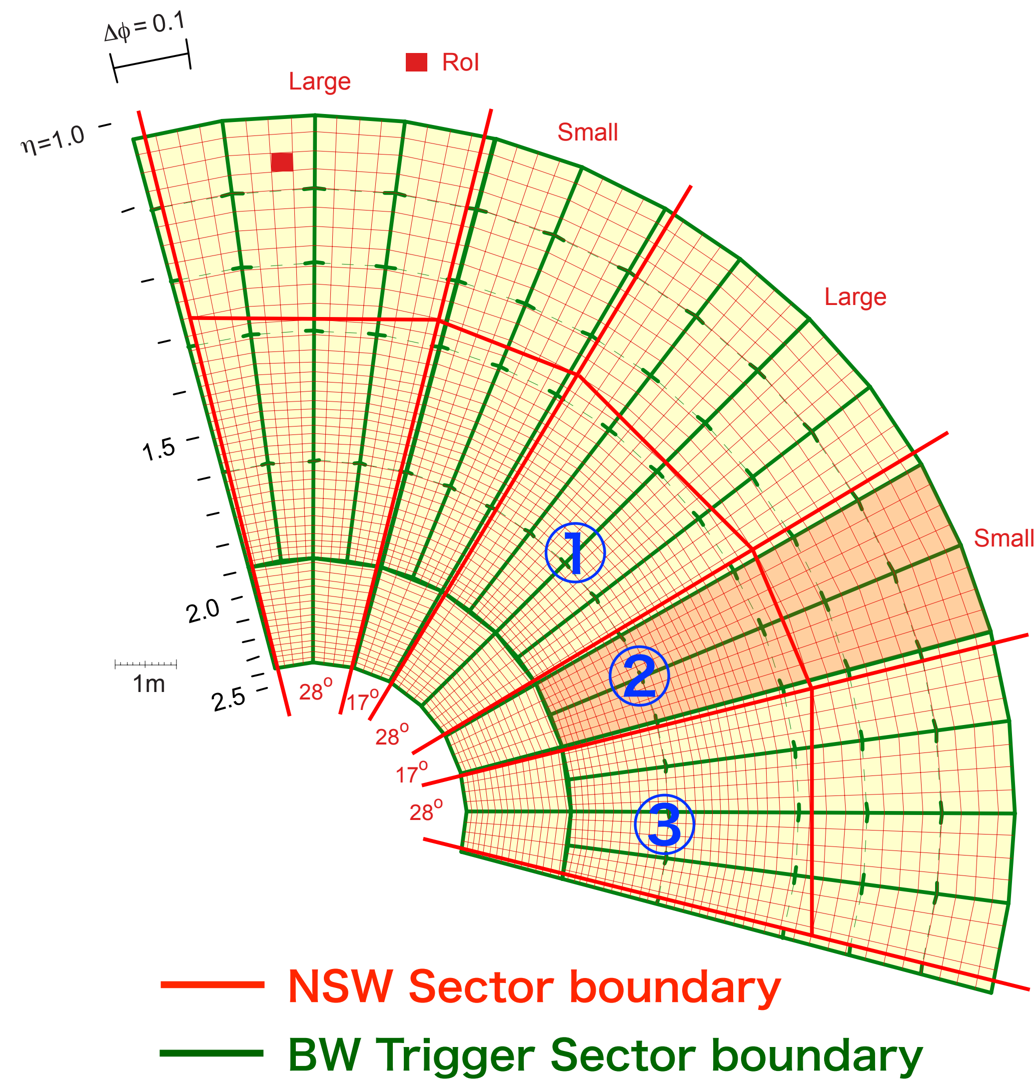
- The smallest unit for the Level-1 Muon Trigger:
  - Each side is divided into 72 parts, shown as green line in this figure → 72 'Sectors' per side
  - Each Sector is divided into 148 (or 64) 'Regions of Interest' (RoI).
  - One New Sector Logic board handles 2 Sectors, i.e. 296 RoIs (or 128 RoIs)
  - Trigger decision is performed RoI by RoI → 296 trigger decision logic should run in parallel inside one FPGA → 296 individual LUTs should be implemented



Data format from the NSW

- One NewSL board receives data from max. 3 NSW sectors.
- Each NSW Sector sends track information of max. 8 tracks using 2 optical fibers.

Words	first byte	second byte
Word-0	comma	comma
Word-1	track-0	
Word-2		
Word-3	track-1	
Word-4	track-2	
Word-5		
Word-6	track-3	
Word-7	ID (4-bit)	BCID (12-bit)



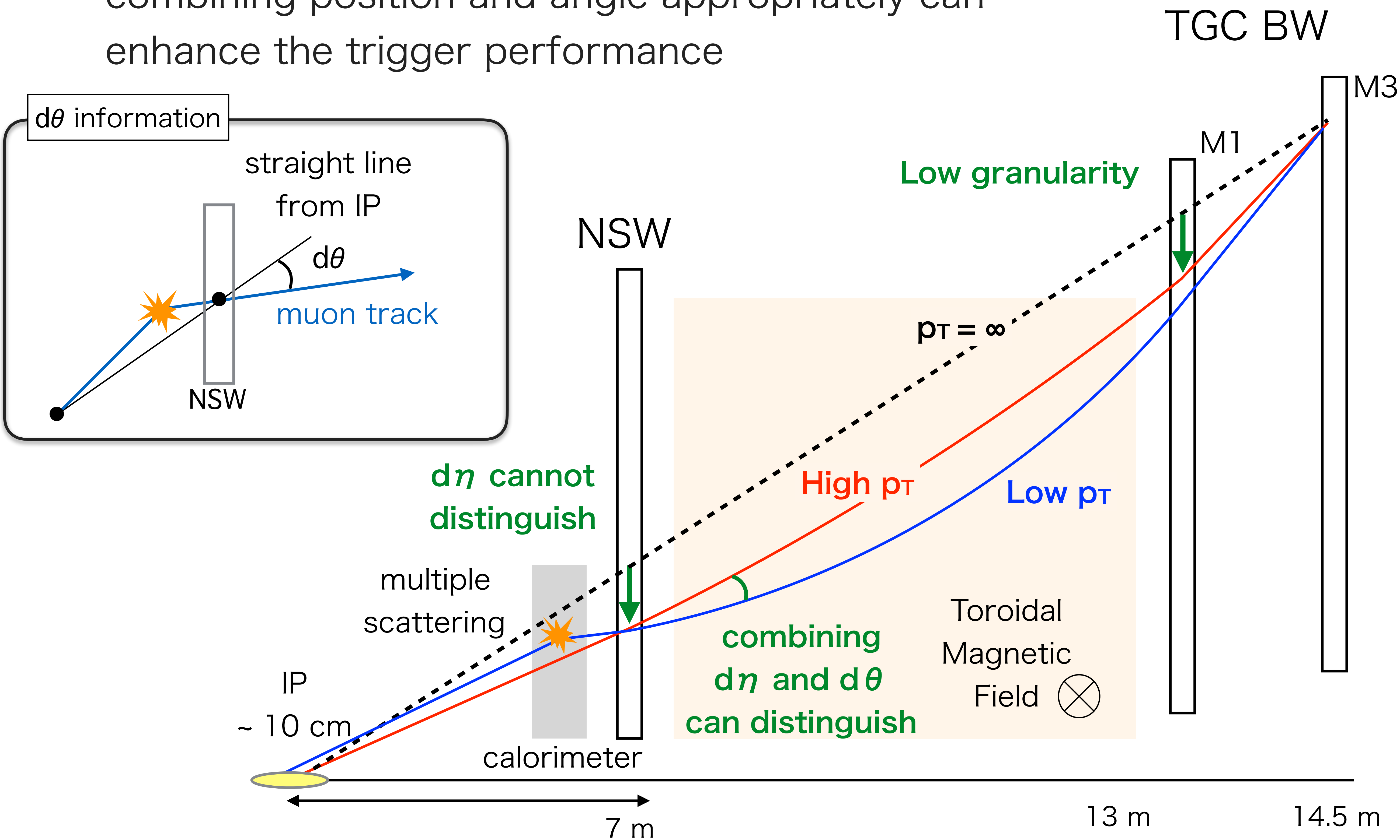
- Data format for each track:

Field:	sTGC type	MM type	Δθ (mrad)	Φ index	R index	Spare
Num of bits:	2	2	5	6	8	1

= **24 bits**

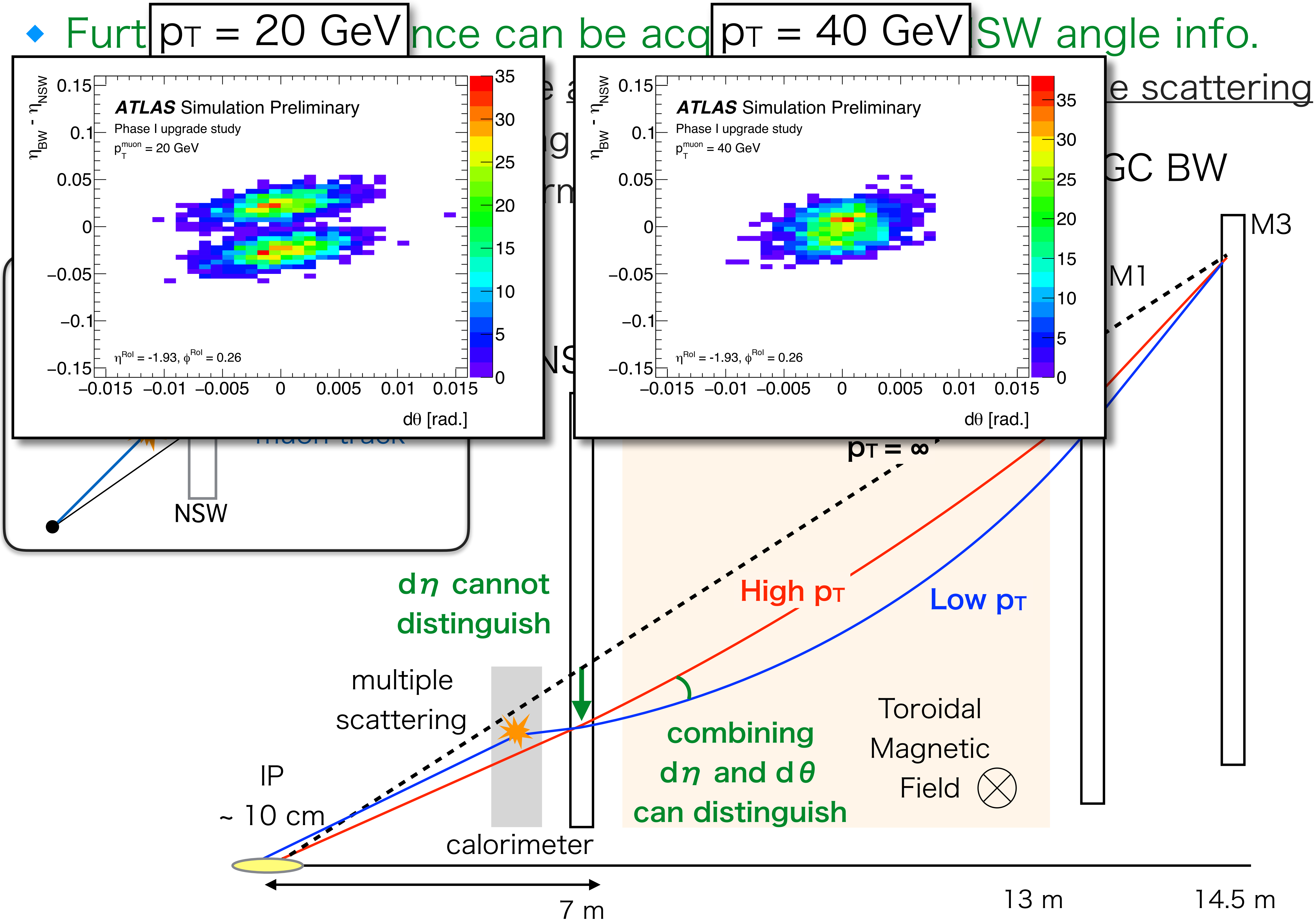
Angle matching algorithm

- Further performance can be acquired using NSW angle info.
  - d θ has information on the actual I.P. + the effect of multiple scattering
  - combining position and angle appropriately can enhance the trigger performance



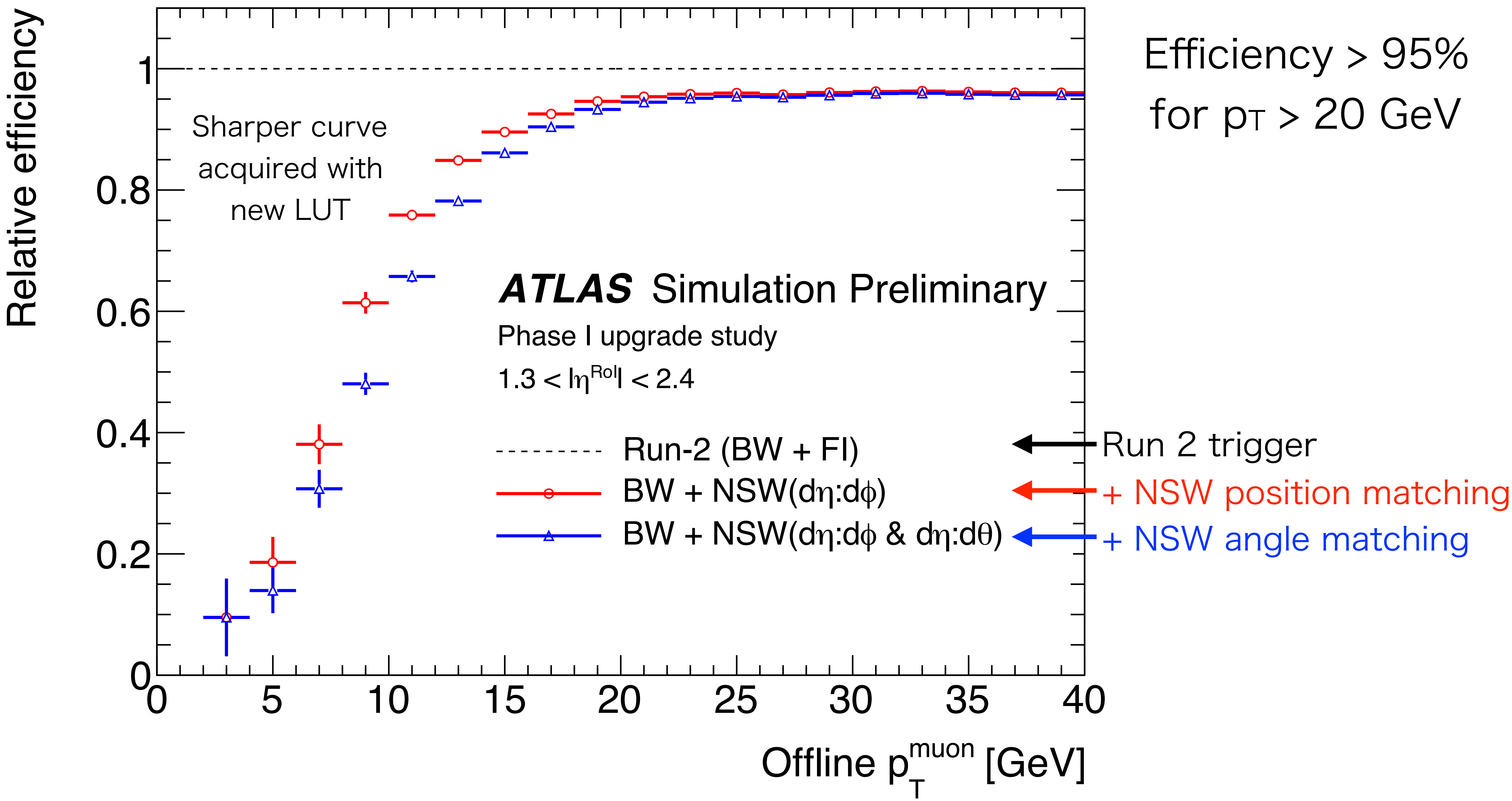
Angle matching algorithm

◆ Furt … nce can be acq … SW angle info.



Trigger Performance

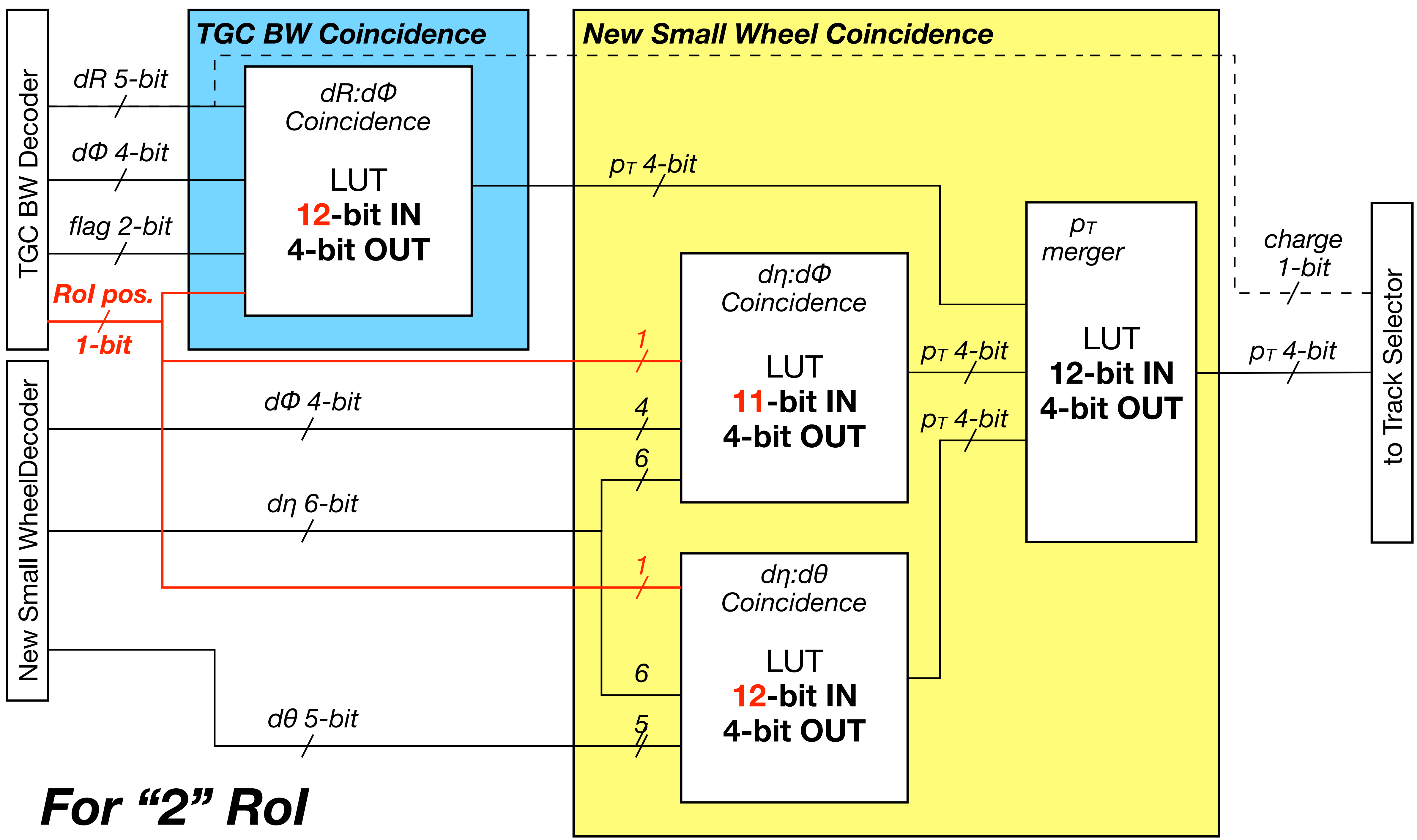
- New Inner LUTs uses NSW position & angle information
- Efficiency is calculated by simulation, for L1_MU20
  (L1_MU20: Level-1 trigger for muon with p_T > 20 GeV)
- The track finding efficiency is assumed to be 97%



Efficiency > 95% for p_T > 20 GeV

Implementation of LUTs

- 3 LUTs, BW (dR-dϕ), NSW (dη:dϕ), and NSW (dη:dθ) are implemented separately, and their results are merged afterwards at the last LUT, p_T merger LUT.



For "2" RoI

S-LINK Card

- Developed a PCI-express card supporting S-LINK
  - Needed for the SROD to send data via S-LINK
  - Final board came in the end of Feb. 2017

- Key Function:
  - FPGA: Xilinx Kintex-7, XC7K160T
  - SFP+: 3 SFP+ ports available, for optical transceiver
  - Open-drain output: for busy output

- Test status
  - Sent data from the S-LINK card via SFP+, to the receiver board on another PC.

    → Succeeded in data transfer.
    Rate test is going to be done.
    Started to finalize the software and the firmware.