Advanced DAQ systems for current and future colliders

ZhenAn LIU
Inst. Of High Energy Physics

International Workshop on High Energy Circular Electron Positron Collider

Beijing, Nov. 6 2017

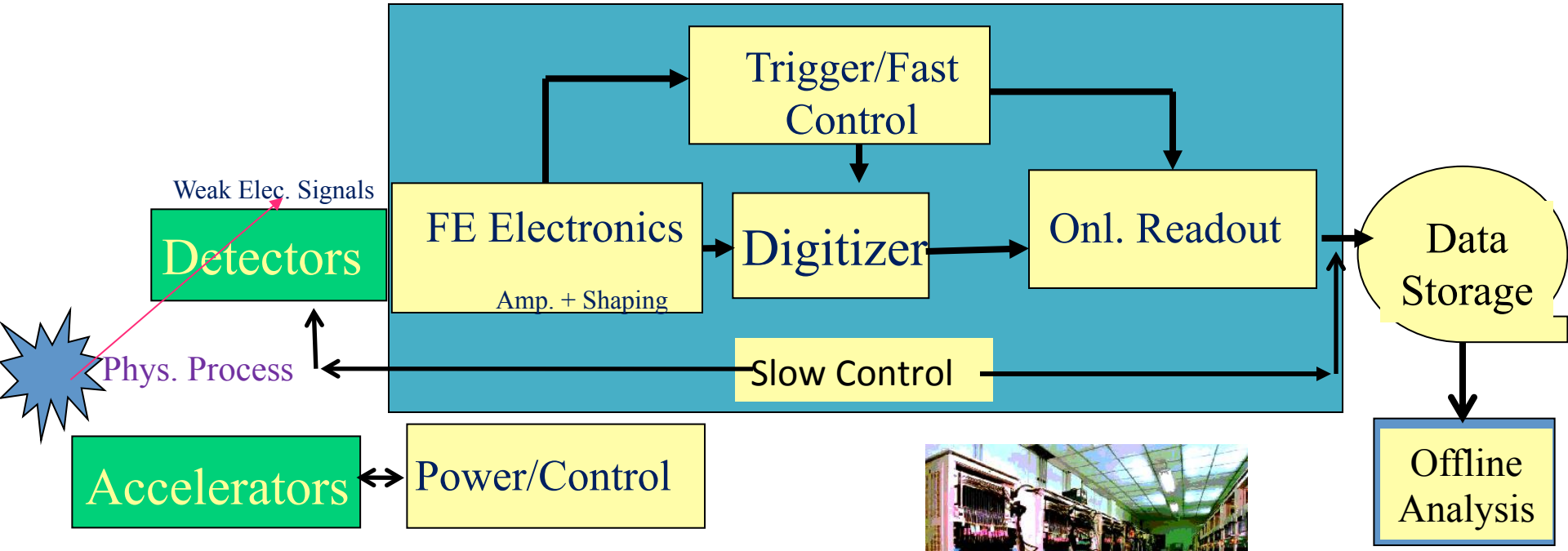
- Thanks to the workshop organizer's invitation, but indeed this topic is big So I will try to give my personal thinking based on my relevant work in recent years.

Outline

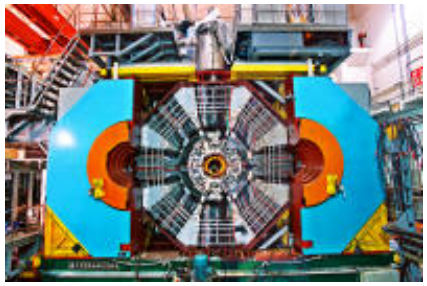
- Background on Trigger and DAQ
- Examples of present Trigger and DAQ system
- Merging of Trigger and DAQ(Hardware triggerless)
- Future trend in DAQ
- Summary

Components in a large Experiment

- Huge amount of different instruments



Accelerators



Detectors

Electronics

- **Working Mode**
  - **Old days: Latch-Process(digitize)**
  - **Nowadays: Pipelinded**
- **Clear margin Trigger/DAQ**

Multi-level trigger

Required rejection is orders of magnitude

- Algorithms to attain required rejection are too sophisticated.
- Accelerator backgrounds can also contribute to the problem
  - → e^+e^- vs pp

Level 1 is hardware based

- Crude signatures (hits, local energy deposit over threshold…)
- Operates on reduced or coarse detector data

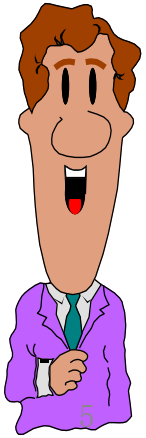
Level 2 is often a composite

- Hardware to preprocess data
  - Some Muon processors, Silicon Triggers
- Software to combine
  - Matches, Jet finders, etc.

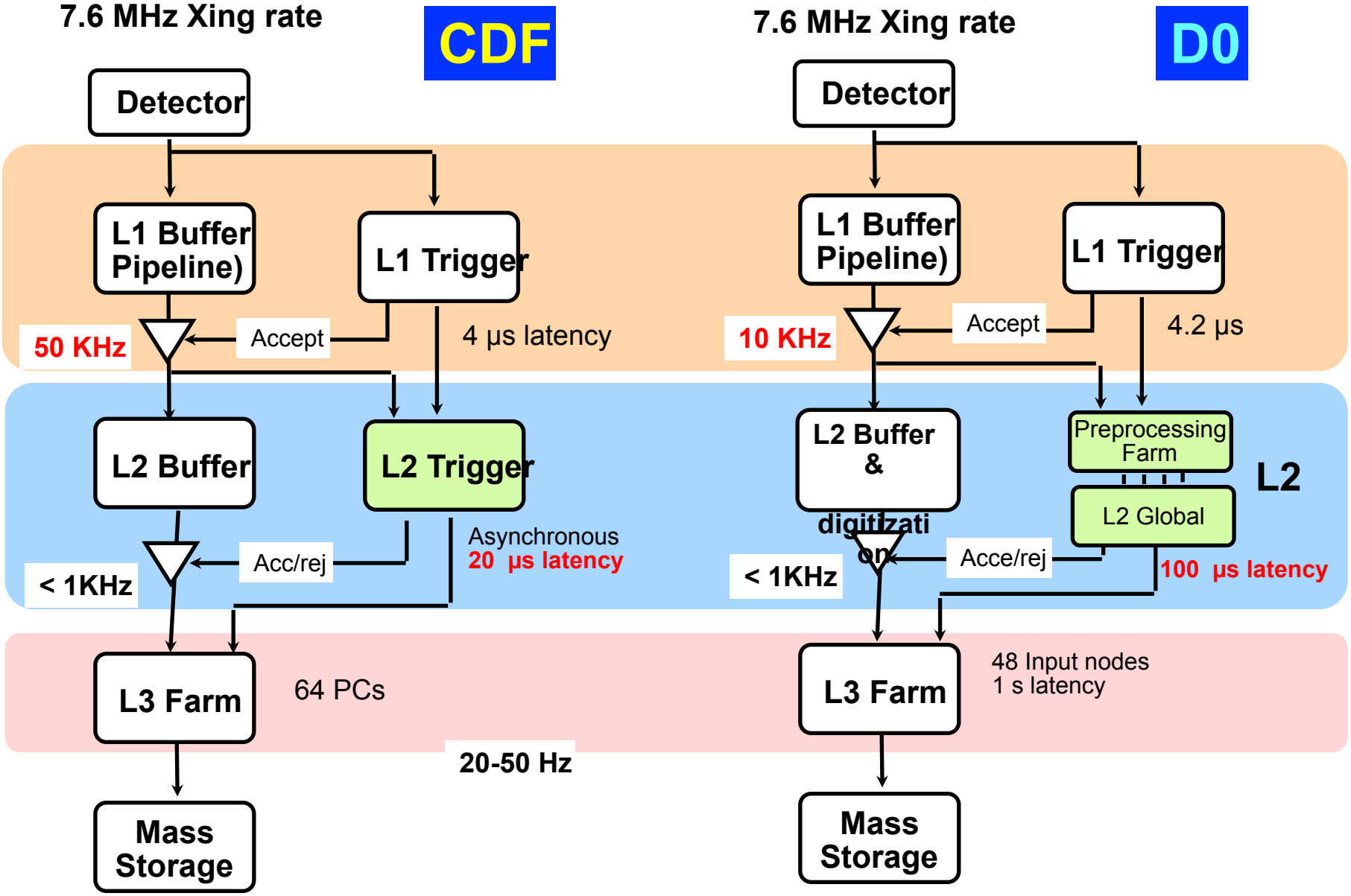
Level 3 is a farm → General Purpose CPUs

Almost every one uses this scheme

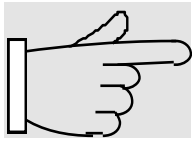
- Vary number and function of levels.



Trigger stream in FNAL Tevatron



Trigger at LHC



40 MHz

L1

100 KHz

L2

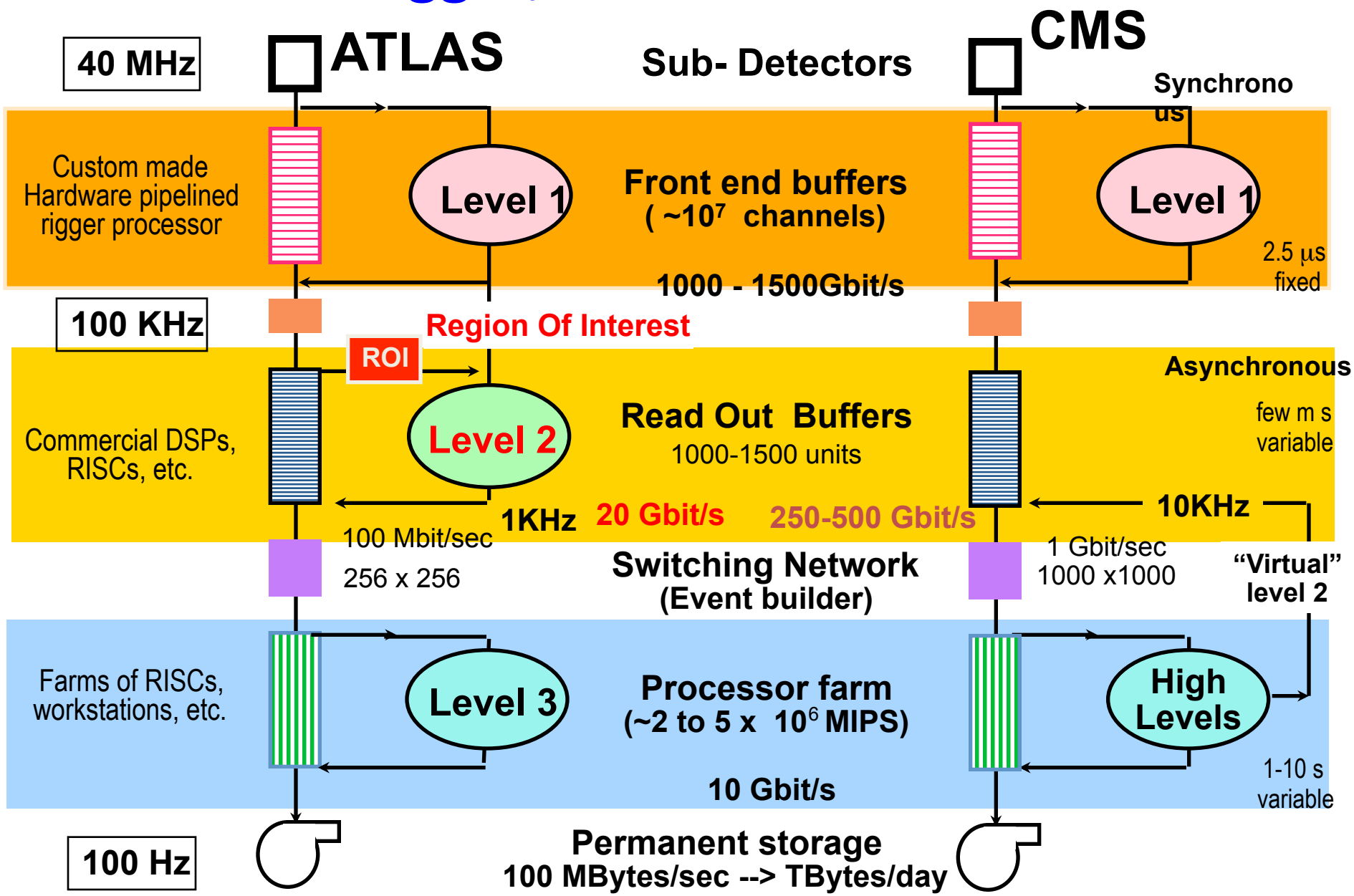
1 KHz

L3

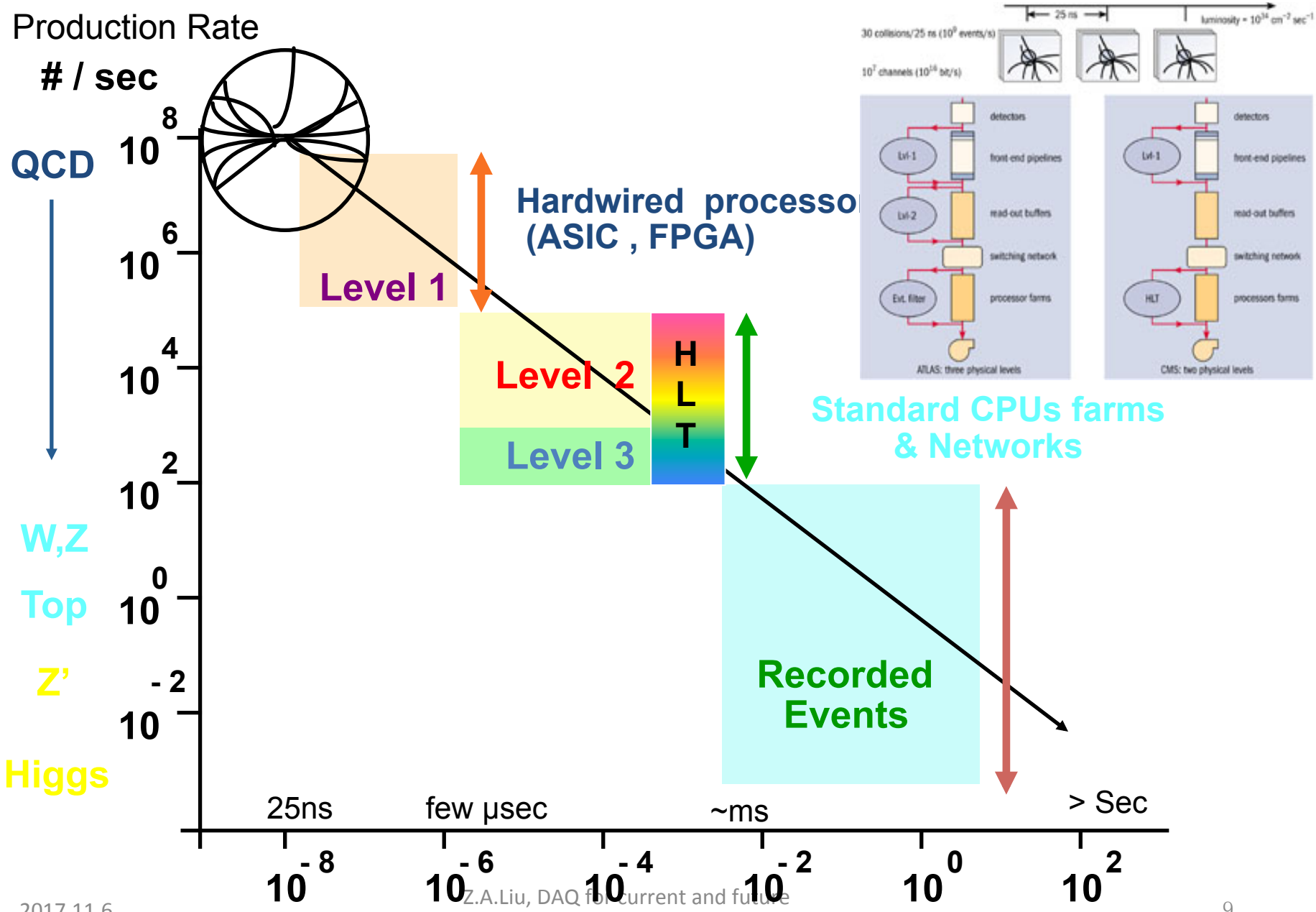
100 Hz

- "Local" identification of high Pt objects → *use coarse dedicated data*
  - Electrons /Photons , Hadrons & Jets → Energy clusters
  - Muons → Track segments
  - Neutrinos → Missing Et
- Particle signature (e/g,h,Jet, μ ...) → *use final digitized data*
  - Refine Pt cuts → fine granularity & track reconstruction
  - Combine detectors → Converted electron ,"Punchthrough", decays
- **Global topology** → multiplicity & thresholds
- Identification & classification of physics process → trigger menu
  - Partial event reconstruction → Vertices , Masses ,Missing Et....
- **Physics analysis**
  - "Off-line" type analysis of classified events

Trigger/DAQ data stream

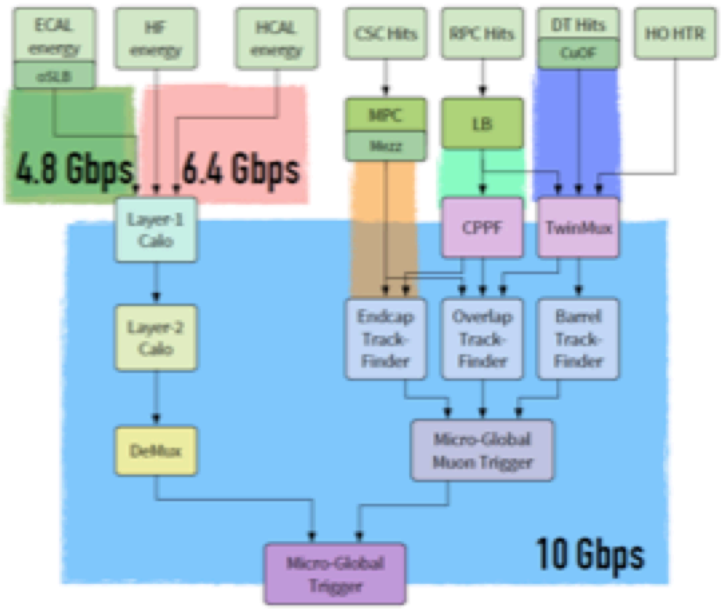


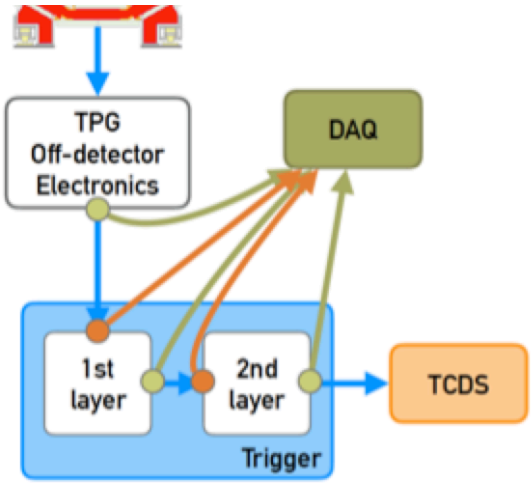
multi level scheme



Key technologies

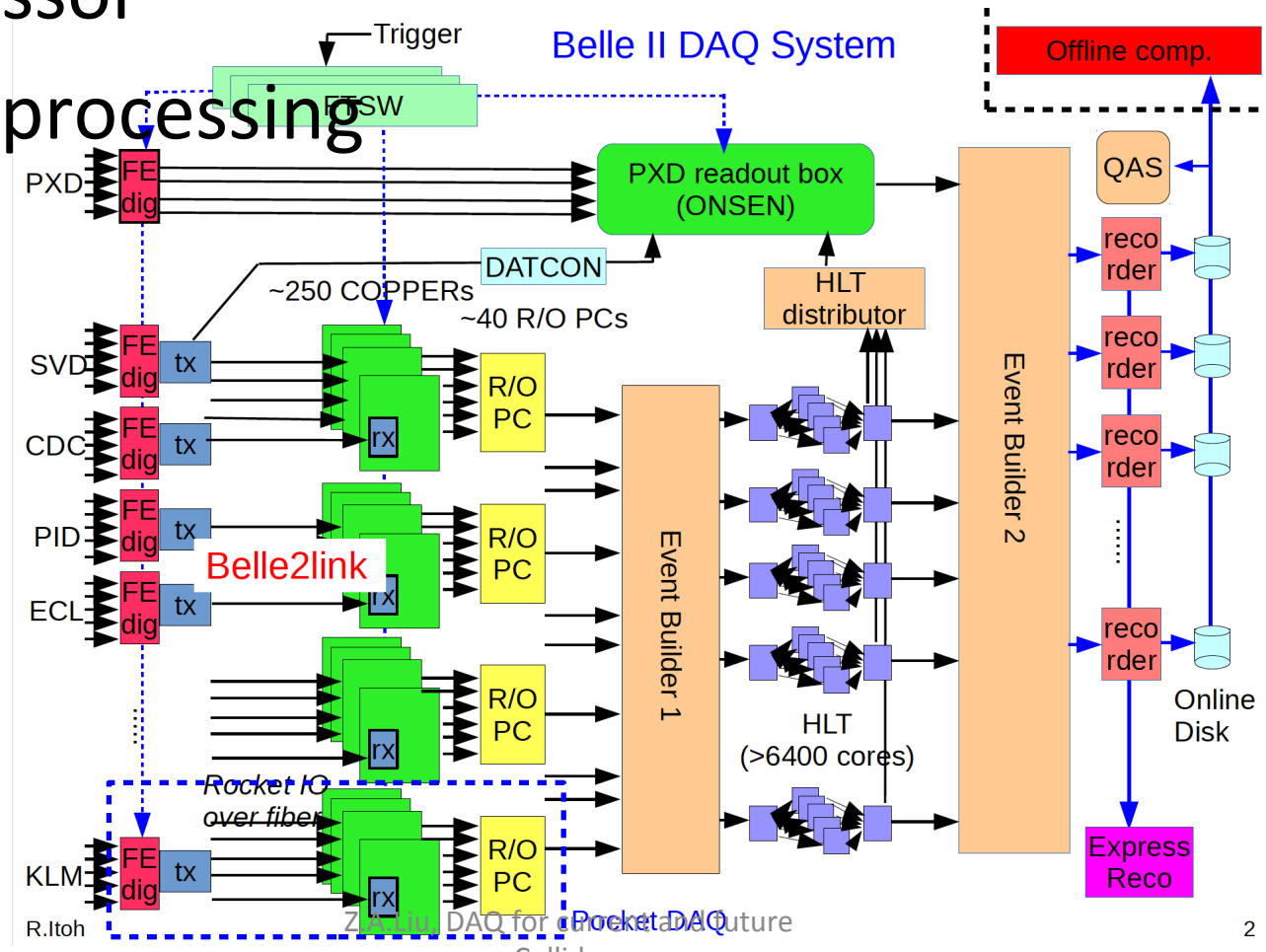
- Centralized timing and control
- Higher digitization speed and data bandwidth(1.6Gbps-6.4Gbps)
- Unified readout
- New data BUS architecture(VME to MTCA/ ATCA)
- Scalable system
- Upgradable system





Unification in Belle II

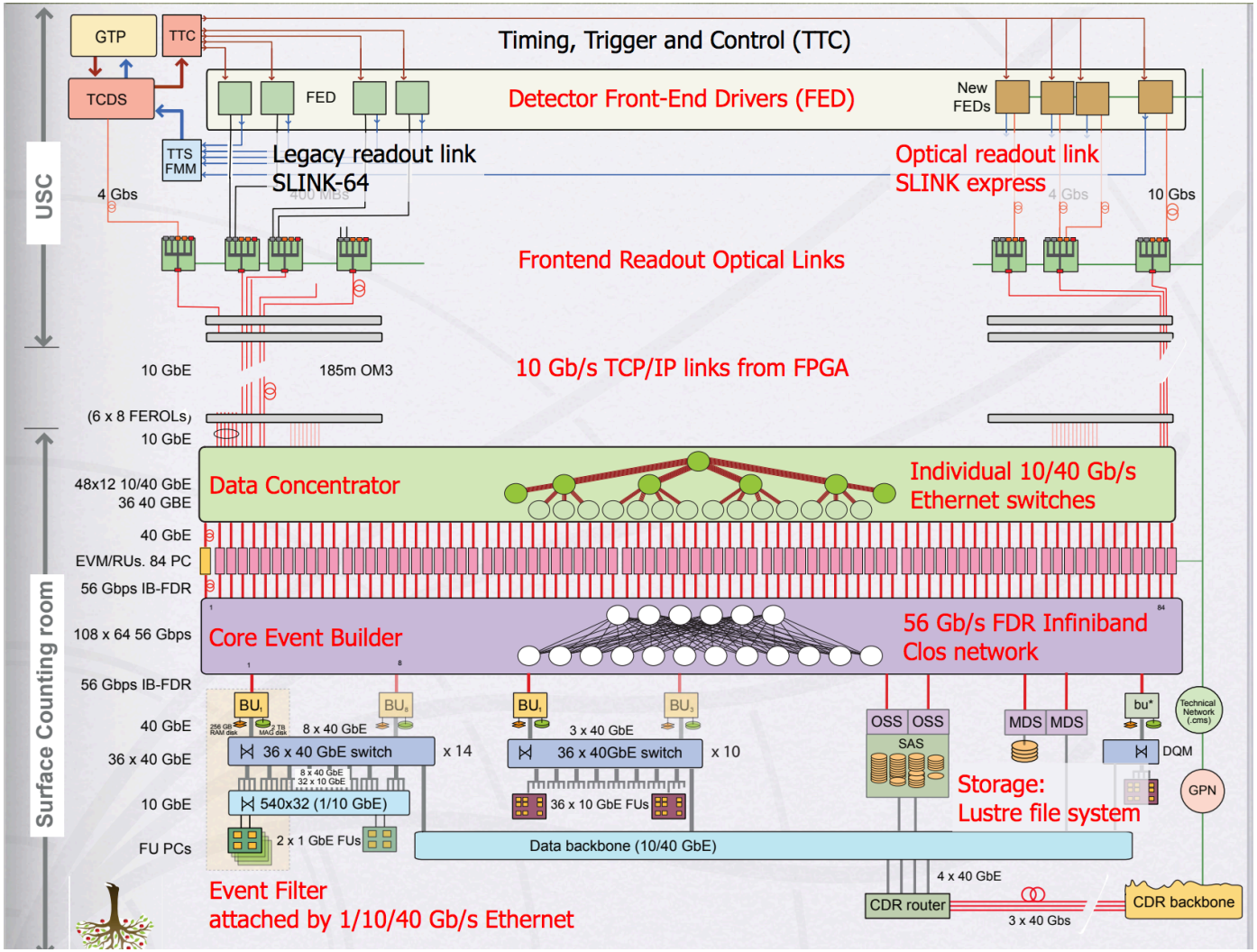
- Readout unification:Belle2link
- Processing: common processor, COPPER/new processor
- Local processing



Present CMS DAQ as example

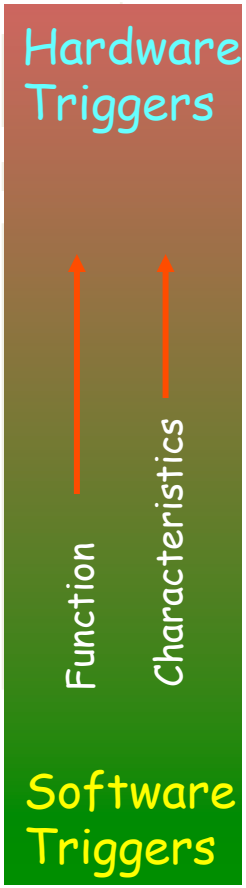
- FEE in MTCA
- 10Gbps bandwidth in data concentrator
- Networking, Ethernet
  - Not a reliable network in switched environment
  - Speed
    - 40 GbE exists on switch and NIC since ~2012
    - 100 GbE exists but still very expensive
    - 400 Gbps defined
  - High-Performance Computing (HPC) Fabric interconnect
    - Low-latency, reliable
    - Infiniband 4xFDR 56 Gbps and 4xEDR 100 Gbps available
    - New fabric interconnect forthcoming ..
      - 128 Gbps (2017-18), 200 Gbps (after 2020)
      - Integration of fabric port onto the CPU socket
  - Both technologies have switches with ~50 Tbps

CMS DAQ block diagram



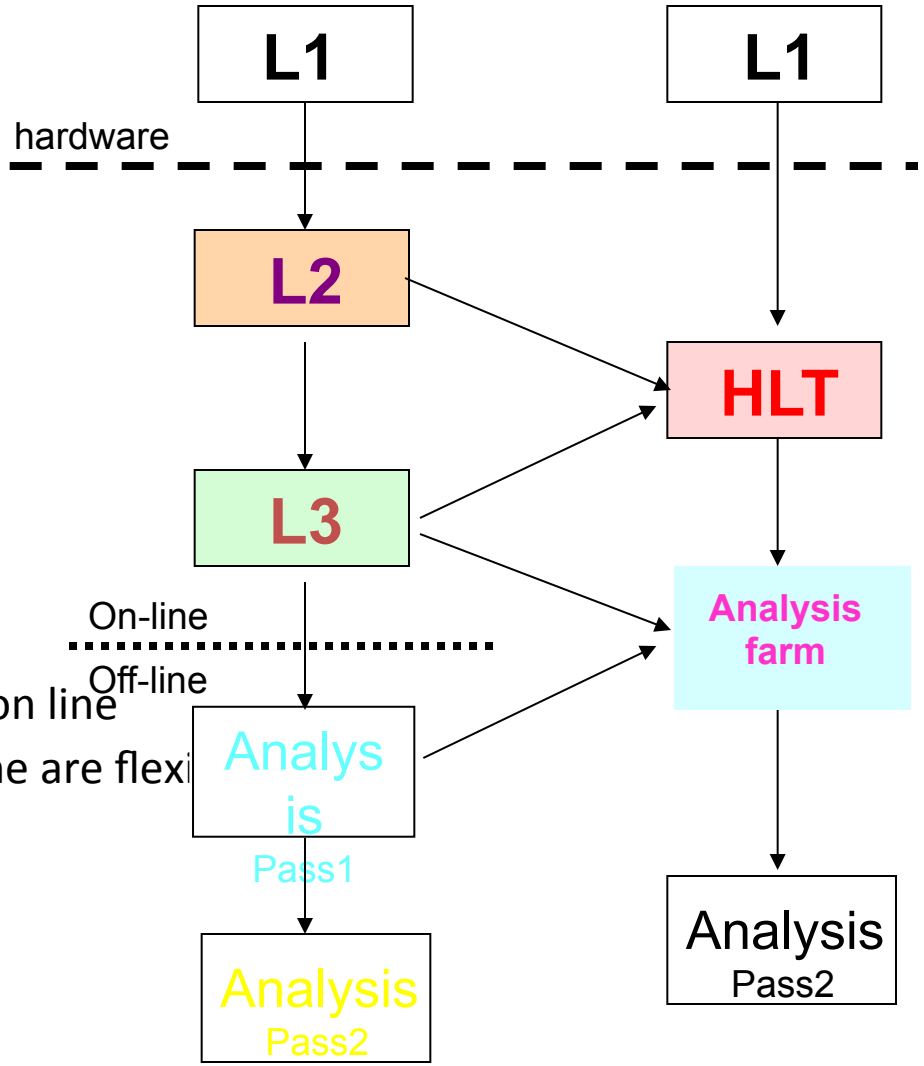
Technology evolution (Tevatron,LHC …)

- **Higher level trigger decisions are migrating to the lower levels**
  → **Software Migration is following functional migration**
  - Correlations that used to be done at Level 2 or Level 3 in are now done at Level 1.
  - More complex trigger (impact parameter!) decisions at earlier times (HLT) → Less bandwith out of detector?
- **Boundaries**
  - L2 and L3 are merging into High Levels Triggers
  - DAQ and trigger data flow are merging
  - On-line and off-line boundaries are flexible
- **Recent Developments in Electronics**
  - Line between software and hardware is blurring
  - Complex Algorithms in hardware (FPGAs)
  - Possible to have logic designs change after board layout
  - Fully commercial components for high levels.



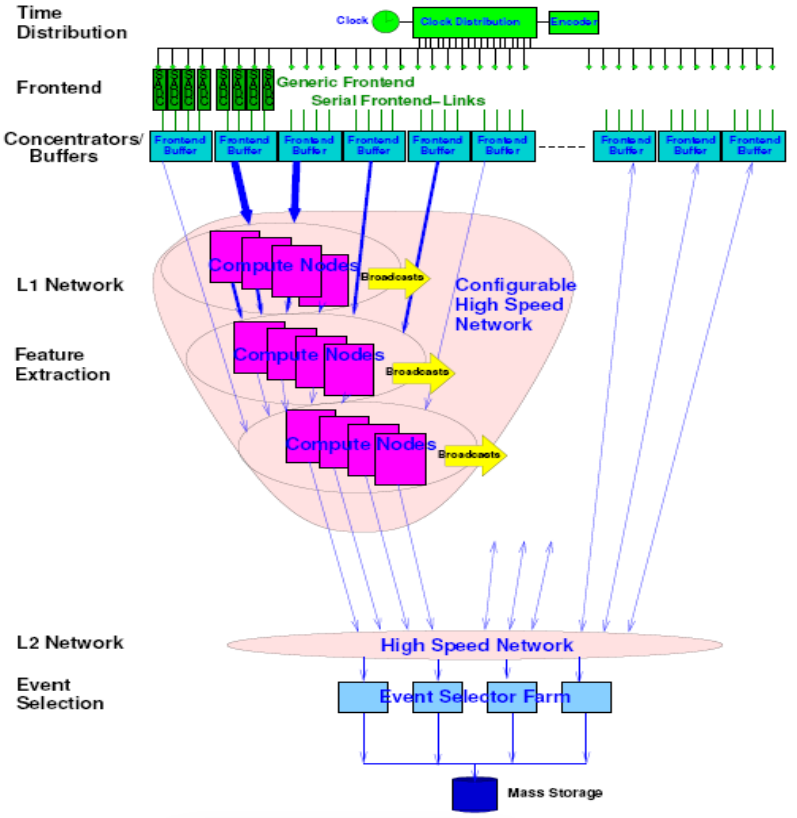
Hardware trigger less TDAQ

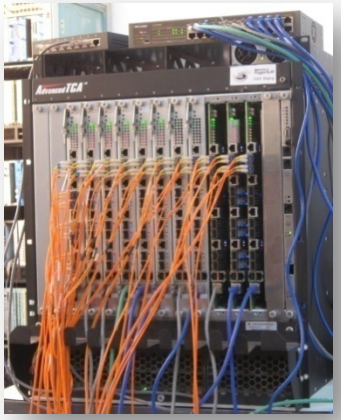
- Today
  - Tree structure and partitions
  - Processing farms at very highest levels
  - Trigger and DAQ dataflow are merging
- Near future
  - Data and control networks merged
  - Processing farm already at L2 (HLT)
  - More complex algorithms are moving on line
  - Boundaries between on-line and off-line are flexi
  - Commodity components at HLT



Hardware triggerless in PANDA Experiment

- Long time collaboration between Labs
  - TrigLab, Exp. Phys. Center,IHEP
  - II. Phy. Institut, Giessen Univ,Germany
  - Since 2006 on
    - PANDA Experiment
    - DEPFET Project
- Research
  - New Trigger and DAQ (TDAQ) Archietecture
  - Design of High Performance Compute Node(CN)
  - Firm/Software design of TDAQ with Built-In system on FPGA
- IHEP Responsibility
  - Responsible for Hardware Design, system test
  - Responsible for Setup of system platform
  - Participate in software development
  - Responsible and accomplishment of EMC trigger study





CN's under testing at IHEP

New standard for Physics: xTCA

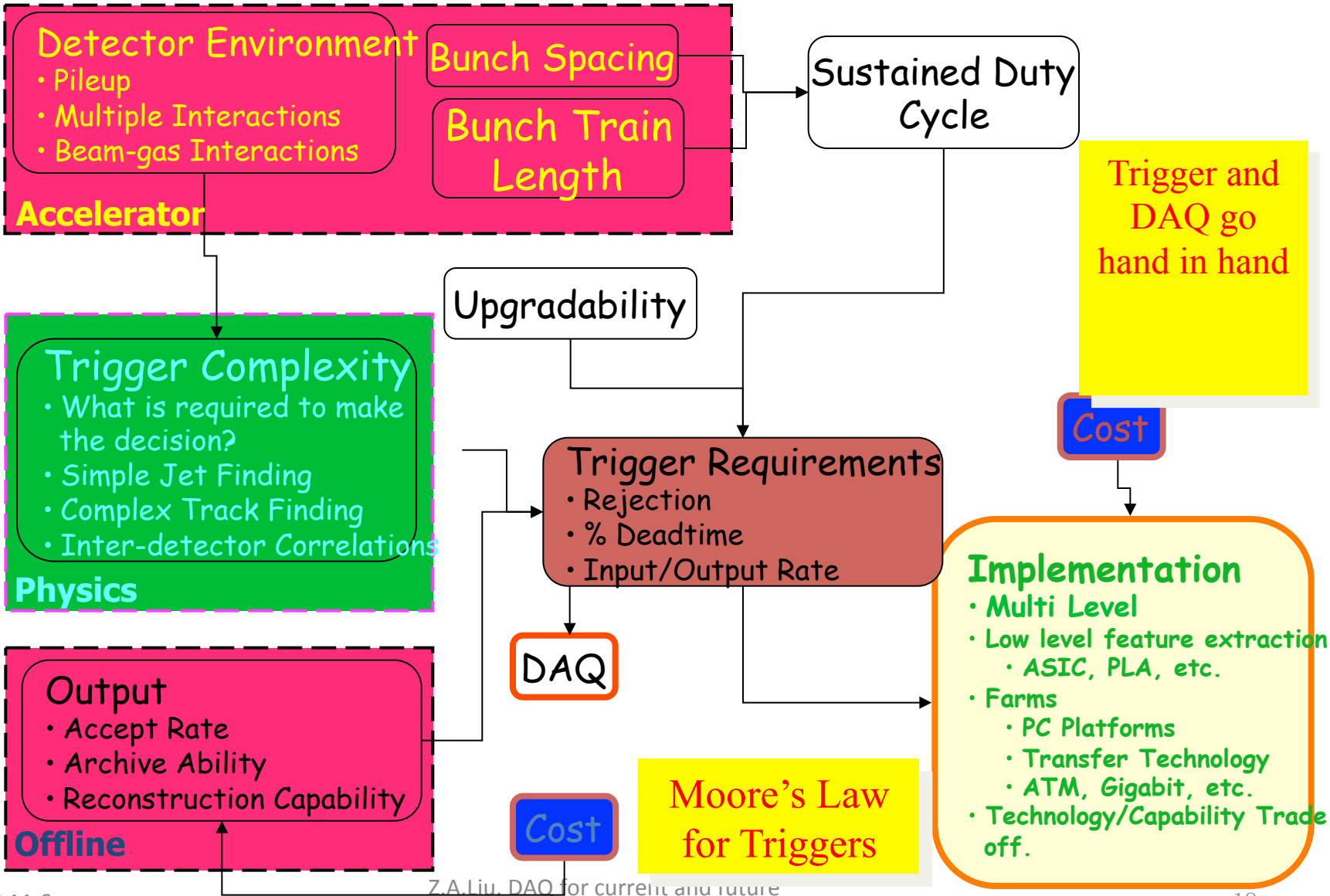
- xTCA:
  - New standard after VME, CPCI, CAMAC,…
  - For machine control and measurement
  - Standands for: ATCA,MTCA,AMC, with new extentions
- IHEP is a co-founder of this new standard
  - DESY, FNAL, IHEP , SLAC
  - Cypress Point Research and Performance Technologies
- Organization
  - Coordination Committee(CCTS),PICMG
  - Officers:Chair(SLAC),Secretery(Triple Ring), Document Editor（IHEP）
  - Hardware working group (weekly meeting)
  - Software working Group(weekly meeting)
- Status
  - IHEP organized 3rd xTCA workshop in IHEP/Beijing
  - Two hardware specifications officially issued
    - PICMG 3.8
    - MTCA.4
- Reference
  - http://www.picmg.org/pdf/PICMG_Physics_Public_Web_Update_061209_R5-3.pdf

phyTCA
xTCA™ for Physics

PICMG 3.8
AdvancedTCA Rear Transition Module

MTCA.4
MicroTCA® Enhancements for Rear I/O and Precision Timing

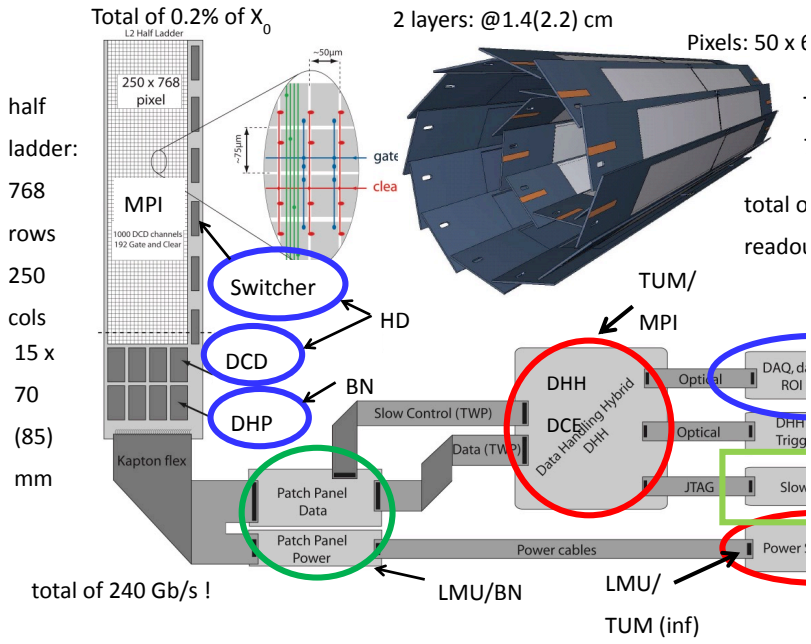
Constraints → a multiparameters problem

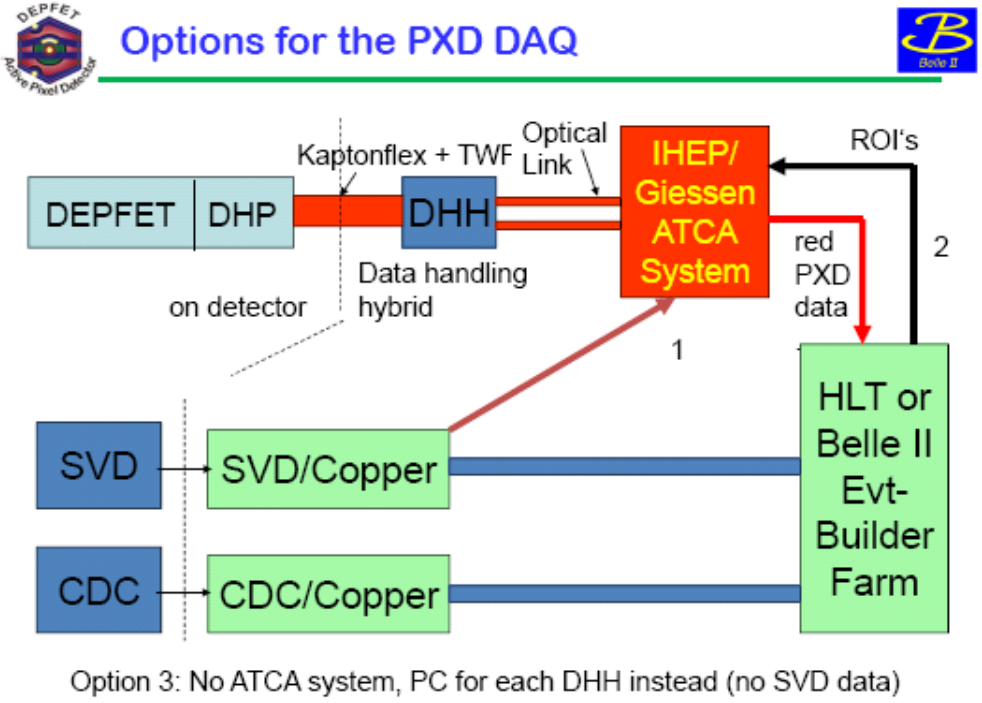


More thinking for future DAQ

- Backwards of present event building
  - Uses hardware inefficiently
  - Needs a lot of resources to transport data which is mostly unused
    - Used only for L1 trigger
    - Not processed by HLT and then discarded
  - Network b/w is used only in one direction
- Think more of a mesh (or even idea of IoT)
  - Leave data as close as possible to the detector
  - Pre-process it locally
    - Specialized processors(custom or commercial)
    - Generic CPUs
  - Access it remotely
    - Event-building on demand
  - Continuous calibrations with feedback to processors
    - Allows near offline-quality selection to reduce the event rate
    - Blurs boundary between online and offline reconstruction

Idea for Local Processing in Belle II PXD

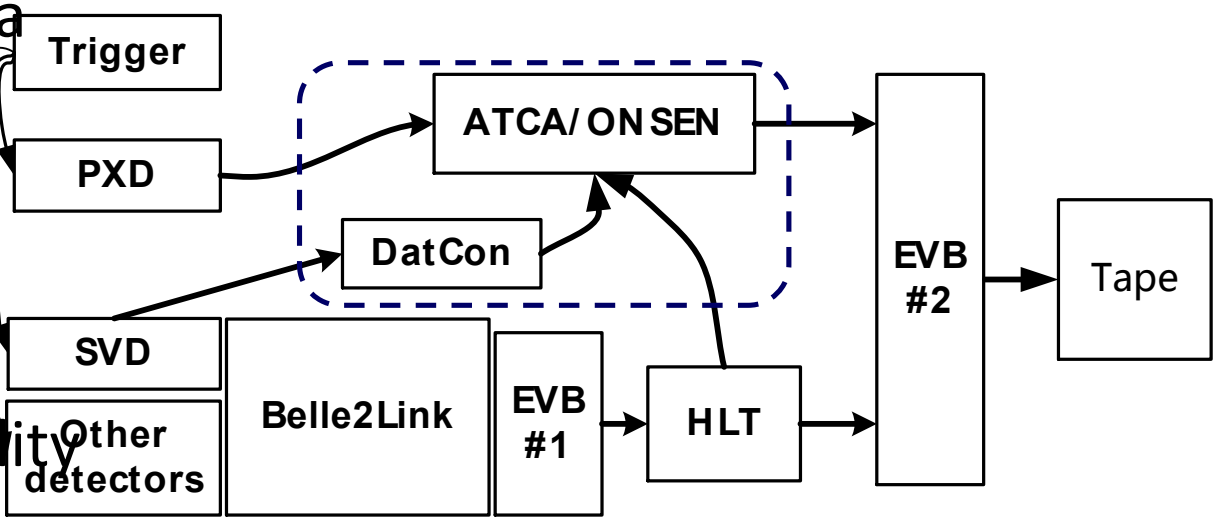


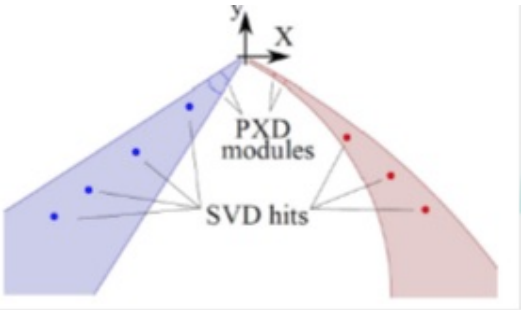


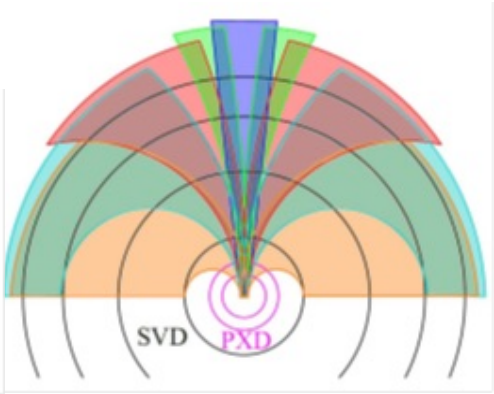
- Huge data output
  - 240Gb/s
  - >sum of Belle II others
- Reduction 1/10

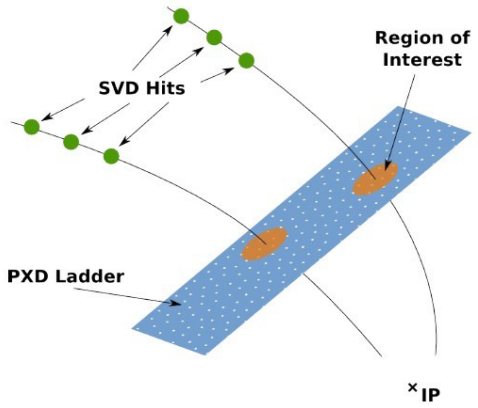
Principle of reduction

- PXD reduction
  - Based on HLT result
  - Help with SVD data
  - Tracking back
  - ROI searching
  - Data extraction
- Difficulties
  - Computing capability
  - Algorithms
  - 5s data buffer



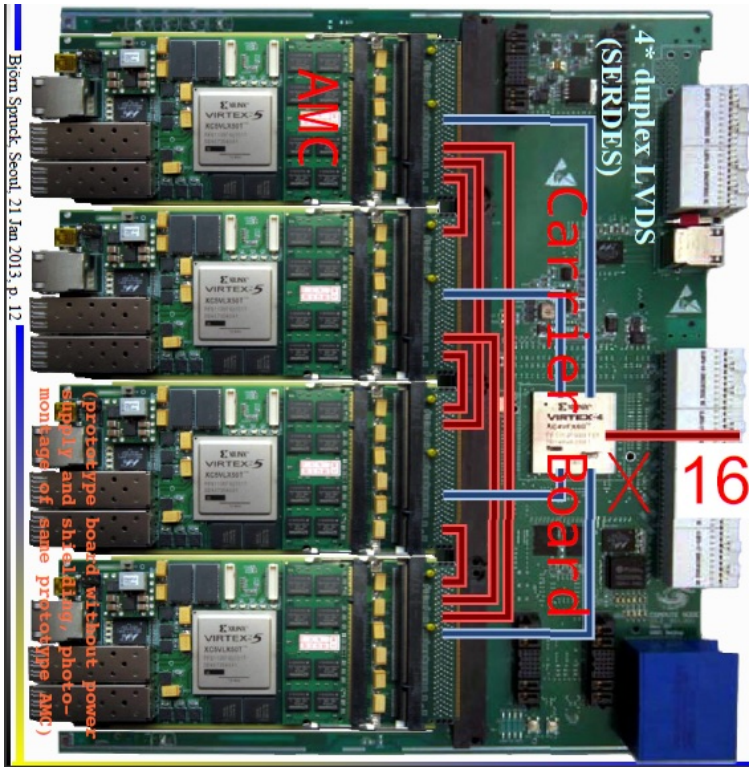


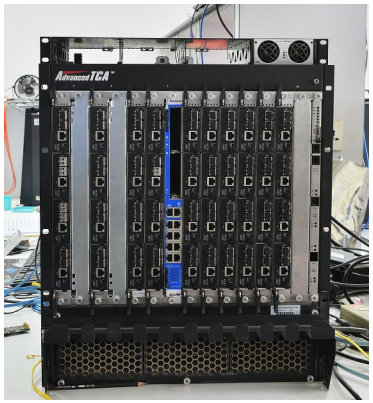




Key parts of PXD-reduction

- ONSEN/PXD-DAQ
  - Firmware(Giessen Uni)
  - Hardware(IHEP Beijing)
    - 1 ATCA Shelf
    - 2 shelf managers
    - 1 Power Supply
    - 10 Compute Node(CN)
      - 1 ATCA Carrier(PICMG3.8)
      - 1 Power Board
      - 4 xFP/AMC cards
      - 5 MMCs





Summary

- By giving some of the present examples, I am trying to give a hint on how the future DAQ system would move, but it is hard to predict new technology more than 10 year ahead
- We need our own thoughts like xTCA
- We need development from Industry
  - New FPGA, high IO
  - Powerful CPUs,PPUs
- We should not wait, but keep working/improving

(Ref. PAND/Belle II/CMS docs, special thanks to Remigius K Mommsen)