Overview of SOI development

(from the HEP perspective)

International workshop on CEPC, 6-8 Nov. 2017, Beijing

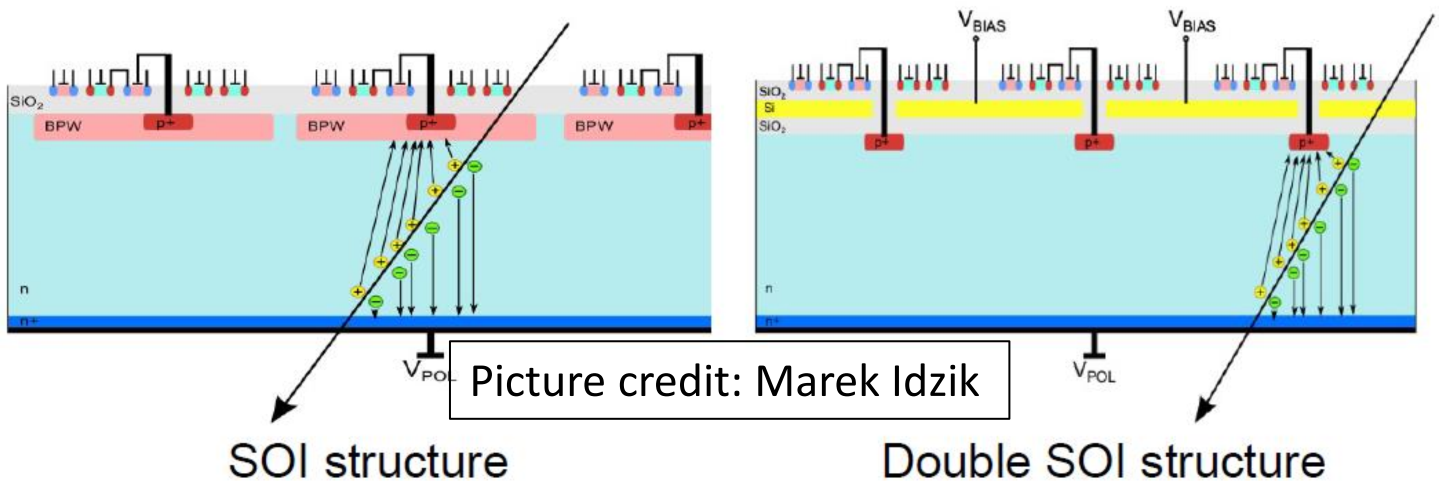
Yunpeng Lu on behalf of SOIPIX collaboration

Outline

- Concept of SOI pixel sensor
- Technology development
  - Shielding
  - Radiation
  - Transistor layout
  - 3D integration
  - Stitching
- Applications in high energy physics
  - FPIX for general study
  - SOFIST for ILC vertex
  - CPV for CEPC vertex
- Summary

Introduction

- Advantages of SOI technology for tracking
  - Full CMOS circuit at 0.2um process node
  - High resistive (up to >10kΩcm) substrate, full depletion/ over depletion(fast charge collection)
  - Pixel pitch below 10um possible
  - Sensor can be thinned to ~50um
  - Double SOI wafer and process available (for better shielding & radiation hardness)



Wafer types

- A variety of n/p-type substrate
  - Double-SOI wafer in continuous optimization

Layer	Single SOI	D-1 (SOITEC)	D-2 (Shinetsu)	D-3 (Shinetsu)
SOI1	P-type 40nm, ~18 Ωcm	p-type 88nm, < 10 Ωcm	p-type 88nm, < 10 Ωcm	p-type 88nm, < 10 Ωcm
BOX1	200nm	145nm	145nm	145nm
SOI2	n/a	p-type 88nm < 10 Ωcm	n-type 150nm < 10 Ωcm	p-type 150nm 3 ~ 5 Ωcm
BOX2	n/a	145nm	145nm	145nm
Substrate	n/p-type CZ, FZ 725um, 0.7 ~ 25 kΩcm	n-type CZ 725um, >700 Ωcm	p-type CZ 725um, > 1.0 kΩcm	p-type FZ 725um, > 5.0 kΩcm

Sensing diode

- Two ways of implantation
  - P+, highly doped
  - BPW, moderately doped
- Dedicated contacts to access the collection electrode.

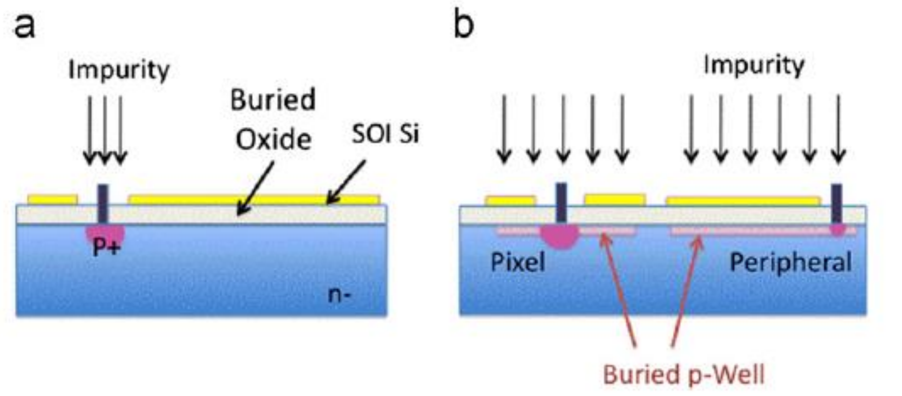


Fig. 5. (a) Normal implantation method to create p–n junction in the substrate and (b) buried p-well implantation method. By fixing the BPW potential under peripheral circuit, the back gate effect is completely suppressed. In the pixel area, BPW may be used to extend sensor area.

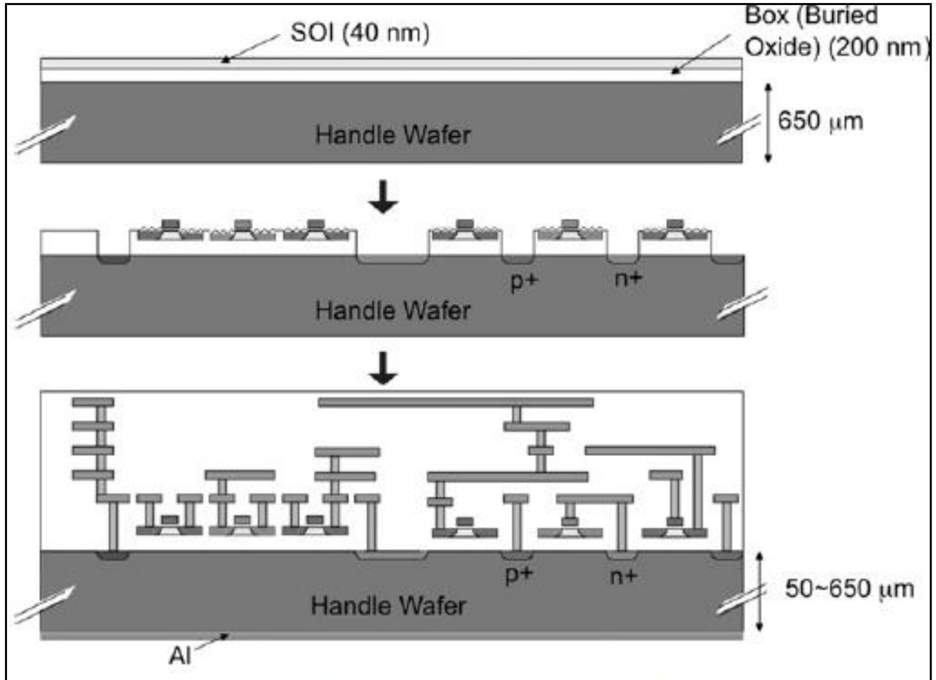
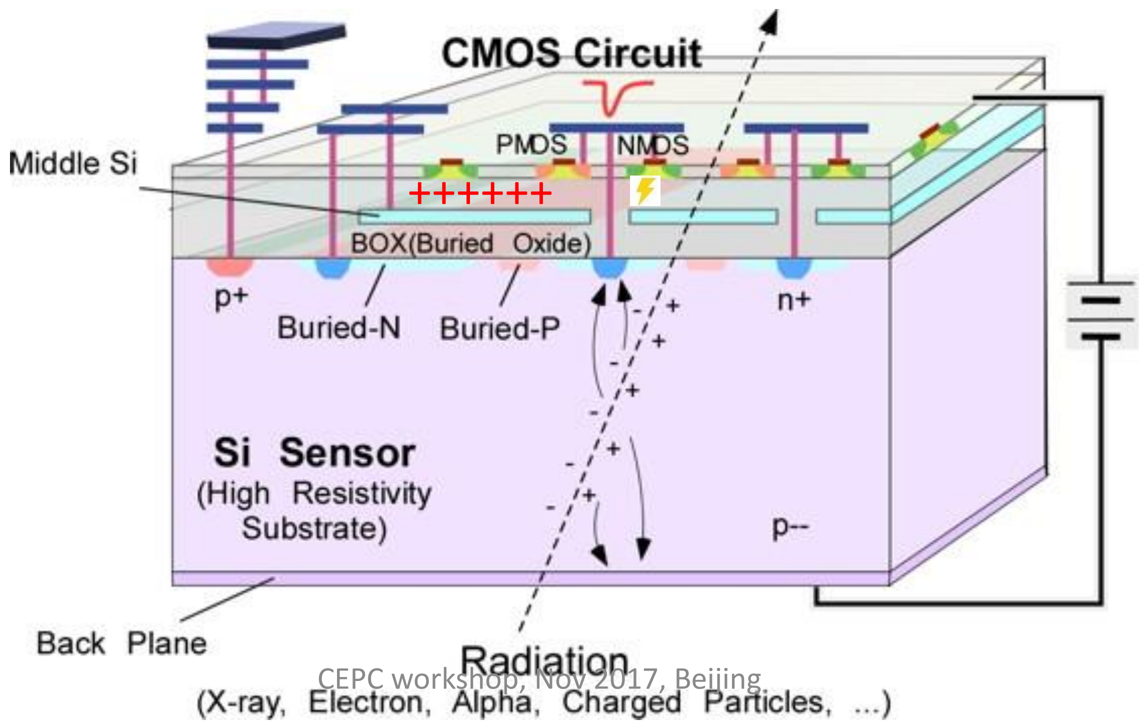


Fig. 2. Simplified SOI pixel process flow.

Double SOI

- Shield the capacitive coupling between sensor and circuit
  - Enable complex function
  - Improve frontend performance
- Compensate the trapped charge by TID
  - Enhance TID tolerance



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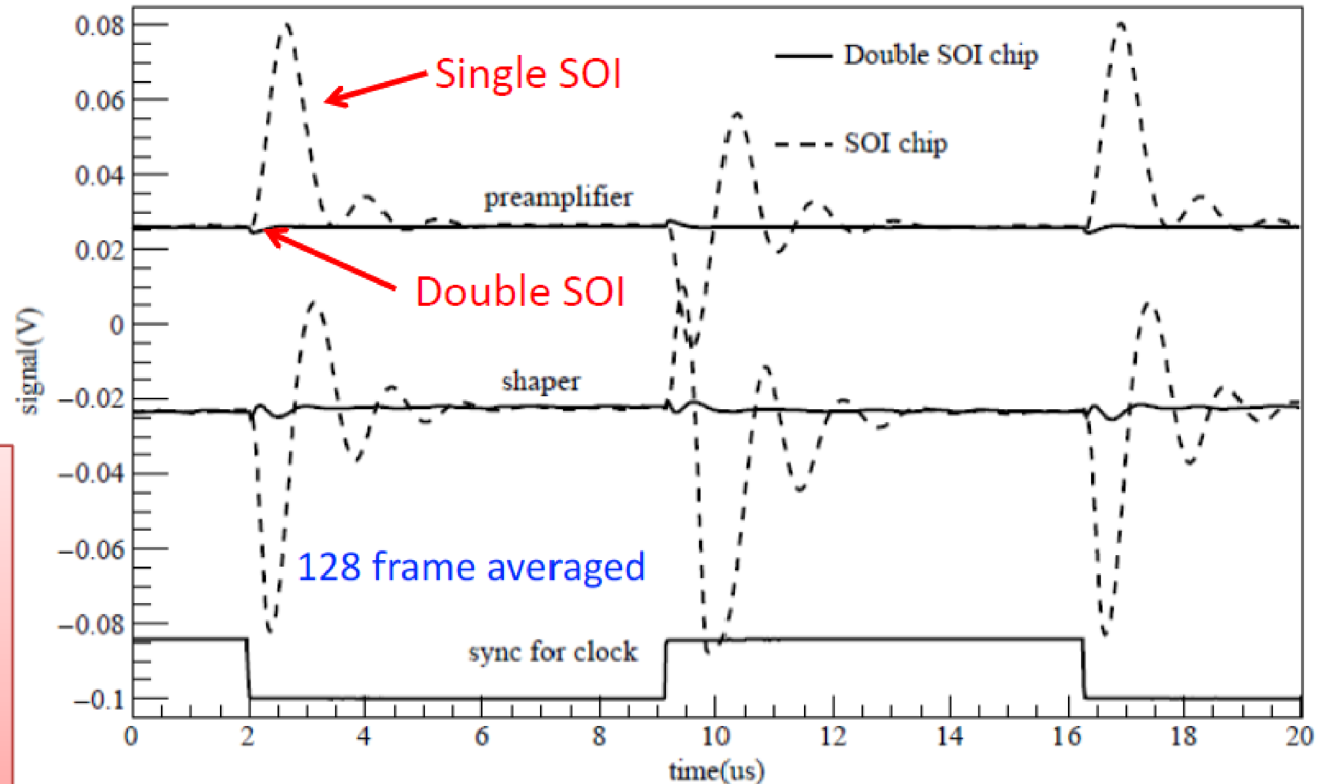
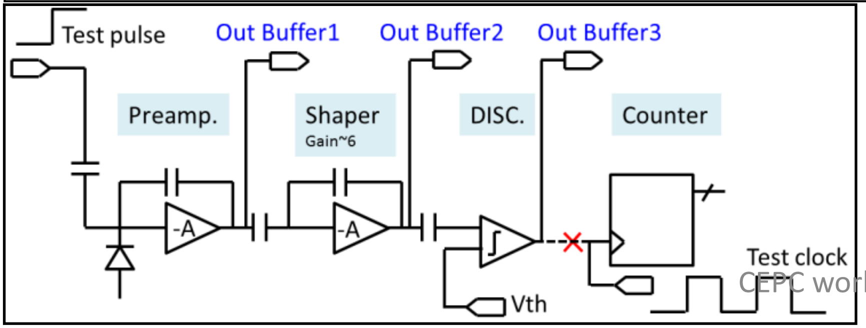
Effect of Double SOI

Cross Talk from Clock line



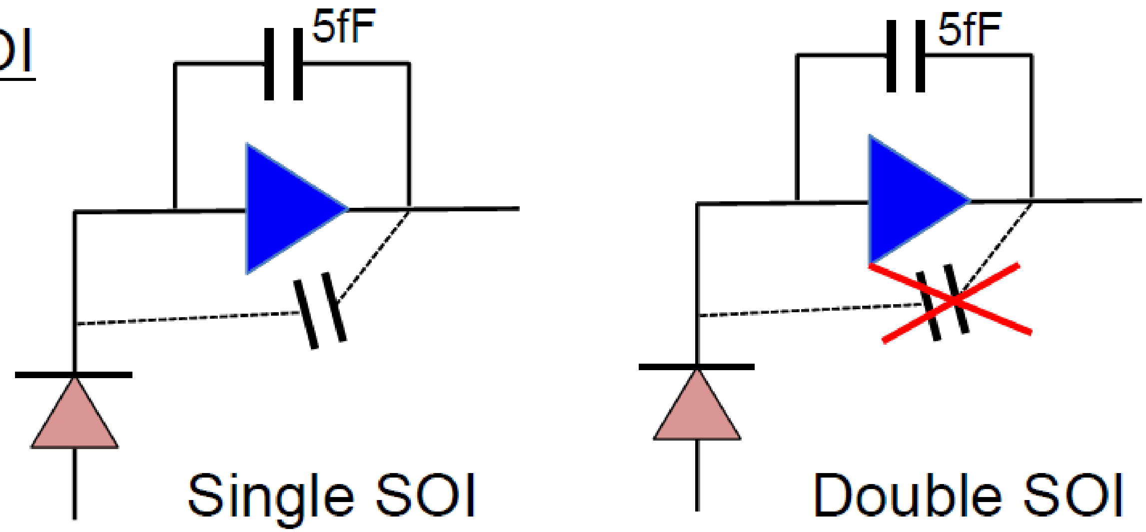
(by Lu Yunpeng (IHEP))

Shield:
Cross Talk between Circuit and Sensor is reduced to 1/20.

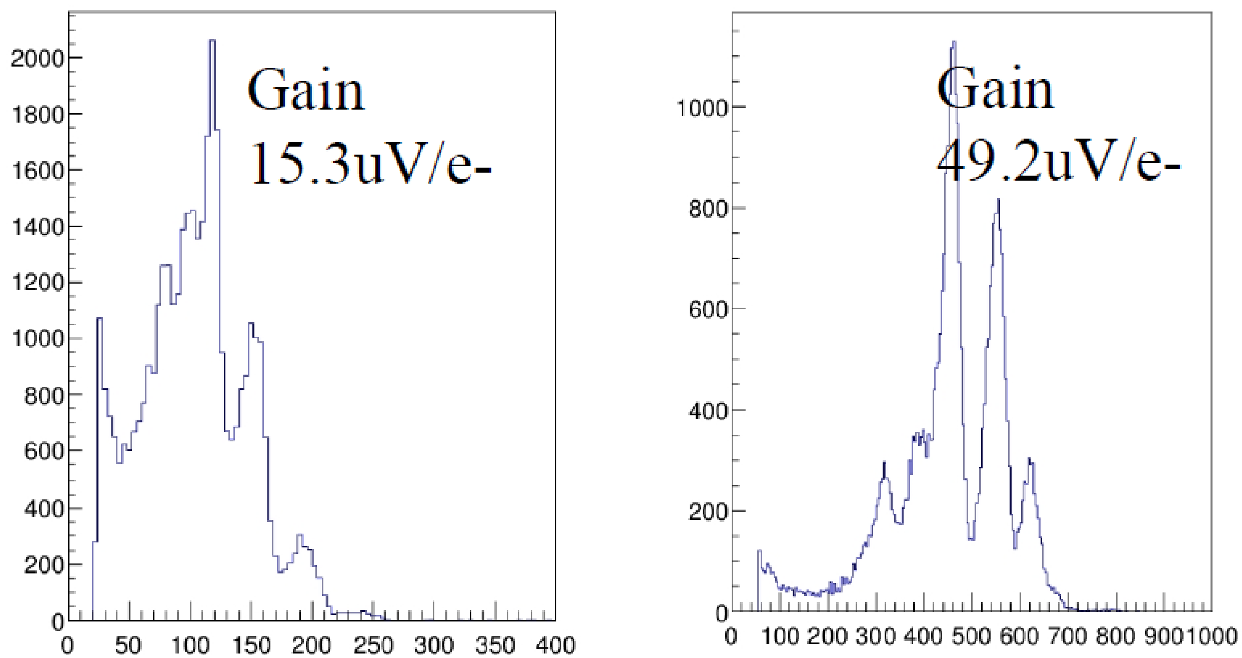


Effect of Double SOI

Coupling:
Gain of Charge Amp increases ~3 times by cutting parasitic C.

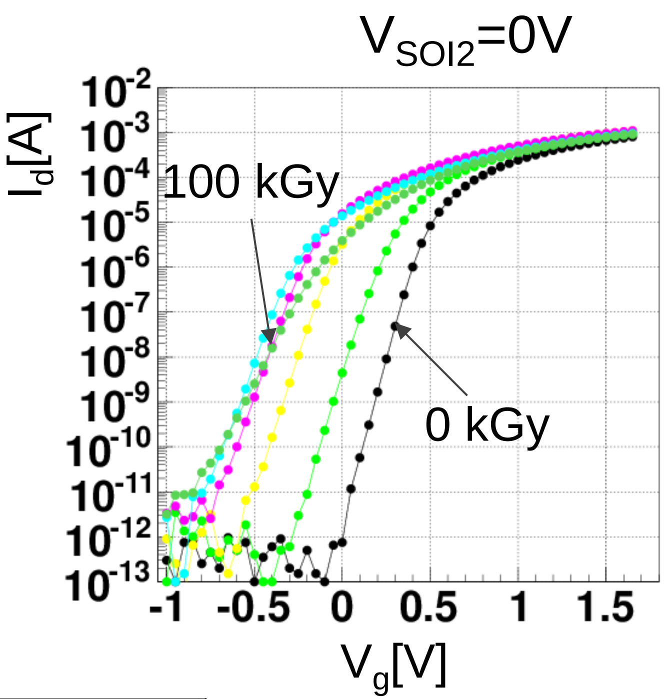


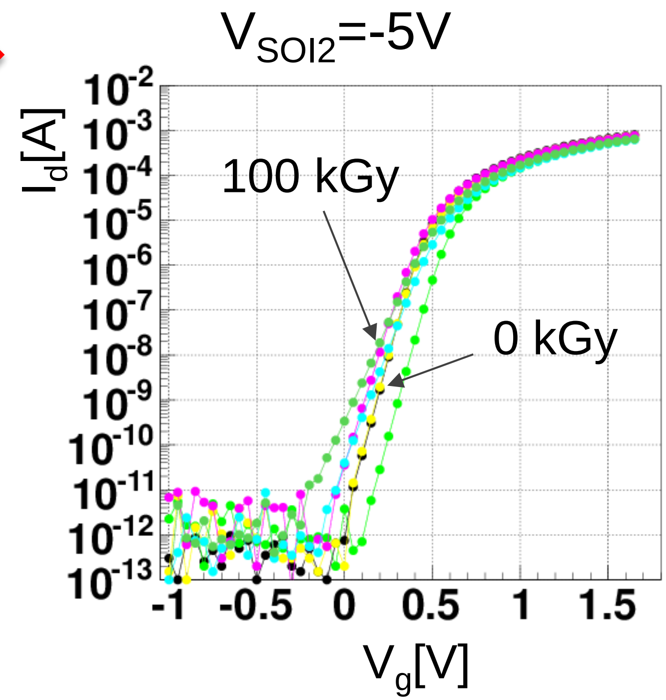
Am241



Irradiation with Gamma-ray

NMOS
I/O normal Vth
Source-Tie Tr.
L/W =0.35um/5um

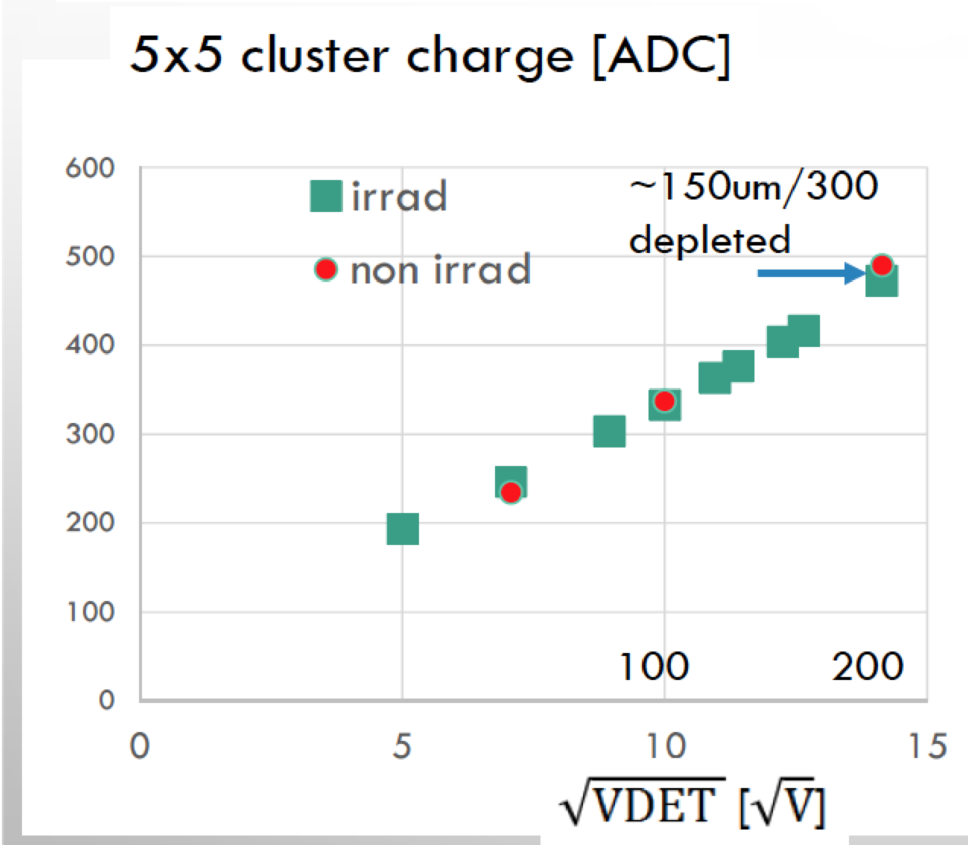


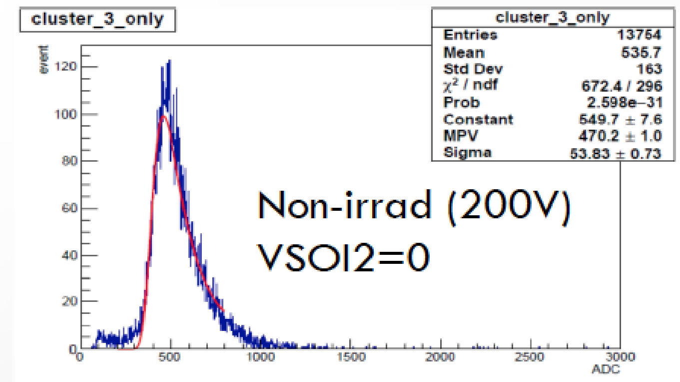


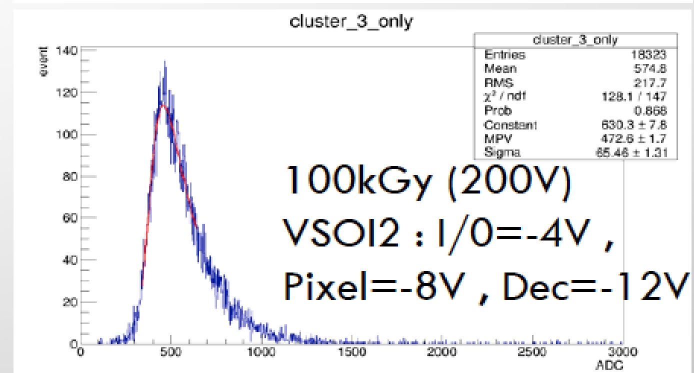
(by U. of Tsukuba)

FPIX2:DSOI 100KGY

5x5 cluster charge about the maximum charge pixel in an event

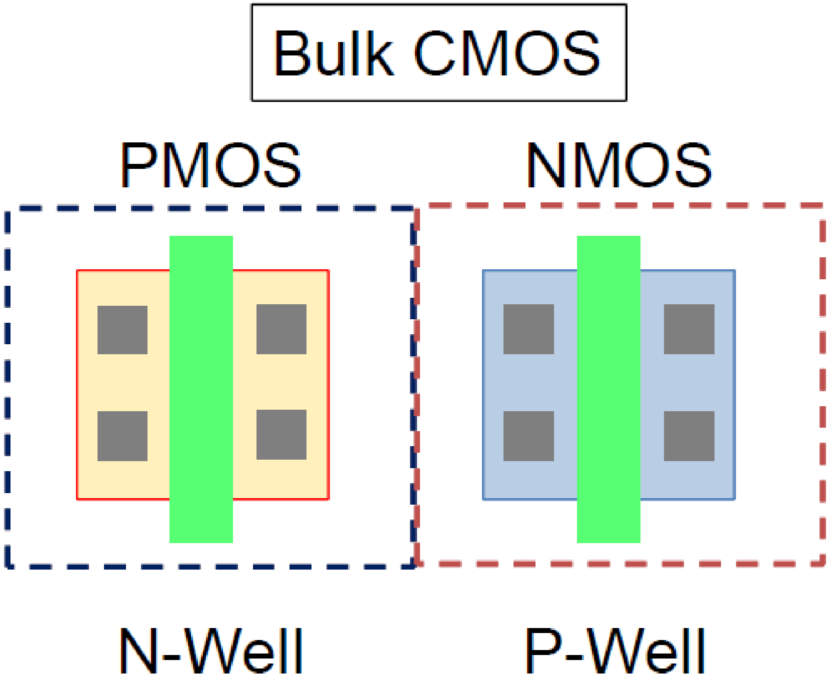


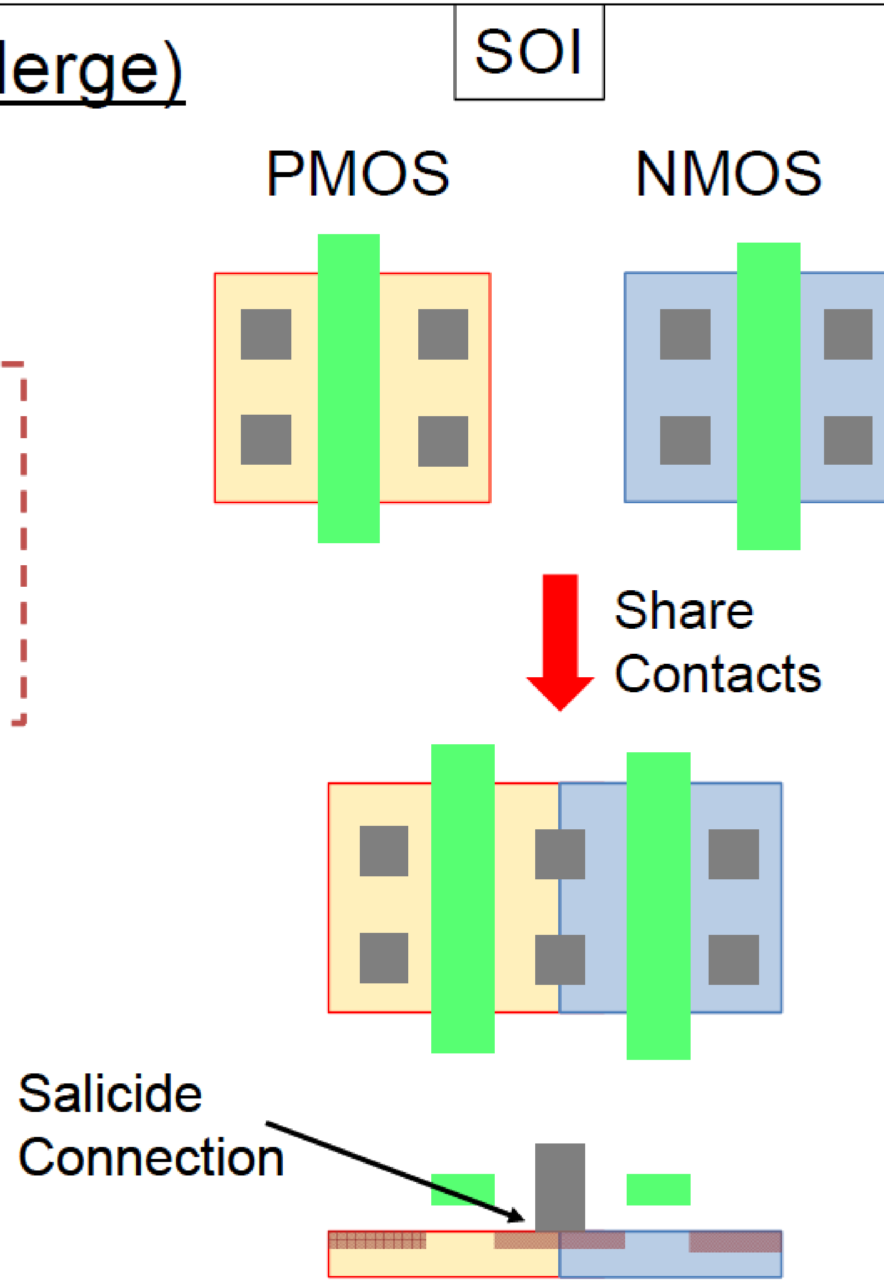




Innovative double-SOI allows operation of SOI devices to 100kGy
Recent study extended to 1MGy

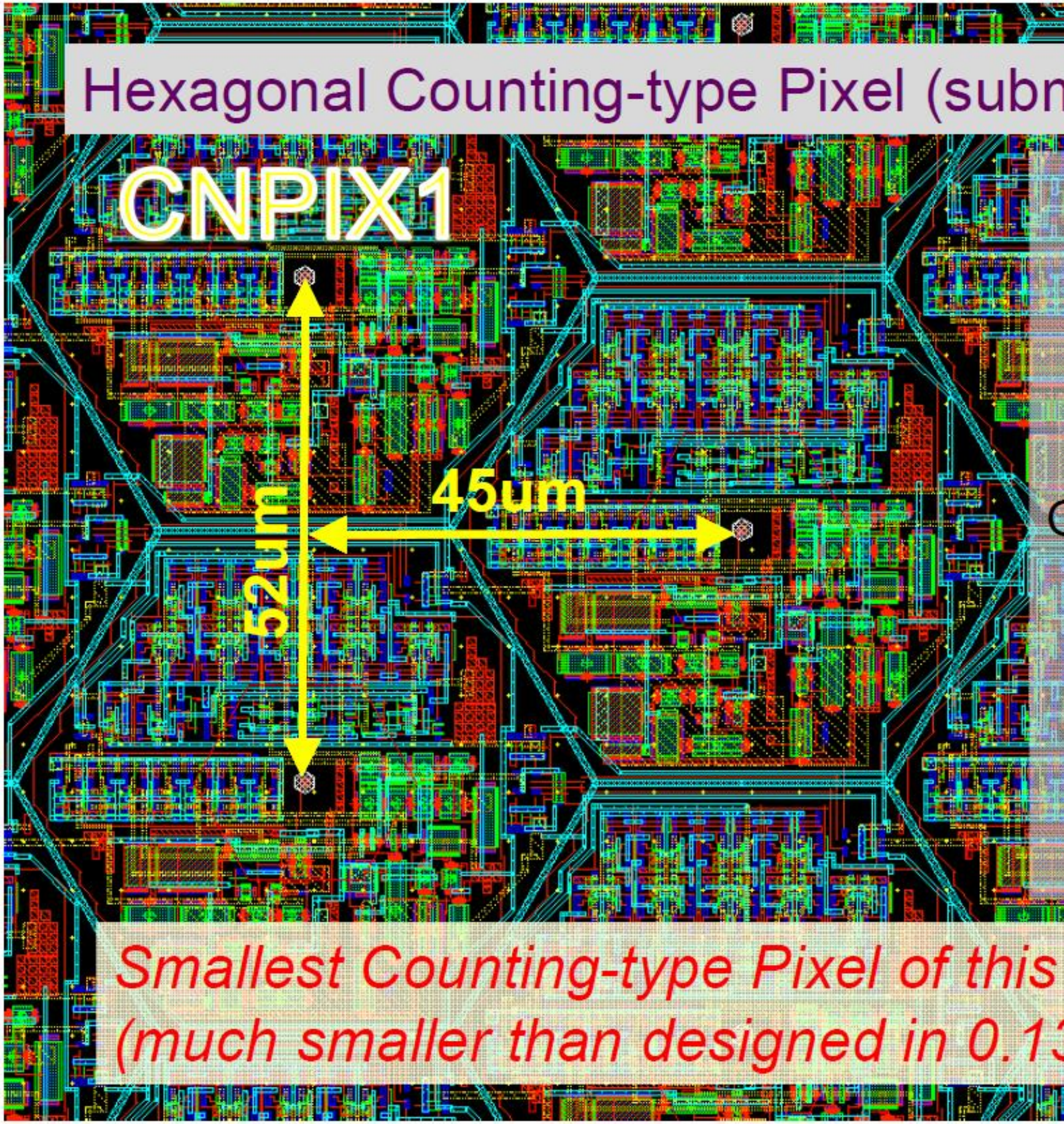
Layout Shrink（Active Merge)





In the SOI process, it is possible to merge NMOS & PMOS Active region and share contacts.

Hexagonal Counting-type Pixel (submitted in June)



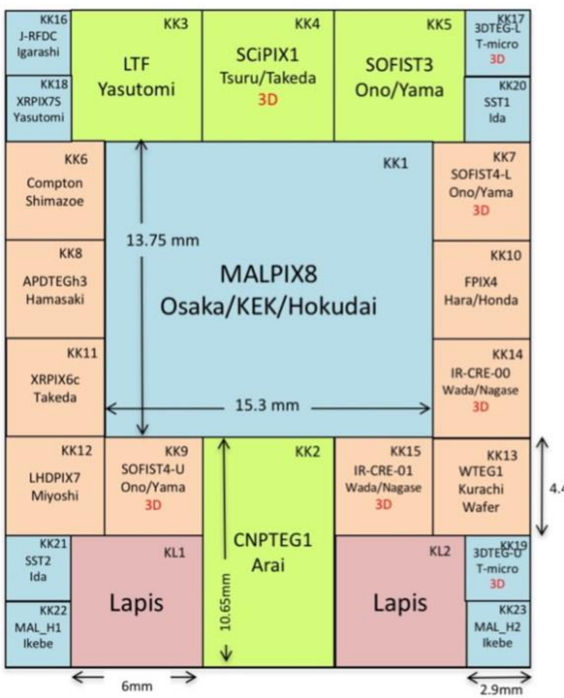
Charge Amp
+
Shaper
+
Discriminator
+
Q Share Handling
+
19bit Counter
+
7bit register

(in 2,340 um^2)

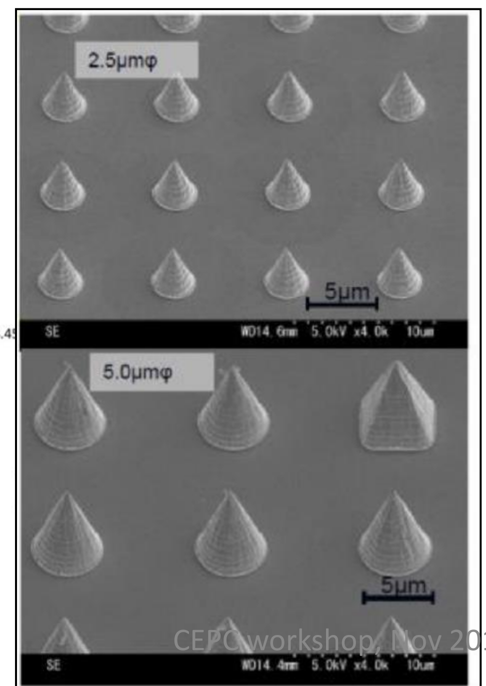
Smallest Counting-type Pixel of this kind.
(much smaller than designed in 0.13um process)

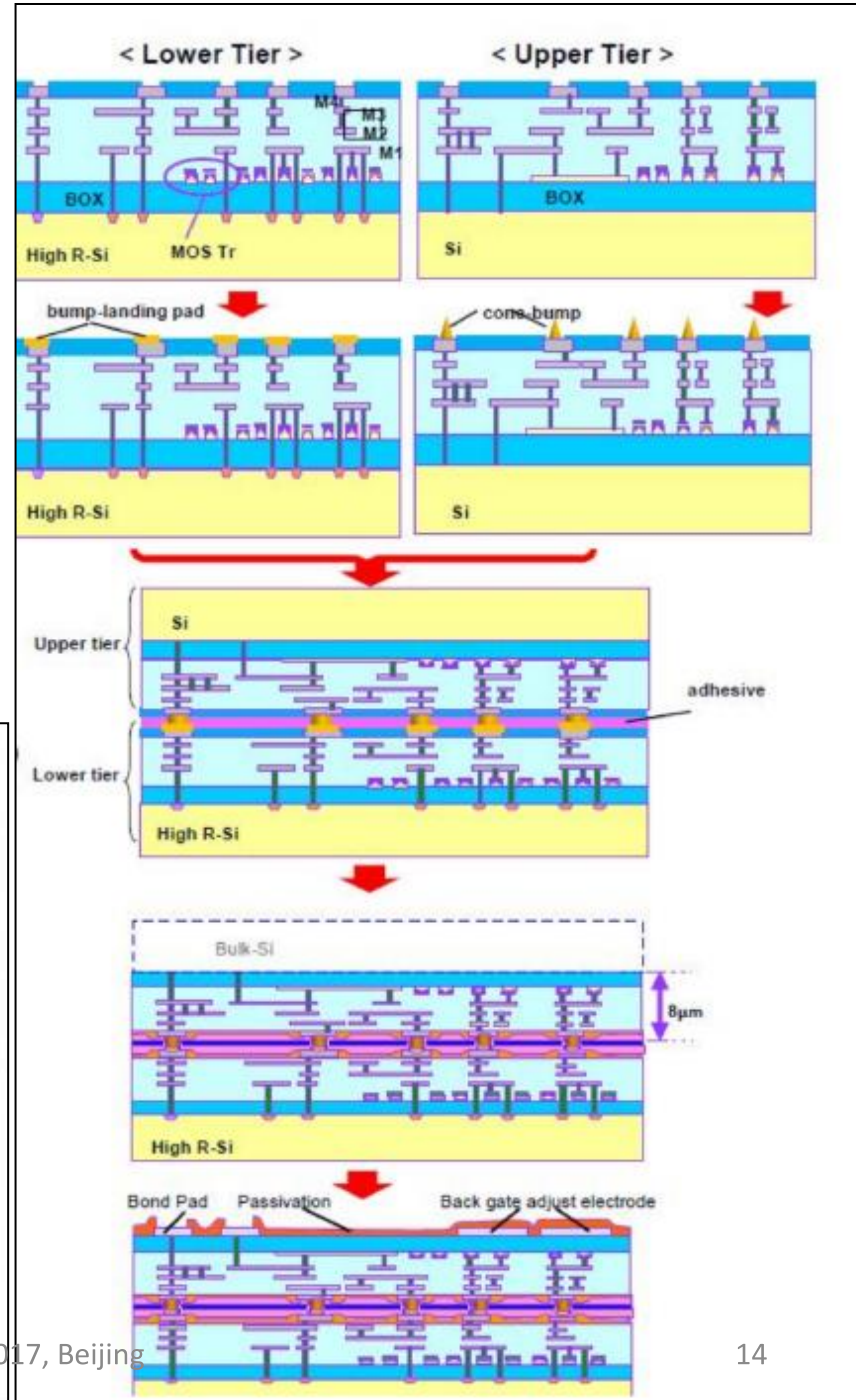
3D integration

- Lower Tier (Sensor + Analog)
- Upper Tier (Digital)
- MPW available through SOIPIX



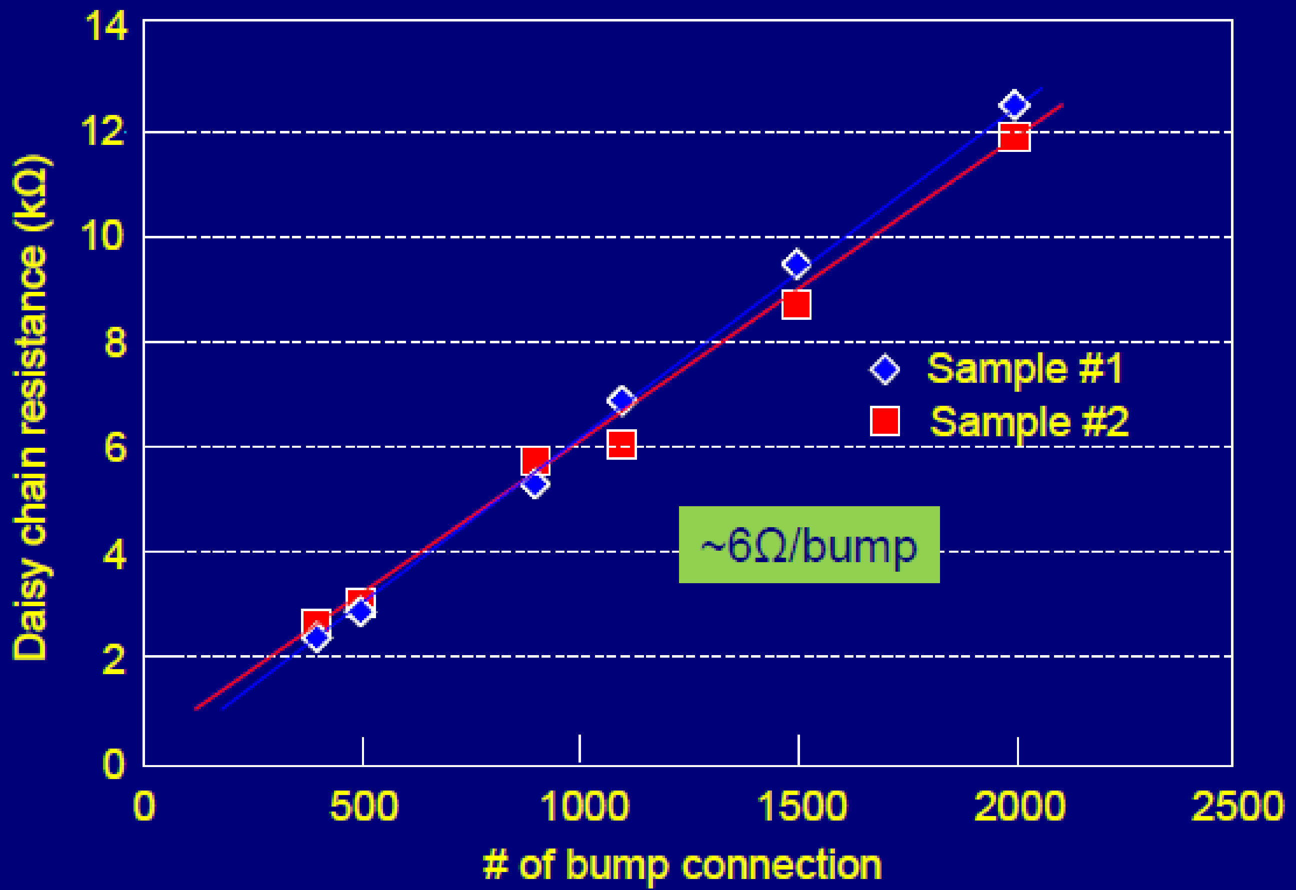
FY17-1 MX2166
SOI MPW Floor Plan
2017.6 Submission





T-Micro

Daisy Chain Resistance



Ref. ~5Ω by 4 terminal resistance

Transistors in the upper/lower tier

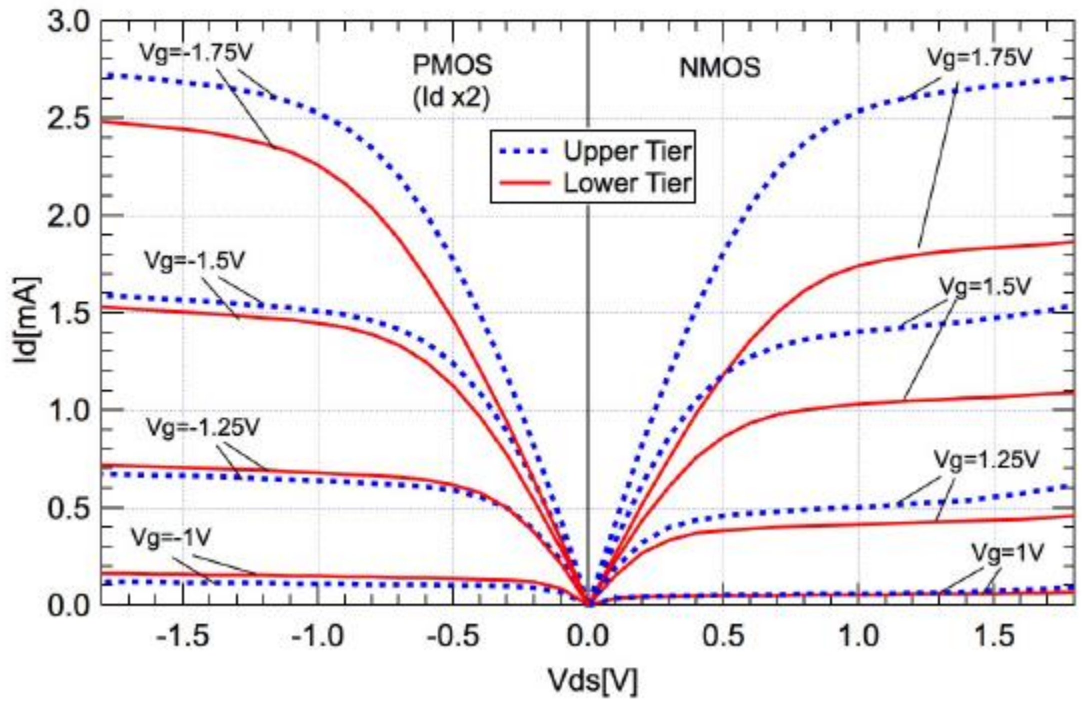
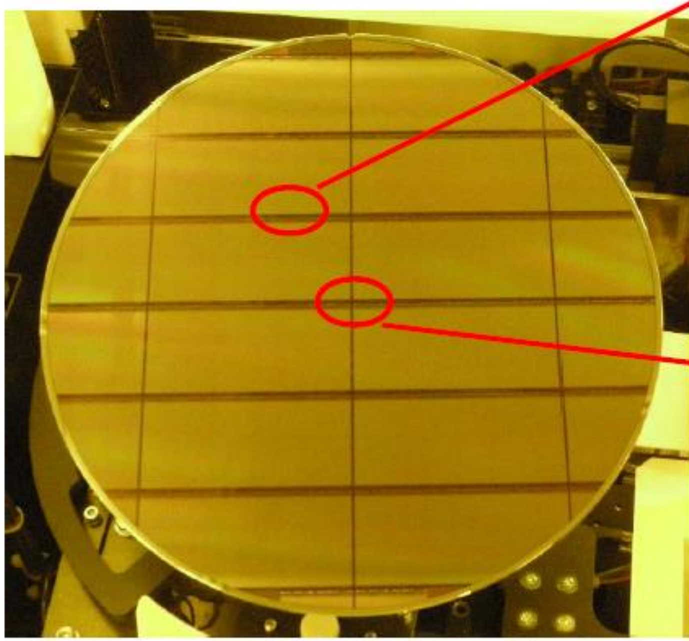


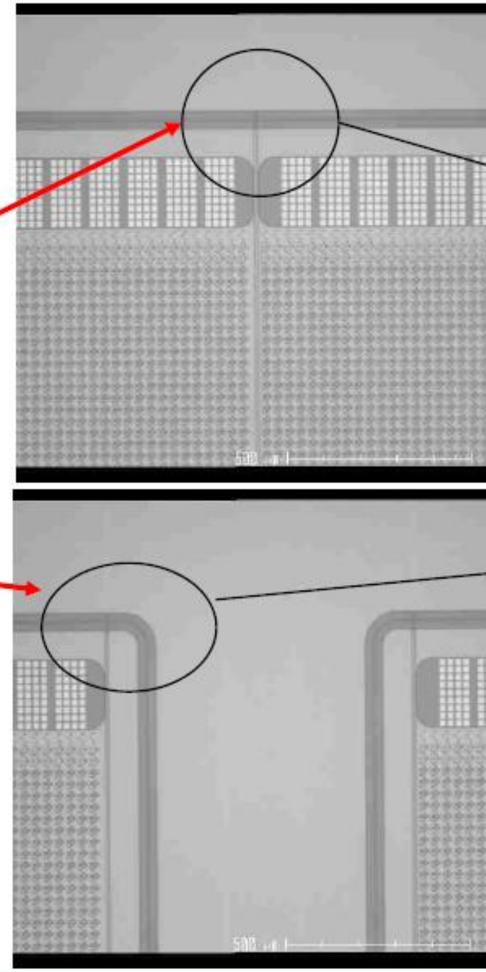
Fig. 5 Id-Vds characteristics of NMOS and PMOS transistors located at lower and upper tiers.

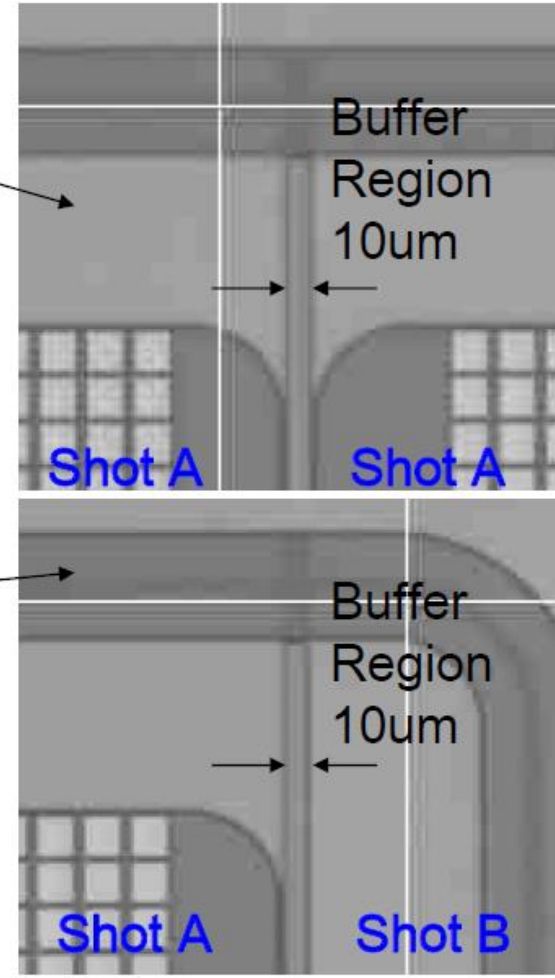
Stitching Exposure for Large Sensor

SOPHIAS by RIKEN

Reticule size
~25mm x 31mm







- Width of the Buffer Region can be less than 10um.
- Accuracy of Overwrap is better than 0.025um.

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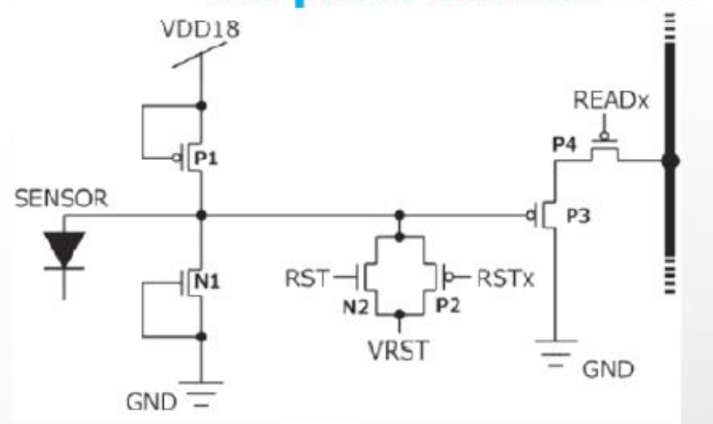
FINE-PIXEL DETECTOR: FPIX2

- **Pixel size: 8μm□**
- **#Pixels: 128×128**
- **Handle wafers:**
  - **>single SOI**
    25kΩ·cm p, 500 umt
  - **>double SOI**
    1kΩ·cm p, 300 umt
- **Rolling shutter RO**
  8 parallel outputs

On-pixel circuit

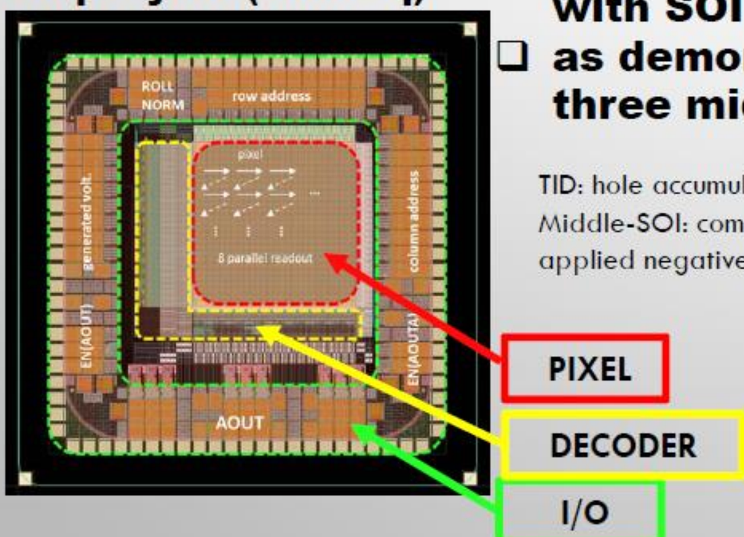


In Development:

- ❑ **to demonstrate excellent spatial resolution achievable with SOI technology (=>tracker for SOFIST TB)**
- ❑ **as demonstrator of TID tolerance (FPIX2 equipped with three middle-SOI regions)**

TID: hole accumulation in BOX/GOX
Middle-SOI: compensate TID effects by applied negative voltages

chip layout (3mm-sq)



Analog signals are digitized (2ms) by external SEABAS2 12-b ADCs (8 parallel)

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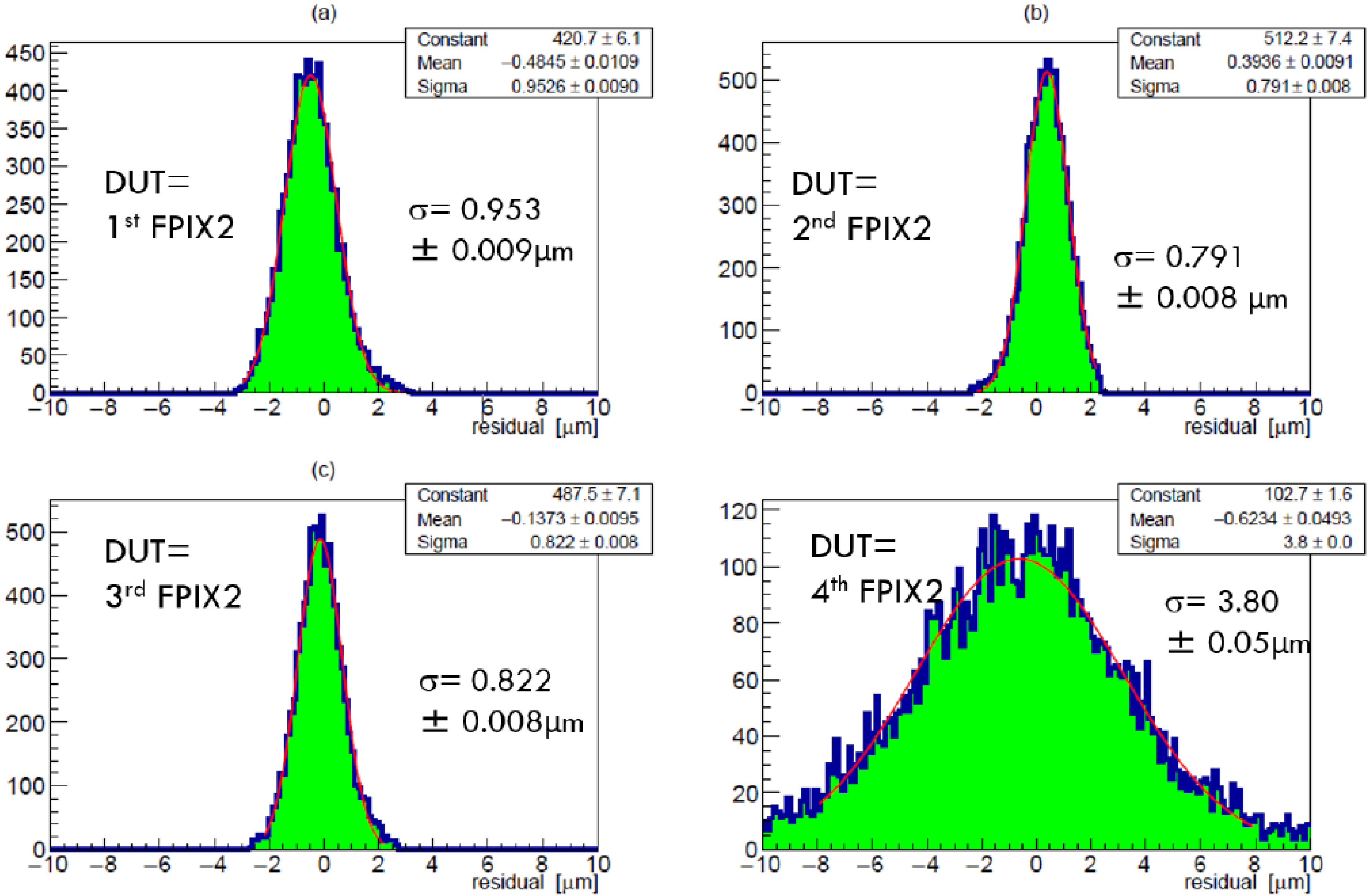
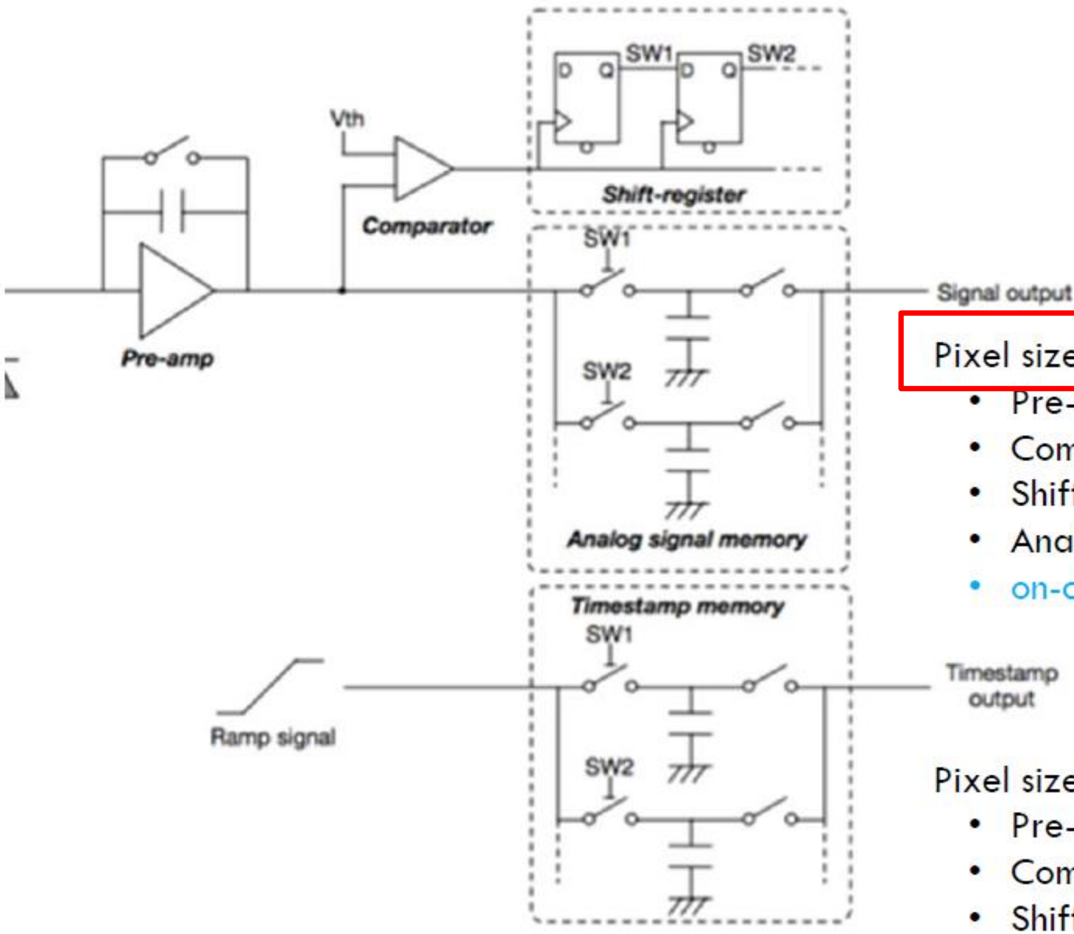
RESIDUALS in X

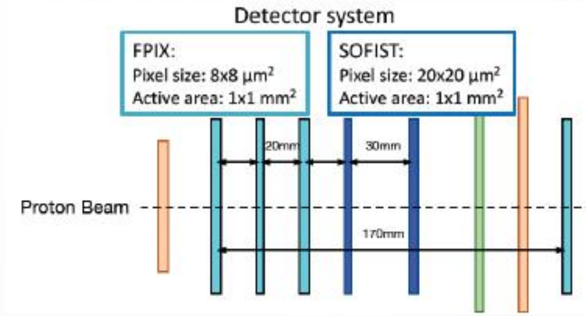
Residuals of DUT hit wrt the track reconstructed using other three FPIXs



SOFIST

SOI PIXEL FOR FINE SPACE AND TIME





Pixel size: 20x20 μm^2

- Pre-amplifier
- Comparator (Signal discrimination)
- Shift register (Switch memories)
- Analog signal memories (Store signal charge)
- on-chip 8-b column ADCs /column

SOFIST V.1: beam tested

Pixel size: 25x25 μm^2

- Pre-amplifier
- Comparator (Signal discrimination)
- Shift register (Switch memories)
- Timestamp memories (Store hit timing)

(time info digitized by the same column ADCs)

SOFIST V.2

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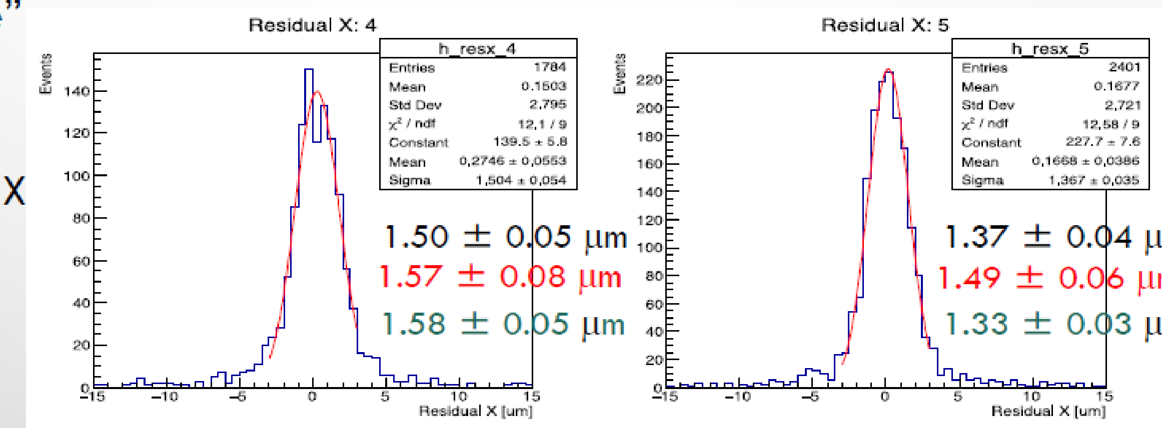
SOFIST SPATIAL RESOLUTION

SOFIST residual to FPIX track (σ_track~0.57/0.65µm)
Bias=130V (~500um depletion) =>15V (~200µm depletion)
Readout: external 12-b ADCs =>on-chip 8-b ADCs

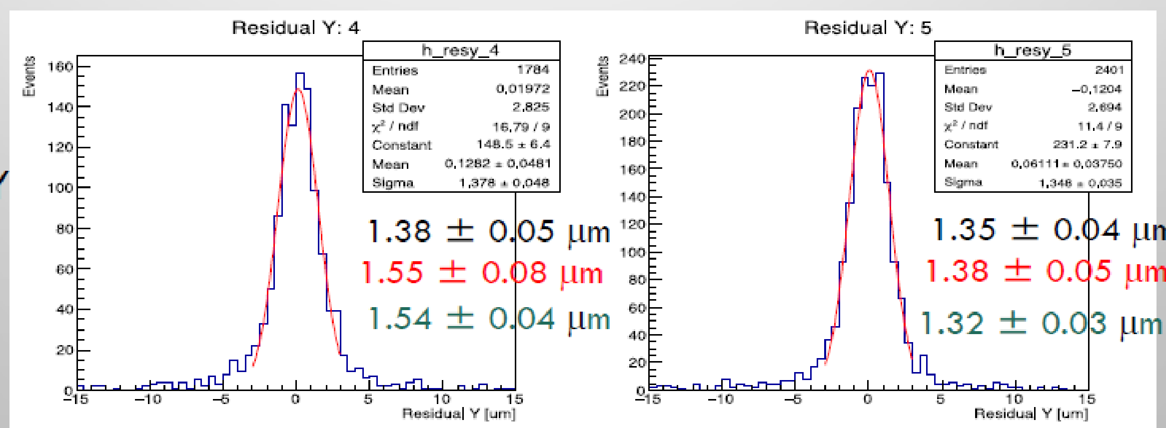
SOFIST#1(BPW14x14) SOFIST#2(BPW16x16)

plots for "black case"

Residual X



Residual Y

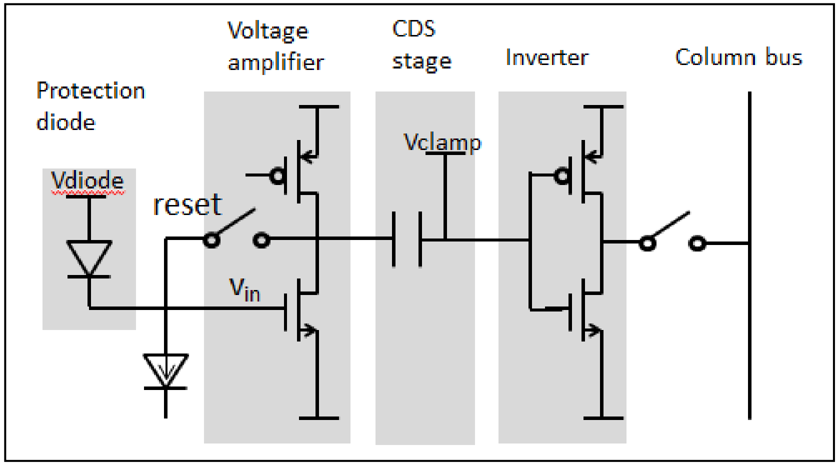


S/N~300

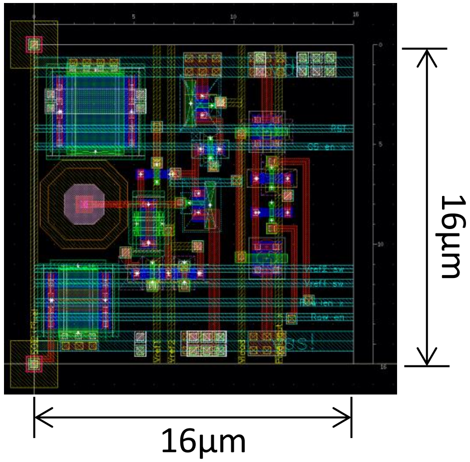
CPV chip concept

- Fine pitch matrix with in-pixel discriminator
  - 16um pitch to achieve single point resolution < 3um
  - In-pixel discriminator to enable a low power operation in a continuously colliding mode
- Pixel structure
  - Sensing diode, amplifier, discriminator
  - Half of matrix are analog readout for calibration
- Thinned down to 75um thick
  - Backside process

CPV2 function blocks

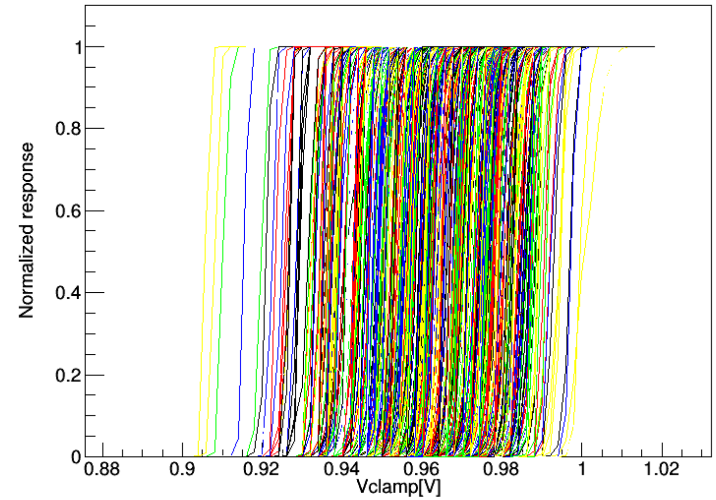


CPV2 pixel layout

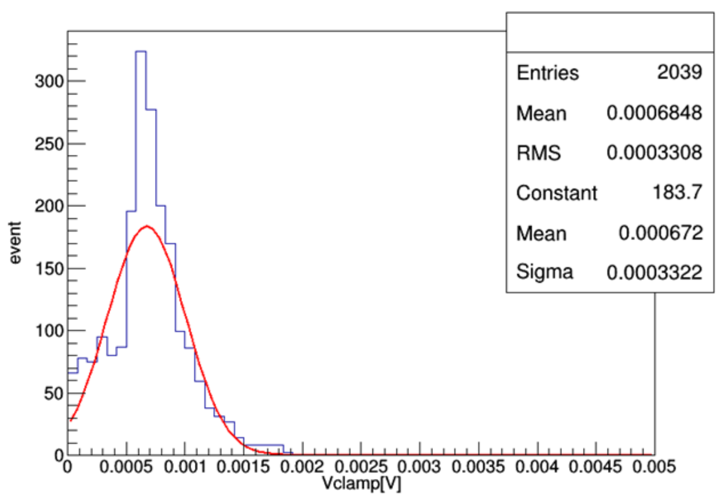


Noise and threshold

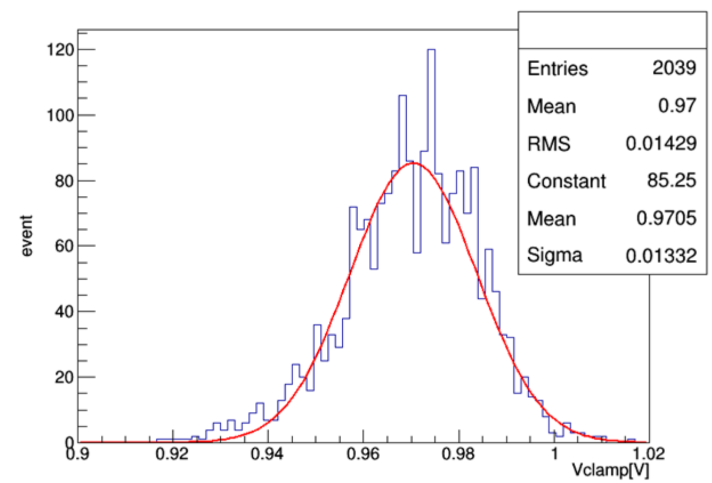
- S-curve measurement
- Temporal noise ~6e$^-$
- Threshold dispersion (FPN) ~114e$^-$
  - Offset cancellation is needed



temporal noise



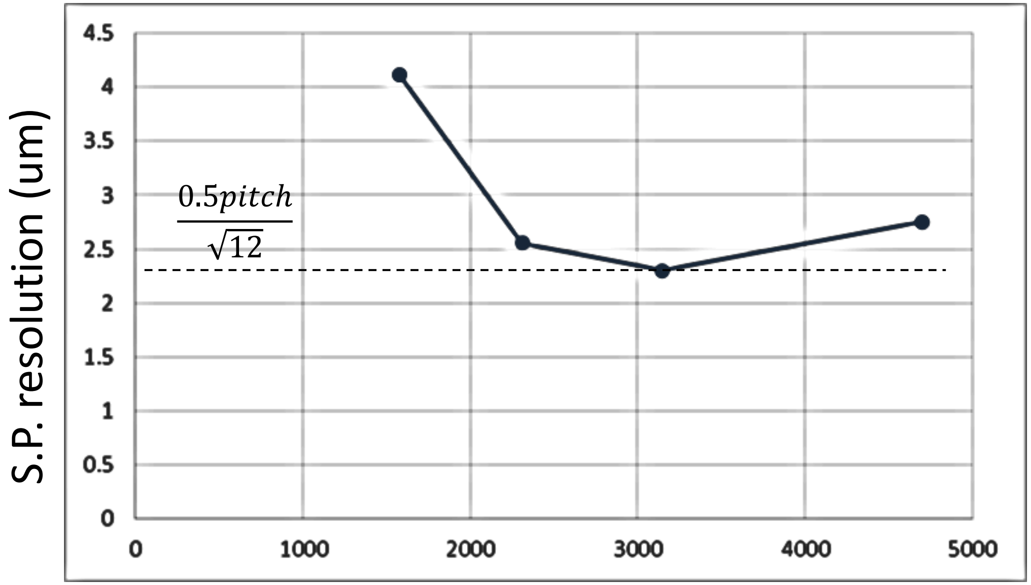
FPN



Single point resolution

- Single point resolution measured at different laser beam intensity
  - Increase of signal amplitude favors single point resolution
  - 2.3um achieved at the optimum signal/threshold ratio

S.P. resolution measured as a function of threshold



Signal charge of laser beam (e^-)

Summary

- Applications for the future e^+e^- colliders are trying to exploit following SOI features:
  - HR substrate that can be fully depleted
  - Full CMOS signal processing capability at 0.2um feature size
  - Improved shielding and radiation hardness by Double-SOI
  - SOI wafers that greatly simply 3D integration
  - Regular submissions to foundry accessible via MPW run
- Synergy can be made among these HEP applications:
  - Thinning
  - 3D integration
  - Radiation hardness

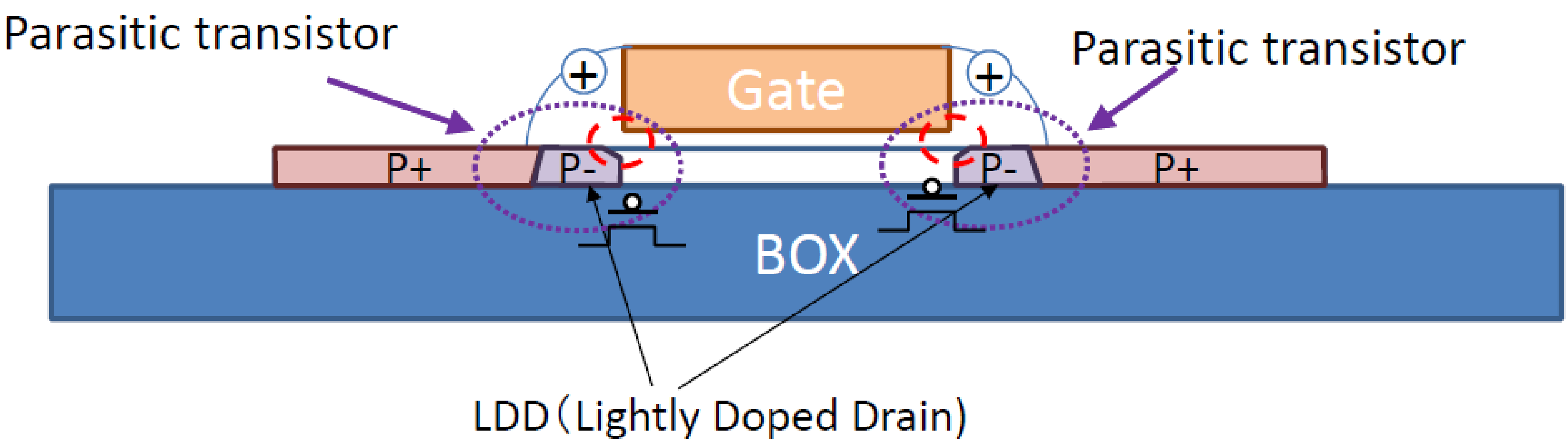
Acknowledgements

- This work is supported by the National Nature Science Foundation of China, Grant 11575220.
- And the CAS Center for Excellence in Particle Physics (CCEPP)

- Backup slides

Dose Increase in Lightly Doped Drain (LDD) Region

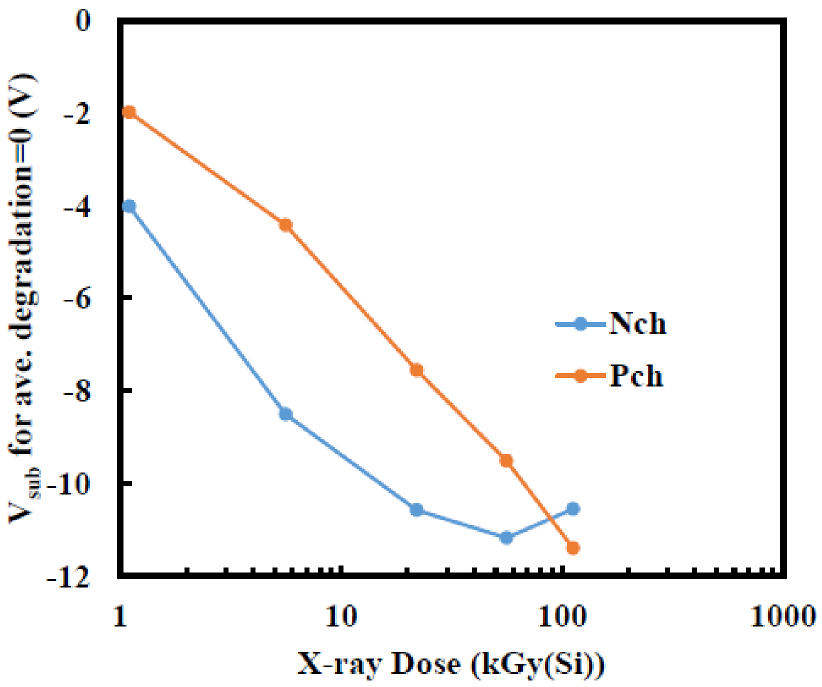
- Major cause of the drain current degradation by radiation is Vth increase at gate edge due to positive charge generation in spacer.
- Charge in spacer control the Vth of the parasitic transistor.
- To reduce this effect, lightly doped drain (LDD) dose should be increased.
- Present process has rather low dose in LDD region to aiming lower power.

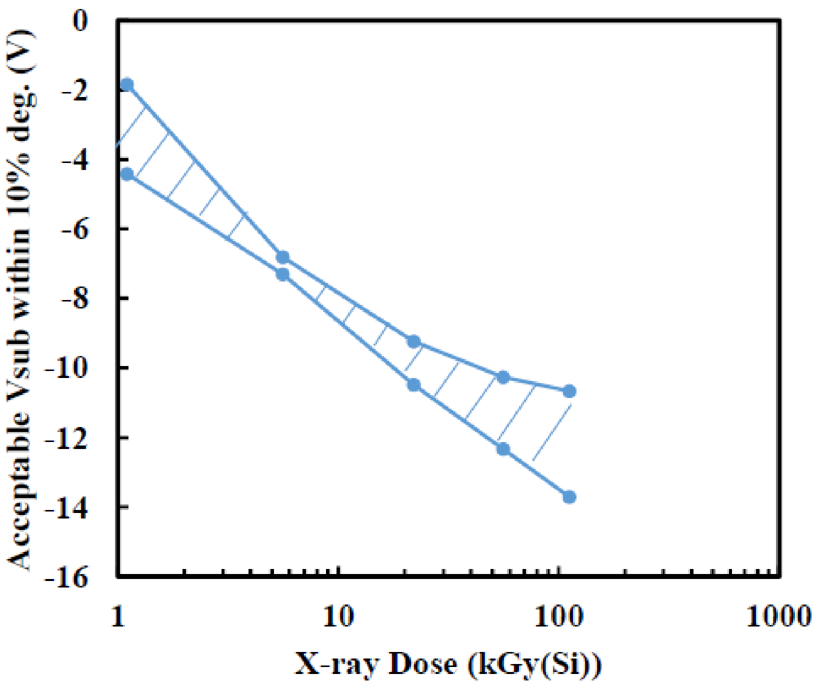


(by I. Kurachi)

Drain Current Change Compensation by Applying Vsub

- Required Vsub to recover drain currents are different between NMOS and PMOS.
- Even though, Vsub to make drain current change within 10% for NMOS and PMOS with L=0.2-10 mm up to 100 kGy exists.
- Compensation of BOX charge by applying Vsub may be the best way to improve radiation hardness to MGy range even for FD-SOI MOSFET.





Dose Rate : 3 Gy(Si)/s

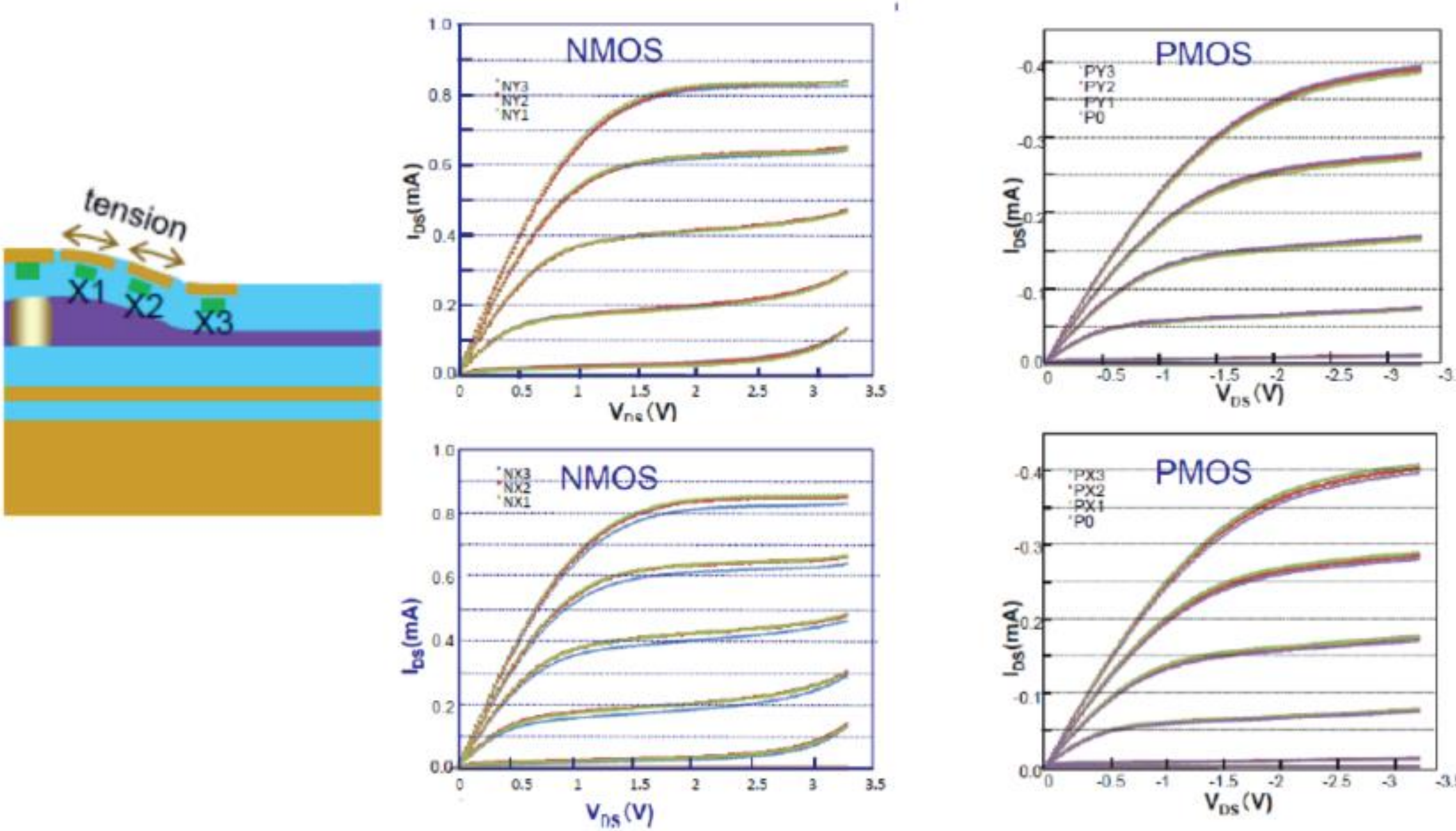
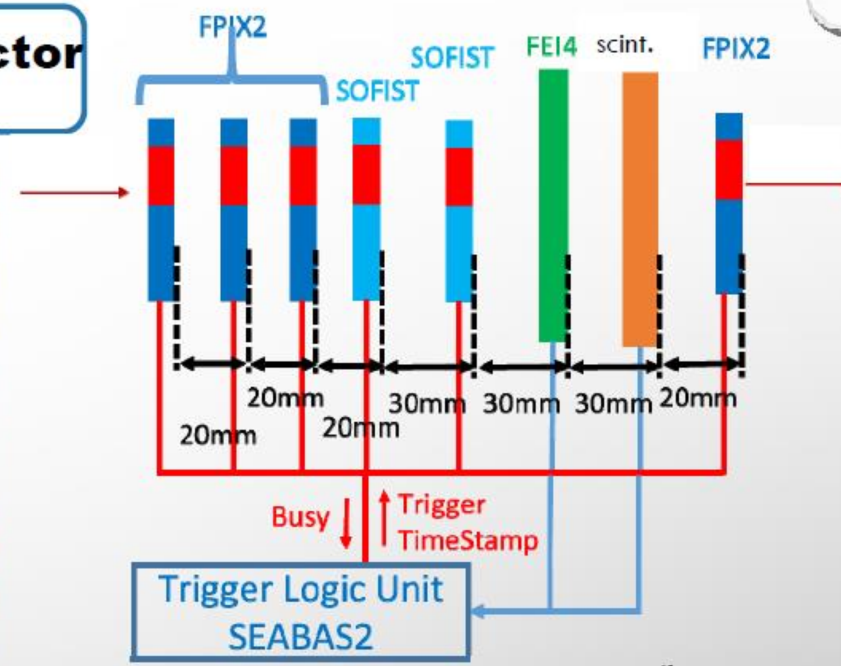


Figure 10. I_{DS}-V_{DS} characteristics of the NMOS/PMOS transistors.

FNAL TEST BEAM

FTBF: 120GeV protons from Main Injector
4.2s beam spill every 1 minute



R.Nishimura et al. "high speed DAQ system..."

- **Trigger generated by a SEABAS2 board using Scint.(5mm-sq) and ATLAS FE-I4 (2mmx1.75mm ROI)**
- **Data of 4 FPIX2 and 2 SOFIST sensors acquired per TLU request.** DAQ~1.2k/spill
  All R/O boards (SEABAS2) implemented with same TimeStamp firmware
- **Last FPIX2 made accessible for exchanging to irradiated DSOI**

SEABAS2(Soi EvAluation BoArd with Sitcp): 16ch 12bit 40MHz ADCs, Giga-bit Ethernet

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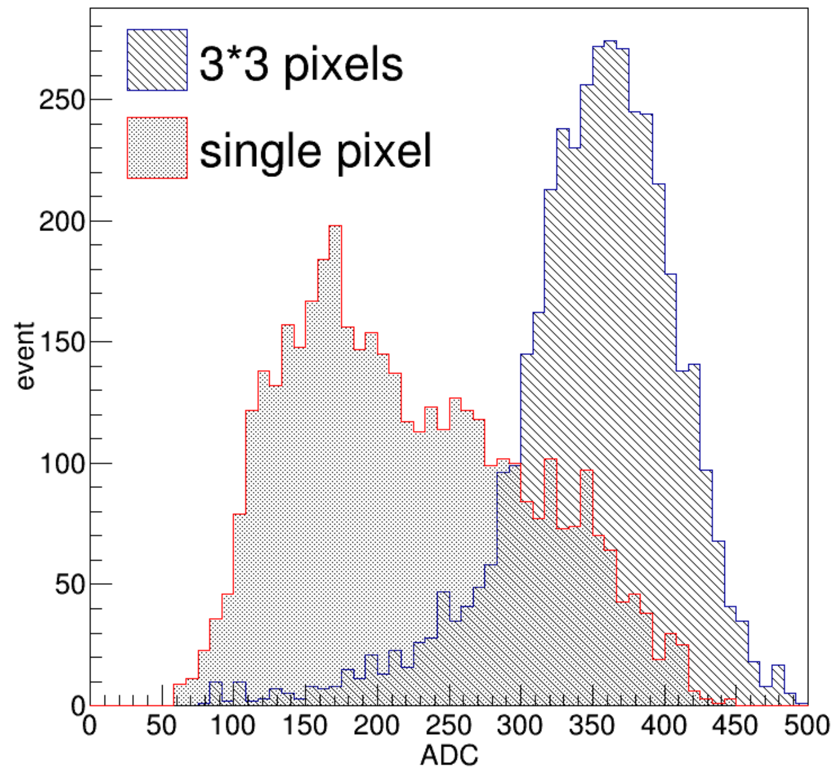
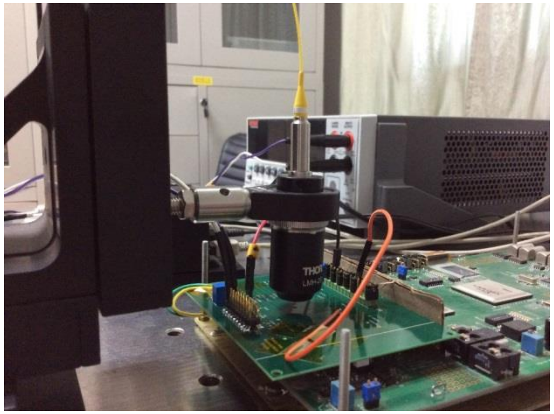
Analog pixel calibration

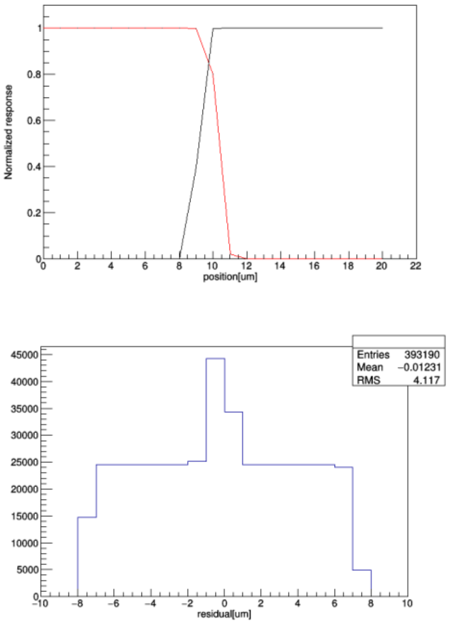
- ^{55}Fe radiative source 5.9 keV peak
- CVF = 123.3uV/e^-



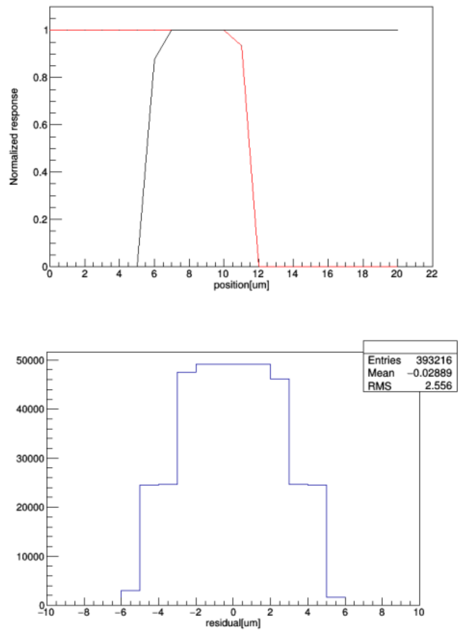
Infrared laser test

- Focused infrared laser beam
  - 1064nm wavelength to simulate MIP track
  - Micro-focused beam waist 3.4um
  - Adjustable pulse energy ~pJ
- Pixel response and position residual measured
  - With a step size 1 um
  - With beam intensity tuned to change the signal charge

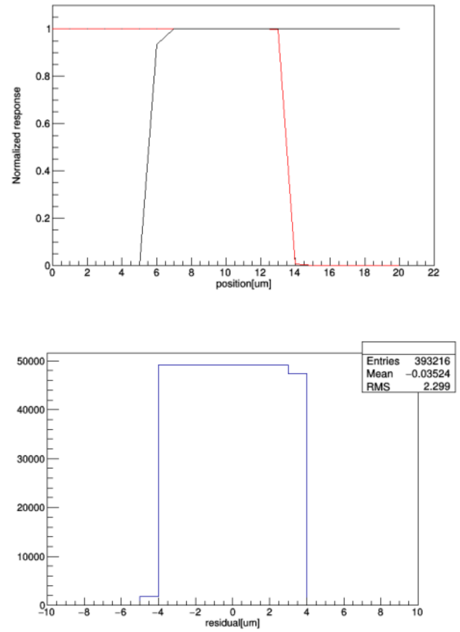




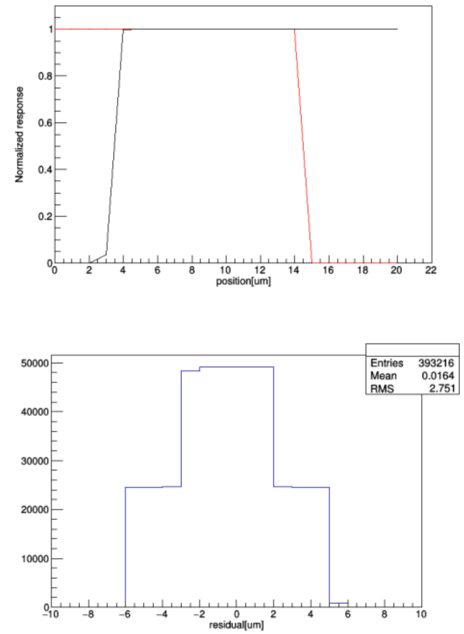
signal charge ~ 1600e⁻



signal charge ~ 2300e⁻



signal charge ~3200e⁻



signal charge ~ 4700