环形正负电子对撞机
Circular Electron Positron Collider

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Pixel sensor prototypes design for CEPC vertex detector

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On behalf of the CEPC VTX study group

12-13 October 2017, NME'2017, IHEP, Beijing

Outline

- **Introduction on CEPC vertex detector**
- **R&D activities**
  - CMOS pixel sensor
  - SOI pixel sensor
- **Summary and outlook**

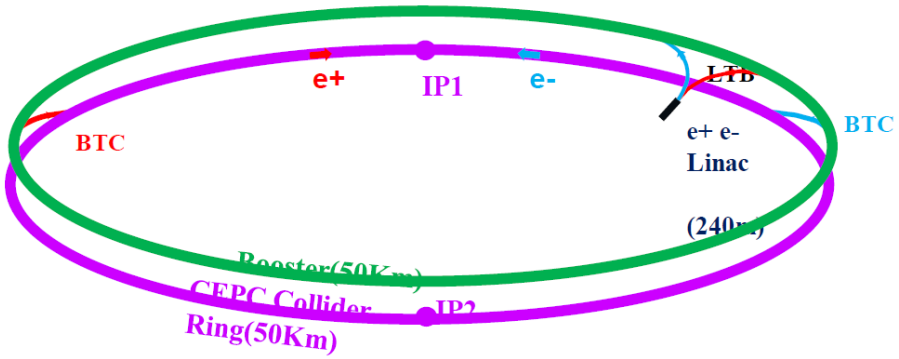
Introduction

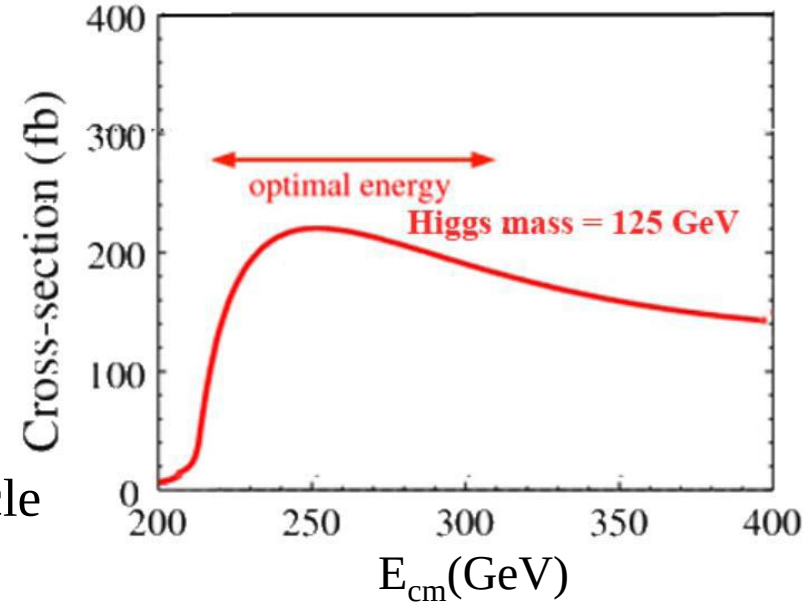
CEPC – SppC

- **Phase 1: e^+ e^- Higgs [Z] factory two detectors, 1M H events in ~10yrs**

  Circular Electron Positron Collider (CEPC)

  - **E_{cm} ≈ 240 GeV, luminosity ~2×10^{34} $cm^{-2}s^{-1}$, can also run at the Z-pole**
  - **Precise measurement of the Higgs boson and the Z boson**
- **Phase 2: a discovery machine for new physics; pp collision with E_{cm} ≈ 50-100 TeV Supper proton-proton Collider (SppC)**

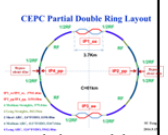
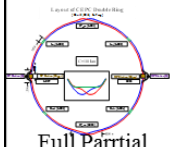




CEPC – possible accelerator based particle physics program in China after BEPCII

Ref: CEPC-SppC workshop, X. LOU, Sep. 2, 2016, Beijing, China.

CEPC accelerator layout option comparison

Option	Pretzel	Sawtooth effect	Beam loading	Dynamic Aperture	Orbit Correction	H luminosity	Z-pole luminosity	AC power	SRF syetem compatible for H and Z
Pre-CDR Baseline  Single Ring (SR)	Yes ★	Very high ★	Low ★★★★★	Very small ★	Very hard ★	Low ★★★	Very low ★	High ★	Difficult ★★★
 Partial Double Ring（PDR）	No ★★★★★	High ★★	Very High ★	Medium ★★★	Hard ★★	Medium ★★★	Medium ★★★	Low ★★★★★	Difficult ★★★
 Advanced Partial Double Ring （APDR）	No ★★★★★	High ★★★	High ★★★	Medium ★★★	Medium ★★★	Medium ★★★	High ★★★★	Low ★★★★★	Difficult ★★★
CDR Baseline  Full Parrtial Double Ring （FPDR）	No ★★★★★	Vey Low ★★★★★	Low ★★★★★	Large ★★★★★	Easy ★★★★★	High ★★★★★	Very High ★★★★★	Low ★★★★★	Very good ★★★★★

Ref: J.Gao, Circular Electron Positron Collider workshop, Wuhan, April 19-21, 2017.

Physics driven requirements

Table 2.1 Required performance of the CEPC sub-detectors for critical benchmark Higgs processes.

Physics Process	Measured Quantity	Critical Detector	Required Performance
$ZH \to \ell^+\ell^- X$	Higgs mass, cross section	Tracker	$\Delta(1/p_{\mathrm{T}}) \sim 2 \times 10^{-5}$
$H \to \mu^+\mu^-$	BR($H \to \mu^+\mu^-$)		$\oplus 1 \times 10^{-3}/(p_{\mathrm{T}} \sin\theta)$
$H \to b\bar{b},\ c\bar{c},\ gg$	BR($H \to b\bar{b},\ c\bar{c},\ gg$)	Vertex	$\sigma_{r\phi} \sim 5 \oplus 10/(p \sin^{3/2}\theta)\ \mu$m
$H \to q\bar{q},\ VV$	BR($H \to q\bar{q},\ VV$)	ECAL, HCAL	$\sigma_E^{\mathrm{jet}}/E \sim 3-4\%$
$H \to \gamma\gamma$	BR($H \to \gamma\gamma$)	ECAL	$\sigma_E \sim 16\%/\sqrt{E} \oplus 1\%$ (GeV)

- **Efficient tagging of heavy quarks (b/c) and τ leptons**

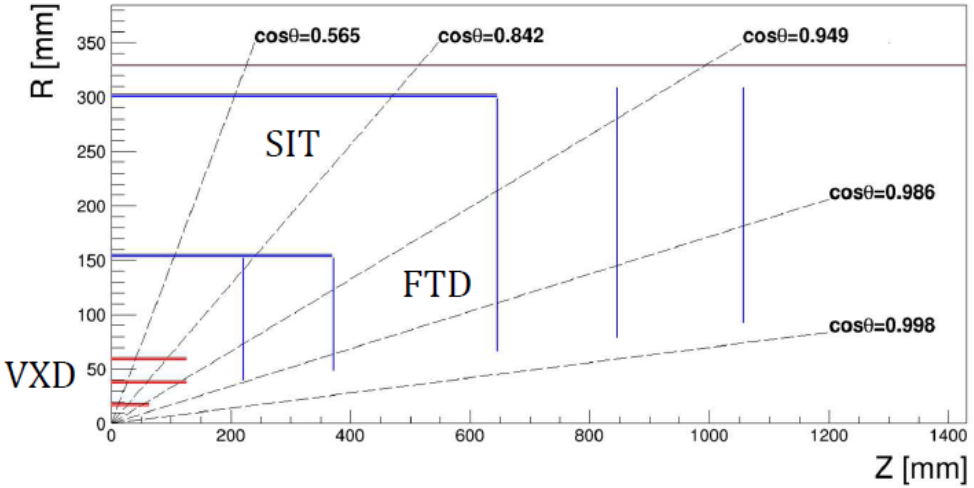
  ➔ Impact parameter resolution, $\sigma_{r\phi} = a \oplus \frac{b}{(p \cdot sin^{3/2}\theta)}\ \mu m$

- **Design constrains on vertex (to achieve a=5 and b=10, B=3.5T)**
  - spatial resolution near the interaction point $\sigma_{sp} \leq 3$ μm
  - material budget ≤ 0.15% X_0/layer
  - first layer located at a radius: ~1.6 cm

CEPC vertex detector concept

Baseline design for the pre-CDR: ILD-like but different forward region design

- 3 layers of double-sided pixels
- σ_{SP} = 2.8 μm, inner most layer
- readout time < 20 μs



VXD Geometry

	R (mm)	|z| (mm)	$\|\cos\theta\|$	σ_{SP} (μm)	Readout time (μs)
Layer 1	16	62.5	0.97	2.8	20
Layer 2	18	62.5	0.96	2.8	20
Layer 3	37	125.0	0.96	4	20
Layer 4	39	125.0	0.95	4	20
Layer 5	58	125.0	0.91	4	20
Layer 6	60	125.0	0.90	4	20

Beam induced backgrounds

Results of the Single Ring Scheme

Background Type	Generators	Sub-type	Particle Flux at VTX $[cm^{-2}BX^{-1}]$	Particle Energy [GeV]	Priority
Synchrotron Radiation	*Geant4; BDSIM*	*Dipole*	~ 10^{10}	~ 0.001	★★★
		Quadrupole	~ 10^{6}	~ 0.007	
Beam Lost Particles	*BBBrem; SAD*	*Radiative Bhabha*	~ 10	~ 120	★★
		Beam Gas Scattering	↑	↑	
Beamstrahlung	*Guinea-Pig++; PYTHIA6*	*Pairs*	~ 10^{-2}	~ 0.05	★
		Hadrons	~ 10^{-5}	~ 2	

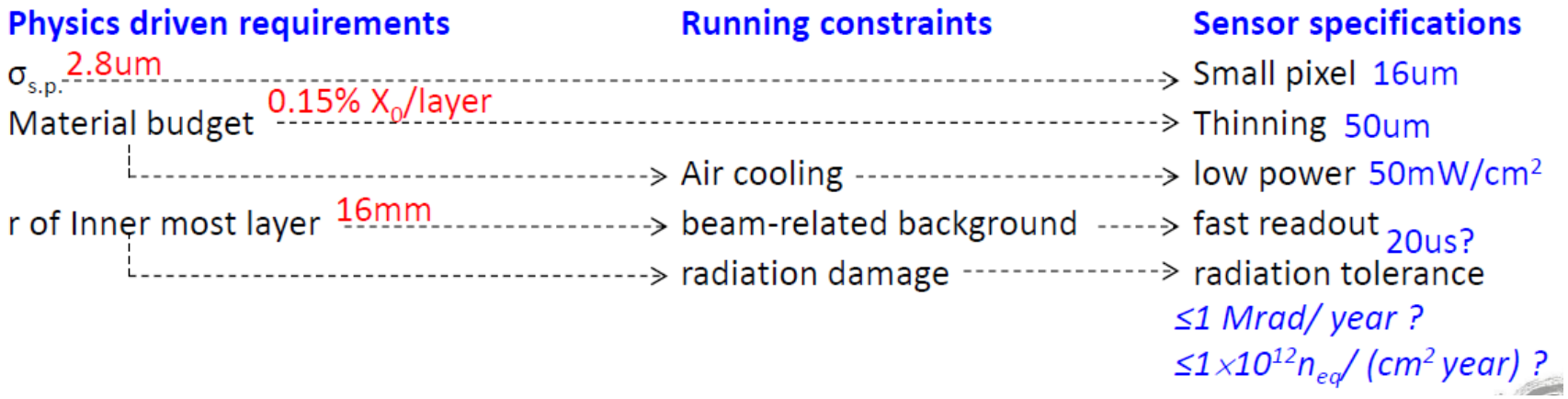
- The synchrotron radiation is the most important beam induced backgrounds in the single ring scheme
  - Require to reduce the critical energy and radiation power in the double ring scheme

2017-4-20 CEPC-SPPC Workshop, CCNU, Wuhan 3

Ref: Q. Xiu, Circular Electron Positron Collider workshop, Wuhan, April 19-21, 2017.

Pixel sensor challenges

- To achieve S.P. resolution
  - Digital pixel ~ 16um
  - Analog pixel ~ 20um (power pulsing mode in ILC)
- To lower the material budget
  - Sensor thickness ~ 50um
  - Heat load < 50 mW/cm^2 constrained by air cooling
- To tackle beam-related background
  - 20us/frame?
  - 300krad/year & 3×10^{12}neq/ (cm^2·year)?



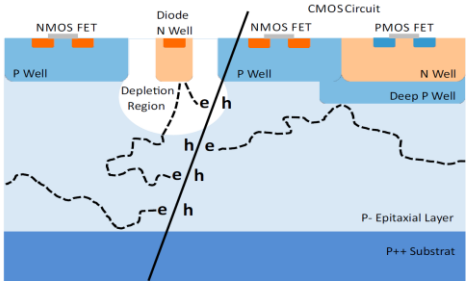
Ref: Y. Lu, Circular Electron Positron Collider workshop, Wuhan, April 19-21, 2017.

R&D activities

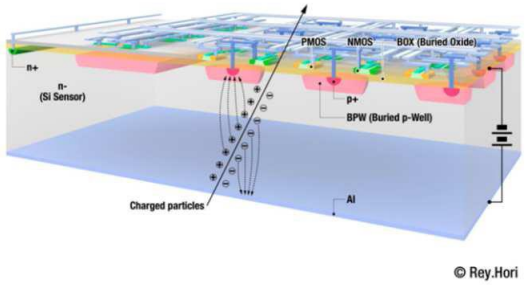
Pixel sensor R&D activities

Unprecedented specifications

- Severer low power constraint than ILD
  - ILD duty cycle 1ms/199ms
  - CEPC needs a reduction by a factor of 4
- Higher s.p. resolution than ALICE-ITS upgrade
  - 1/3 pixel size of ALICE pixel sensor



- **HR-CMOS pixel sensor**
  - Towards compete CMOS & thick, fully depleted substrate
  - More in-pixel functional circuitry → faster read-out & less power, radiation tolerance
  - TowerJazz CIS 0.18 μm process
- **SOI pixel sensor**
  - Fully depleted substrate: 50 μm thick, larger signal charge
  - Develop in-pixel circuit for minimum layout area
  - LAPIS 0.2 μm process

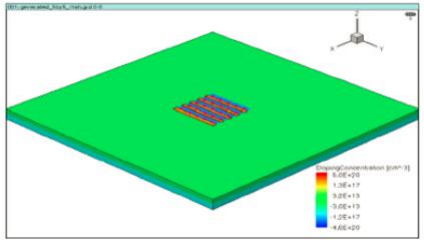


R&D activities

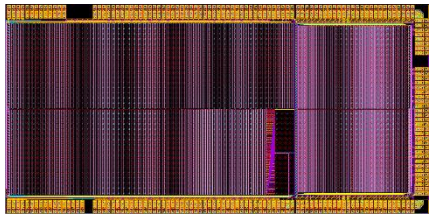
- **CMOS pixel sensor**
- **SOI pixel sensor**

CMOS pixel sensor R&D activities

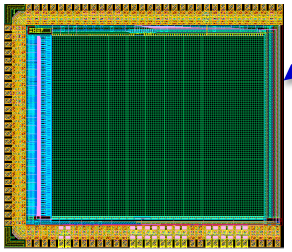
- **TCAD simulation on charge collection**

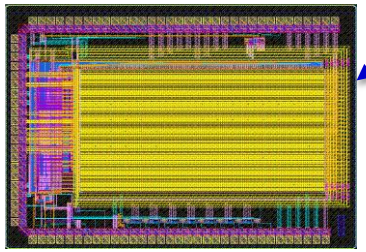


- **First submission in Nov. 2015**
  - Exploratory prototype, analog pixel
  - Sensor optimization and radiation tolerance study



- **Second submission in May 2017**
  - Tow prototypes with digital pixels (in-pixel discriminator)
  - Tow different readout schemes: rolling shutter & asynchronous





CPS – Charge collection simulation

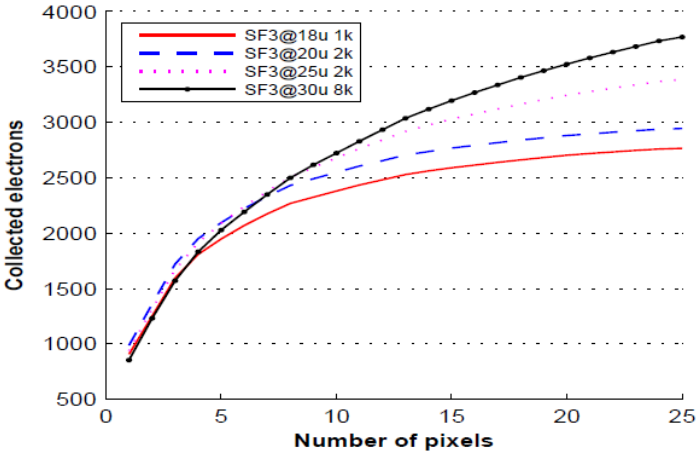
Y. ZHANG et al., NIMA 831 (2016) 99-104

Motivation:

- Guide the diode geometry optimization and study radiation damage with different types of epitaxial layer

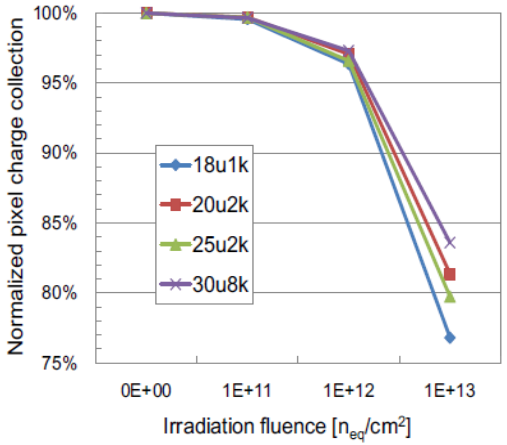
Simulated with different parameters

- Hit position
- Diode geometry
- Thickness and resistivity of the epitaxial layer
- Radiation damage

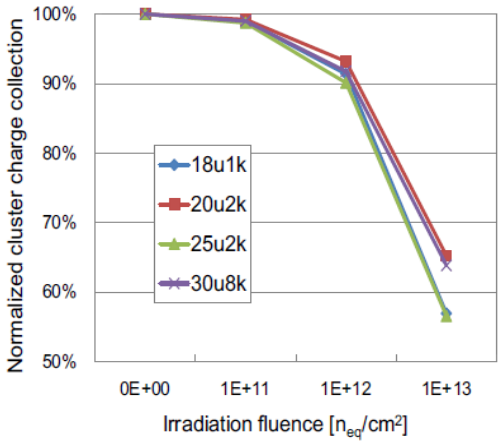


Pixel cluster charge with different epitaxial layers

Seed pixel



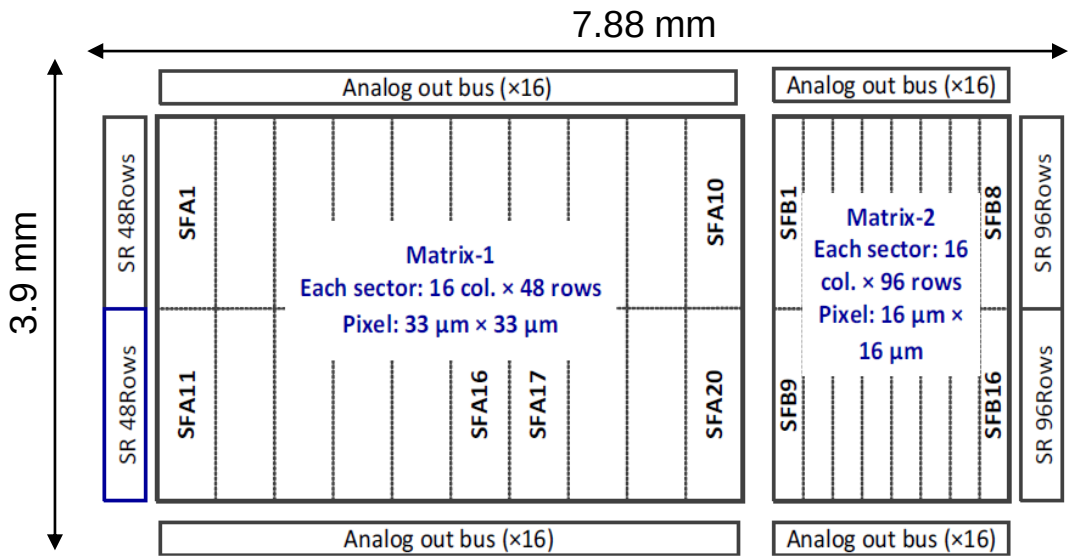
5 × 5 cluster



Charge collection with non-ionizing damage

First CPS prototype design

- **Goals：sensing optimization and in-pixel pre-amplifier study**
- **Floorplan overview**
  - Two independent matrices: Matrix-1 with 33 × 33 μm^2 pixels (except one sector SFA20 with 16×16 μm^2 pixels), Matrix-2 with 16×16 μm^2 pixels.
  - Matrix-1 includes 3 sectors with in-pixel pre-amplifier
  - SFA20 in Matrix-1 contains pixel with AC-coupled pixels

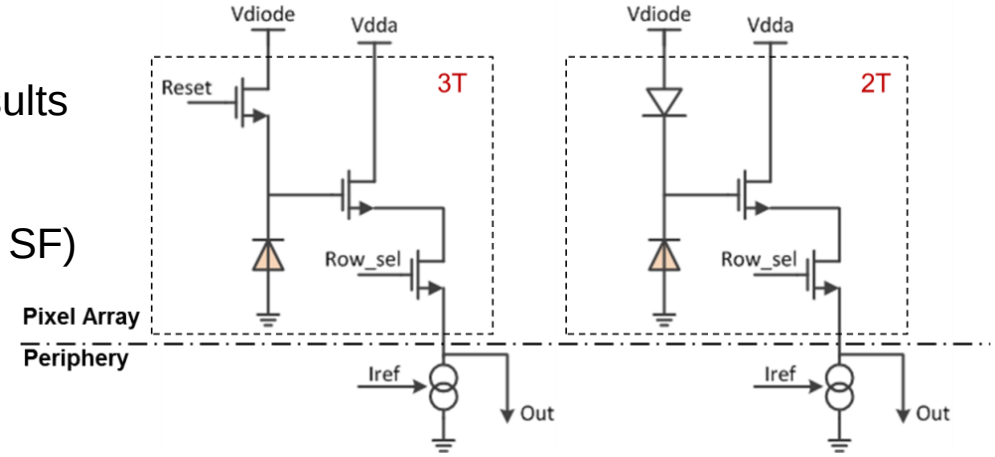


- TowerJazz 0.18 μm CIS process November 2015 submission
- Chip received in 2016 June, test in progress

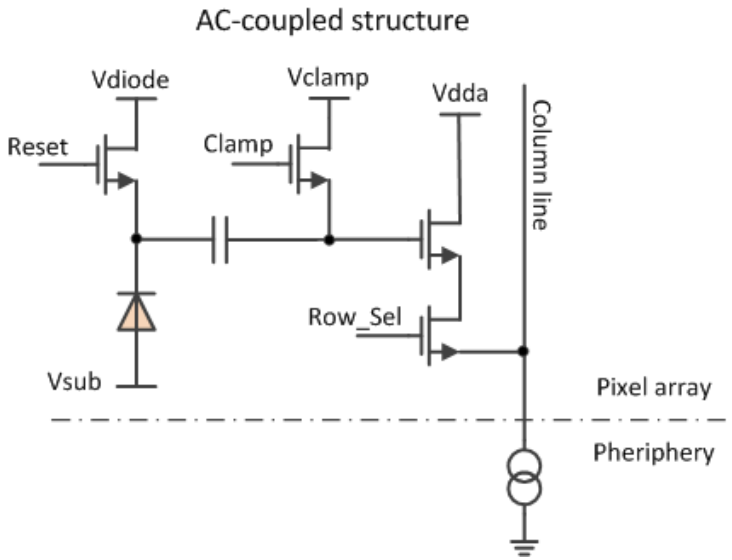
First CPS prototype design — pixel structures

Y. ZHANG, Y. ZHOU (IHEP)

- **DC-coupled SF pixels: 2T/3T structure**
  - different diode geometries
  - ➔ to verify the TCAD simulation results
  - two biasing modes (2T/3T)
  - two transistor types (nmos/pmos SF)



- **AC-coupled pixel**
  - sensing node AC-coupled with circuit
  - diode bias voltage could be higher than power supply, i.e. up to 10 V
  - ➔ **larger depletion region & lower Cd**
  - ➔ **higher SNR**



First CPS prototype design — pixel structures

Y. ZHANG (IHEP)

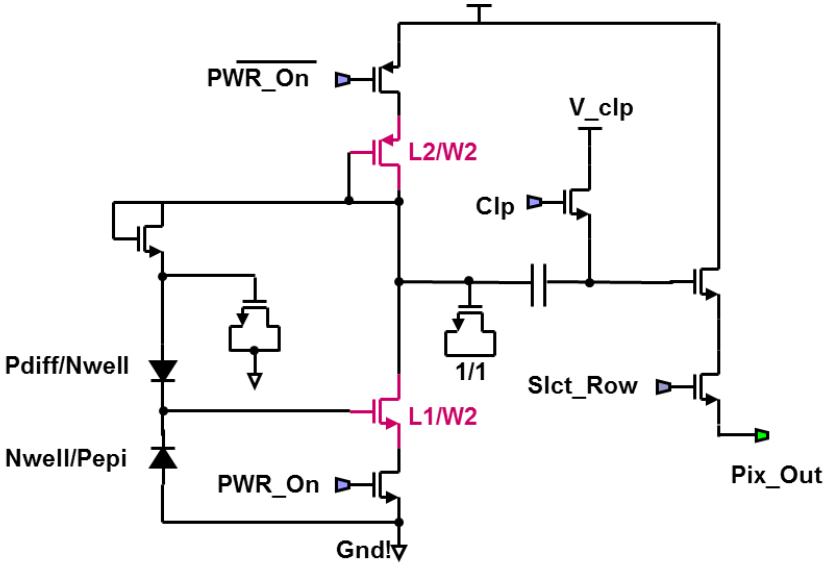
- **In-pixel pre-amplifier**
  - Common source amplifier with AC feedback, CDS in pixel
  - Only active when the row is selected to be read → power saving
  - Using a twin-well process only NMOS can be used, **while both types of transistors are used in our prototype**

Trade-off between :

✓ *Noise (TN, 1/f, RTS)*

✓ *PSRR*

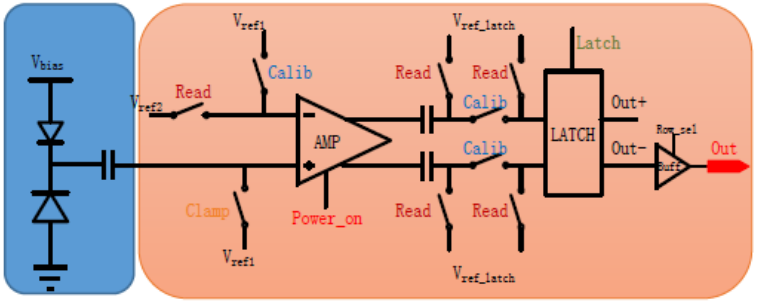
✓ *Diode Bias Voltage*



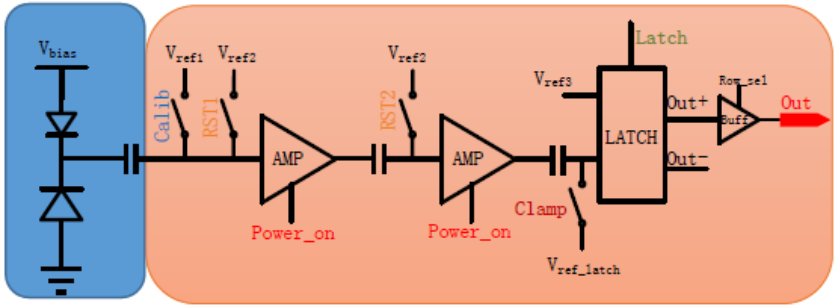
2nd submission – rolling shutter prototype

Y. ZHOU (IHEP)

Digital pixels in rolling-shutter readout mode: 2 different versions

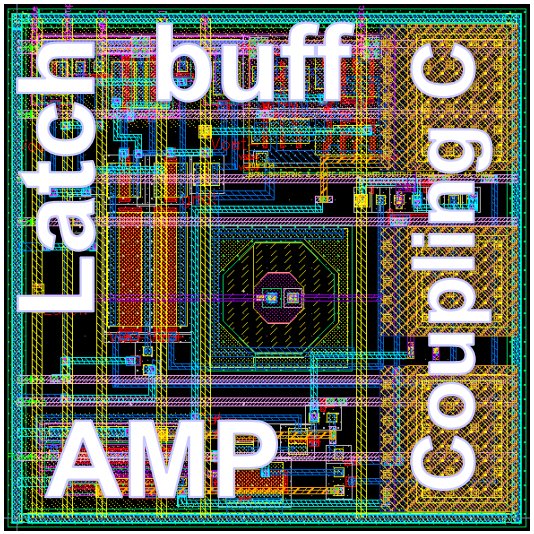


Version 1: differential amplifier + latch

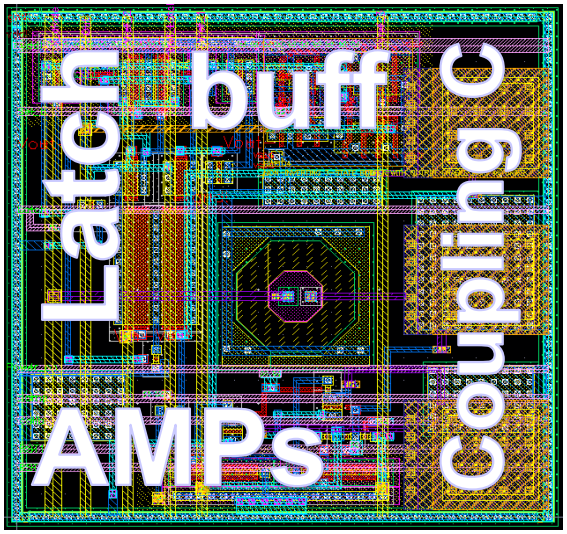


Version 2: two stage CS amplifiers + latch

Pitch size: 22 μm



- Same amount of transistors;
- Offset cancellation technique;
- Version 2 has higher signal gain, but suffers "more" from "Latch" input voltage distortion.

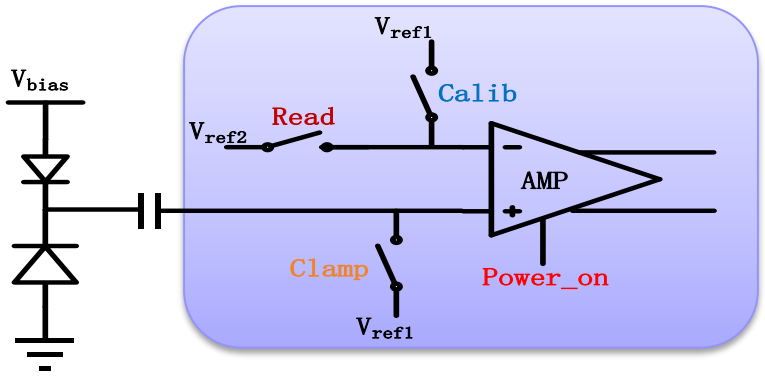


Pitch size: 22 μm

2nd submission – rolling shutter prototype

Y. ZHOU (IHEP)

- **Version 1:**



Differential Amplifier Noise simulation:

Input DC level: 600 mV

Biasing current: 3.7 μA

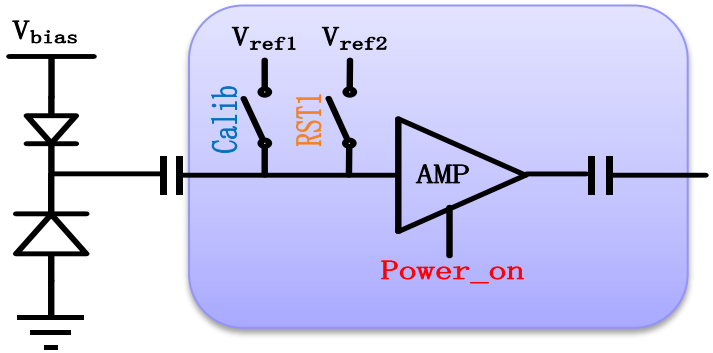
Gain: 8.3

RMS noise: 1.962 mV

ENC: ≈ 7 e^- (for best case; highly relaied on the equivalent $C_{sensing\ point}$)

Readout speed: **100 ns/row**

- **Version 2:**



Single-end CS Amplifier Noise simulation:

Input DC level: 520 mV

Gain: 8

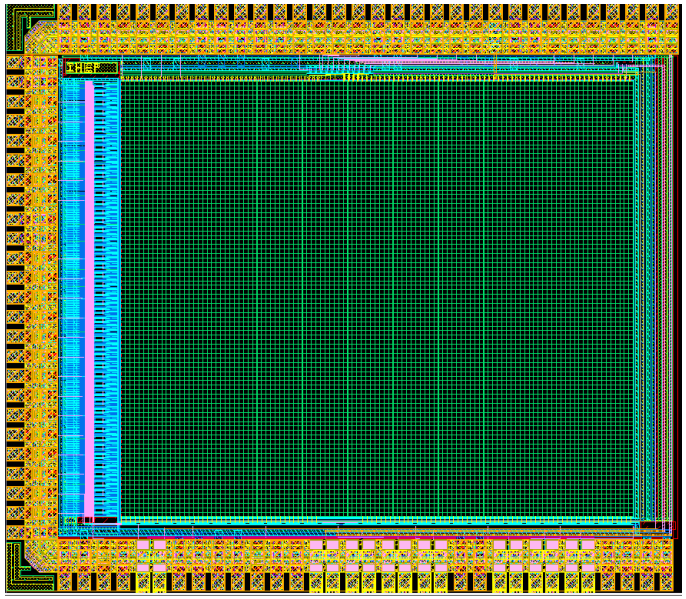
RMS noise: 1.566 mV

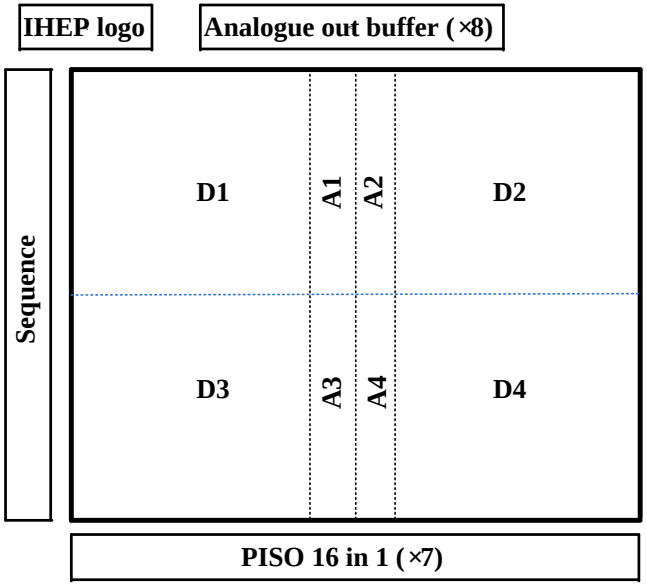
ENC: 6.3 e- (for best case)

Readout speed: **80 ns/row**

2nd Submission: rolling-shutter mode prototype

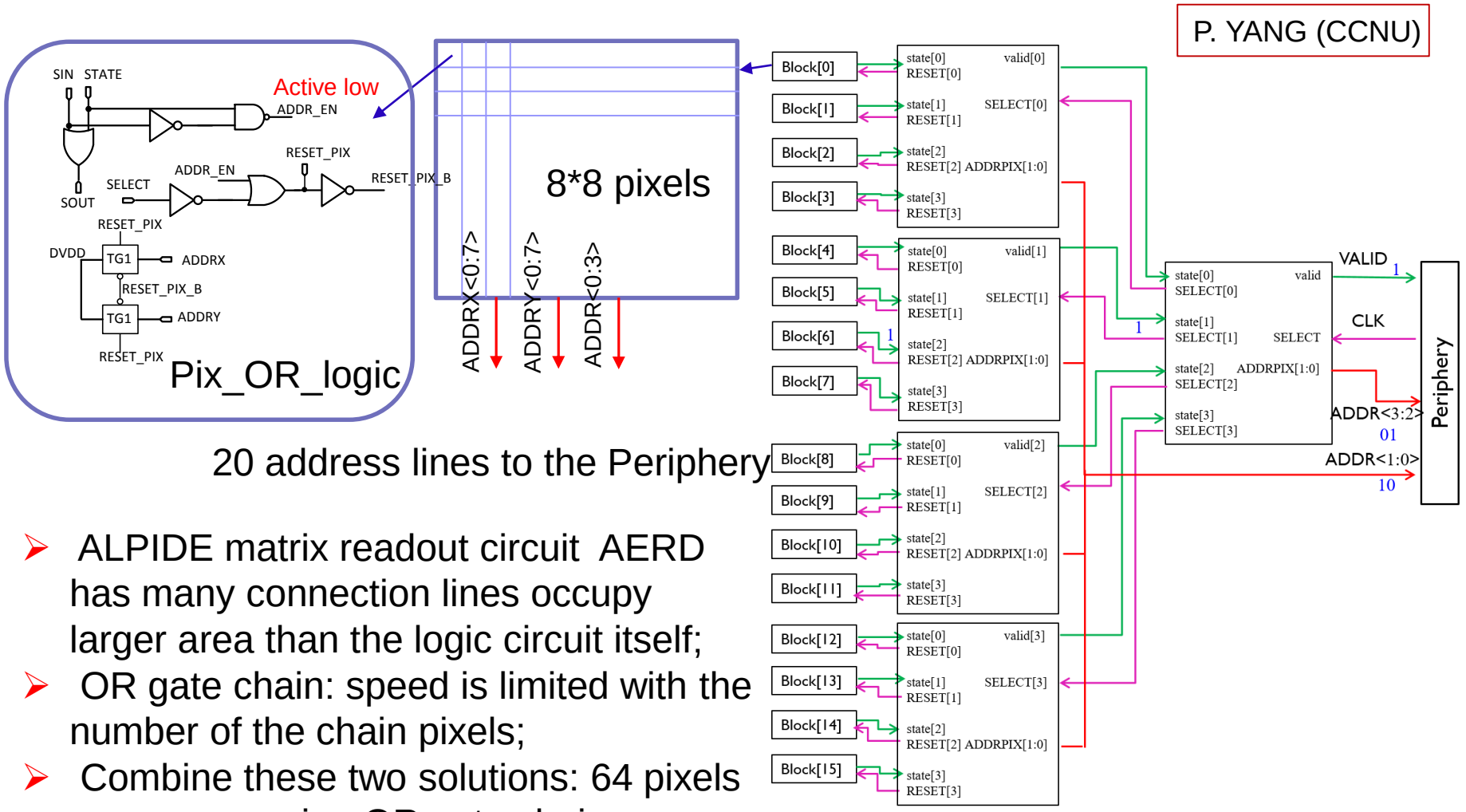
Y. ZHOU (IHEP)





- *3 × 3.3 mm²;*
- *96 × 112 pixels with 8 sub-matrix*
- Processing speed: 11.2 μs/frame for 100 ns/row;
- Output data speed: 160 MHz;
- Power:3.7 μA/pixel;

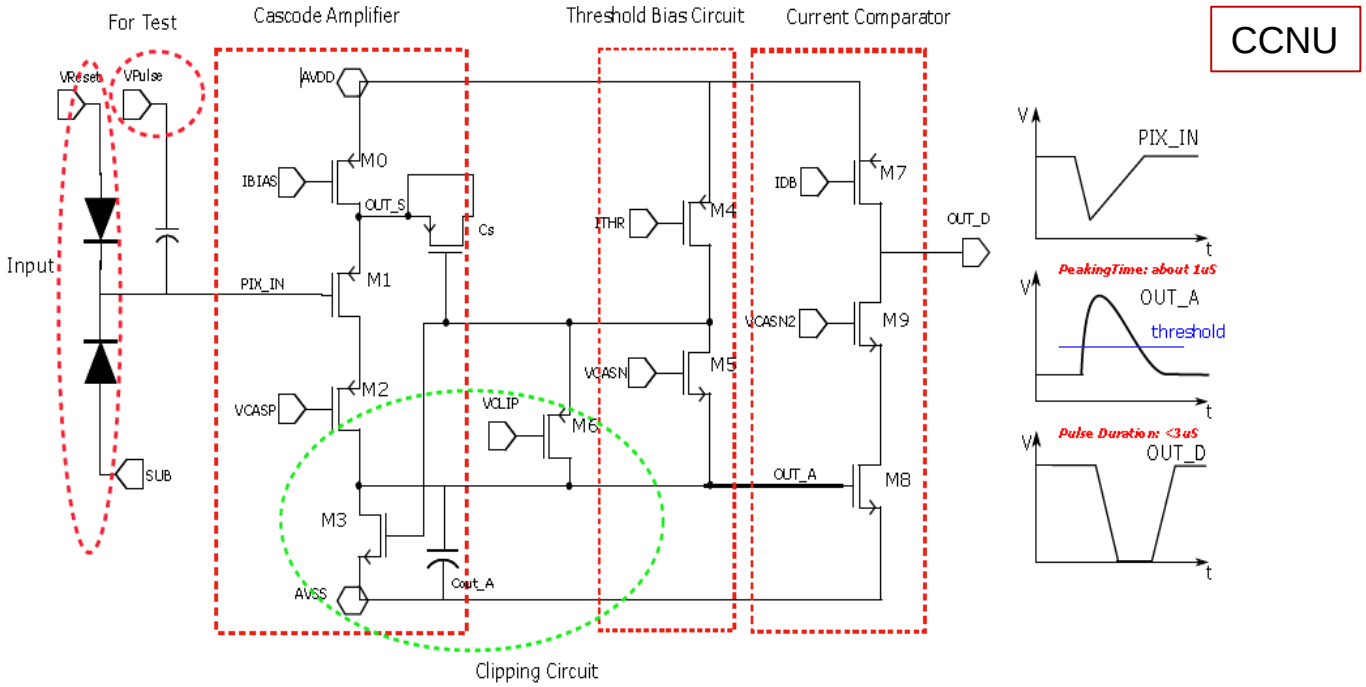
2nd Submission: asynchronous mode prototype



20 address lines to the Periphery

- ALPIDE matrix readout circuit AERD has many connection lines occupy larger area than the logic circuit itself;
- OR gate chain: speed is limited with the number of the chain pixels;
- Combine these two solutions: 64 pixels as a group using OR gate chain, groups using AERD structure to readout

Asynchronous mode prototype – front-end I



- Signal charge creates negative voltage step ΔV_{PIX_IN} at input node(PIX_IN).
- From OUT_A baseline voltage to point where discriminated output OUT_D flips when $I_{M8} > I_{DB}$.

$$\Delta V_{OUT\_A} \approx \frac{C_s \bullet \Delta V_{PIX\_IN}}{C_{OUT\_A}} = \frac{C_s}{C_{OUT\_A}} \bullet \frac{Q_{in}}{C_{PIX\_IN}}$$

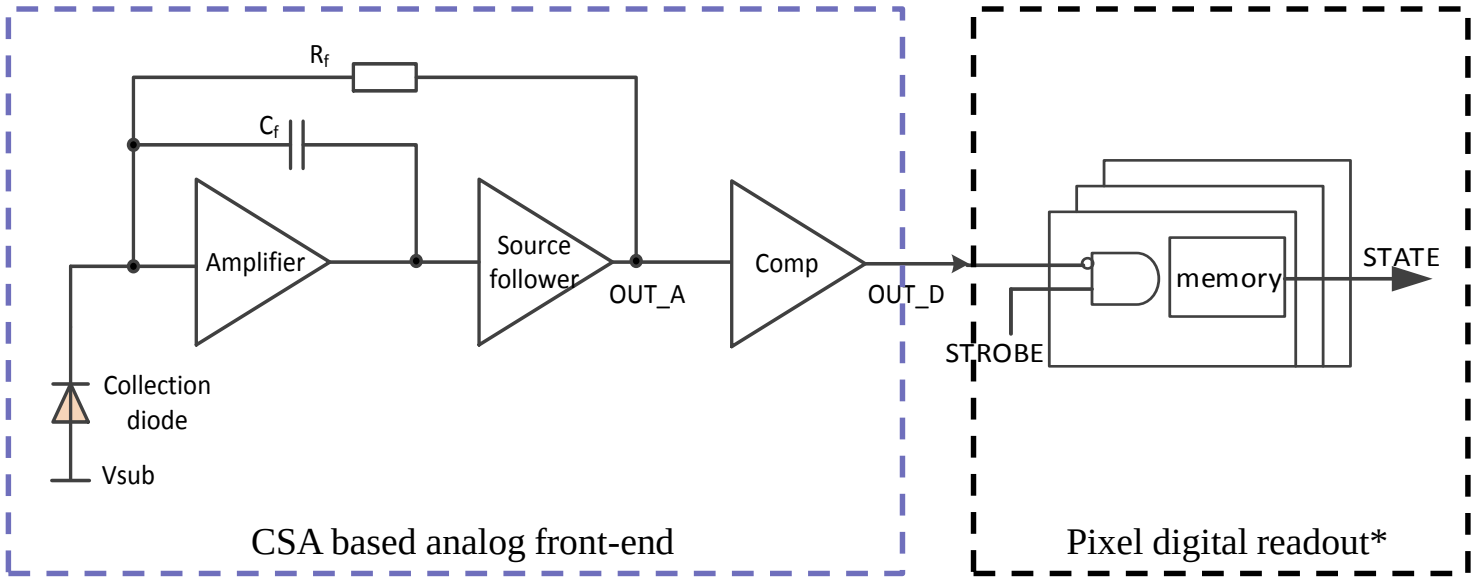
Simulation results

- ENC: 8 e^-
- Power cons.: 61 nA/pixel
- Threshold: 140 e^-
- Peaking time < 1 us
- Pulse duration < 3 μs

Asynchronous mode prototype – front-end II

Y. ZHANG (IHEP)

- **CSA based front-end circuit**
- **Signal process chain**
  - Pixel size: 25 × 25 μm^2

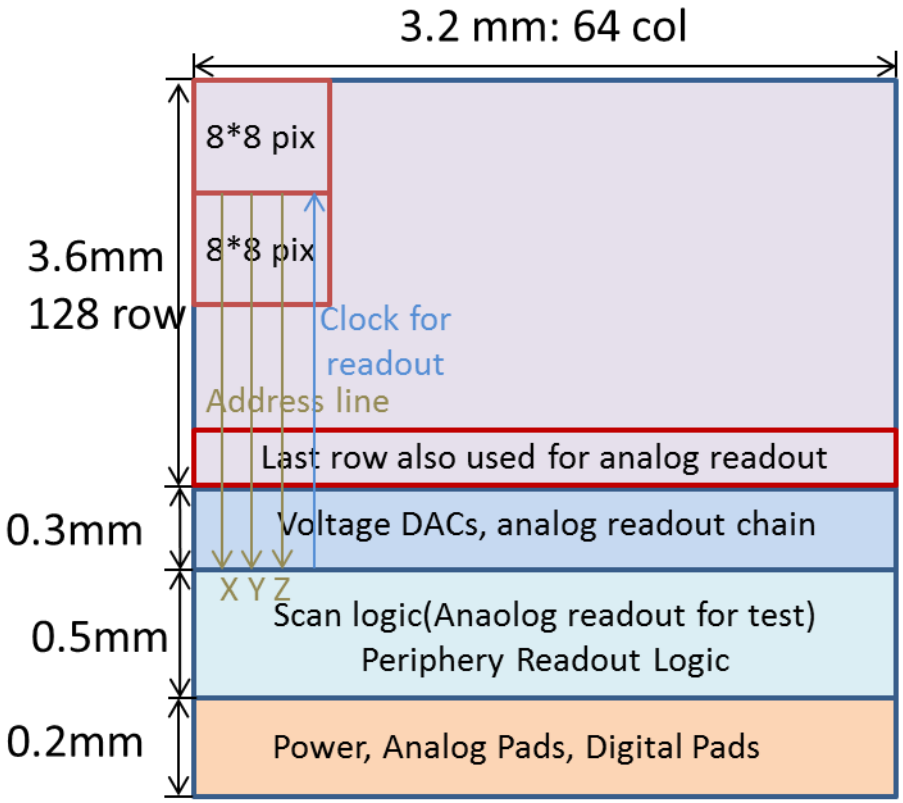


* Designed by Ping @ CCNU

Asynchronous mode prototype overview

- **MIC4 chip:**

P. YANG et al. (CCNU)



- 3.2 × 3.7 mm^2
- 128 × 64 pixels
- Integration time: < 5 μs
- Power consumption: < 80 mW/cm^2

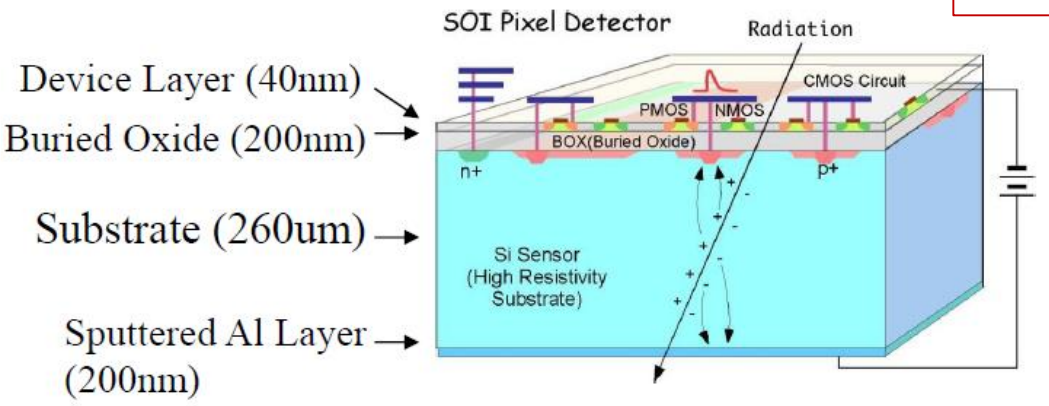
- Chip periphery
  - Band gap
  - Voltage DAC
  - Current DAC
  - LVDS
  - Custom designed PADs

R&D activities

- CMOS pixel sensor
- **SOI pixel sensor**

SOI pixel sensor R&D activities

Y. LU et al. (IHEP)



- **INTPIX2P5 prototype for the sensor depletion study, 2015**
  - Fully depleted around 190 V
  - Seed/cluster ration decrease with V_{bias}

- **CPV prototypes for CEPC**
  - CPV1/2, 2015/2016
  - Small pixel size, 16 μm pitch
  - Focus on Sensing diode + Front end
  - Digital pixel (in-pixel hit discrimination)

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A comparison of digital pixels

	ASTRAL	ALPIDE	CPV
Process technology	*0.18 μm* CMOS		0.2 *μm* SOI
Readout strategy	Rolling shutter	asynchronous	Rolling shutter
Readout time	20 μs	<2 μs	
Power	85 mW/cm^2	39 mW/cm^2	Analog power < 10 mW/cm^2
Pixel size	*22 × 33 μm^2*	*28 × 28 μm^2*	*16 × 16 μm^2*
Spatial resolution	*≈ 5μm*		Expected < 3*μm*
Total signal for MIP	*≈1200 e$^-$ (20μm* epi-layer partly depleted*)*		*≈4000 e$^-$* (back thinning to 50*μm*, fully depleted)

- Unique opportunity to explore very compact pixel circuit
  - 3 times larger MIP signal
  - Possibly smaller cluster size

Ref: Y. Lu, Circular Electron Positron Collider workshop, Wuhan, April 19-21, 2017.

First SOI pixel prototype

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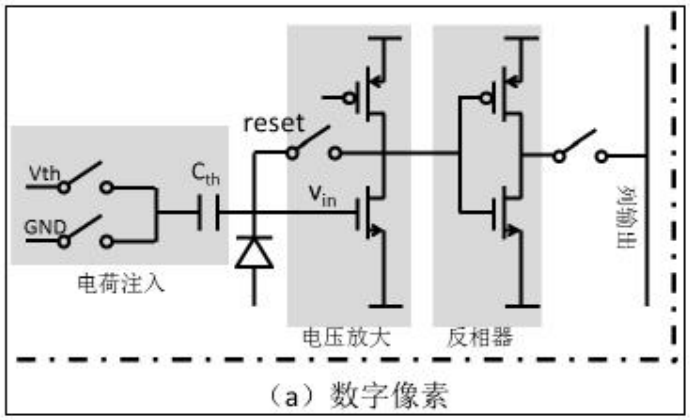
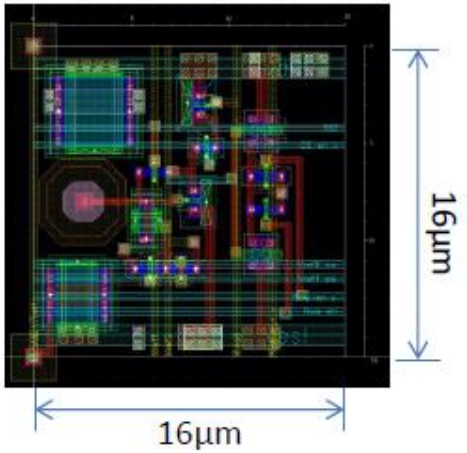
- First digital pixel of 16um pitch
- CS voltage amplifier, gain ~ 10
- Inverter as discriminator
- Threshold charge injected to sensing node
- Pixel array: 64*32 (digital) + 64*32 (analog)
- Double-SOI process for shielding and radiation enhancement
- Submitted June, 2015



CPV1 digital pixel



Ref: Y. Lu, Circular Electron Positron Collider workshop, Wuhan, April 19-21, 2017.

First SOI pixel prototype

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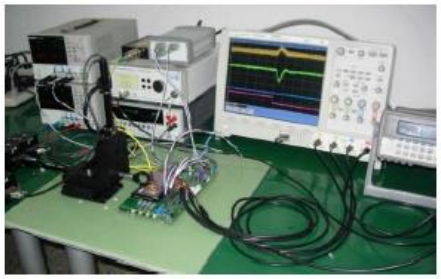
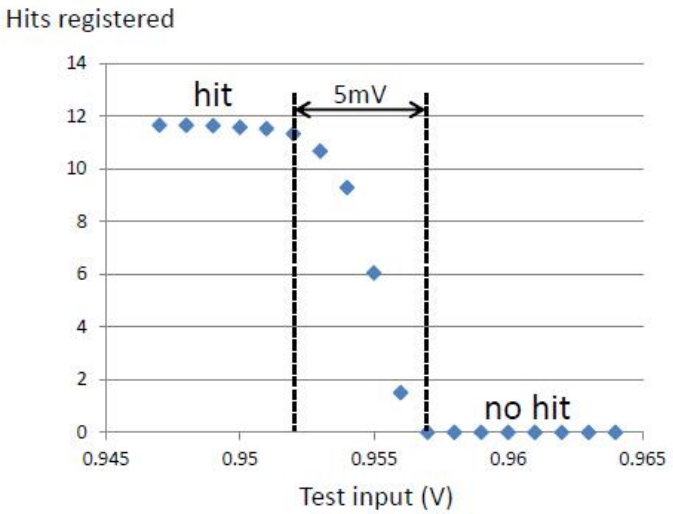
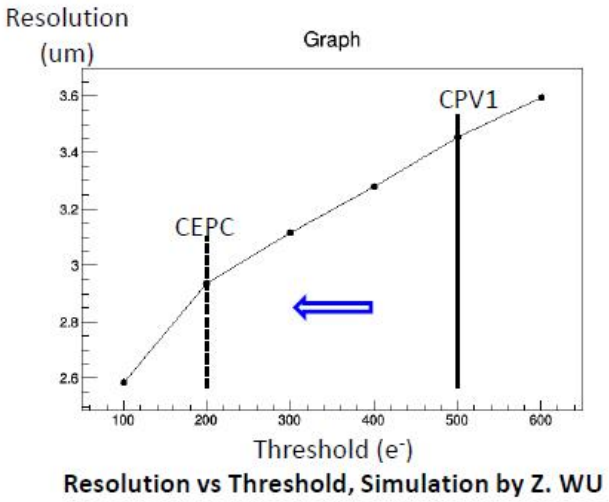
Single pixel test

- Chip circuit function verified on single pixel
  - Voltage gain of amplifier ~ 10
  - Threshold scan
  - Temporal noise ~ 50e$^-$ (< 20 e$^-$ expected)
- Bias voltage not applicable due to a design fault
  - Diode capacitance 3 times larger







Resolution vs Threshold, Simulation by Z. WU

Circular Electron Positron Collider Workshop, 2017.4.20, Wuhan 19

Ref: Y. Lu, Circular Electron Positron Collider workshop, Wuhan, April 19-21, 2017.

Second SOI pixel prototype design

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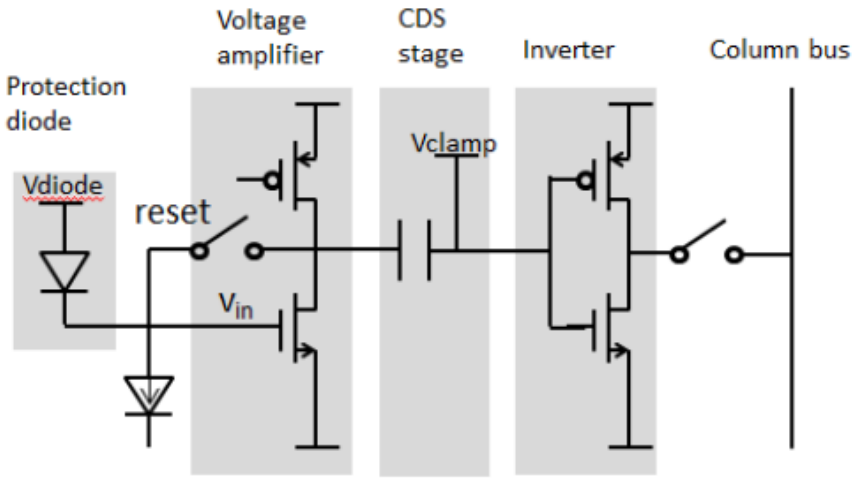
- Protection diode added
  - Enable full depletion on sensor
- In-pixel CDS stage inserted
  - improve RTC and FPN noise
  - replace the charge injection threshold
- Submitted June, 2016



Ref: Y. Lu, Circular Electron Positron Collider workshop, Wuhan, April 19-21, 2017.

Summary and outlook

- **Pixel sensor is the core component for VTX**
  - R&D started along the physics driven requirement
  - Running constraints not settle yet
- **CMOS pixel sensors prototypes**
  - Exploratory prototype under test
  - 2nd CPS submission under fabrication, targeting on highly compact digital pixels and fast readout development
- **Two compact SOI pixel sensor prototypes**
  - Fully depletion of SOI verified
  - Circuit function verified on single pixel
  - Evaluation of digital pixel array underway
- **Optimization study of vertex system needed**
- **Possible change of sensor design**
  - Beam related background level
  - Impact of partial-double ring scheme, with time-stamp of microsecond

Thanks for your attention !