TDC ASIC Design for MDT in ATLAS Phase II Upgrade

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in cooperation with University of Michigan

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Content

- Basic structure of the MDT readout electronics
- Structure of the first version TDC ASIC prototype
- Testing of the prototype TDC
- Design consideration of the second version
- conclusion

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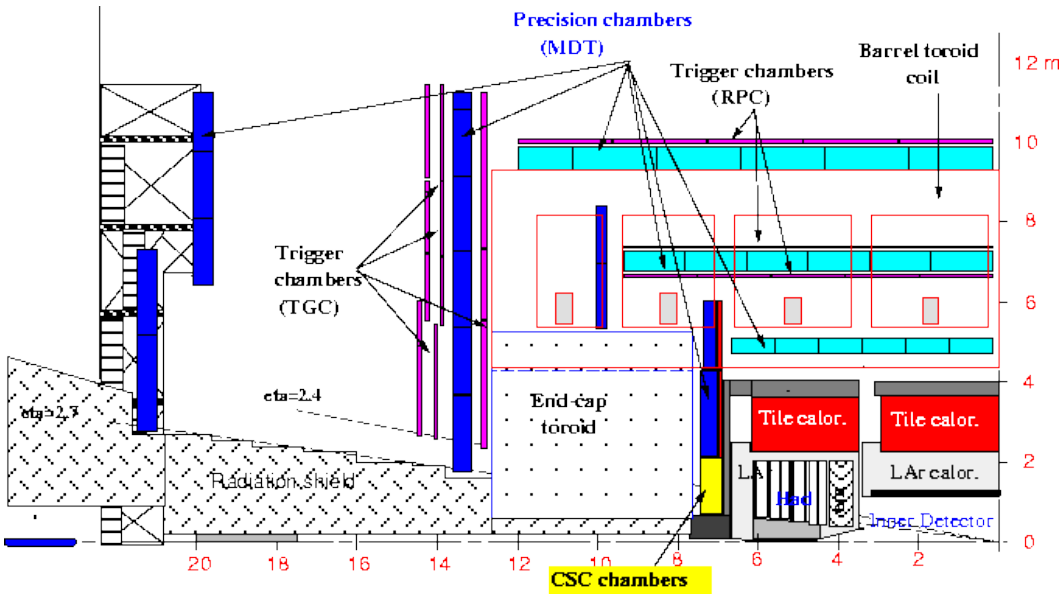
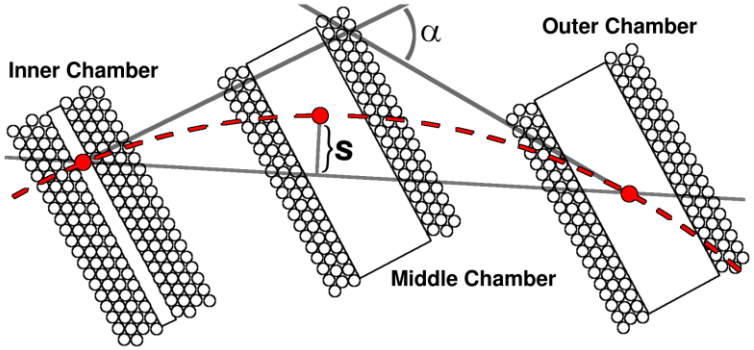
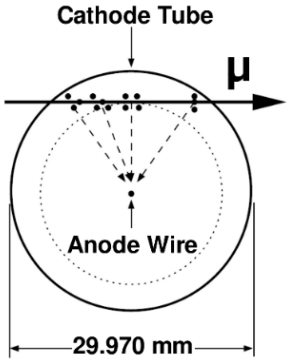
ATLAS MDT detector

- ATLAS muon spectrometer is mainly used for muon triggering, identification and momentum measurement
- Provide a standalone momentum measurement (10% at 1 TeV), mainly by the monitored drift tube (MDT) chambers
- 1150 chambers with 354k tubes covering an area of 5500 m^2



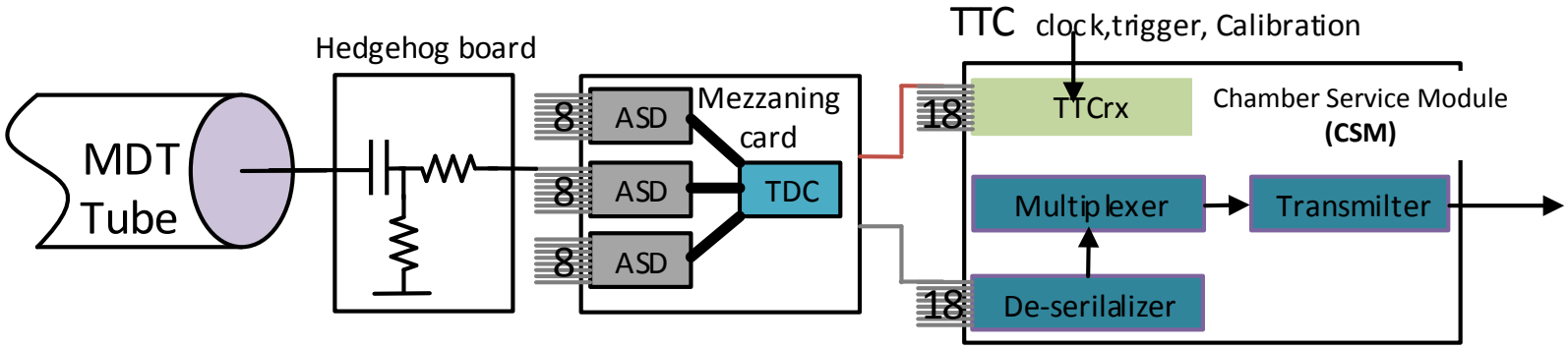


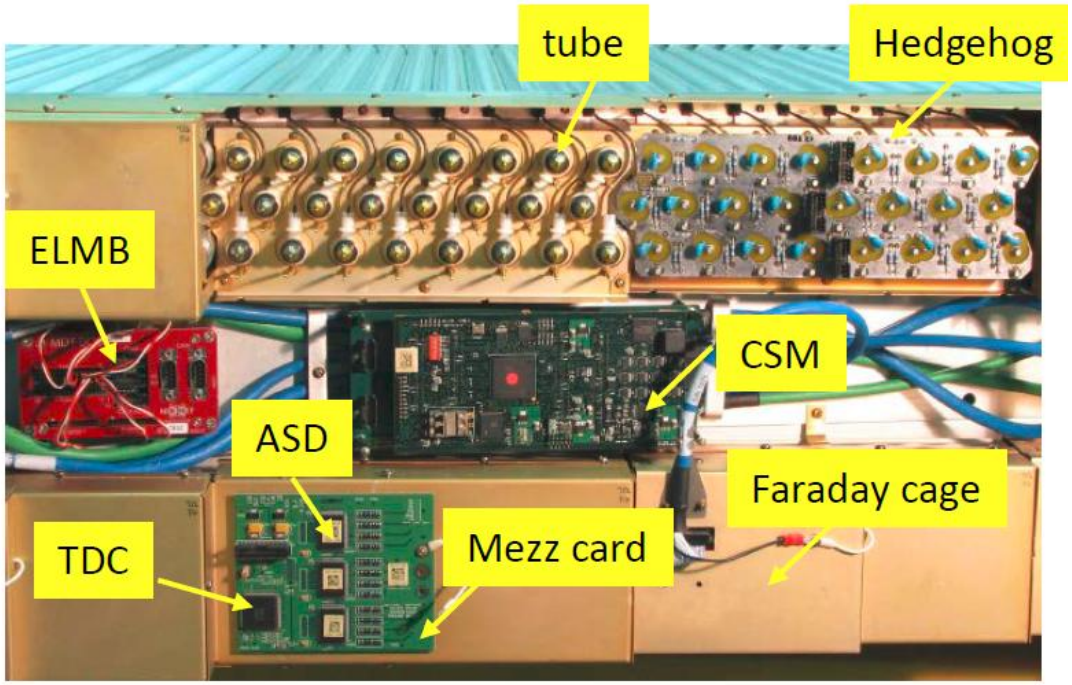


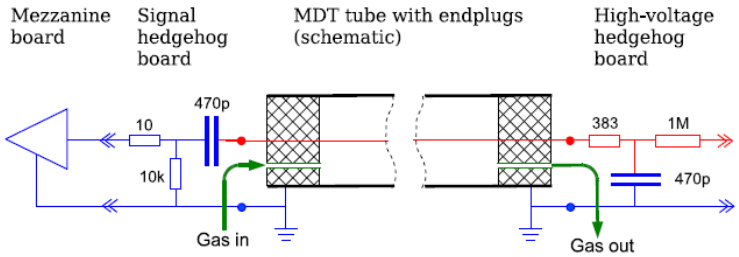
RPCs/TGCs are used as primary trigger detectors
MDTs/CSCs are used as precision trackers

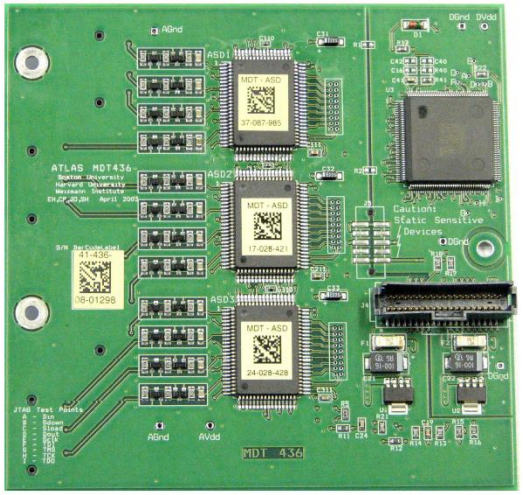
Current MDT Frontend Electronics

- MDT is currently only used for precision readout



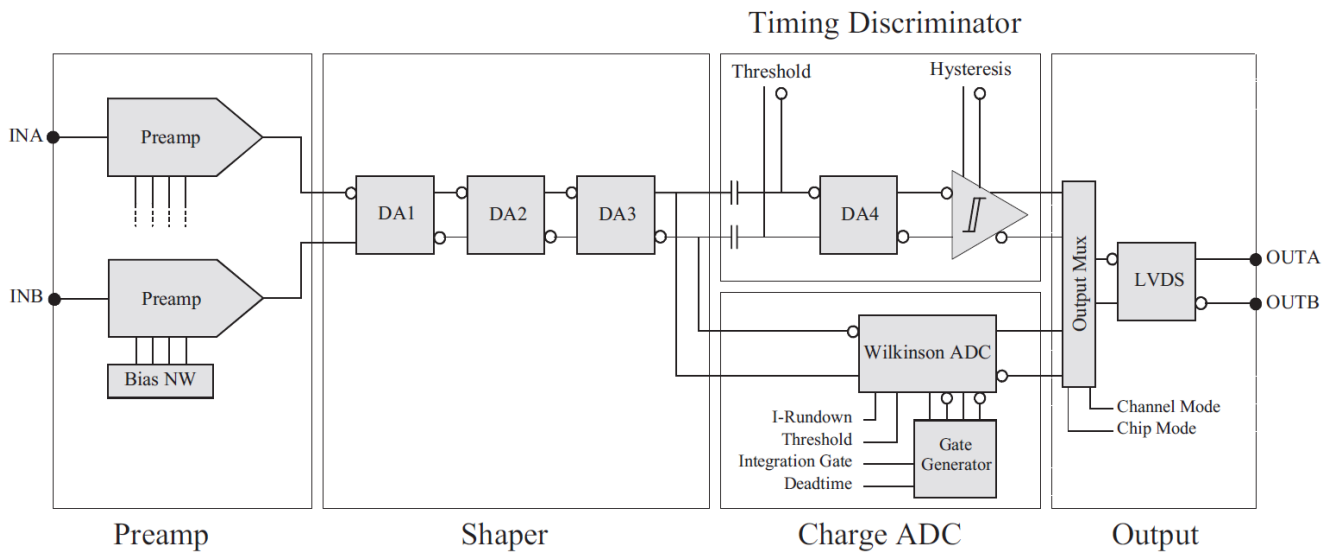


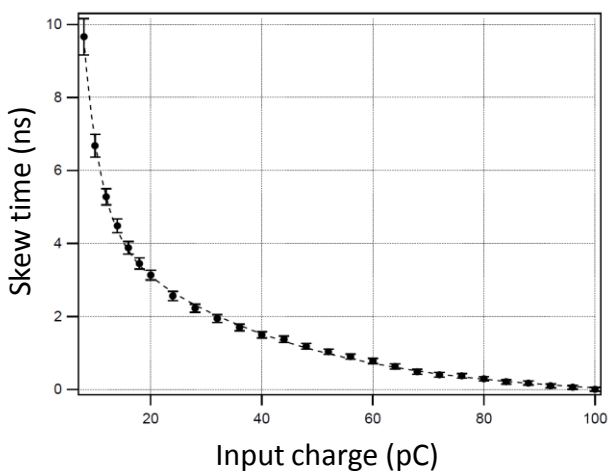


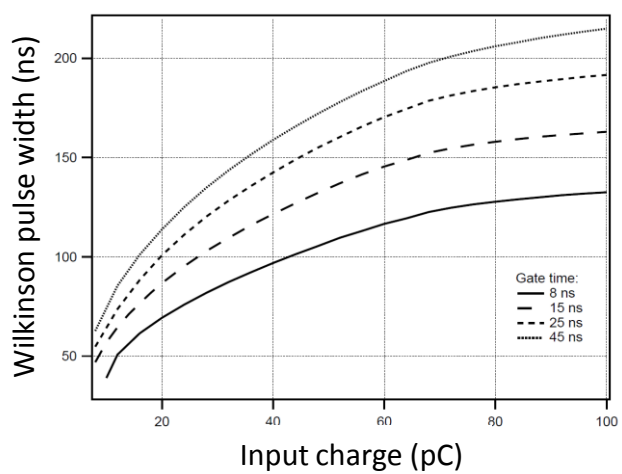


ASD ASIC

- Charge Sensing Preamplifier (CSP)→DA1/DA2/DA3(three shaping stages) → discriminator
- A Wilkinson ADC is used to reduce the dependence of the drift time measurement on the amount of incoming charge, i.e. time walk correction. The output pulse width corresponds to the input charge information, which can be digitized by following TDC ASICs.

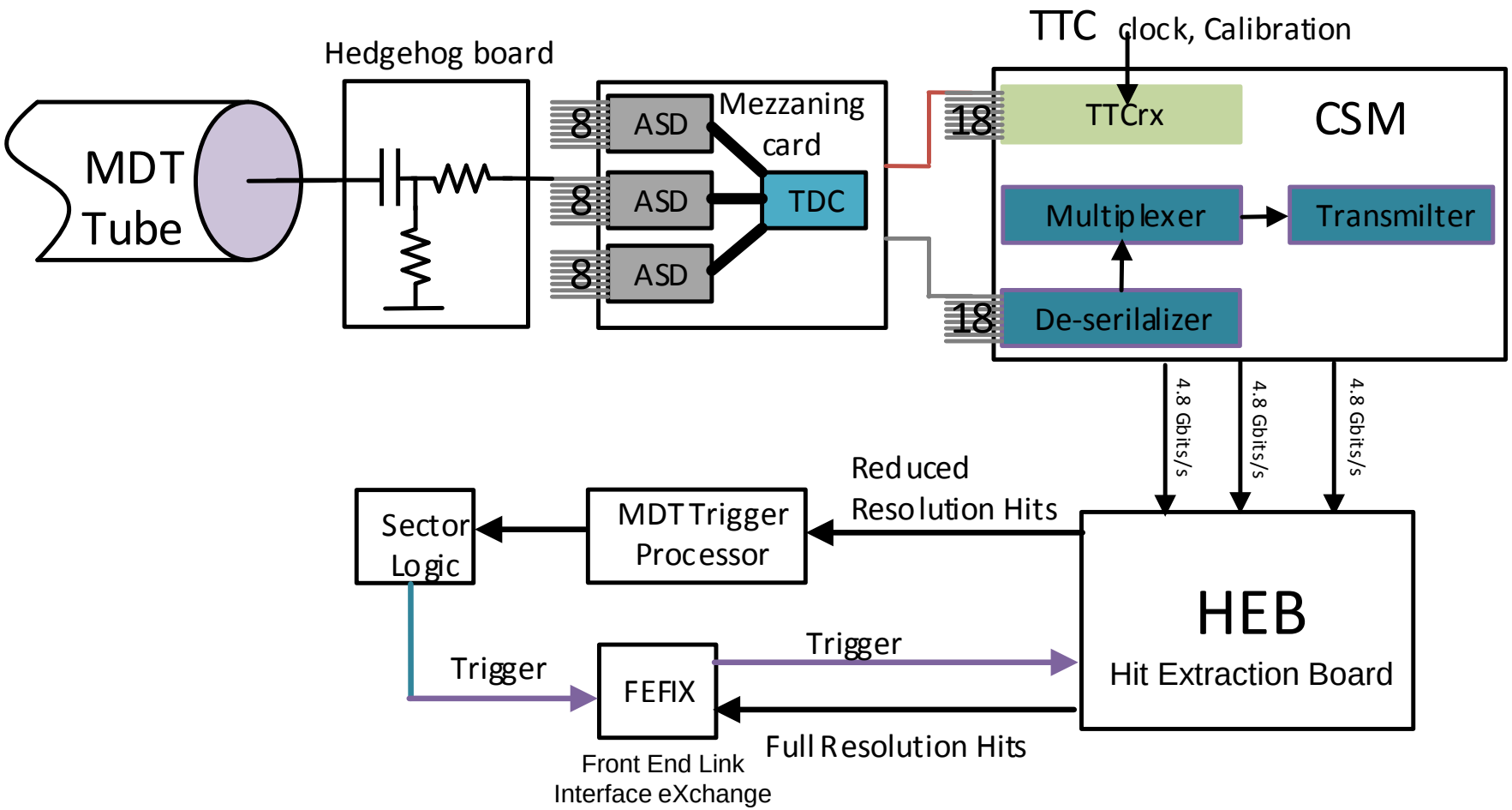






Future MDT front end electronics

- MDT electronics needs to cope with new proposed ATLAS TDAQ scheme (1 MHz L0 trigger rate with a latency of 10 μs)
- In addition, MDT will be used at L0 to further sharpen the L0 trigger turn-on curve



A New TDC Design

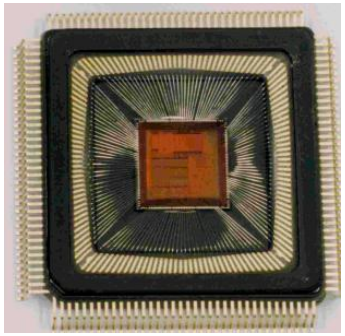
Why a new TDC IS NEEDED?

- Previous AMT (TDC) is no longer available for production.
- Output data bandwidth not enough for high rate.
- Issues found with the AMT chip.

  Ref: https://indico.cern.ch/event/504237/contributions/2138705/

Design a new TDC ASIC for the MDT phase II upgrade

- Comparable timing performance (Tubes unchanged)
- Additional features: Triggerless mode + Trigger mode



AMT3

UM-TDC v0

Comparison	AMT	MDT-TDC ASIC
Technology	0.3 µm CMOS Toshbia	0.13 µm CMOS GF
# of channels	24	24
Resolution	0.78 ns	0.78 ns (~200 ps)
Dynamic Range	102.4 us	102.4 us
Measurement	Rising/falling/TOT	Rising/falling/TOT
Double-hit Resolution	<10 ns	~10 ns
Trigger Mode	Trigger buffer	Triggerless mode + Trigger buffer (early installation)
Output bandwidth	One 80 Mbps line	Two 320 Mbps line

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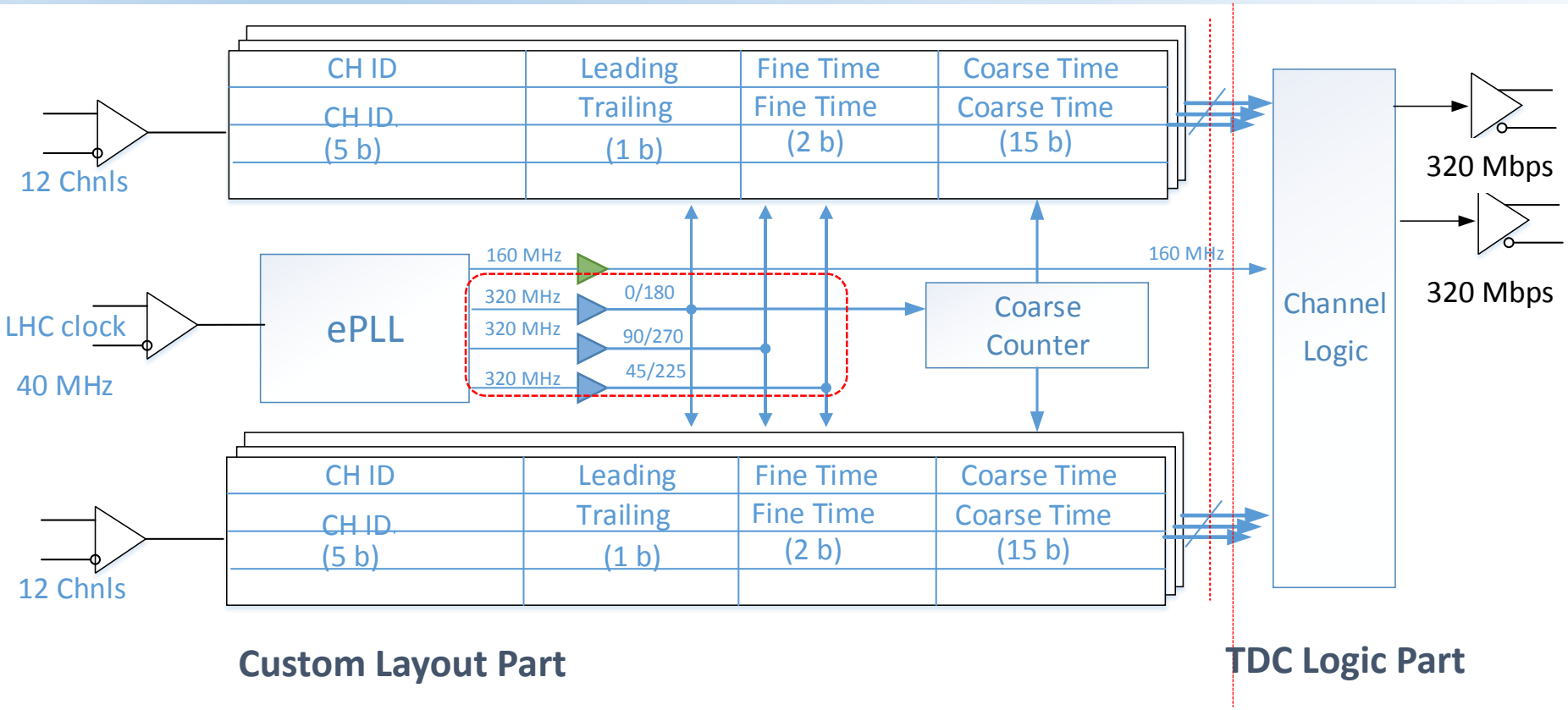
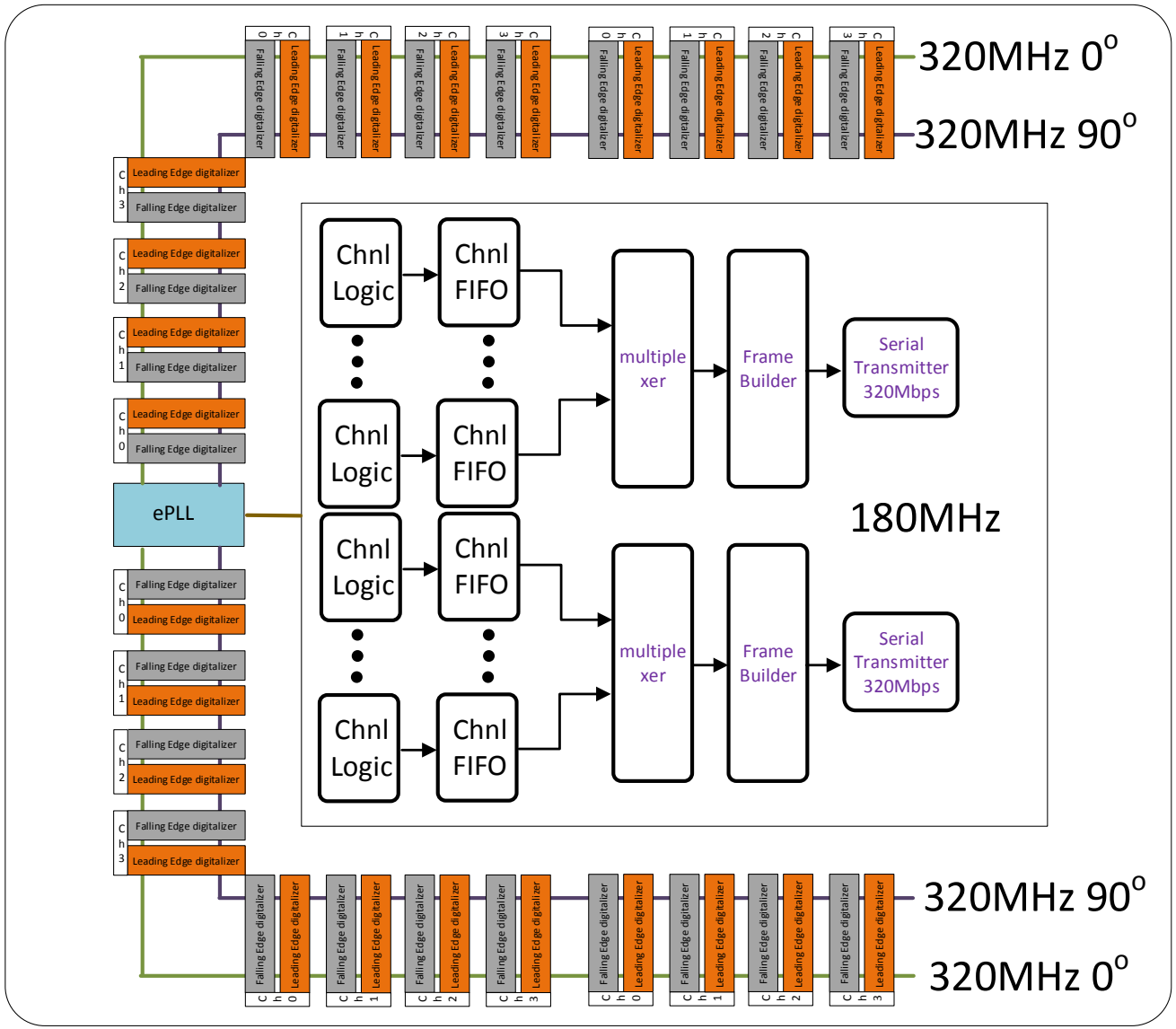
Architecture of MDT TDC ASIC



- Timing resolution determines optimal architecture:
  Multiple clock phases interpolator @ 320 MHz: ***4*** phases of 320 MHz => 3.125 ns /4 = 0.78 ns LSB
- Main components:
  => Generation of multiple clock phases: ePLL (CERN)
  => Time Digitization: TDC channels (x24)
  => Time processing/calibration, output serial interface (TDC logic part)

  } Custom Layout

TDC v0 Design



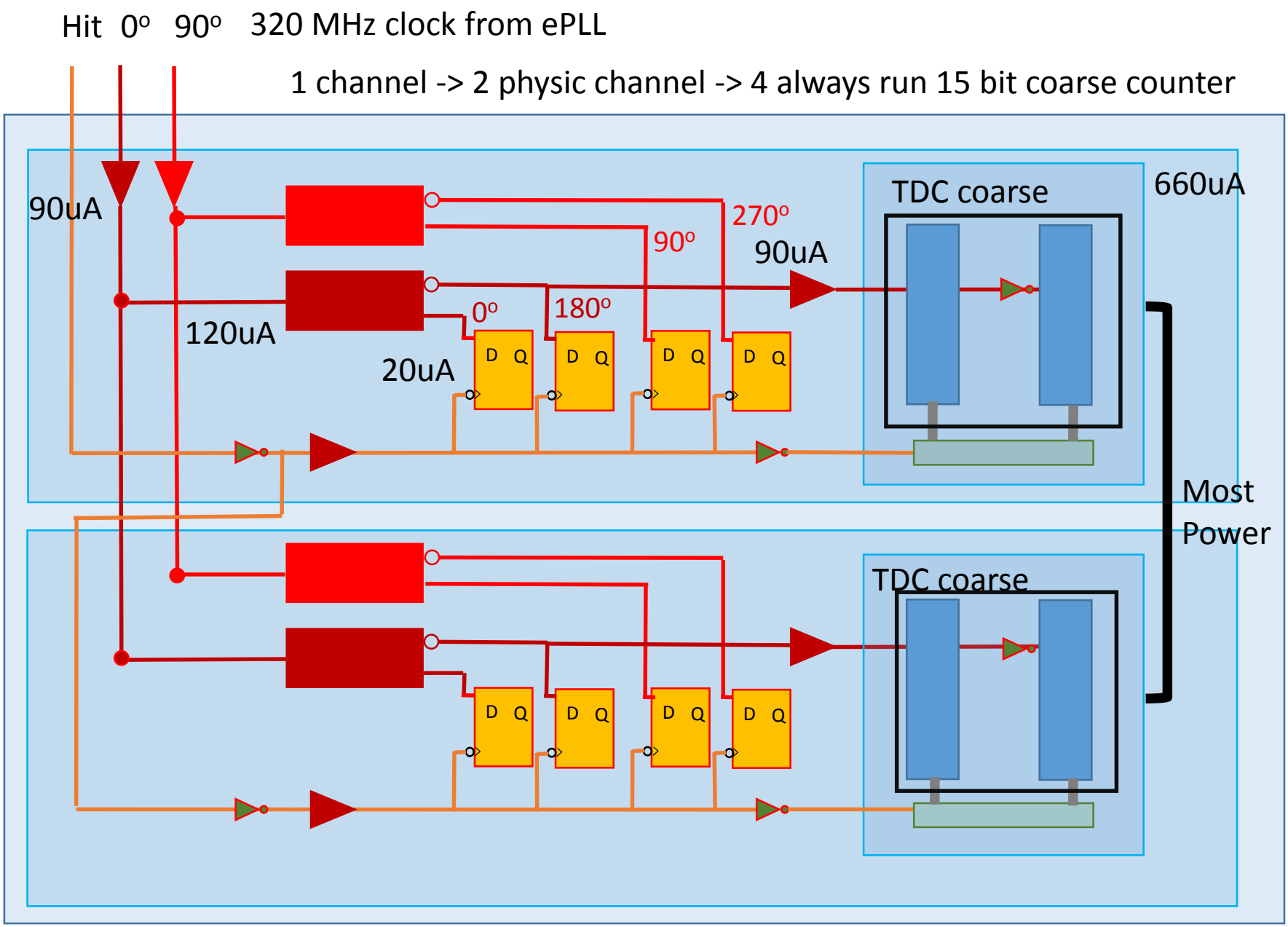
Leading Edge digitalizer　Falling Edge digitalizer

前沿量化器　后沿量化器

- ***Multiple clock phases interpolator*** @ 320 MHz: ***4*** phases of 320 MHz => 3.125 ns /4 = 0.78 ns LSB
- Main components:
  => Generation of multiple clock phases: ePLL (CERN)
  => Time Digitization: TDC channels (x24 chnl; dual edges)
  => Time processing/calibration, output serial interface (TDC logic part)

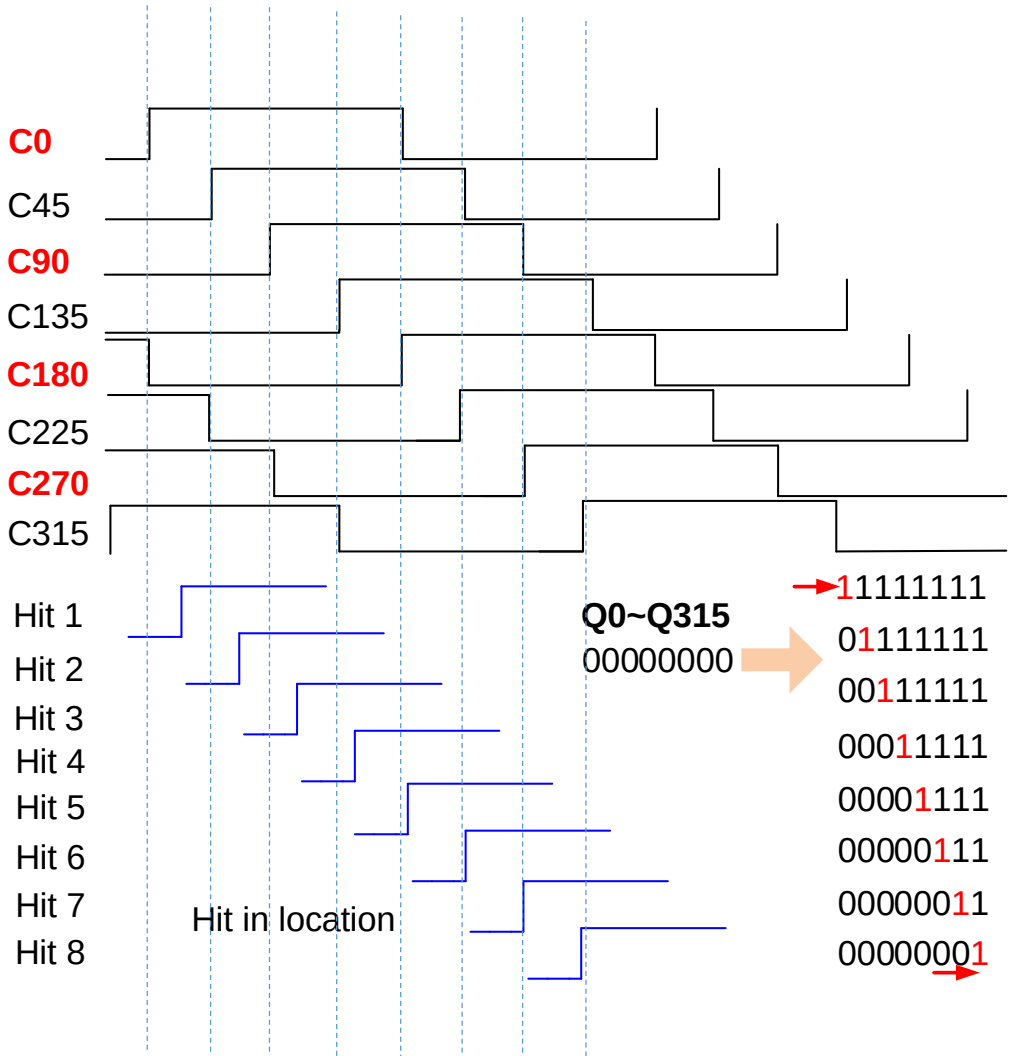
Custom Layout

TDC channel


Hit 0º 90º 320 MHz clock from ePLL
1 channel -> 2 physic channel -> 4 always run 15 bit coarse counter
90uA
120uA
20uA
0º
180º
90º
270º
90uA
D Q
TDC coarse
660uA
Most Power
TDC coarse

Fine time measurement

- Fine time measurement is done based on multi-phase clock interpolation method.
- PLL can be employed to generate multiple synchronized clock signals with a certain phase shifted, by which one clock period is divided into several tiny time gaps.
- When the hit signals fall into one of the gaps, a thermometer coded data can be generated, and the position of 0 to 1 transition corresponds to the time information of hit signal.

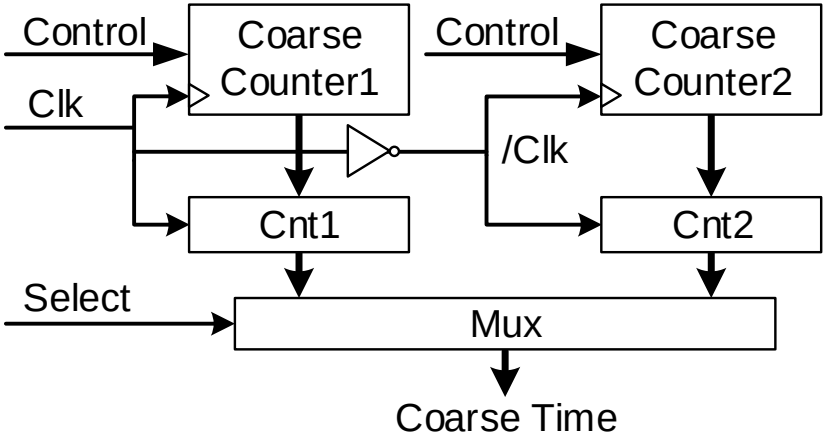


Fine time measurement with 8-phase clock interpolation

In this TDC ASIC, a total of 4 phases are employed.

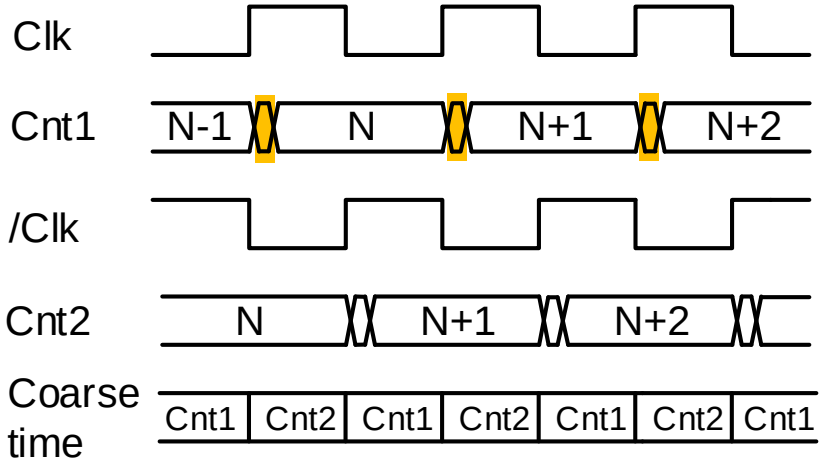
Coarse time measurement

- To expand time measurement dynamic range, coarse time counter is employed.

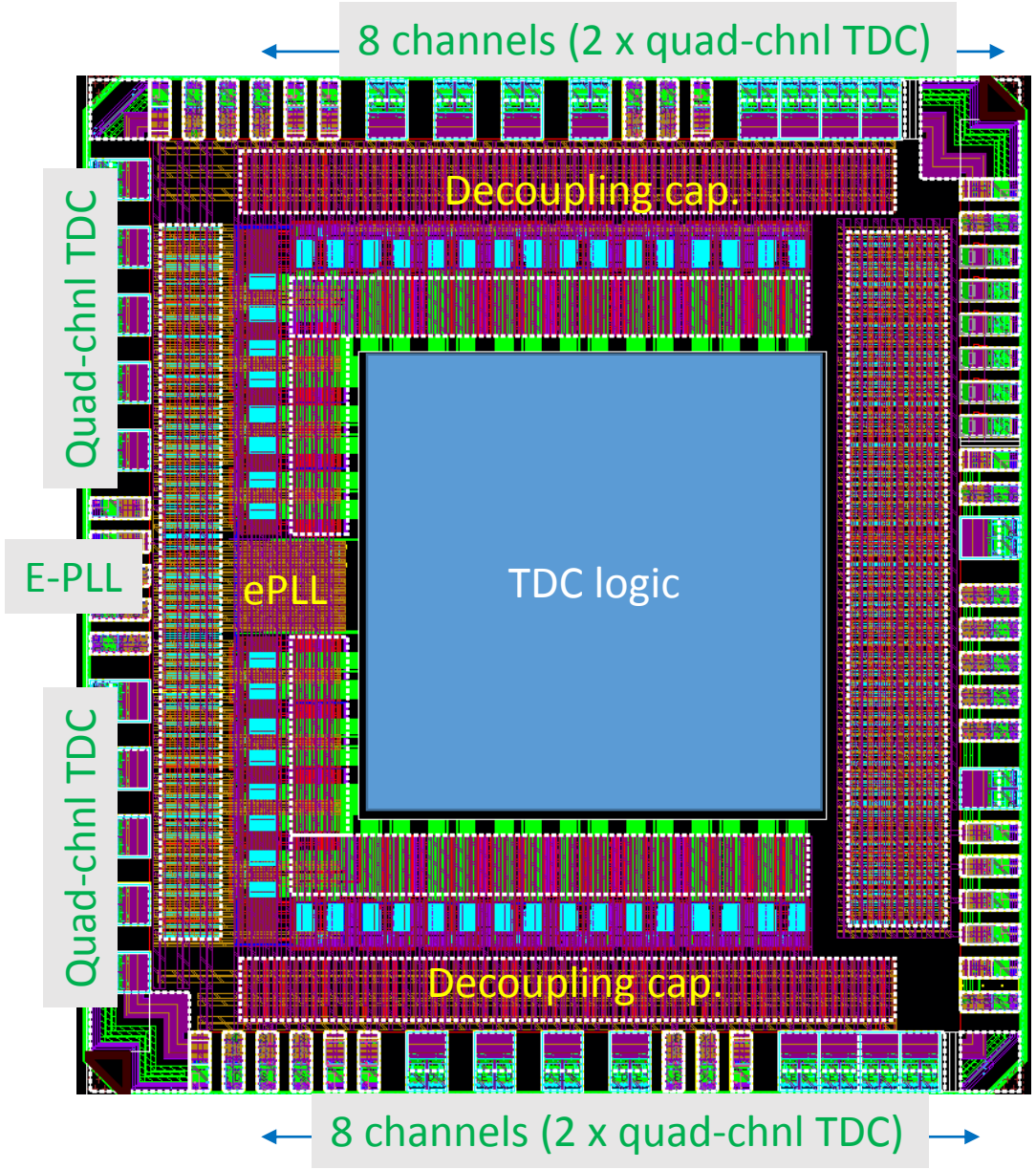


- The problem with one single counter is: input hit signal may fall in the time interval when the counter is in a metastable state, which results in errors.

- To address this issue, a pair of counters are used, with inverted clock inputs.
- No matter where the hit falls, one of the counters outputs stable correct data, which can be selected based on fine time measurement results.



TDC Version 0



Total Power:
Analog: 171 mA @1.5V(ePLL,24chnl,IO)
Digital: 66 mA @1.5V (TDC logic)

3.4 mm × 3.7 mm

GF 130 nm CMOS technology

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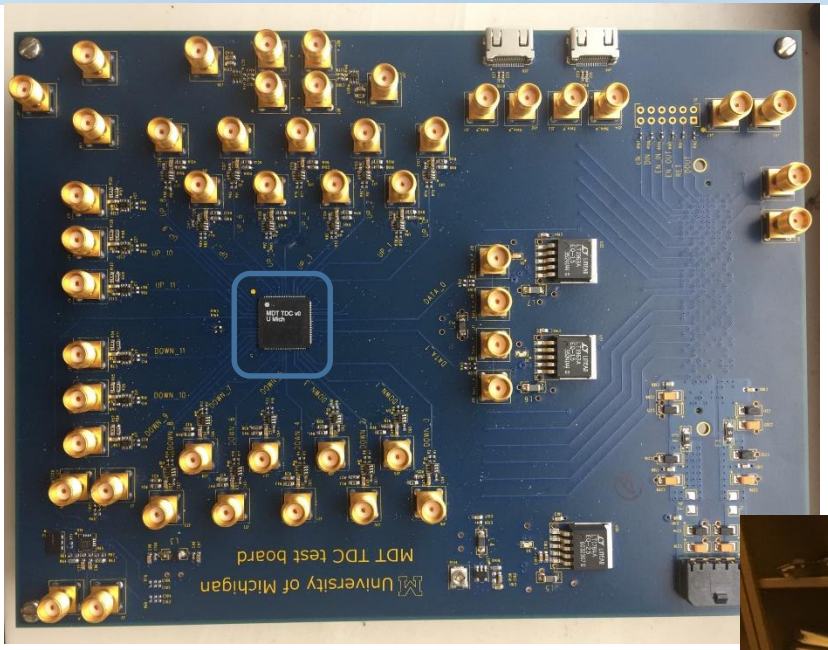
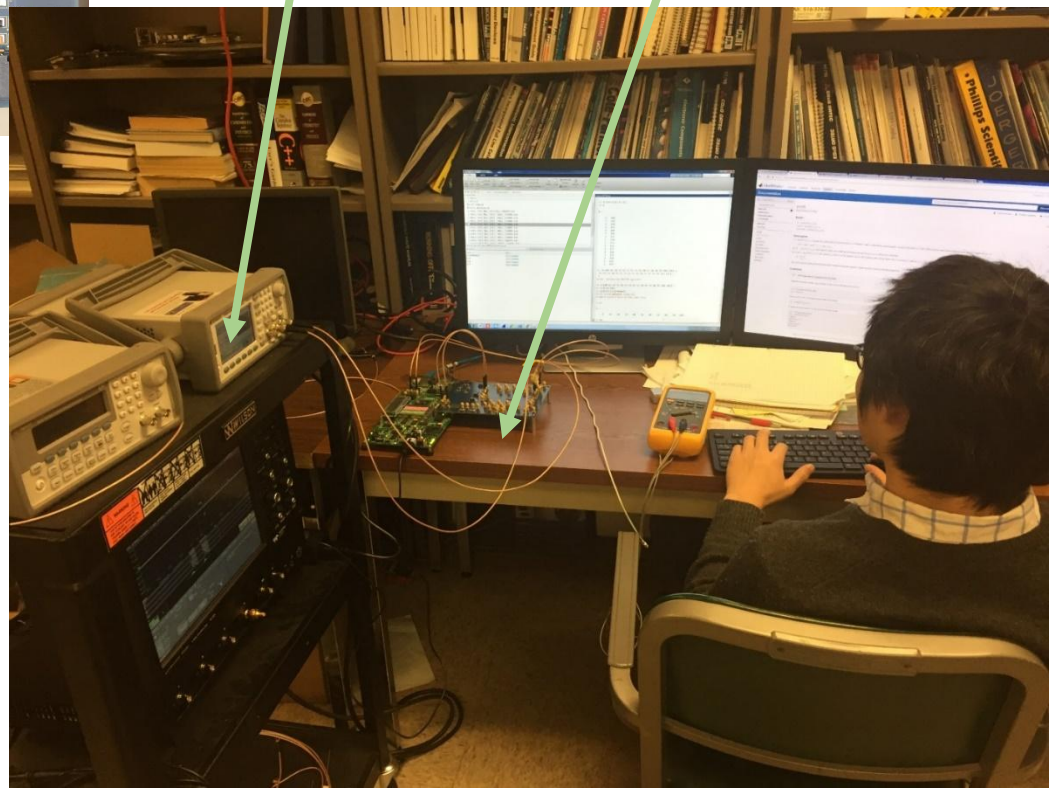
TDC Test Board Setup



- Fabricated in GF 130 nm process in 2016
- Size: 3.4 x 3.7 mm^2 with >2 million transistors
- QFN100 package used

Pulse Generator → TDC Board + AC701

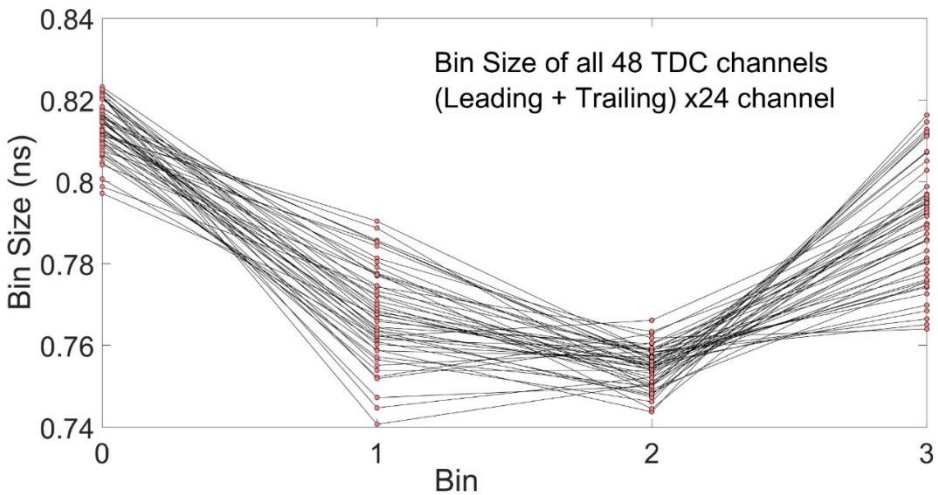


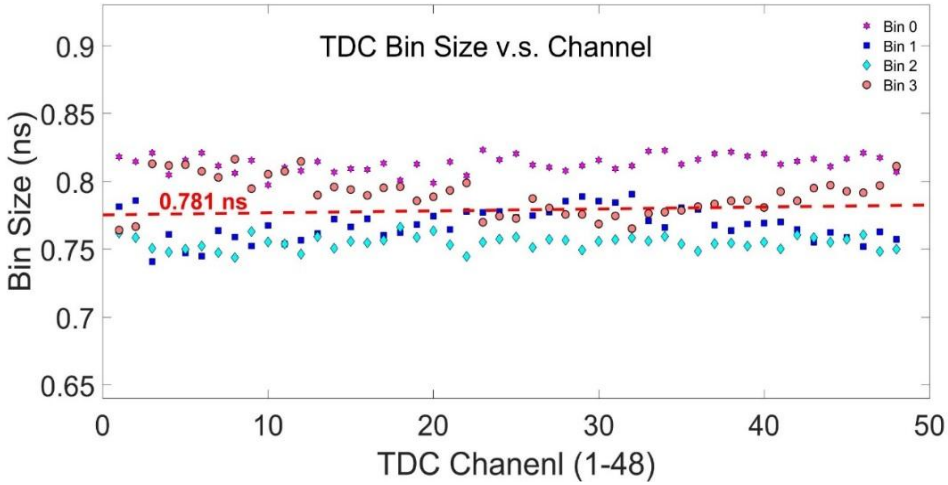
Performance Test:

1) Bin size (LSB)
2) Time resolution (RMS)

Performance of TDC bin size

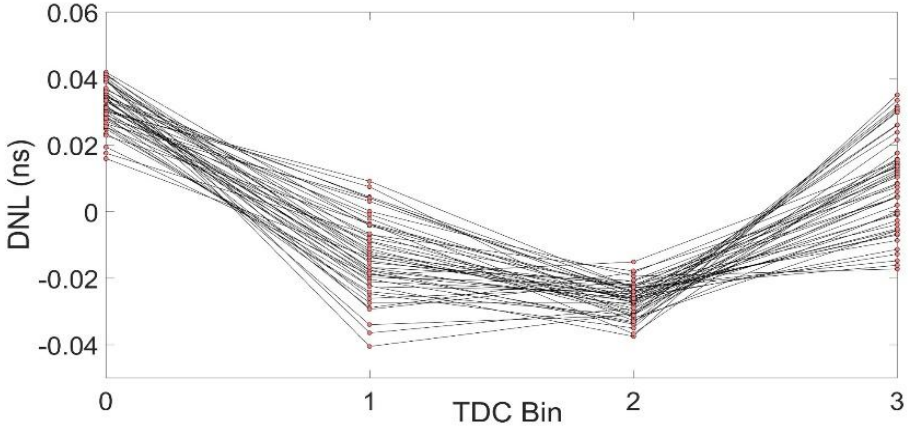
- Bin sizes for all 24×2=48 channels are within (0.78 ± 0.04) ns

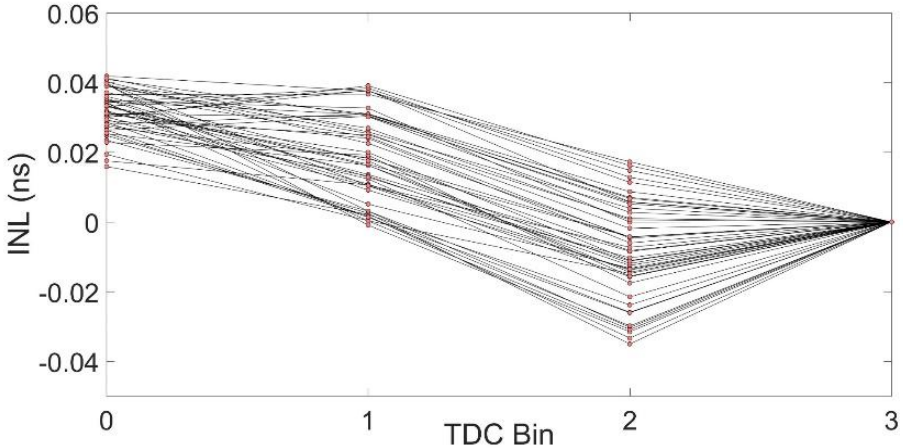




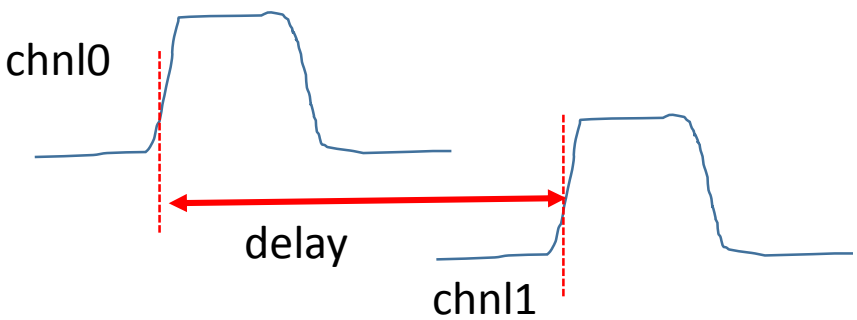
Performance of TDC bin size

- Integrated and differential non-linearity are less than 5% of the bin size

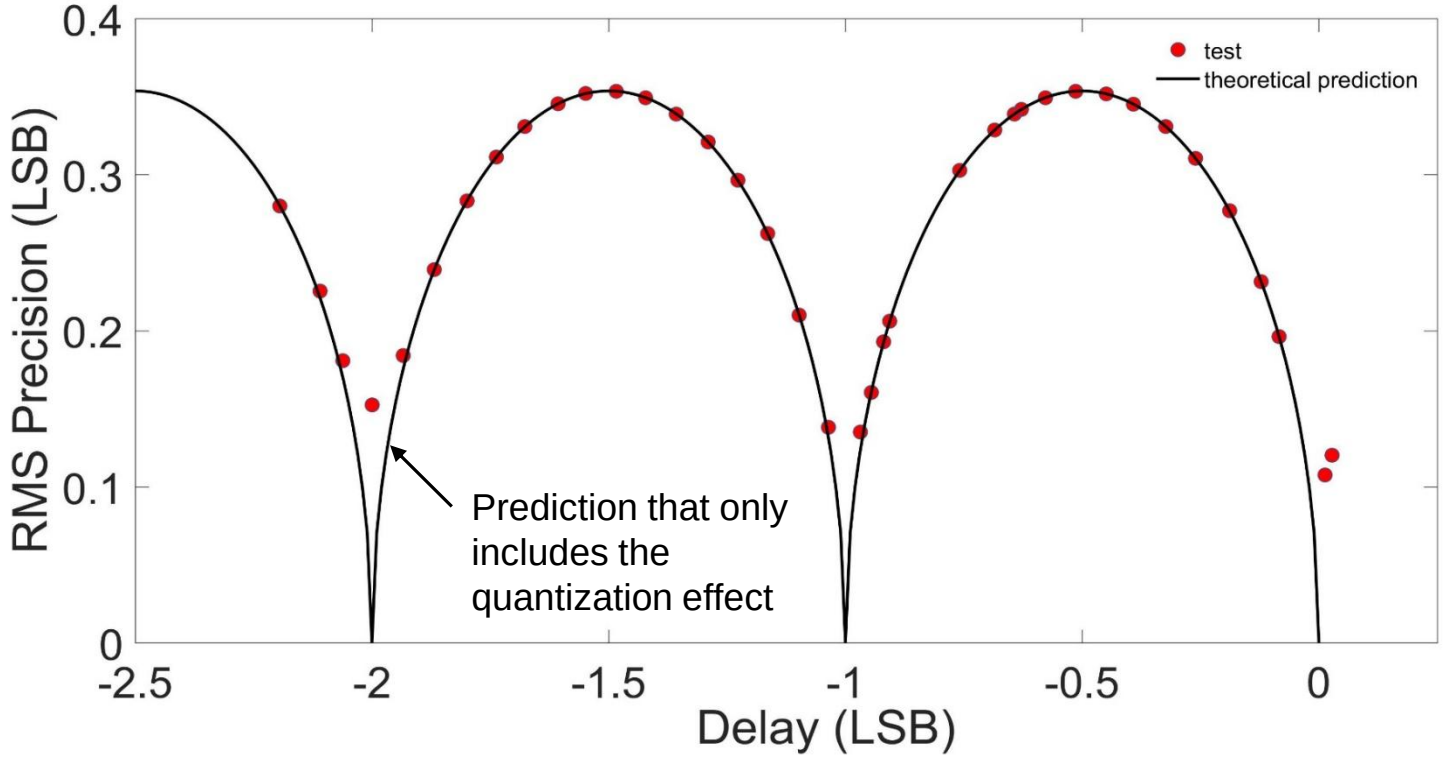




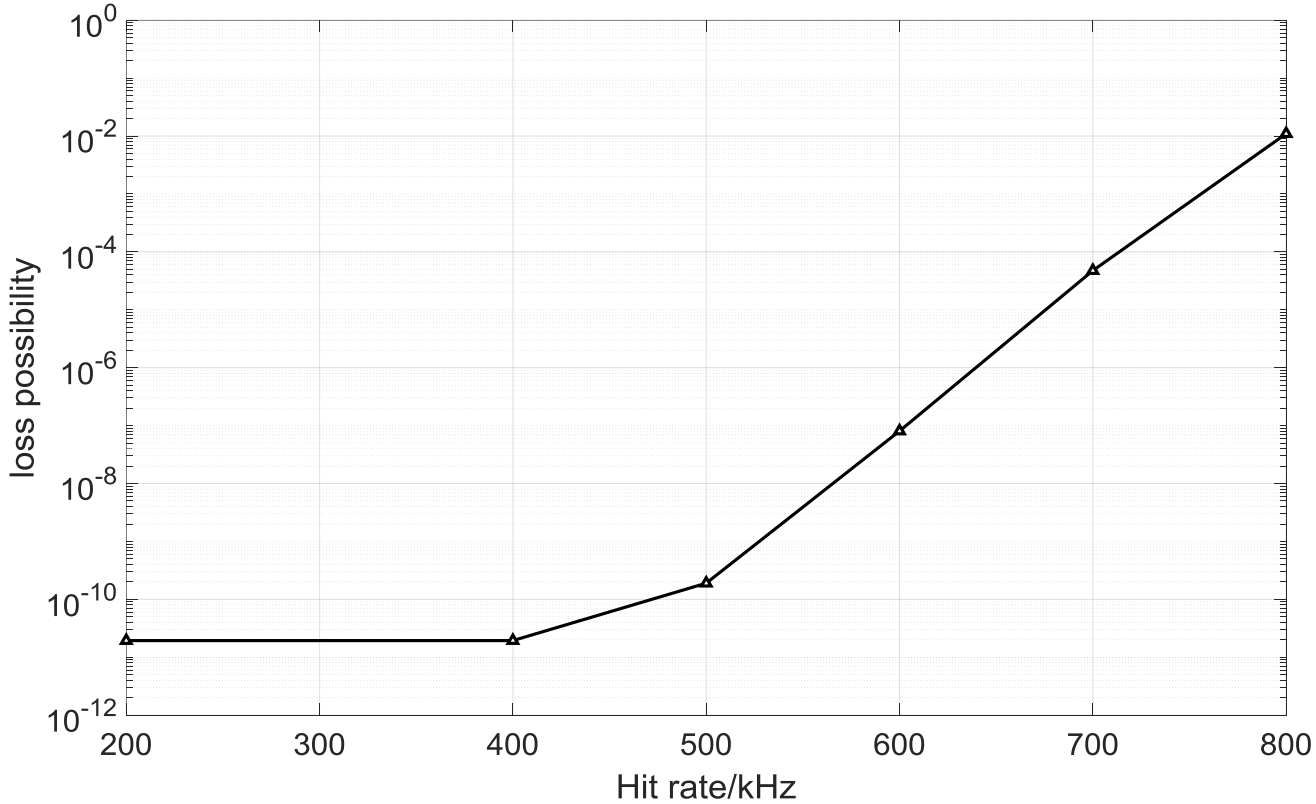
Performance of TDC RMS



- To eliminate the noise influence of signal generator, cable delay test method is employed.
- Power consumption: ~310 mW (TDC fully working).

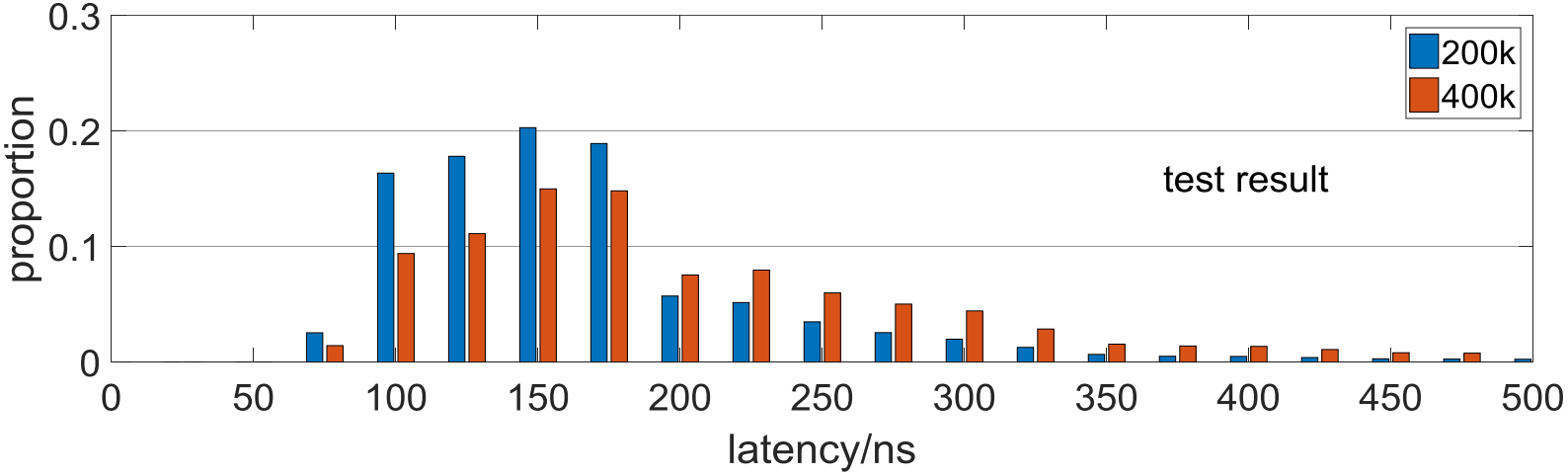


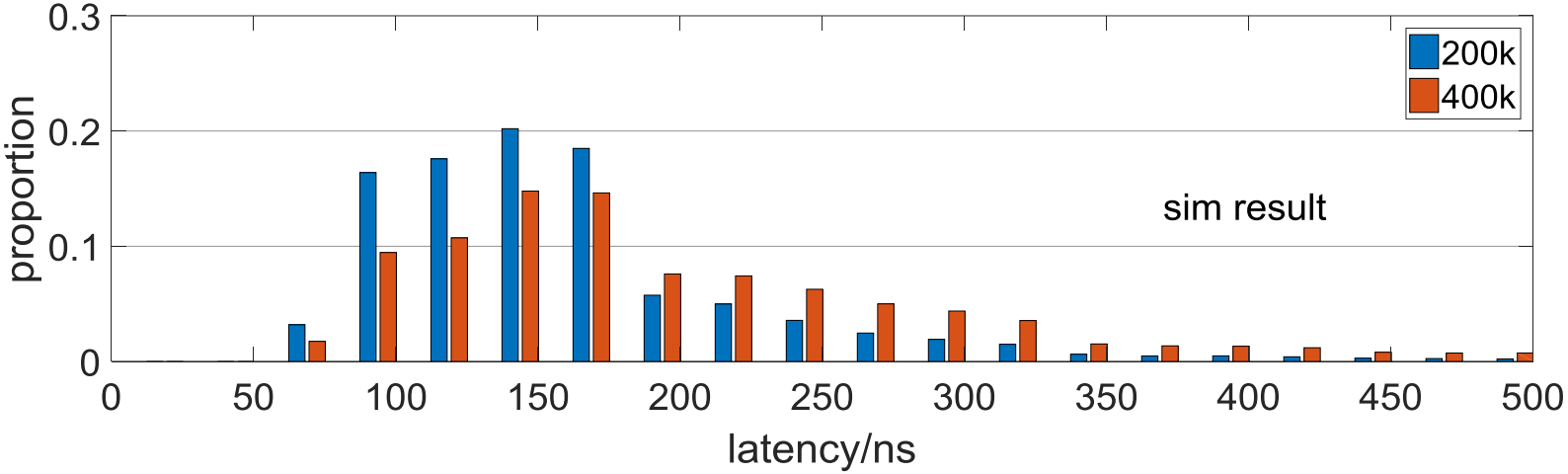
Test results of data loss



- When hit rates decreased, the data loss ratio is reduced exponentially.
- With 200 kHz and 400 kHz hit rate, data loss ratio is below 2×10^{-11}.

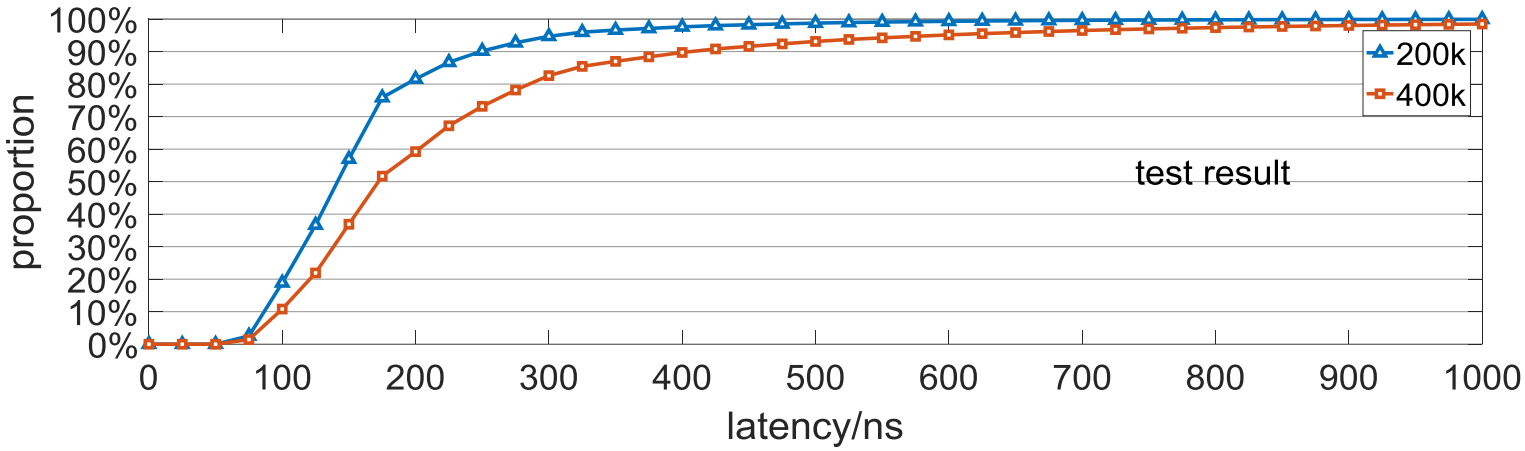
Performance of TDC latency

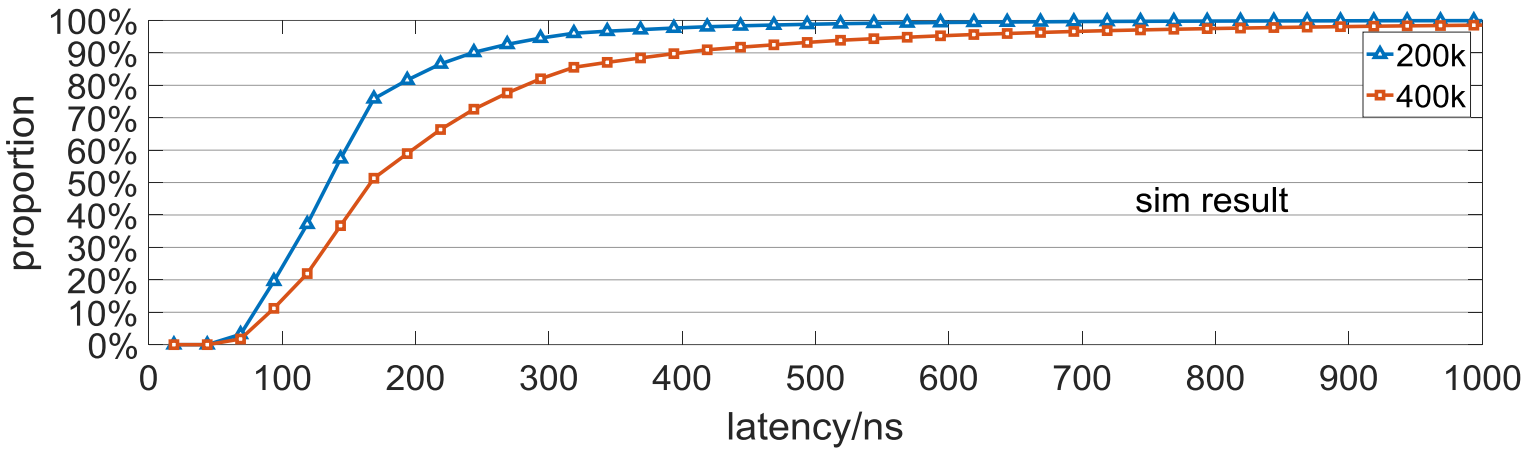




- Simulations and tests were conducted to evaluate the latency of the TDC.
- Pseudo-random data are generated using FPGA as “hit” signals in the tests.
- These two figures are the histogram of the latency. The test results concord well with the simulation results.
- In actual application, the hit rate is around 200 kHz. Extreme rare situation would probably be 400 kHz.

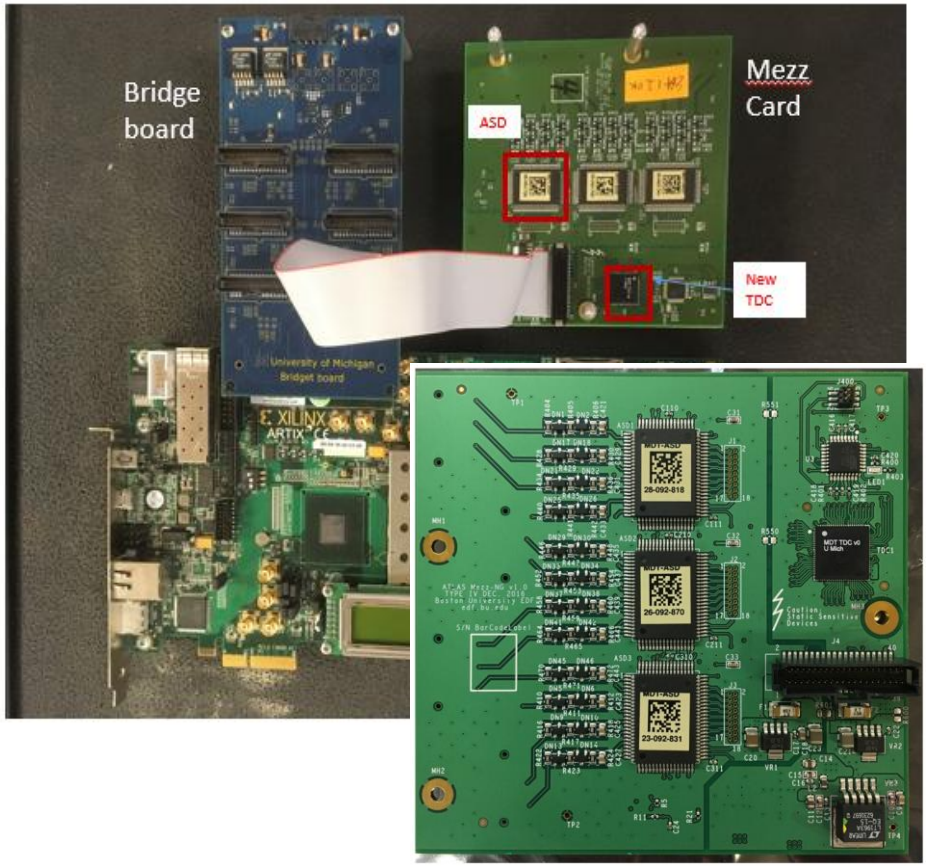
Performance of TDC latency

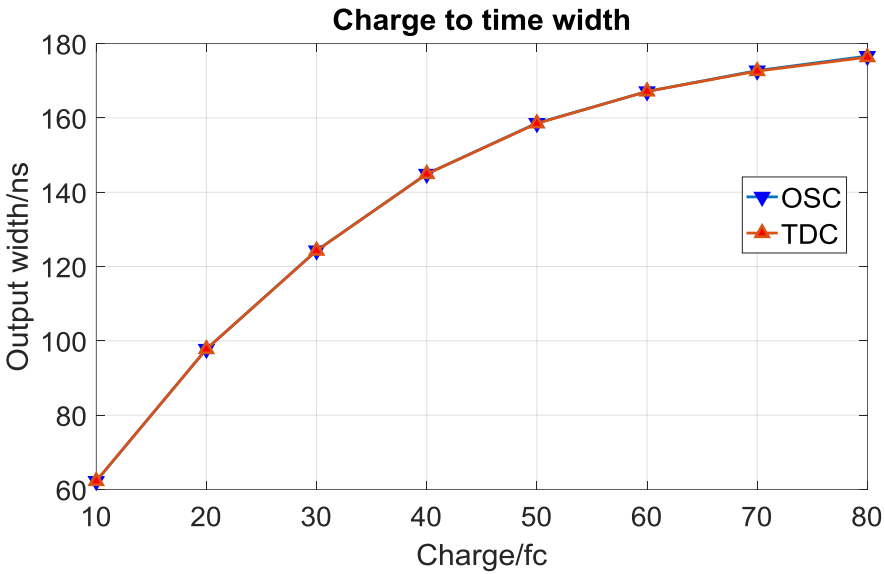


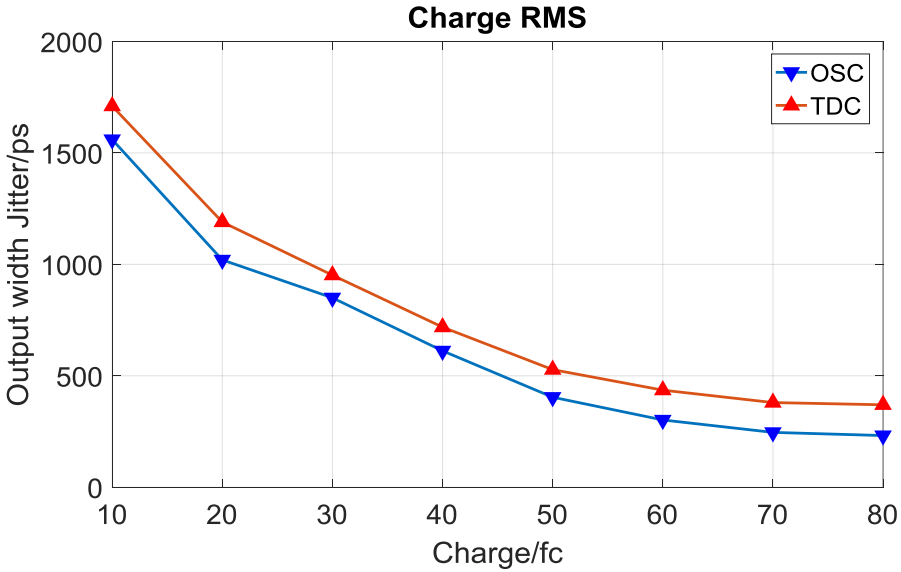


- This is accumulated results of the latency.
- With 200 kHz input hit rate, 95% hits can be read out within 300 ns , and 99% within 550 ns .
- With 400 kHz input hit rate, 95% hits can be read out within 600 ns, and 99% within 1 μs.

Performance of TDC + ASD

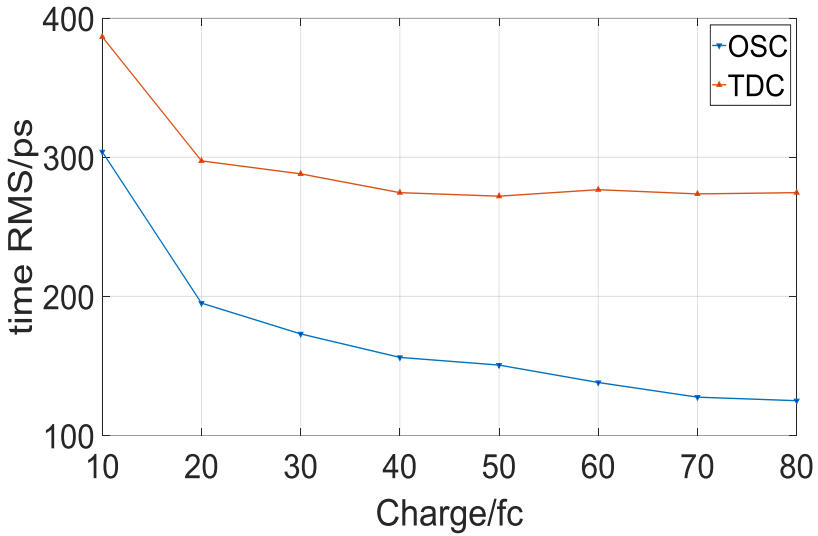


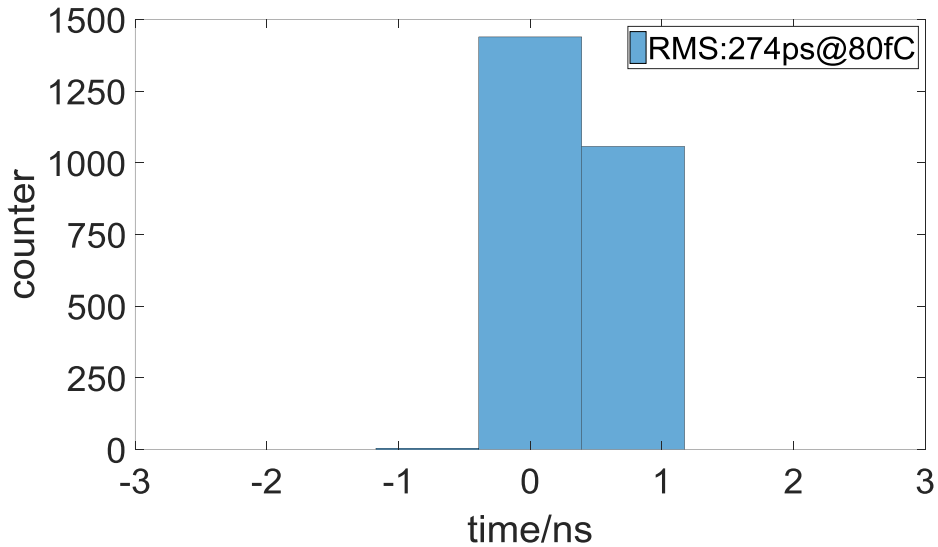




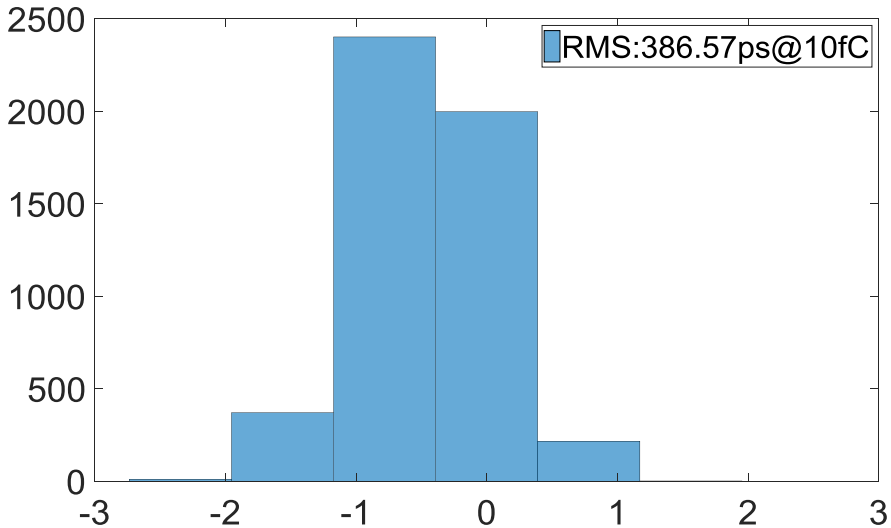
- Combination tests of TDC and current ASD ASIC.
- ASD working in ADC mode, and the output pulse width of ASD presents the charge input to the ASD.
- Using an oscilloscope to test output width of ASD ,used as a reference.
- The width test result using TDC and using oscilloscope are almost same.
- The RMS of the pulse width is only deteriorated slightly due to TDC quantization error.

Performance of TDC + ASD





- We also conducted tests on time measurement resolution (RMS).
- Time resolution is better than 400 ps over the dynamic range from 10 fC to 80 fC.



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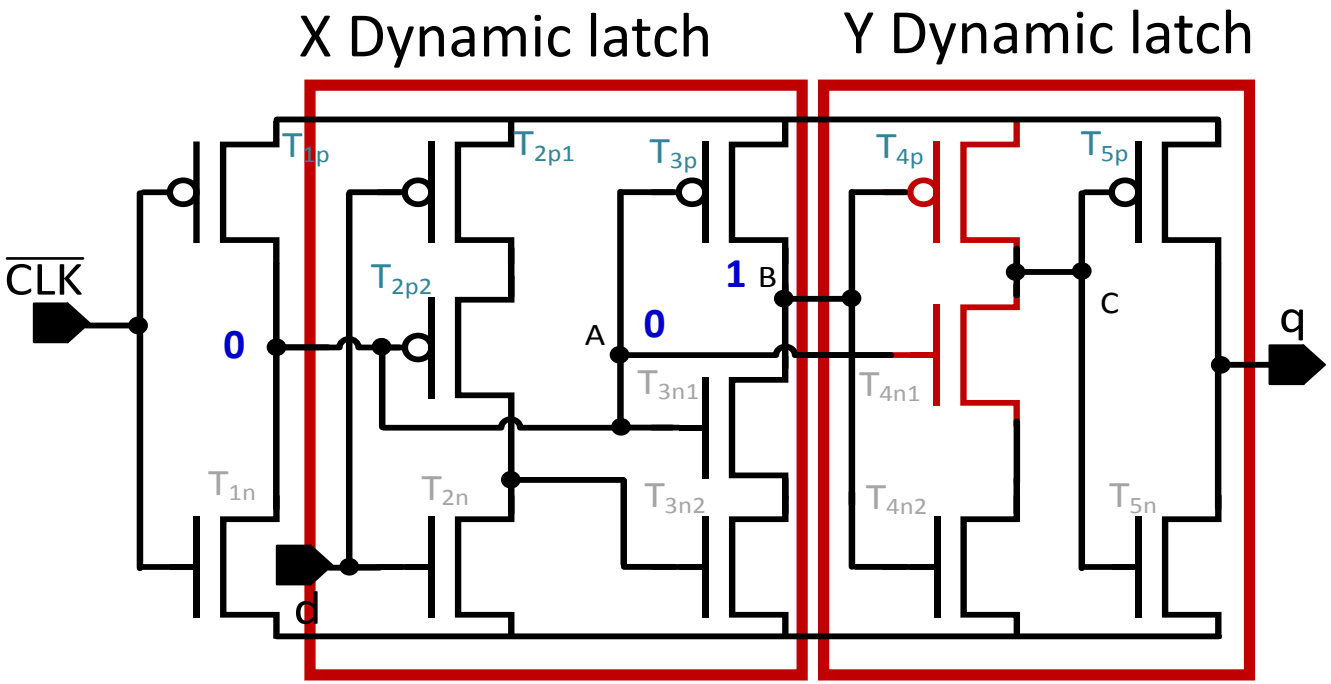
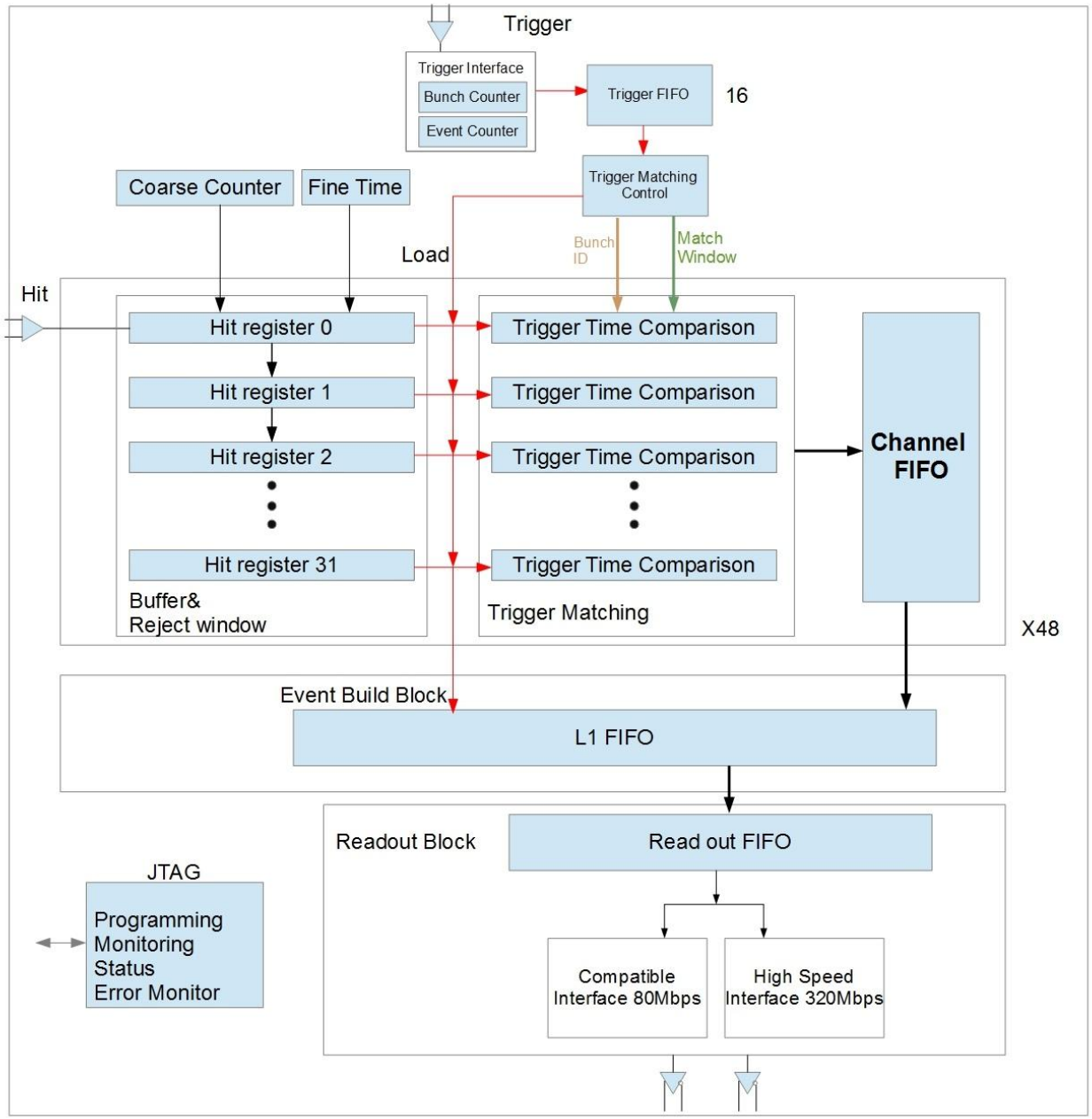
Dynamic DFF



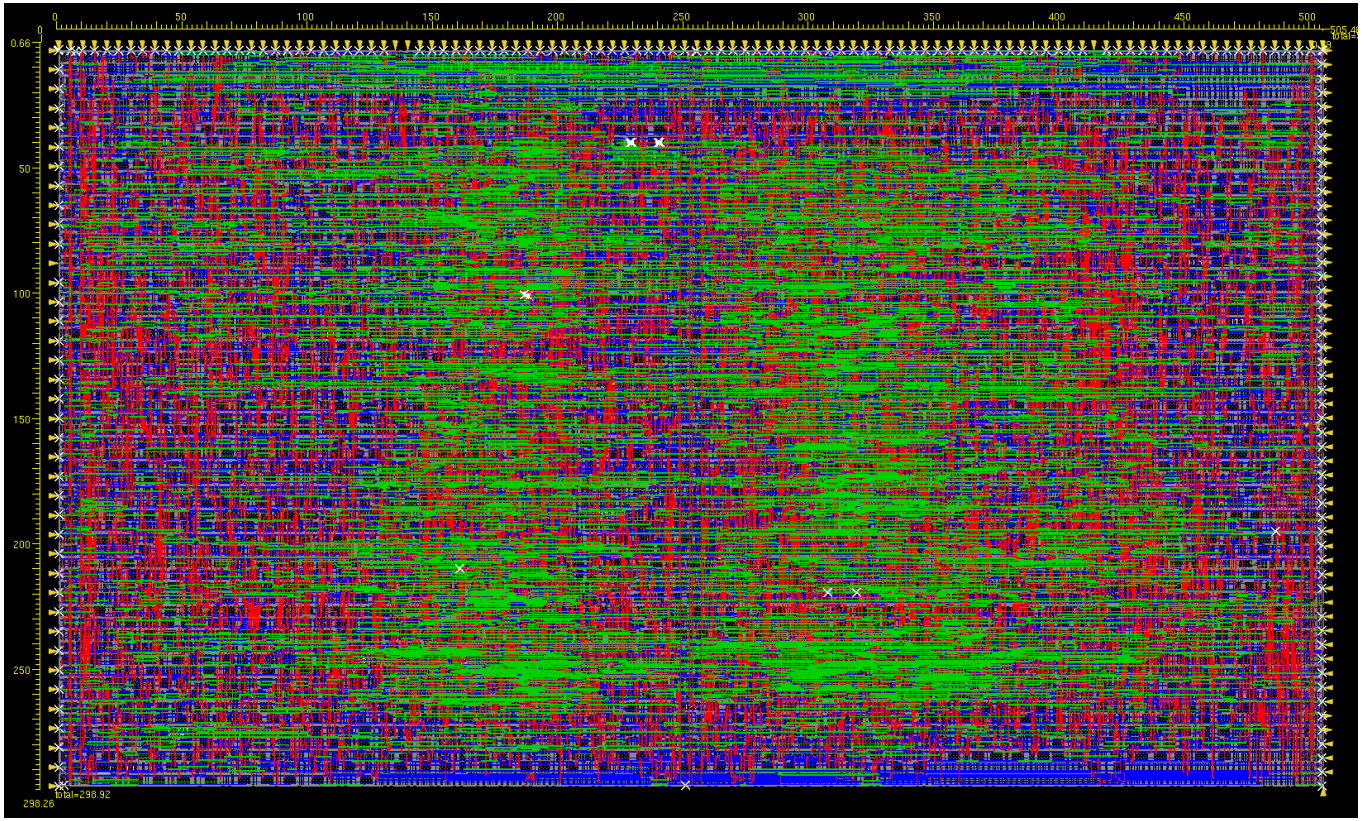
- As one of key components in fine time measurement of the TDC, the D Flip-Flop (DFF) needs to be modified to improve its power consumption.

D	Clk	Tt	Fs	Sf	Ff	ss
0	0	113.7n	146.5n	107.9n	523.3n	17.41n
1	1	42.19u	169.1u	407.9n	860.3u	15.19u
0	1	42.1u	169.5u	334n	861.3u	15.18u
1	0	118.5u	14.06u	494n	266.3u	107.4u
AVE		50u	88u	335n	627u	34u

New TDC Trigger Logic



New TDC Trigger Logic



Type	Instances	Area %
seq	1366	41.9
Inverter	146	1.0
buffer	94	1.2
logic	4655	55.9
total	6261	100

Total power: 11.68 mW @1.5V

Static power: 1.67 mW

Dynamic power:10.01 mW

Density:60%

Total area:500µmX300µm

Conclusion

- We cooperated with University of Michigan, and worked on the TDC ASIC designed for MDT in ATLAS phase II upgrade.
- Up to now, prototype of the first version has been designed and tested.
- The basic functionality of time digitization circuit has been verified, with some structure needed to be improved.
- We will focus on the design of the second version, especially with trigger matching function included while maintaining compatibility for triggerless all data readout mode. This means complex digital ASIC circuit design is required.
- We are also considering shifting the CMOS technology from GF 130 nm to TSMC 130 nm.

Thank you very much.