触发系统介绍

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内容

- BESIII 触发系统
  - 背景知识
  - 一般触发系统的原理与构成
  - 部分实验结果
- BESIII 触发系统
- 未来发展

背景知识

- 什么是触发判选系统（Trigger System）？
  – 中文字典 / 百科全书？
  – 英文字典 / 百科全书？
  – 示波器的触发
  – 实验物理的触发
  – 加速器物理的触发与判选

背景知识

- 什么是触发判选系统（Trigger System）？
  - 有多少人知道？

背景知识

- 什么是触发判选系统（Trigger System）？
  - 中文字典 / 百科全书？
    - 百度百科
      - 触发引信
        - » 触发引信可以配用于杀伤弹、破甲弹、杀伤/破甲两用弹、爆破弹、攻坚弹和破障弹等主用弹，也可以配用于燃烧弹、发烟弹等特种弹。触发引信是现代弹药使用最广泛的引信之一。
      - 触发器（trigger）
        1. 是SQL server 提供给程序员和数据分析员来保证数据完整性的一种方法，它是与表事件相关的特殊的存储过程，它的执行不是由程序调用，也不是手工启动，而是由事件来触发，比如当对一个表进行操作（ insert，delete， update）时就会激活它执行。触发器经常用于加强数据的完整性约束和业务规则等。
        2. 在实际的数字系统中往往包含大量的存储单元，而且经常要求他们在同一时刻同步动作，为达到这个目的，在每个存储单元电路上引入一个时钟脉冲（CLK）作为控制信号，只有当CLK到来时电路才被“触发”而动作，并根据输入信号改变输出状态。把这种在时钟信号触发时才能动作的存储单元电路称为触发器，以区别没有时钟信号控制的锁存器。
        3. 触发器（trigger）是SQL server 提供给程序员和数据分析员来保证数据完整性的一种方法，它是与表事件相关的特殊的存储过程，它的执行不是由程序调用，也不是手工启动，而是由事件来触发，比如当对一个表进行操作（ insert，delete， update）时就会激活它执行。触发器经常用于加强数据的完整性约束和业务规则等。

Trigger/触发

- **WIKI：**
  - **trigger** - lever that activates the firing mechanism of a gun

- Bing:
  - a small device that releases a spring or catch and so sets off a mechanism, especially in order to fire a gun:

- webopedia
  - In a DBMS, a trigger is a SQL procedure that initiates an action (i.e., fires an action) when an event (INSERT, DELETE or UPDATE) occurs. Since triggers are event-driven specialized procedures, they are stored in and managed by the DBMS.

示波器的触发

- 有多少人用过示波器？

示波器的触发

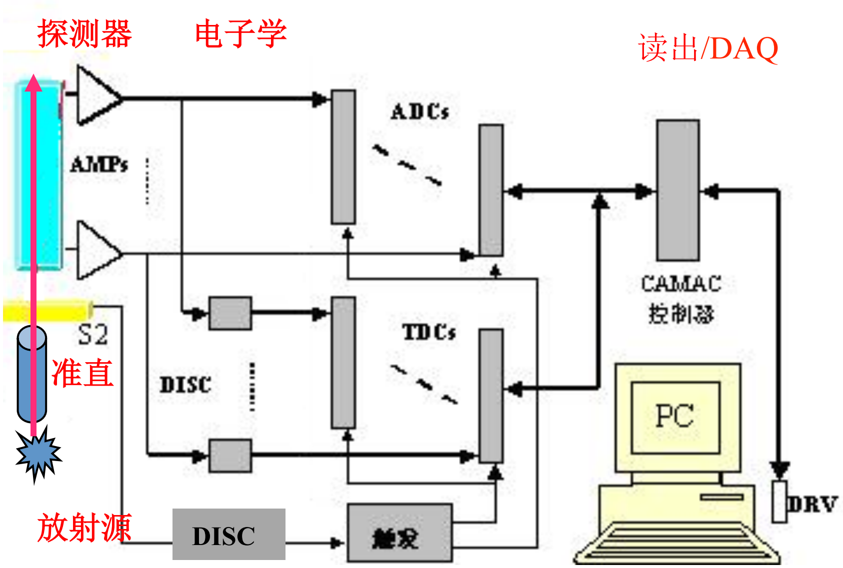
- 示波器：
  - 触发电平：被选定信号的幅度大于该电平时，被测信号的波形被抓取并显示在屏幕上。
- 数字信号分析仪
  - 触发模式：被选定串行信号满足一定的模式结构时，被测信号的结构被抓取并被显示在屏幕上。
- 加速器
  - 事件驱动

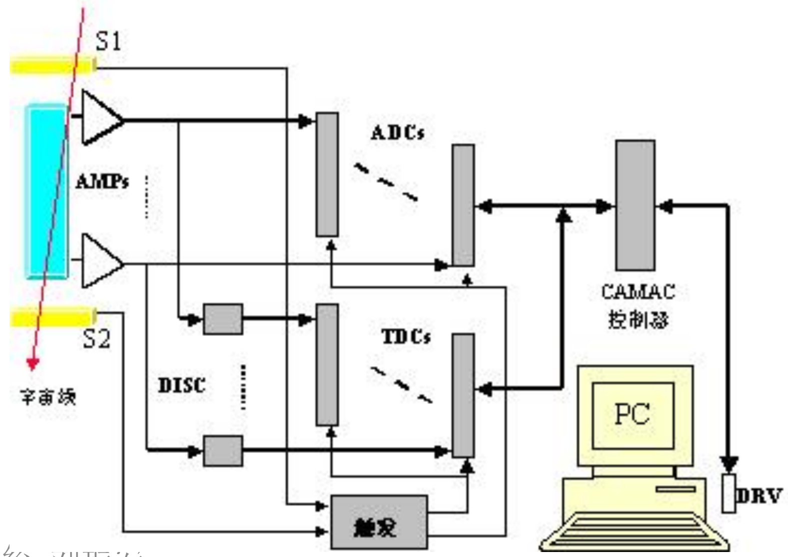
实验物理中的Trigger/触发

- 有多少人在实验室做过探测器的性能测量实验？
- 怎么把探测器的信号数字化并存到计算机上的？

实验物理中的Trigger/触发

- 放射源实验物理
  - 放射源强度
  - 电信号幅度
  - 阈值调节
  - 实验结构简单
  - 数据量小
  - 好事例明确
- 宇宙线实验物理
  - 原理及结构同放射源实验
  - 不同在触发逻辑
  - 特点
    - 时间长
    - 效率低
    - 靠天吃饭





加速器物理实验非常必要

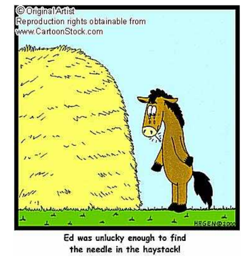
实验物理中的Trigger/触发

- 加速器实验物理
  - 优点
    - 可重复
    - 效率高
    - 时间短
    - 物理目标可控
  - 缺点
    - 本底高
    - 假事例多
    - 存储数据量巨大，资源不够
    - 分析困难耗时

犹如大海捞针：find a needle in a Haystack

加速器实验物理中Trigger/触发的困难

找好事例如大海捞针：find a needle in a Haystack

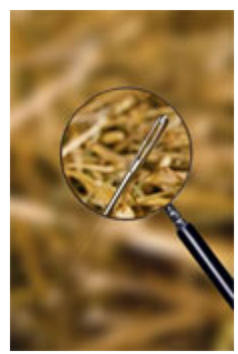


1.怎么办哪？？
无从下手！！

2.苦干加实干不信找不到！！

3.不行啊，哪天能找到啊！！

4.有没有可能？？？

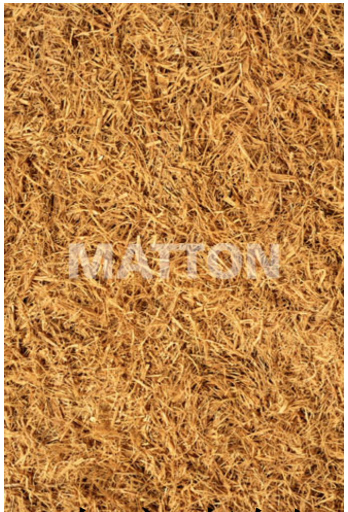


5.愁死啦！！！

6.别愁啦，快找触发组啊！！

实验物理中的Trigger/触发

加速器物理实验中的触发+判选

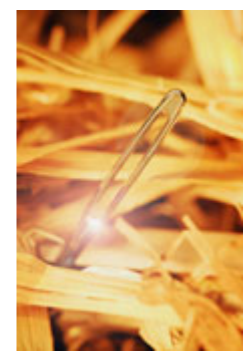


本底事例

好事例

- 设计高效的触发判选
  - 定义好事例（缝衣针）和本底（麦秸）的特征
  - 找出不同（界限）
  - 节省资源
  - 高效
  - 实时

本底事例



找到的好事例

基于加速器之实验物理中的触发目标

触发判选系统的目标:

选择所有感兴趣的事例（好事例），不丢失或少丢失

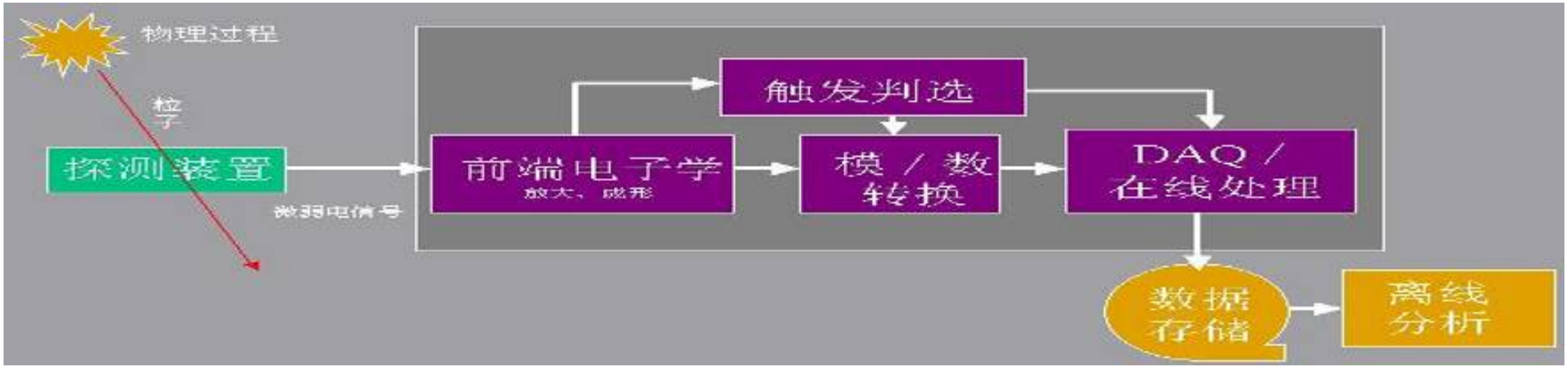
尽量多地拒绝各种本底事例，使得触发事例率DAQ系统足以承受。

死时间少

- 好事例:
  - 任何想要的事例
  - 可以是对撞产生的事例
  - 也可以是宇宙线事例
  - 随实验的目的而定
  - 不同的实验好事例可以不同.

- 本底:
  - 任何与实验的目标不一致的事例.
  - 宇宙线事例
  - 束流丢失粒子（失焦，丢速，Toucheck 效应）

触发和DAQ在高能物理实验中的位置



电子学： 将探测器输出的信号放大、成形等处理后数字化，将信息暂存并作数据预处理；

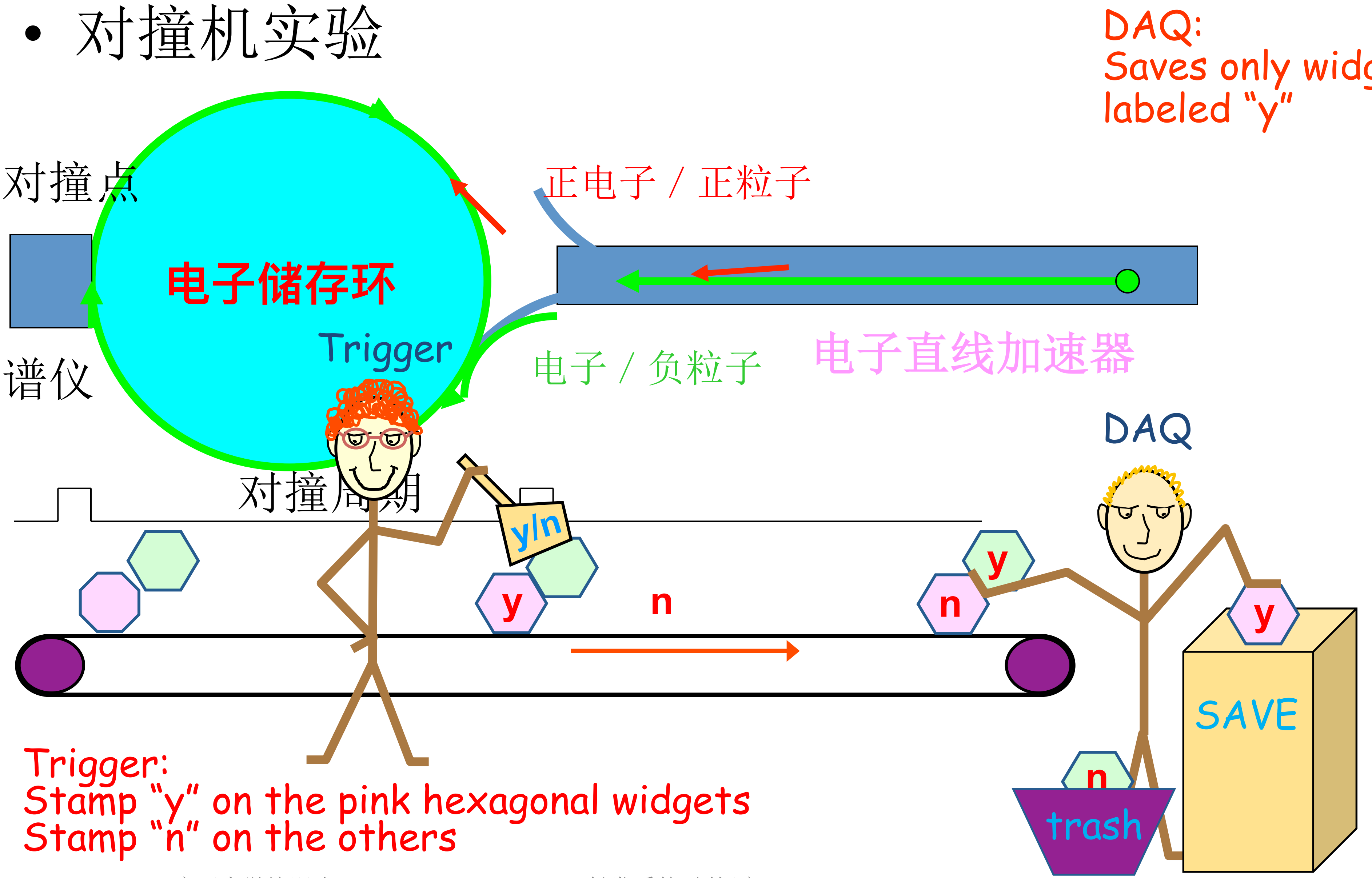
触发+判选： 选择满足物理条件的好事例，压缩本底事例；

数据获取和在线分析： 读出通过触发判选的好事例数据，以数字形式记录下来；给出反映探测器性能的各种统计图形以及所获事例的分类统计图形，监测探测器与电子学工作状态；

离线数据分析： 将在线机上记录下来的数据在离线机上进行分析和处理，把数据还原为粒子种类、能量、动量等物理量。

一般触发系统的原理与构成

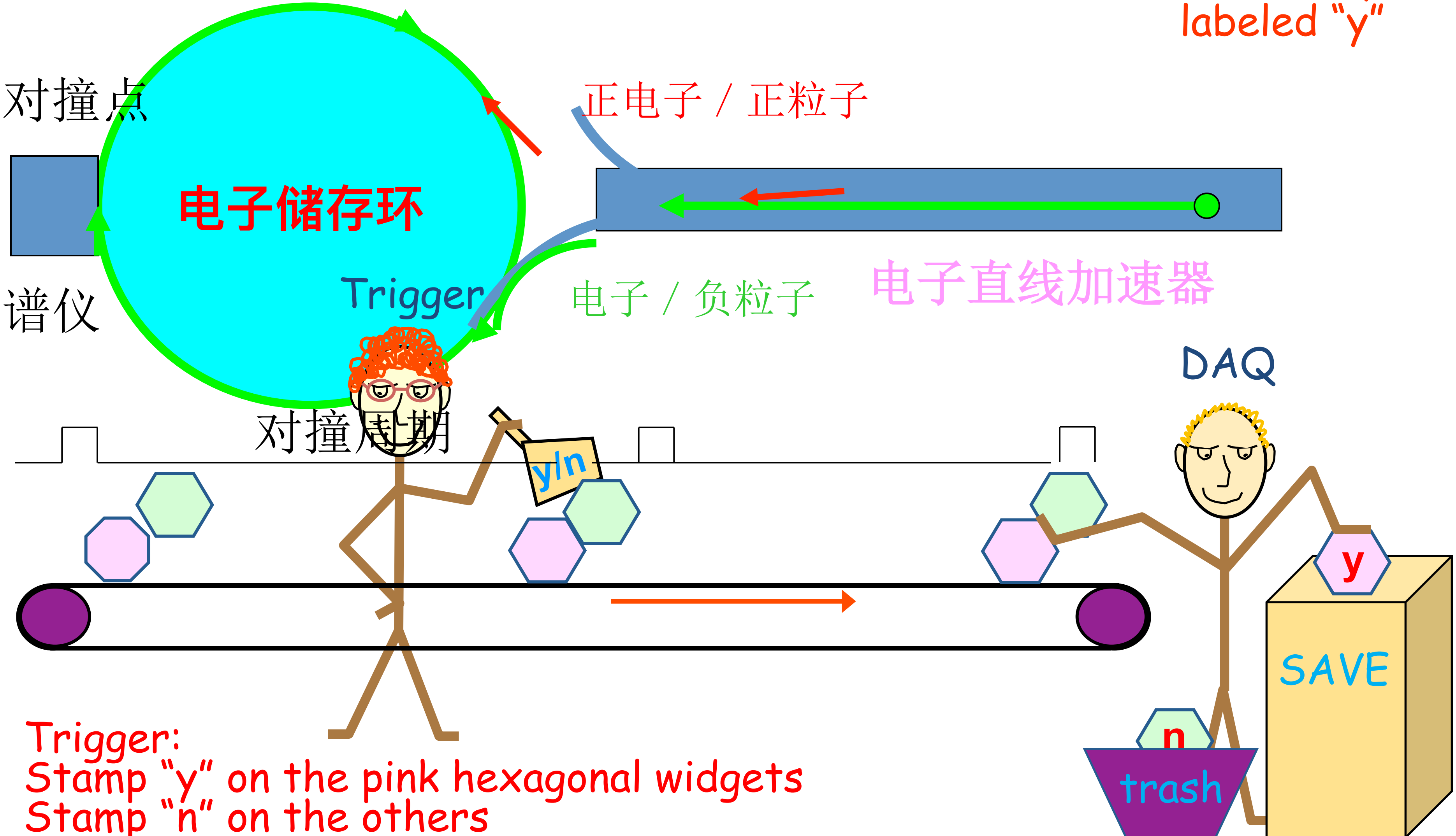
- 对撞机实验



Trigger:
Stamp "y" on the pink hexagonal widgets
Stamp "n" on the others

一般触发系统的原理与构成

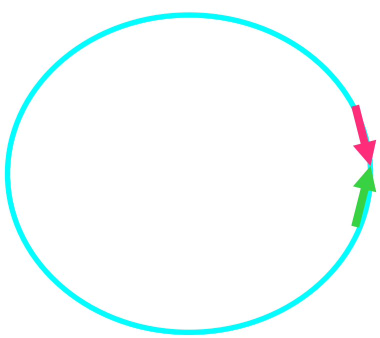
DAQ:
Saves only widg
labeled "y"

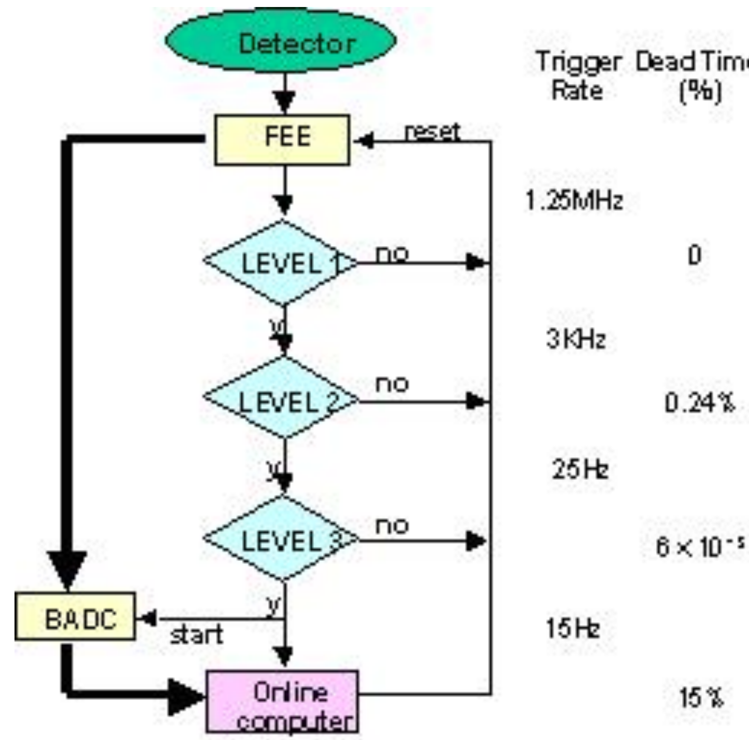


Trigger:
Stamp "y" on the pink hexagonal widgets
Stamp "n" on the others

早期对撞机实验的触发工作模式

- 分级处理
  - 第一对撞周期内完成LVL1判选（快信号）
  - LVL2在第二对撞周期完成（慢信号）
  - 第三对撞周期后开始数字化等



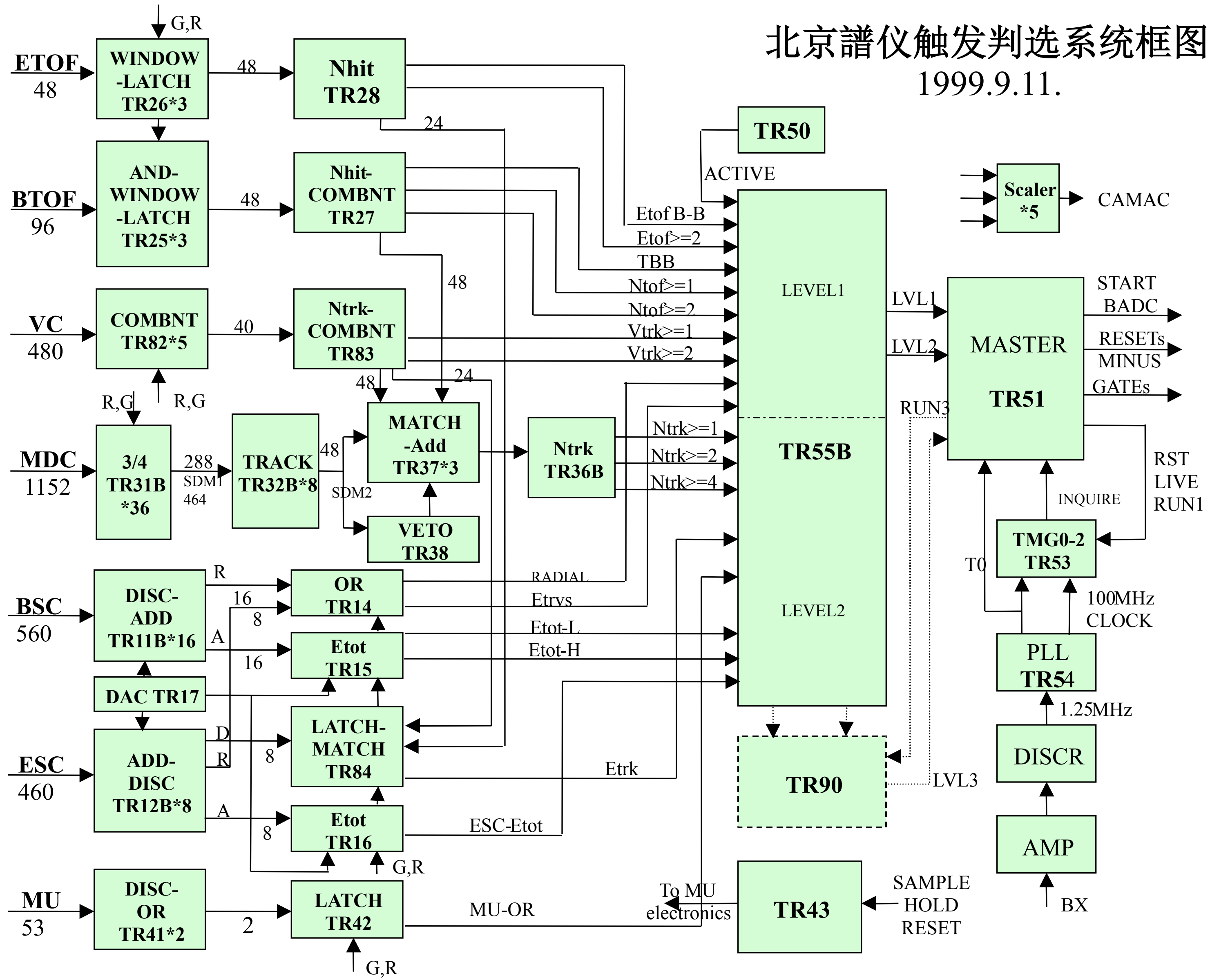


BESI/II Trigger System

早期触发系统案例1
BESI/II触发系统

- BEPCI
  - 低亮度（多少？）
  - 单束团模式
  - 束团间隔: 800ns
- BESI/BESII 触发
  - 信号处理时间足够
  - 锁存-处理-判断
  - 三级处理

BES2 触发系统

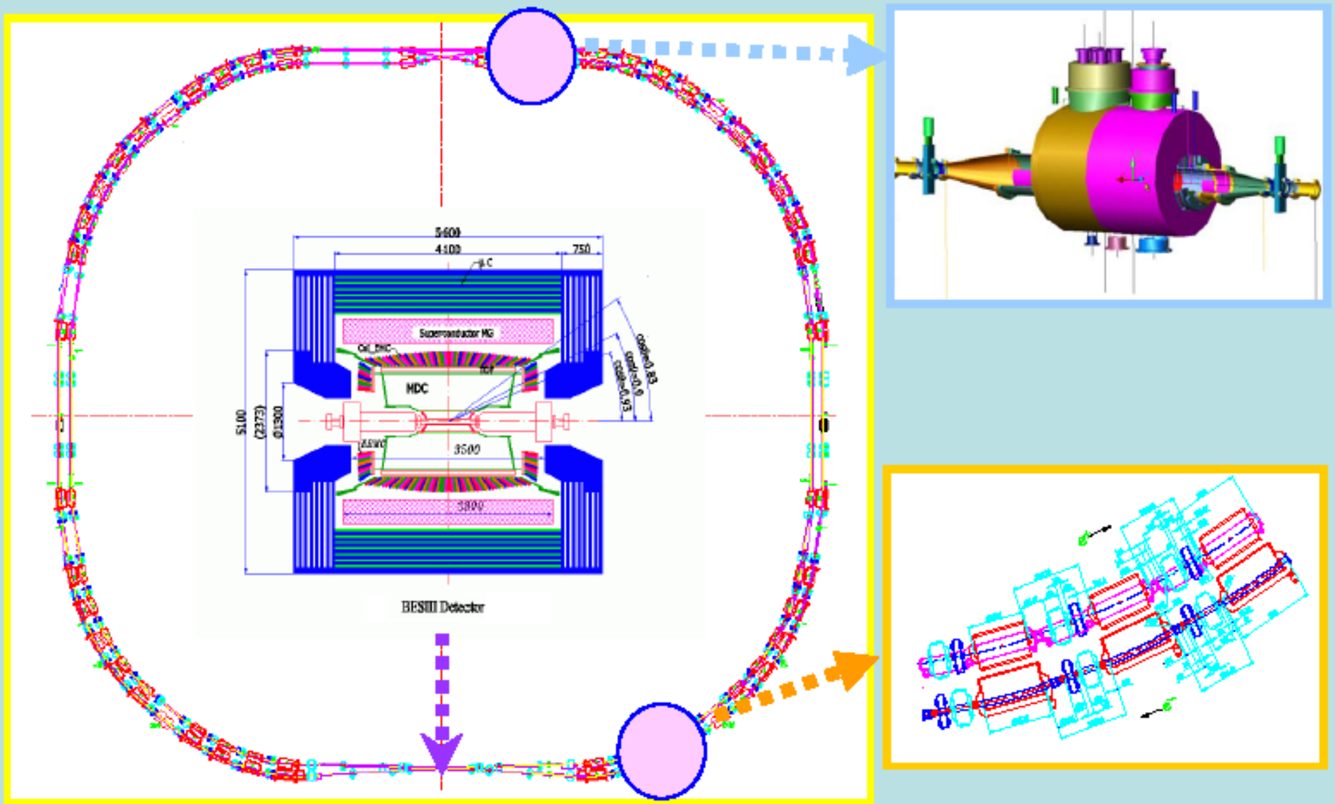


• 单数团，800ns, 有足够的处理时间

实验物理

BEPCII Project

BEPCII: High Lumi. Double–ring Collider

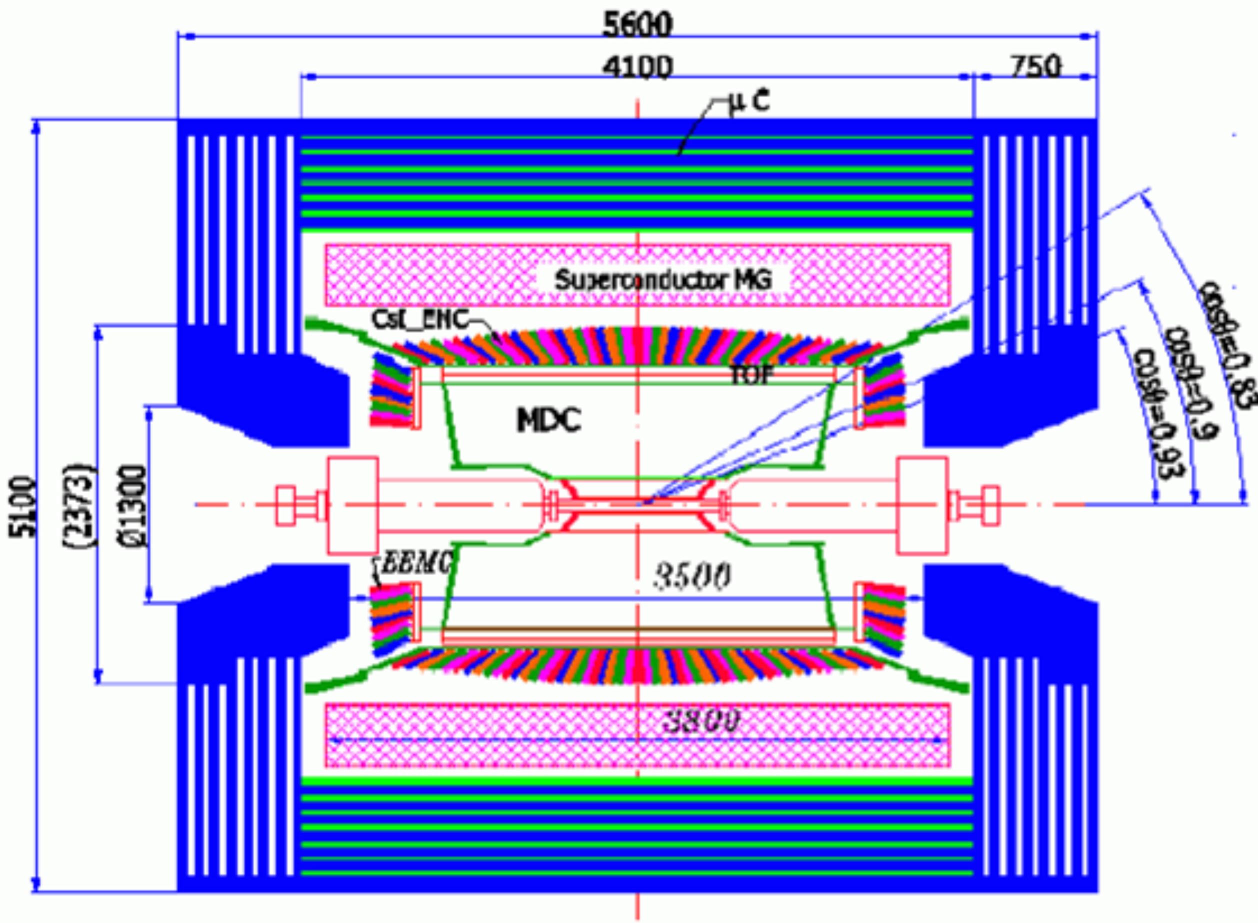


Build new ring inside existing ring . Two half new rings and two half old rings cross at two IR's, forming a double ring collider.

Luminosity: 3~10×10^{32}cm^{-2}s^{-1} @ 3.77GeV

BESIII detector

Magnet: 1 T Super conducting



MDC: small cell & He gas
σ_{xy}=130 μm
s_p/p = 0.5% @1GeV
dE/dx=6%

TOF:
σT = 100 ps Barrel
110 ps Endcap

EMCAL: CsI crystal
ΔE/E = 2.2% @1 GeV
σz = 0.5 cm/√E

Muon ID: 9 layer RPC

Trigger: Tracks & Showers
Pipelined; Latency = 6.4 us

Data Acquisition:
Event rate = 3 kHz
Thruput ~ 50 MB/s

- **Adapt to high event rate of BEPCII:**
  $10^{33}cm^{-2}s^{-1}$ and bunch spacing 8ns
- **Reduce sys. errors to match high statistics**
  photon measurement, PID…
- **Increase acceptance**

新型触发案例2
BESIII触发系统

- BEPCII
  - 亮度高
  - 多束团模式
  - 束团串间隔: 48ns
  - 束团间隔: 8ns
- BESIII+FEE
  - 全新电子学
  - 全新触发思想
  - 流水线工作模式

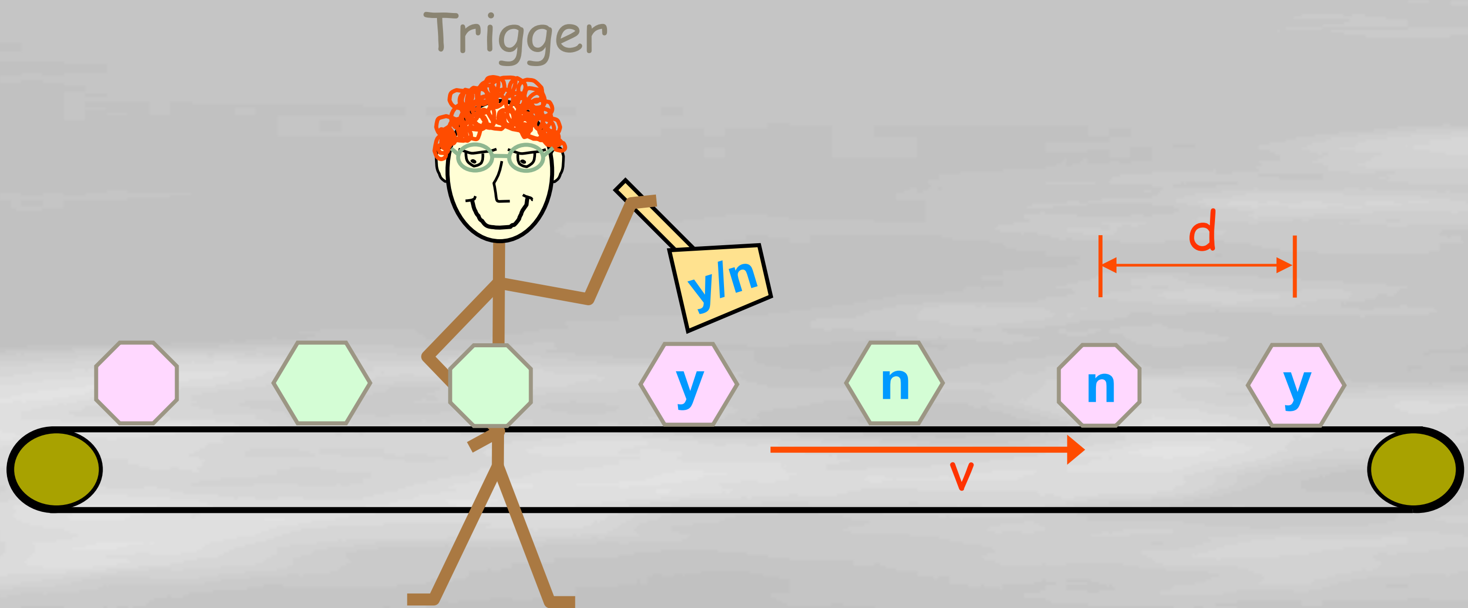
流水线的工作原理

The problem is:
Working fast means you make some mistakes !

Requirements: Decision Time

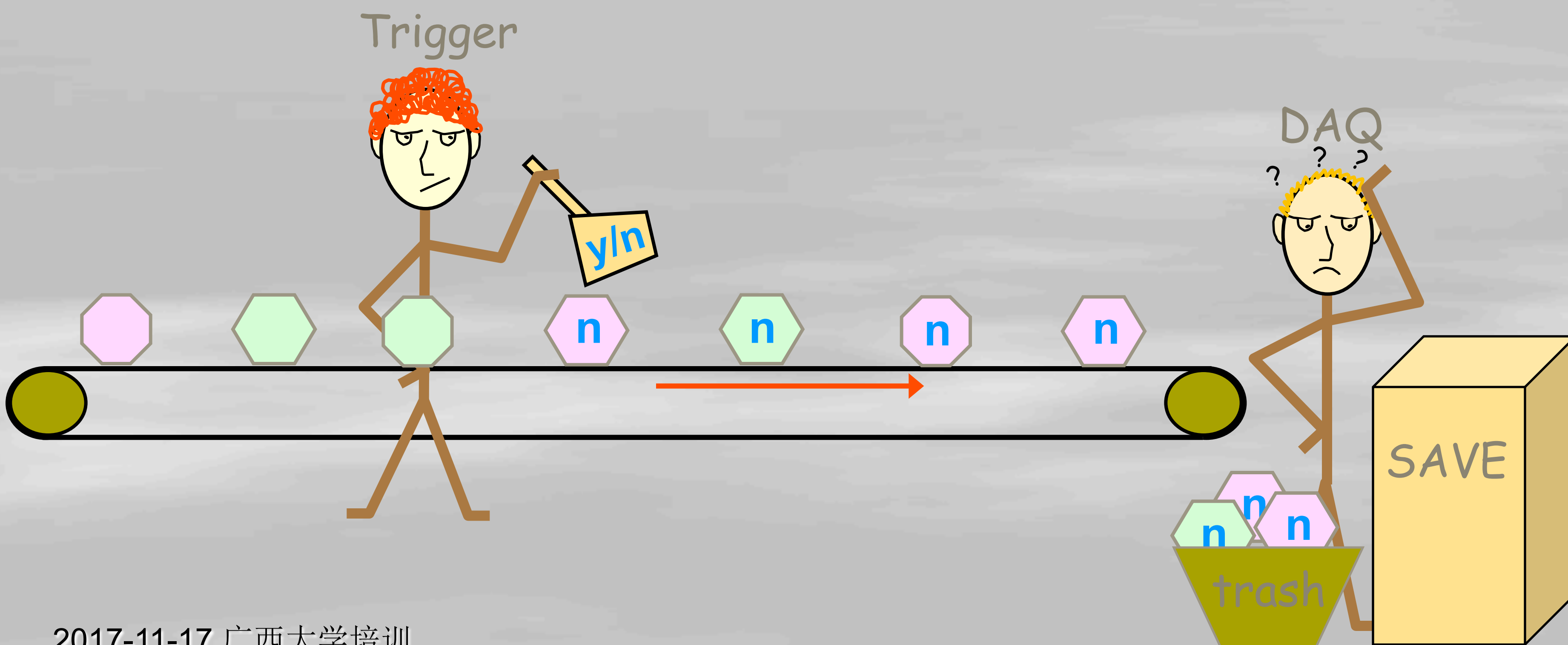
Each widget must get examined and stamped

- To decide on one before the next one comes along.
- The decision can't take longer than $\Delta t = d/v$.
- Taking more time means making less mistakes.



Requirements: Efficiency

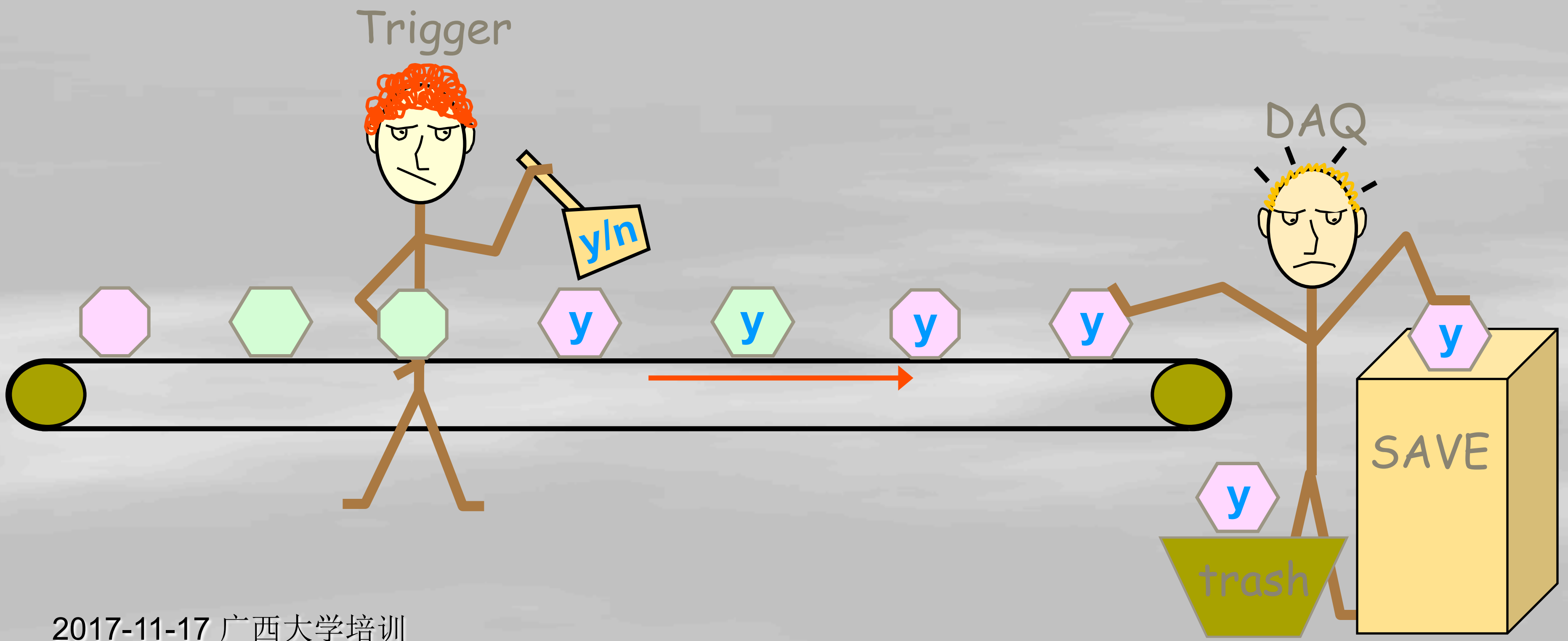
Can't stamp too many pink hexagonal widgets "n":



Requirements: Rejection

The rate of widgets stamped “y” can’t exceed the capacity of the DAQ to save them.

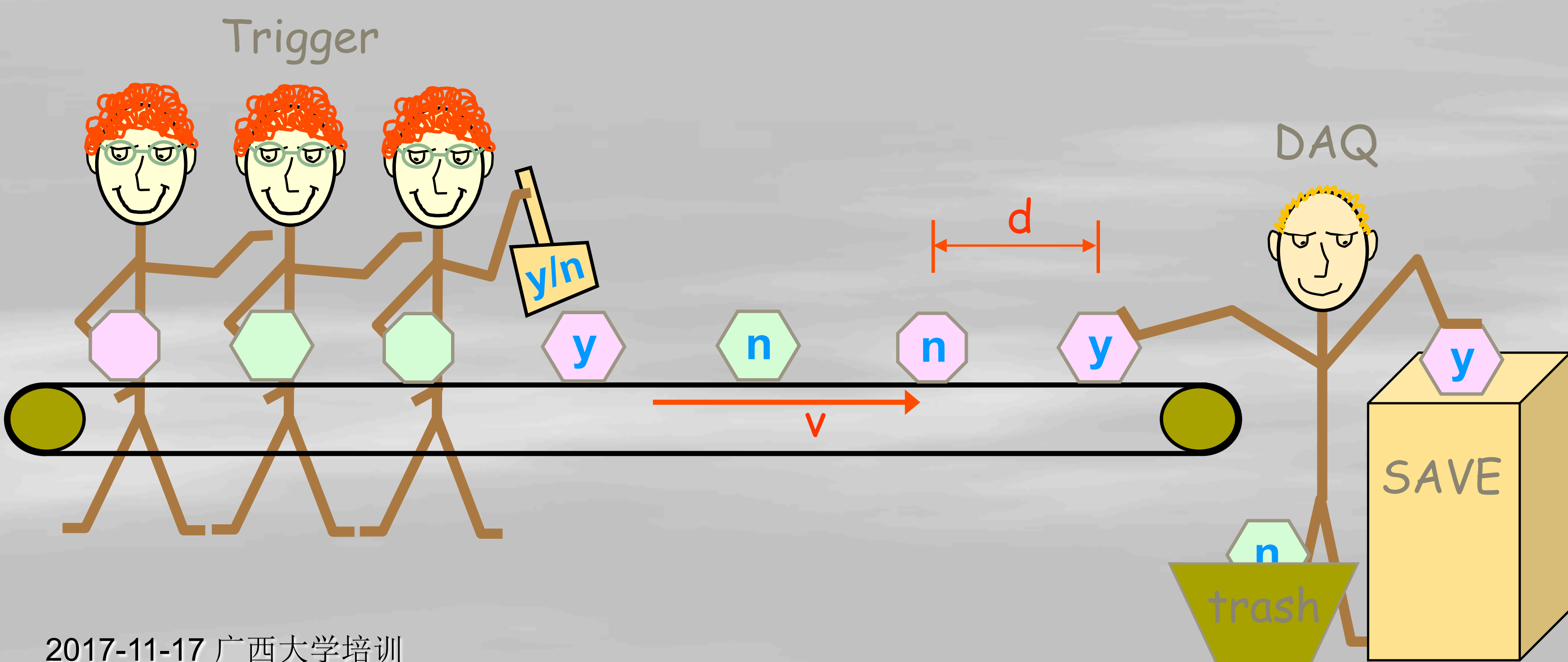
Whenever the DAQ is busy saving something it causes “dead-time” (he will miss the next few widgets). If he misses any marked “y”, this causes a loss of efficiency.



Working in Steps: Pipelining

Have more than one person working in series

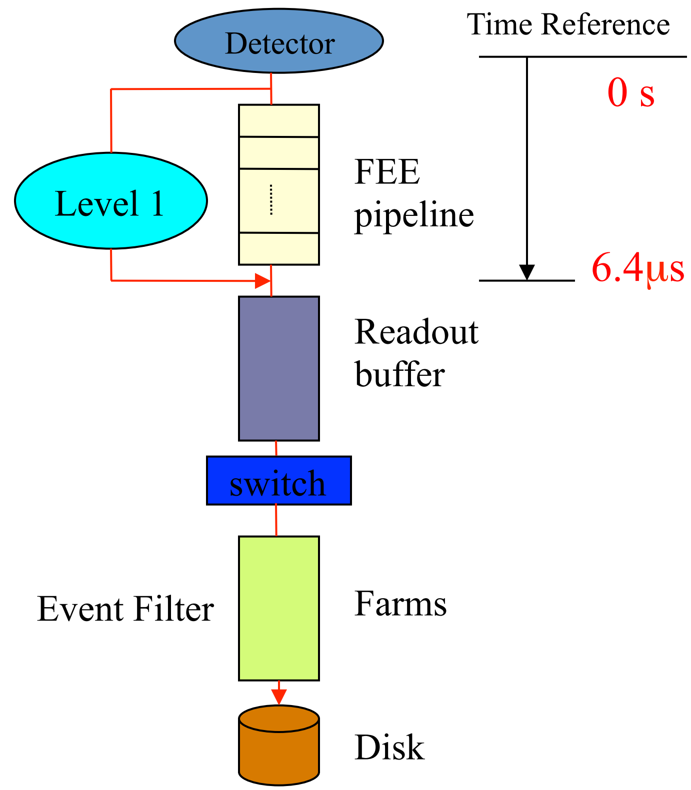
- Each individually one takes less than $\Delta t = d/v$
- Collectively, much more work is done
- A smarter decision can be made – less mistakes



BESIII触发系统方案

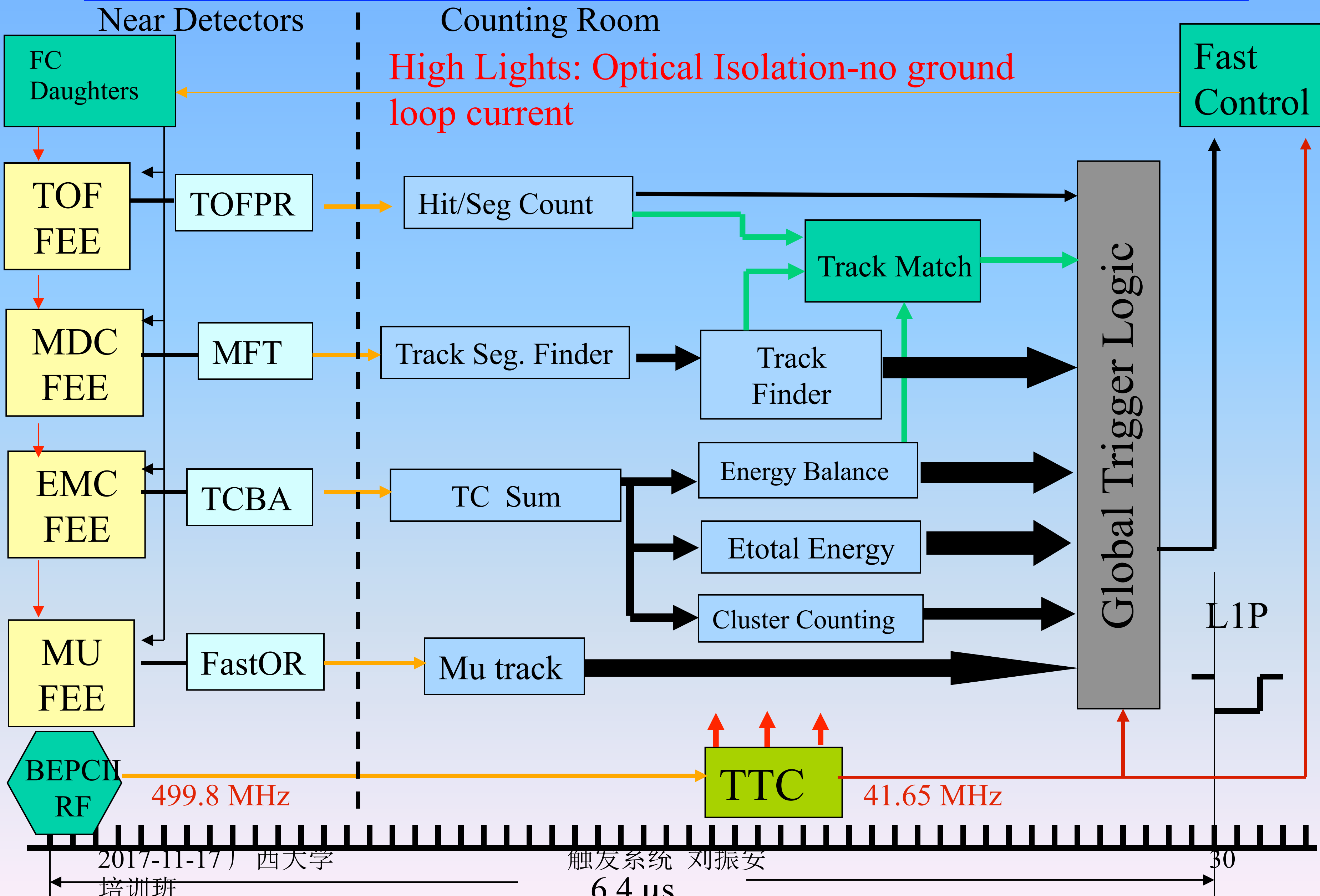
BESIII实验对触发系统的要求：

- 事例率
  - 好事利率: ~ 2000Hz
  - Bhabha 事例率: ~800Hz
  - 宇宙线事例率: <200Hz, rejection > 10:1
  - 束流本底事例率: <2000Hz, rejection > 10000:1
  - 总事例率: 4000 Hz
- 触发流水线工作方式
  - BEPCII 多束团模式（93），束团间距：8ns
- L1不确定性：0.4 μs
- 触发L1信号延迟输出：6.4 μs，数据存储在流水线缓存器
- L1不能做时间参考，只做数据索引

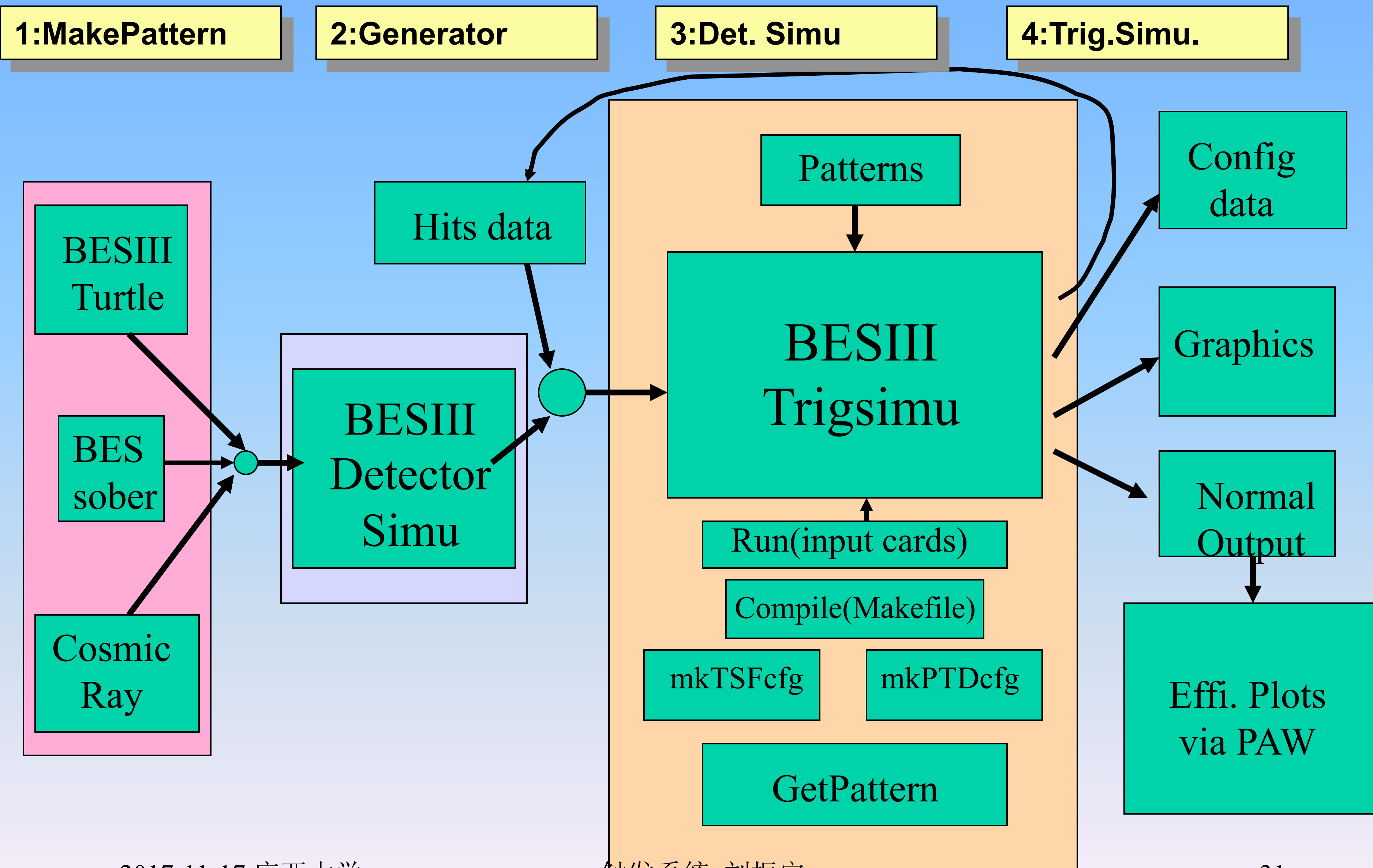


BESIII FEE pipeline and Data flow

BESIII触发方块图



BESIII触发方案可否？模拟先行



研究、比较了各种触发方案；研究了触发方案中各个参数的合理设置，并确定了径迹组合、阈值等

问题

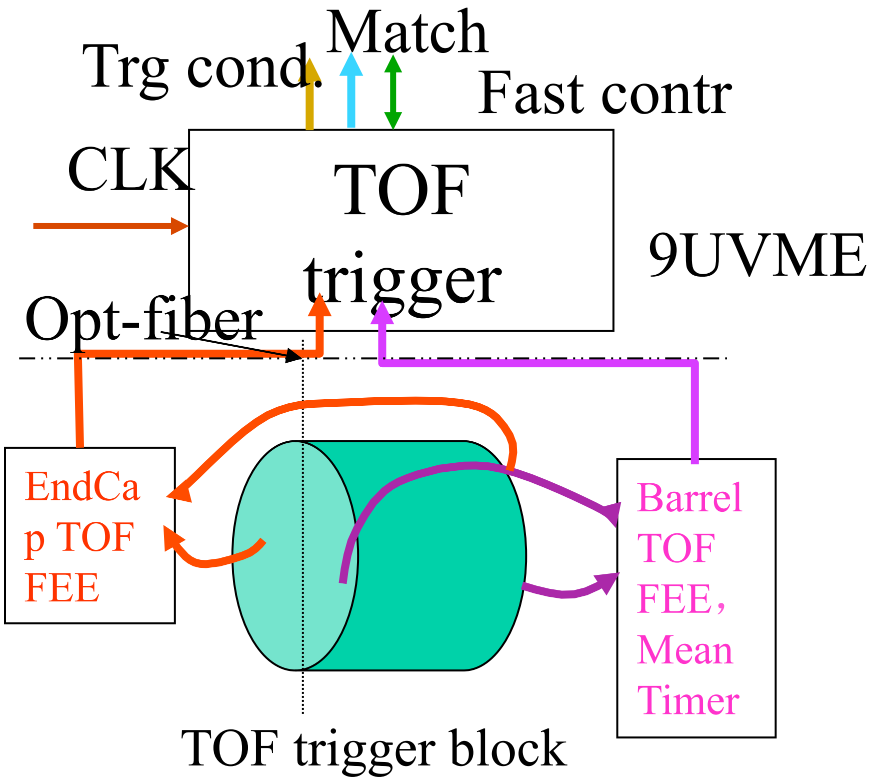
- 基于什么进行触发？

问题

- 基于什么进行触发？
  - 时间
  - 横动量 / 径迹
  - 能量/粗团（cluster)
  - 相关性（匹配）
- 产生触发条件（Primitives)
- 总触发（global/correlation)

BESI / II基于时间的触发

- 飞行时间
  - T = Tparticle_flight + Tsig_go + Tfee_delay ~30ns
- 飞行时间大于30ns
  - 非对撞事例



BESIII 基于TOF的触发

- 精确时刻
  - T = Tparticle_flight + Tsig_go + Tfee_delay ~30ns
- 击中数
- 对称性

模拟触发条件表

Detector	Trigger Condition	bits	**Comments**
TOF	Ntof≥1 Ntof≥2 TBB	3	TOF hits number (TOF timming) Back to back hits
ETOF	Netof≥1 Netof≥2 ETBB	3	(ETOF timming)
MDC	NLtrk>=1 NLtrk>=2 LTrk-BB NLtrk>=N NStrk>=1 NStrk>=2 STrk-BB NStrk>=N NItrk>=1 NITRK>=2	10	Full Track number Back to back tracks Many tracks Short Tracks number With Inner DC hit
EMC	NClus>=1 NClus>=2 BclusBB EclusBB Clus_PHI Clus_Z Diff_B, Diff_E, BL_BEMC, BL_BLK BL_EEMC BL_Z Etot_L, Etot_M BEtot_H EEtot_H	16	Cluster number(EMC timming) Back to back cluster Cluster balance at φ One cluser at each half of EMC Energy difference between each B half Energy difference between each E half Energy Balance between half BEMC Energy Balance of barrel blocks Energy Balance between half EEMC Z energy balance (B+E) Tatol Energy >Thre-l Tatol Energy >Thre-m Tatol energy of Barral EMC Tatol energy of Endcap EMC
MATCH	NAtrk≥1 NAtrk≥2 ATRK-BB NBtrk≥1 NBtrk≥2 BTRK-BB NCtrk≥1 NCtrk≥2 CTRK-BB	9	Atrk=MDC Full track+TOF hit OR MDC Full track+TOF hit+ EMC Cluser Btrk= ETOF hit + EEMC Cluster OR ETOF hit + EEMC Cluster +MDC Short Track Ctrk=MDC Track+Inner MDC hit
		41	

- 作用
  - TOF
    - 带电粒子的定时与触发
    - 排除本底
  - MDC
    - 带电粒子的触发
    - 排除本底
  - EMC
    - 中性粒子的触发
  - Match
    - 径迹匹配进一步排本底

触发表

	Charge1	Charge2	Charge3	common	neutralA	neutralB	BhaBha BEMC	BhaBha EEMC
NLtrk>=1	Y	Y						
NStrk>=2		Y						
Strk-BB			Y				Y	Y
Ntof>=1	Y							
Bclus-BB							Y	
Eclus-BB								Y
Clus-PHI				Y	Y			
Clus-Z				Y				
Diff-E								Y
BL-LBK							Y	
BL-EEMC								Y
BL-Z						Y		
Etot-L	Y			Y				
Etot-M					Y			
Eetot-H								Y

模拟的触发效率

Events generated and simulated with Geant	Trigger efficiency(%)/background rate
Bhabha @3.097Gev	100
Radiative BB(3.097GeV)	100
$J/\psi \to \gamma\ \eta \to 3\gamma$	99.99
$J/\psi \to \omega\ \eta \to 5\gamma$	99.99
$J/\psi \to K^+K^-\pi^0$	99.69
$J/\psi \to$ P Pbar	99.91
$J/\psi \to$ anything	99.80
J/ψ (2S)$\to$anything	99.50
J/ψ (3770)$\to$anything	99.90
Lost beam backgrounds	1.85kHz
Cosmic-ray backgrounds	86Hz

- 我们从中可以看到触发效率是很好的。本底事例率接近边界。在调试过程中通过备用的触发条件加以调整。

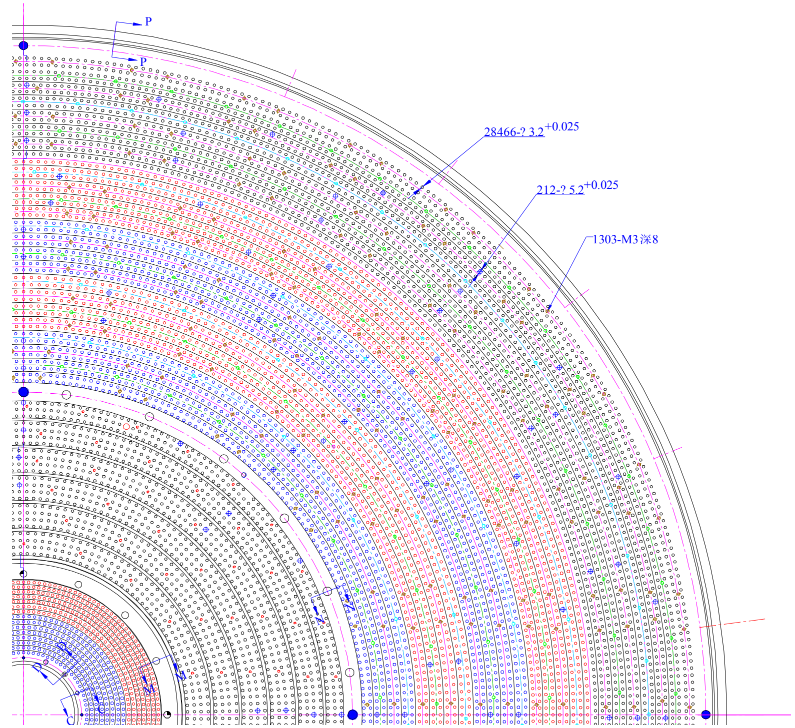
方案与硬件实现原理介绍

- 经过认真仔细地模拟
- 采用光纤传输技术实现所有电子学系统间隔离，排除BESIII电子学的共地干扰问题
- 使用当前先进可靠的FPGA芯片，提高系统可靠性
- 使用IN－SYSTEM下载和VME下载技术，实现系统灵活性
- 硬件设计尽量一致，不同FPGA内容实现不同功能，提高系统可维护性(ITKF1-2,TKF1-8,LTKC/STKC,ETOT/CSUM,SAFA/B/C)
- 采用RocketIO技术，简化系统规模

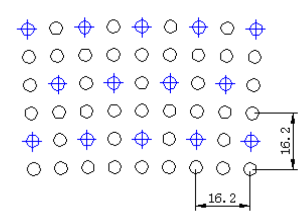
MDC 子系统

- Parameters of MDC trigger

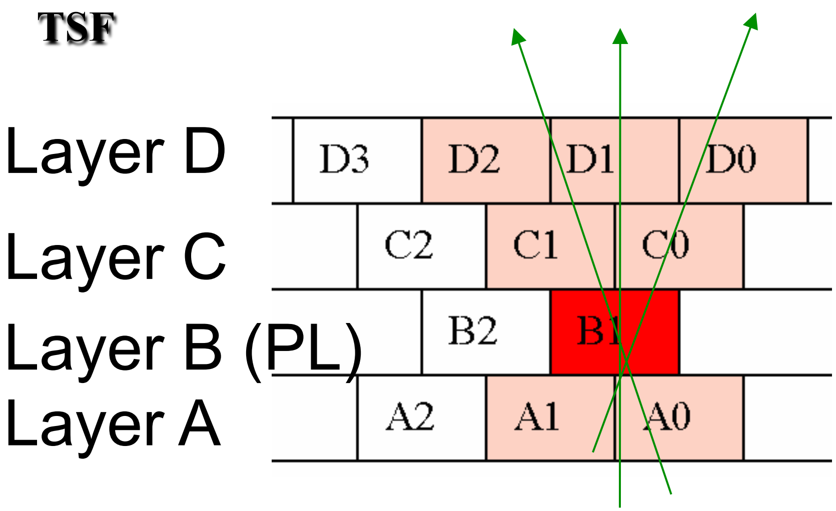
Super Layer	Wire Layer	# of sig.				# of WL in SL	Pivot Layer	# of pivot cells SL
		L1	L2	L3	L4			
SL-1	ST-1/2/3/4	40	44	48	56	4	3	48
SL-2	ST-5/6/7/8	64	72	80	80	4	3	80
SL-3	AX-9/10/11/12	76	76	88	88	4	3	88
SL-4	AX-13/14/15/16	100	100	112	112	4	3	112
SL-5	AX-7/18/19/20	128	128	140	140	4	2	128
SL-6	ST-21/22/23/24	160	160	160	160	4	2	160
SL-7	ST-25/26/27/28	176	176	176	176	4	2	176
SL-8	ST-29/30/31/32	208	208	208	208	4	2	208
SL-9	ST-33/34/35/36	240	240	240	240	4	2	240
SL-10	AX-37/38/39/40	256	256	256	256	4	2	256
SL-11	AX-41/42/43	288	288	288	0	3	2	288
Total	43	6796				/	/	1784

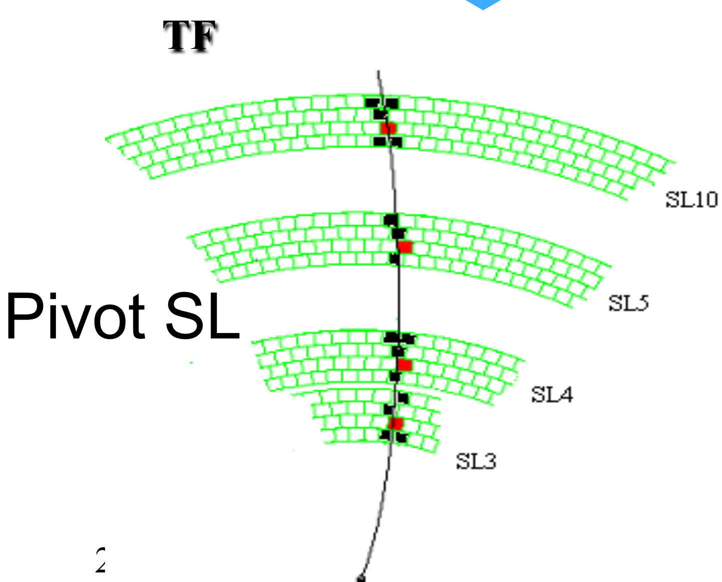


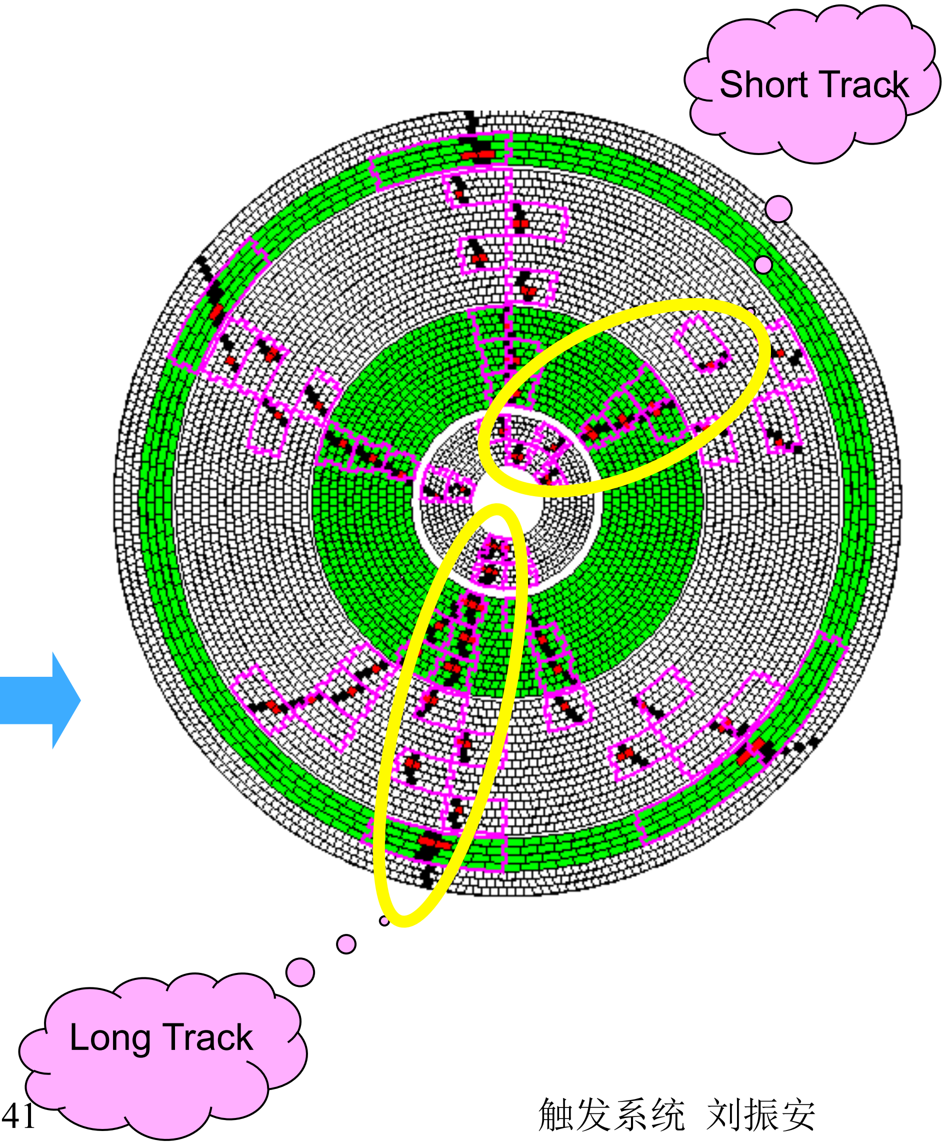
Inner layers
Pivotal layers
Axial layers
Not used layers



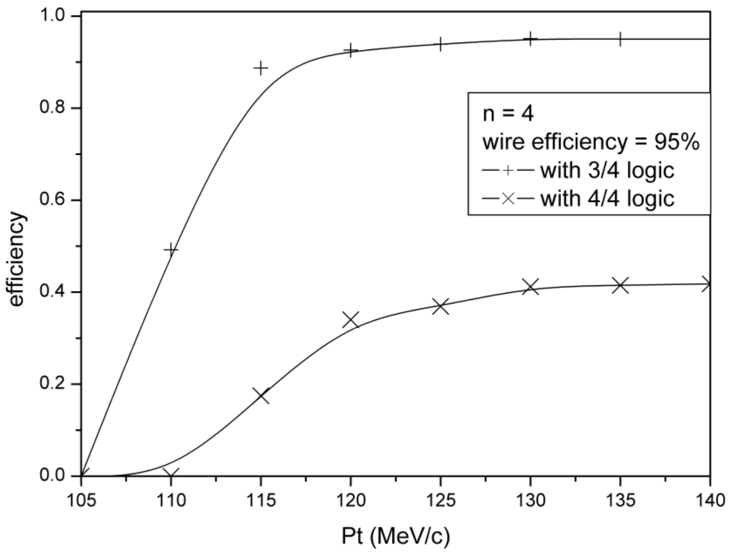
To simplify the hardware implementations, super layers 1^{st} – 5^{th} and 10^{th} are used as MDC trigger sources


TSF
Layer D
Layer C
Layer B (PL)
Layer A
D3
D2
D1
D0
C2
C1
C0
B2
B1
A2
A1
A0

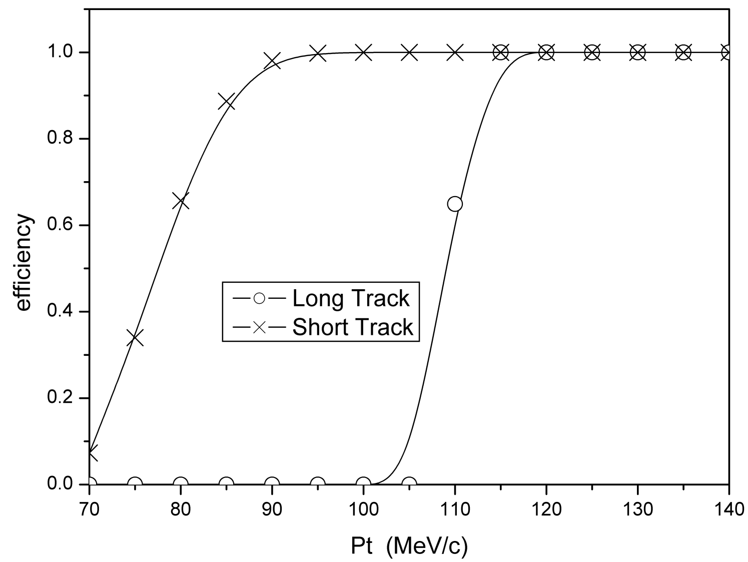

TF
Pivot SL
SL10
SL5
SL4
SL3


Short Track
Long Track

部分模拟结果



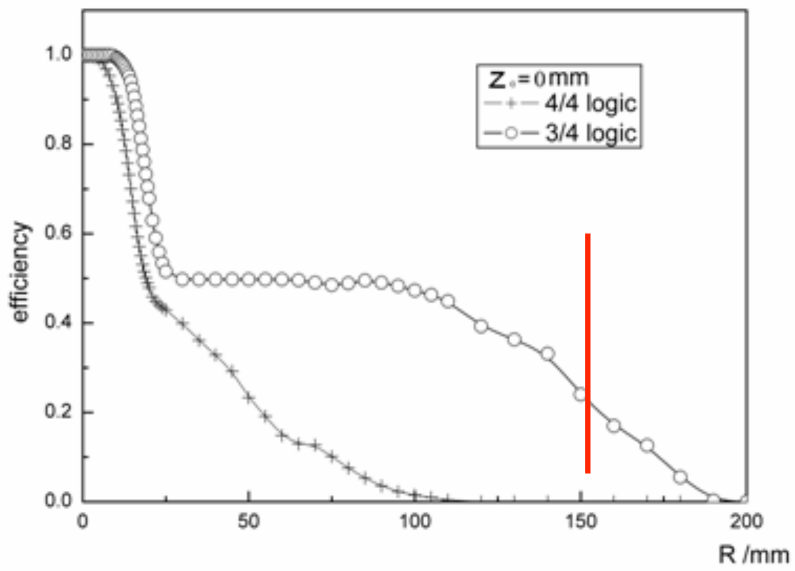
Relations between TSF efficiency and *pt*

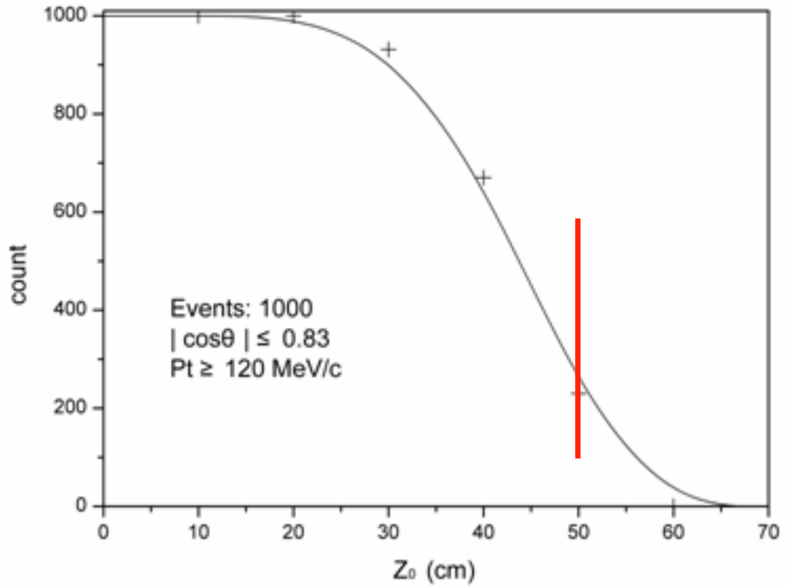


Relations between TF efficiency and *pt*

部分模拟结果(2)

- The track finding efficiencies in the r-ϕ plane and Z direction.
  - For a distance of 15 cm in the r-ϕ plane, the TF efficiency is about 30% for 3/4 TSF logic.
  - For a distance of 50 cm in the Z direction, TF efficiency is about 30%.





It is good to reject backgrounds far from the Interaction Point

MDC 触发条件

- 10 trigger conditions of the MDC trigger are used in BESIII trigger system
- 3 charged channels：
  - Charge1：NLtrk≥1 + Ntof≥1（Number of Hits of TOF）+ Etot-l (Low threshold of the whole EMC total energy，~200MeV)
  - Charge2：NLtrk≥1 + NStrk≥2
  - Charge3：STrk-BB

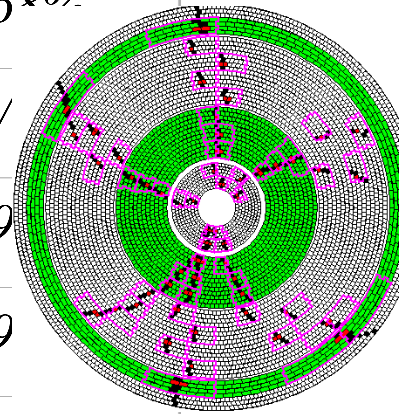
NLtrk⩾1	Number of long track ⩾1；
NLtrk⩾2	Number of long track ⩾2；
NLtrk⩾N	for MDC wires' hits of high voltage sudden discharge
NStrk⩾1	Number of short track ⩾1；
NStrk⩾2	Number of short track ⩾ 2；
NStrk⩾N	for MDC wires' hits of high voltage sudden discharge ；
STrk-BB	Short Tracks back to back ；
NItrk⩾1*	Number of the Track Segments of the SL1 and SL2 are equal to or greater than 1；
NItrk⩾2*	Number of the Track Segments of the SL1 and SL2 are equal to or greater than 2。

* NItrk >= 1 and NItrk >= 2 are for backups to reject beam-related backgrounds.

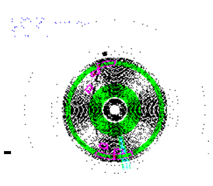
不同物理道的触发效率

Physical channels	Rate of passed charged channels	Rate of passed Global trigger	
$J/\psi \to Anything$	95.38%	97.66%	99.79%
$J/\psi \to K^+K^- \pi^0$	95.58%	97.39%	99.6
$J/\psi \to \pi^0 p\bar{p}$	95.54%	97.94%	/
$J/\psi \to p\bar{p}$	95.08%	95.82%	99.9
$\psi' \to Anything$	97.72%	99.5%	99.9
$\psi'' \to D\bar{D} \to Anything$	97.85%	99.9%	99.97%
Cosmic-ray	/	18Hz	18Hz
Beam related background	/	99.9961%*	(rejection) [illegible]

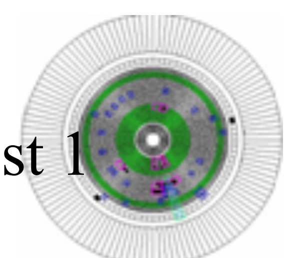
Good Event



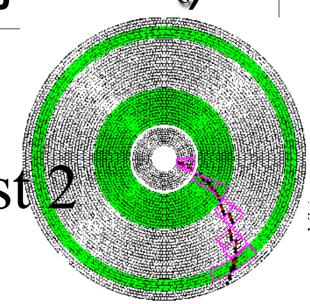
Cosmic



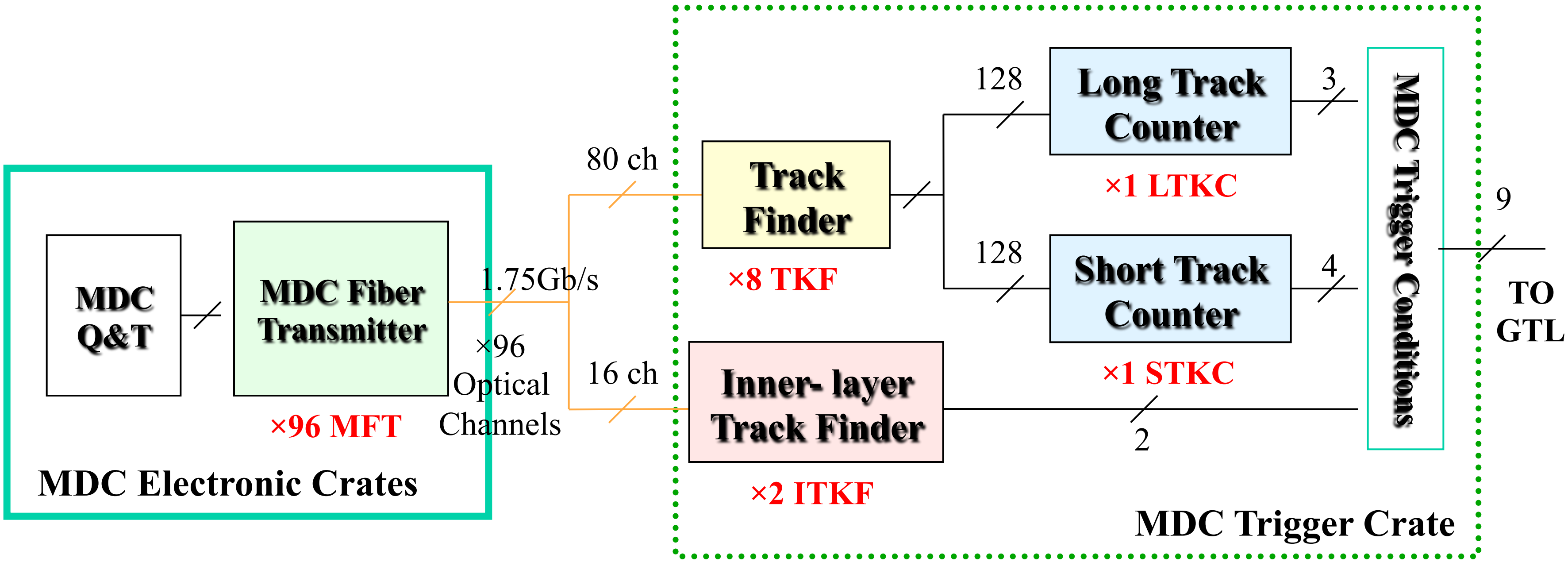
BeamLost 1

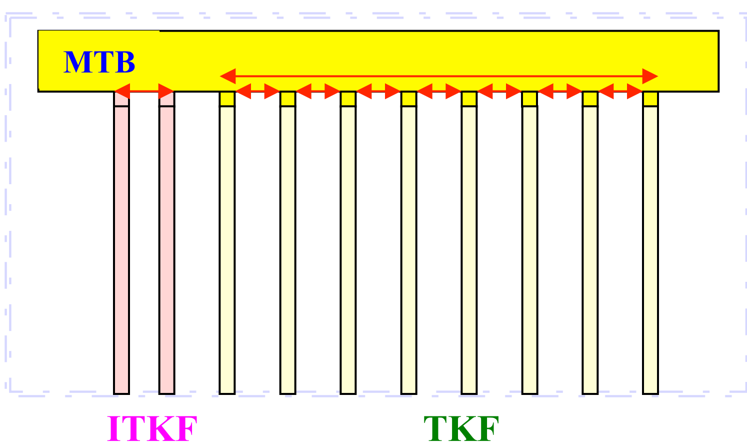


BeamLost 2



MDC 触发的硬件实现

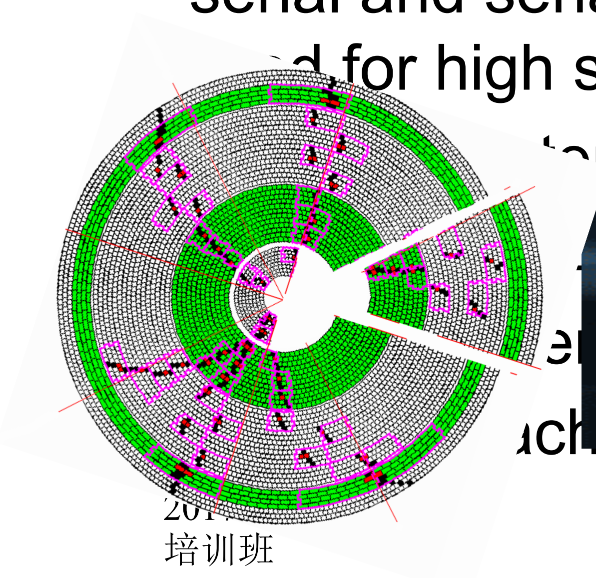


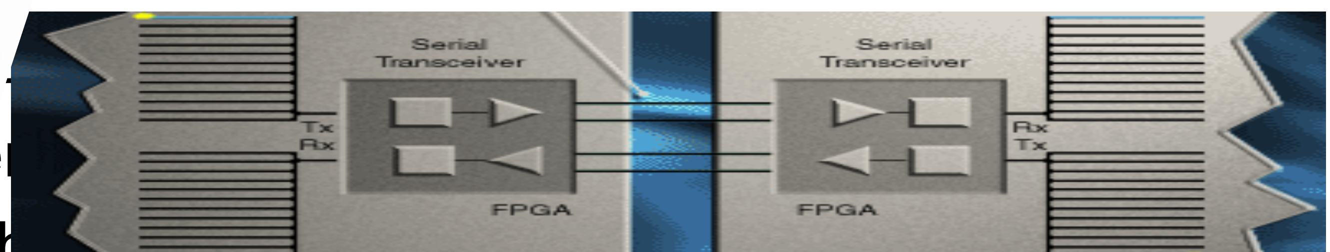


	Type of PCB	Board name	# of boards	FPGA firmware
MDC Fiber Transmitter	1	MFT	96	1
TracK Finder	1	ITKF	2	2
		TKF	8	8
TracK Counter	1	LTKC	1	1
		STKC	1	1
MDC Trigger Backplane	1	MTB	1	
Total	4		109	13

面临的挑战

- **Sectors division and inter-link of neighbour boards**
  - Too many inter-link signals between TKF boards:
  - Input 89, output 89, total 178
  - To reduce cable connect, VME Back-of-Crate card is used in MDC trigger crate to inter-link neighbour boards.
- **RocketIO**
  - All logic, serial-to-parallel and serial-to-parallel are implemented in a Virtex-II Pro FPGA. It has RocketIO Multi-Gigabit Transceivers. The MGTs are flexible parallel-to-serial and serial-to-parallel embedded transceiver cores ...d for high speed data transfer.
  - ...tem data transmission:

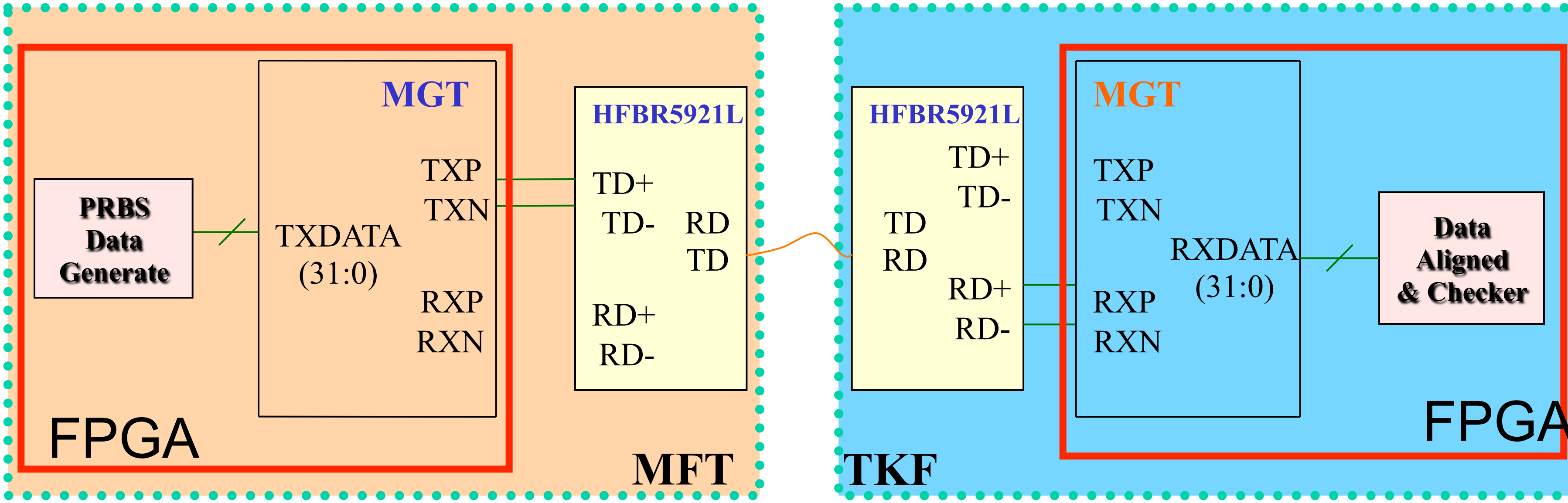


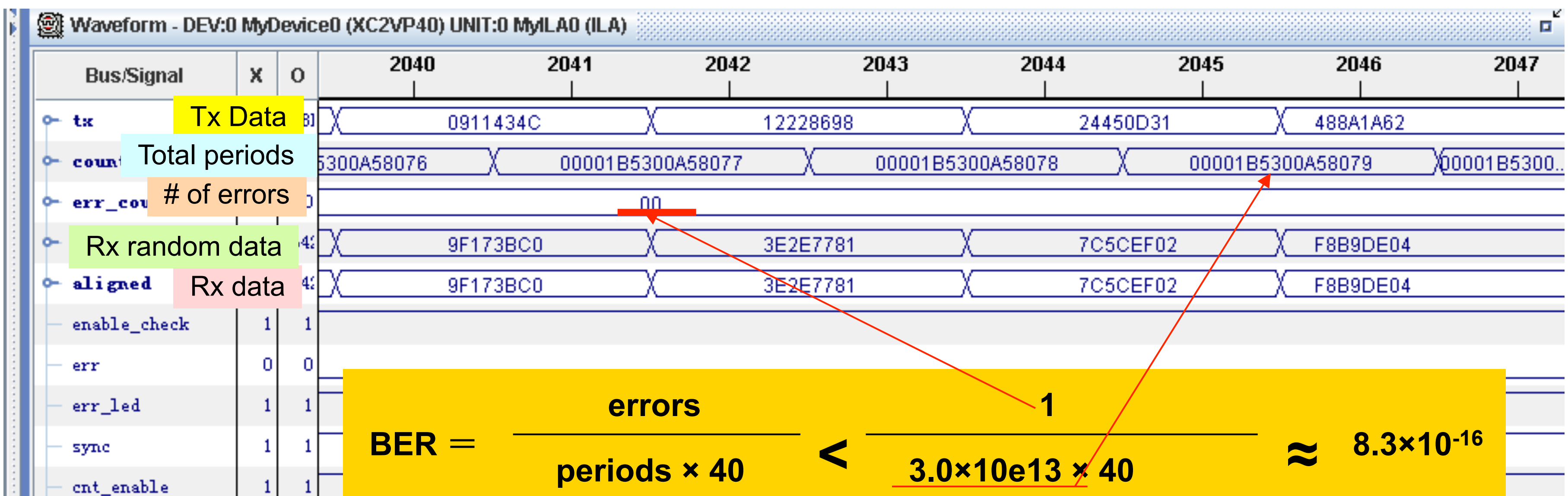


...e...

...ach board.

光纤传输研究





$$\text{BER} = \frac{\text{errors}}{\text{periods} \times 40} < \frac{1}{3.0\times10e13 \times 40} \approx 8.3\times10^{-16}$$


TRACK FINDER
MFT

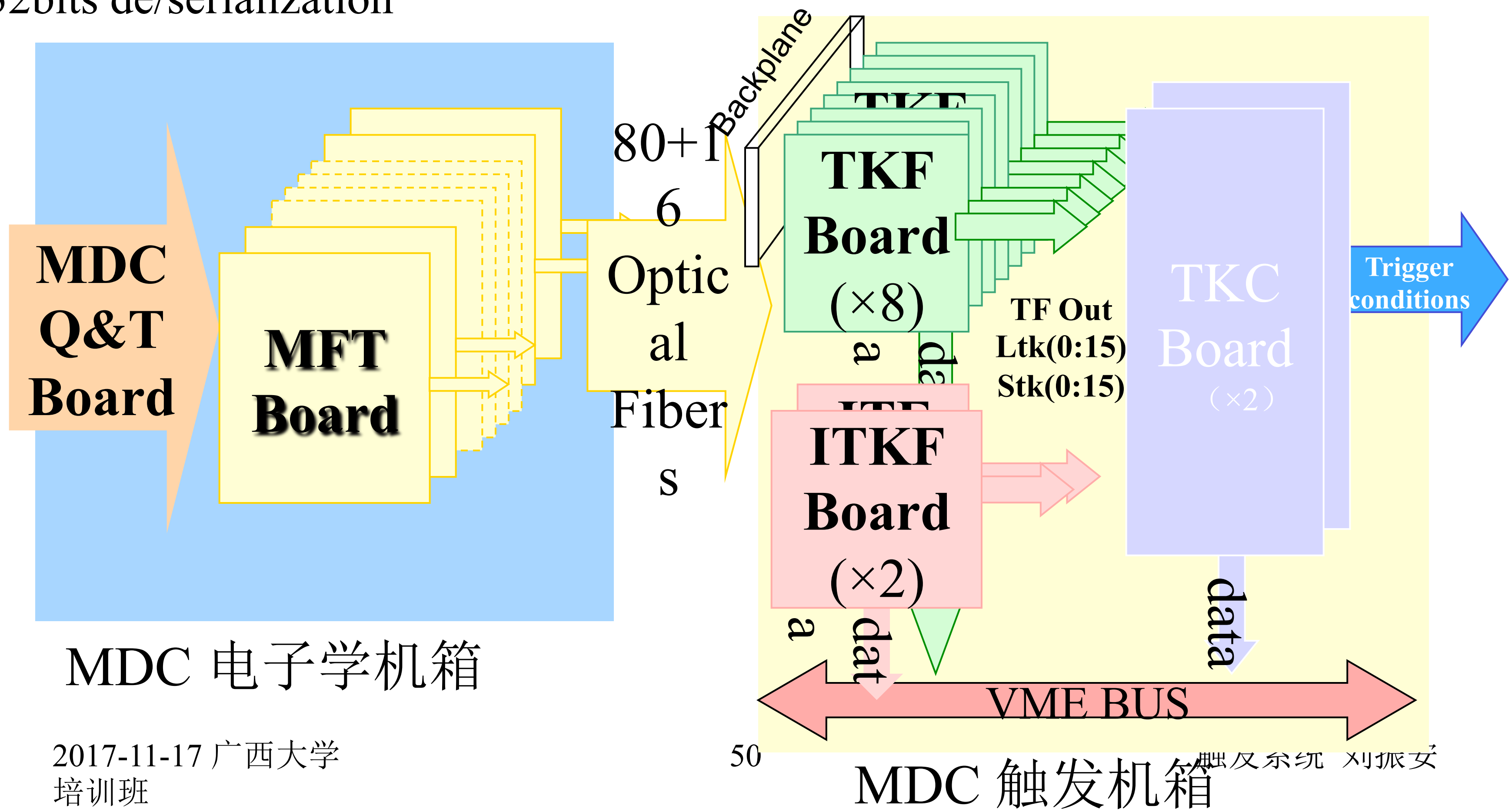
硬件分配

- Xilinx VirtexII Pro
- RocketIO 1.6Gbps
- 32bits de/serialization

MFT: one fiber per board

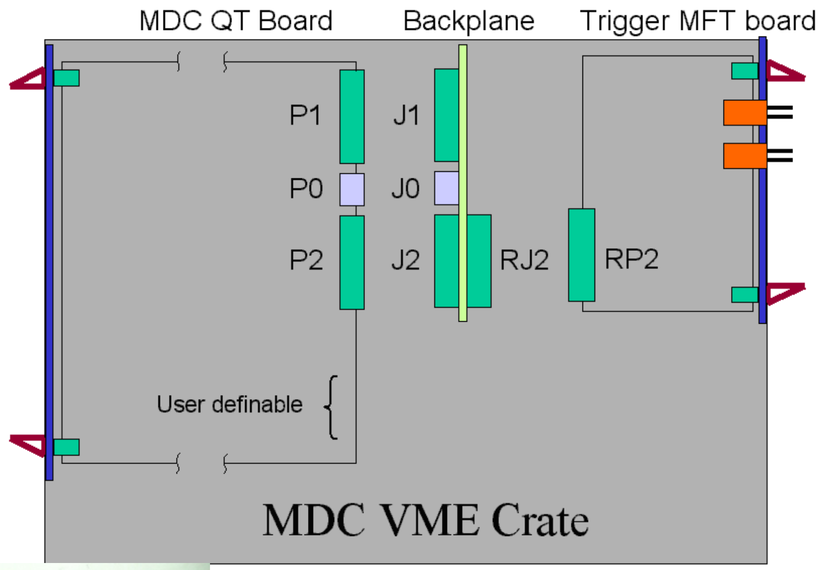
TKF: 8 boards hardware same

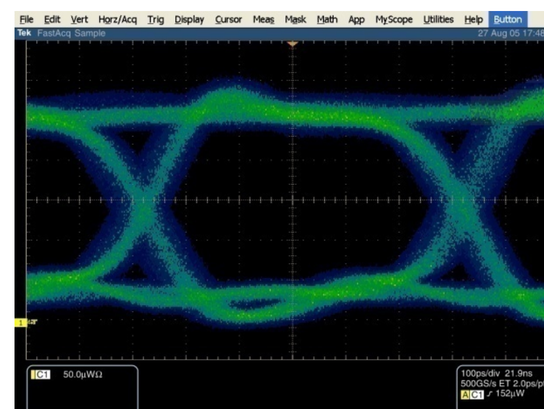
FPGA software similar



MFT (MDC Fiber Transmitter)

- 2796 hits signals from MDC QT boards are collected in MFT, 32 channels per MFT
- Optical fibers are used between MFT and TKF(ITKF) to eliminate common-ground noises
- Virtex-II Pro FPGA: XC2VP2
- 8 layers PCB





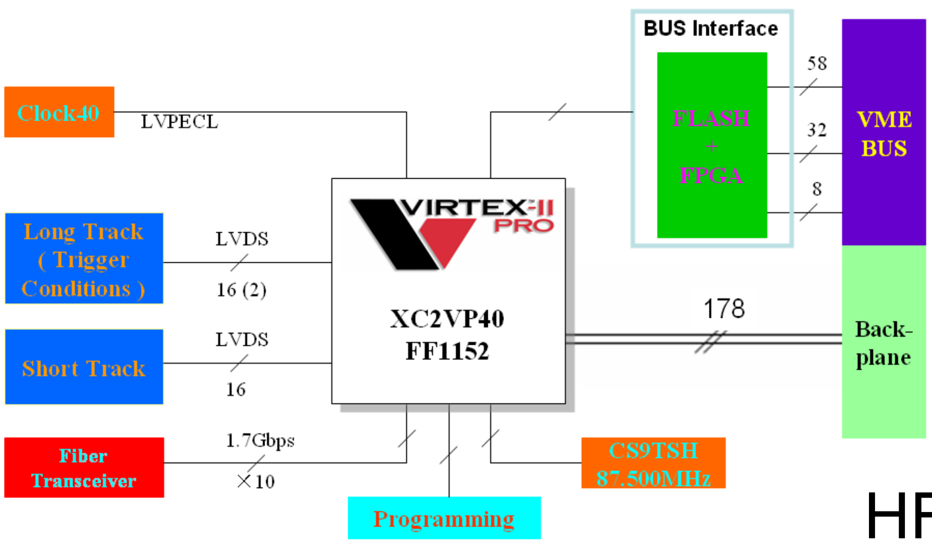
TKF (TracK Finder)寻迹板

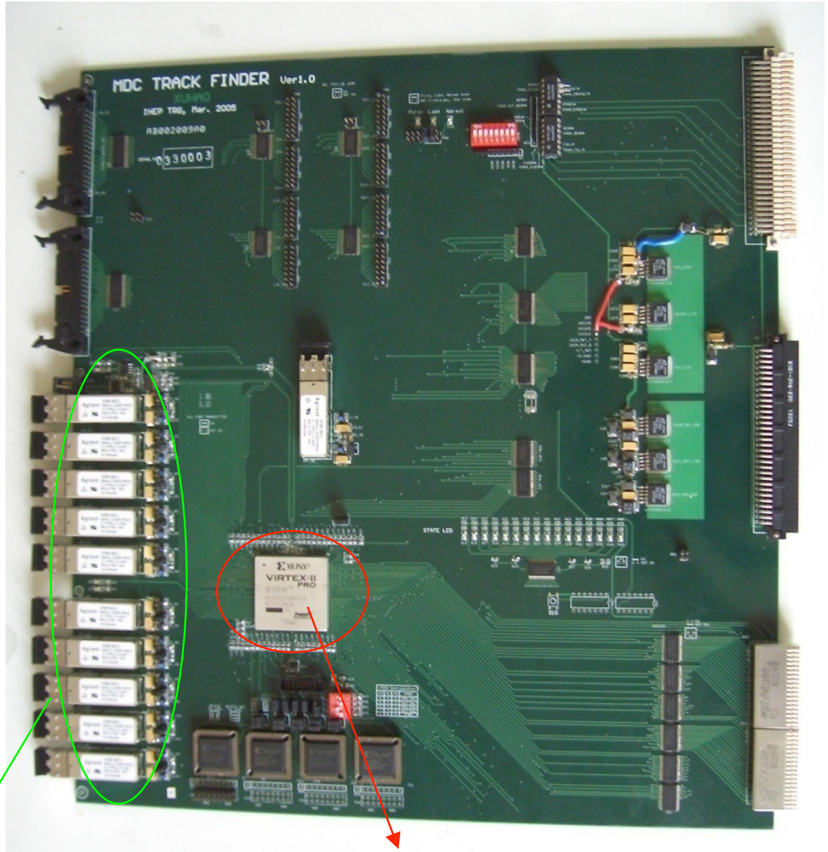
XC2VP40： FF1152, 804 user IOs, 43,632 logic cells, 3,456Kbit BRAM, 12 RocketIOs, 2 PowerPCs, 192 multiplier blocks

10 layers 9UVME PCB

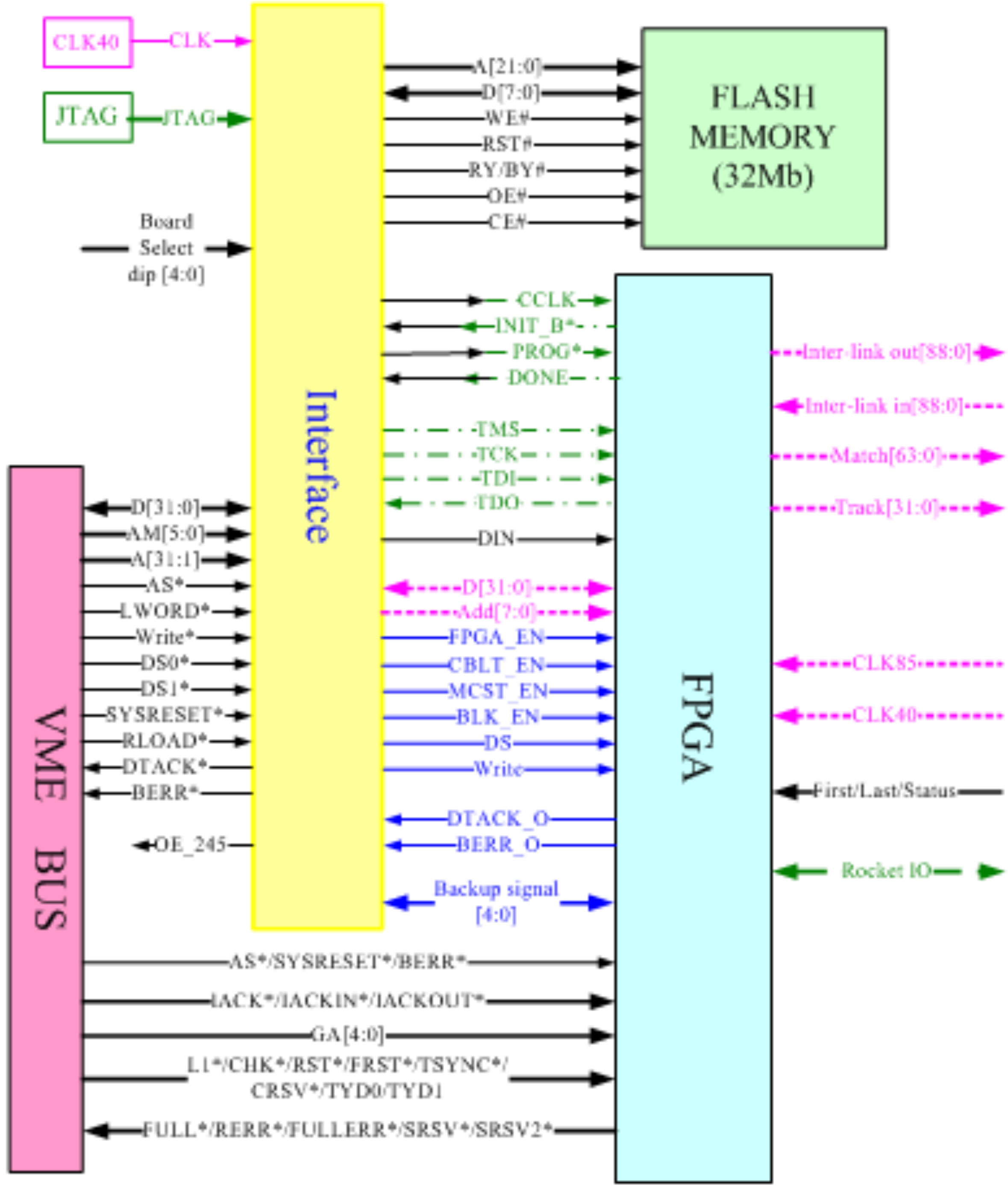
Functions:

- TSF
- TF
- Track information

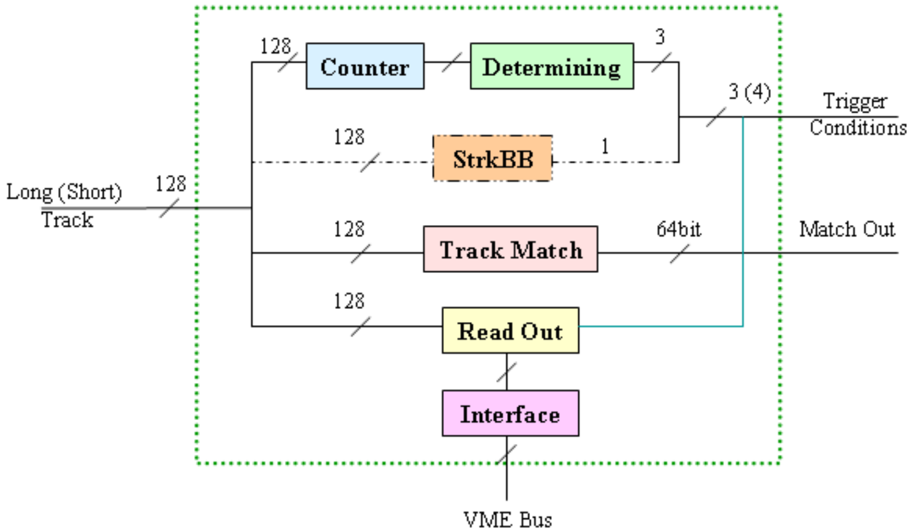


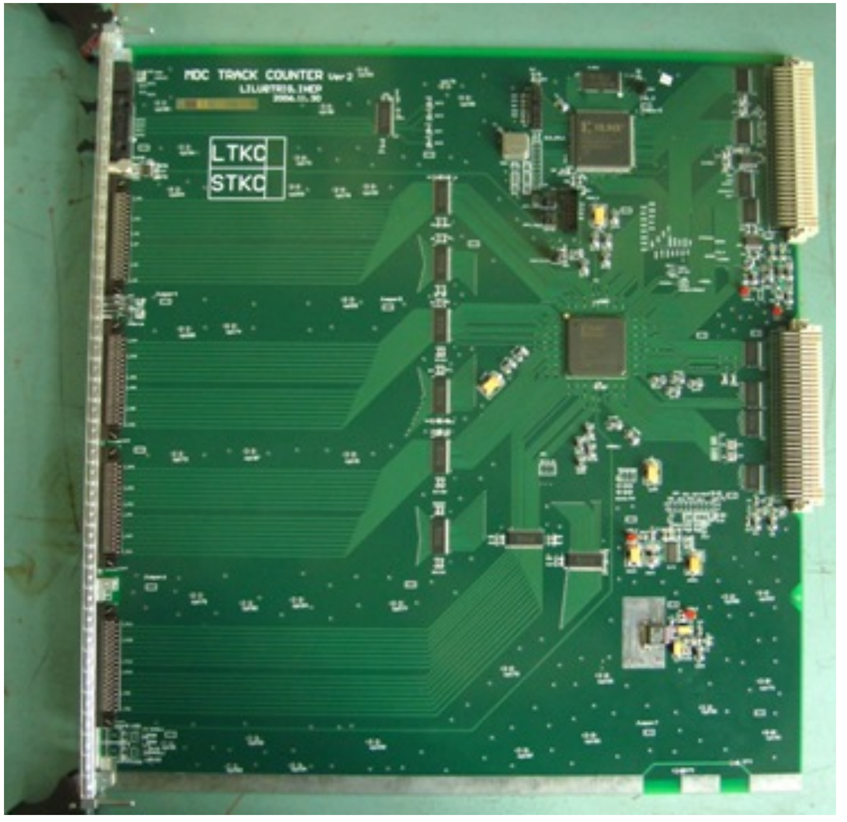


HFBR5921L XC2VP40


CLK40
CLK
JTAG
JTAG
Board Select dip [4:0]
Interface
FLASH MEMORY (32Mb)
A[21:0]
D[7:0]
WE#
RST#
RY/BY#
OE#
CE#
CCLK
INIT_B*
PROG*
DONE
TMS
TCK
TDI
TDO
DIN
D[31:0]
Add[7:0]
FPGA_EN
CBLT_EN
MCST_EN
BLK_EN
DS
Write
DTACK_O
BERR_O
Backup signal [4:0]
FPGA
Inter-link out[88:0]
Inter-link in[88:0]
Match[63:0]
Track[31:0]
CLK85
CLK40
First/Last/Status
Rocket IO
VME BUS
D[31:0]
AM[5:0]
A[31:1]
AS*
LWORD*
Write*
DS0*
DS1*
SYSRESET*
RLOAD*
DTACK*
BERR*
OE_245
AS*/SYSRESET*/BERR*
IACK*/IACKIN*/IACKOUT*
GA[4:0]
L1*/CHK*/RST*/FRST*/TSYNC*/
CRSV*/TYD0/TYD1
FULL*/RERR*/FULLERR*/SRSV*/SRSV2*

TKC (TracK Counter)径迹计数板

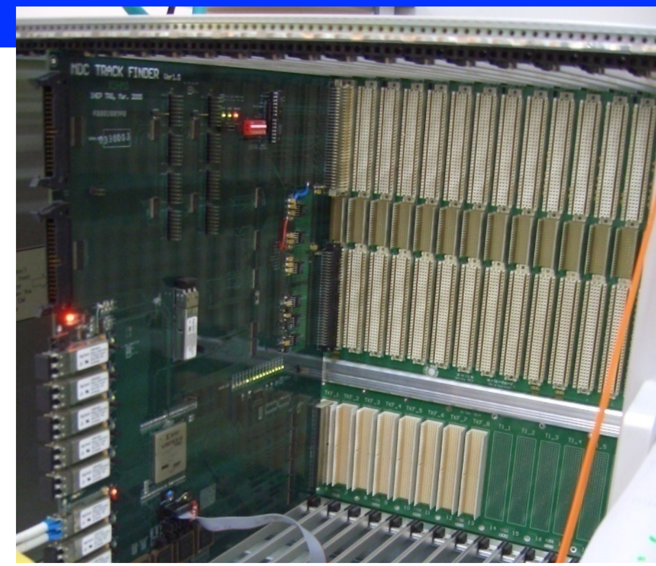


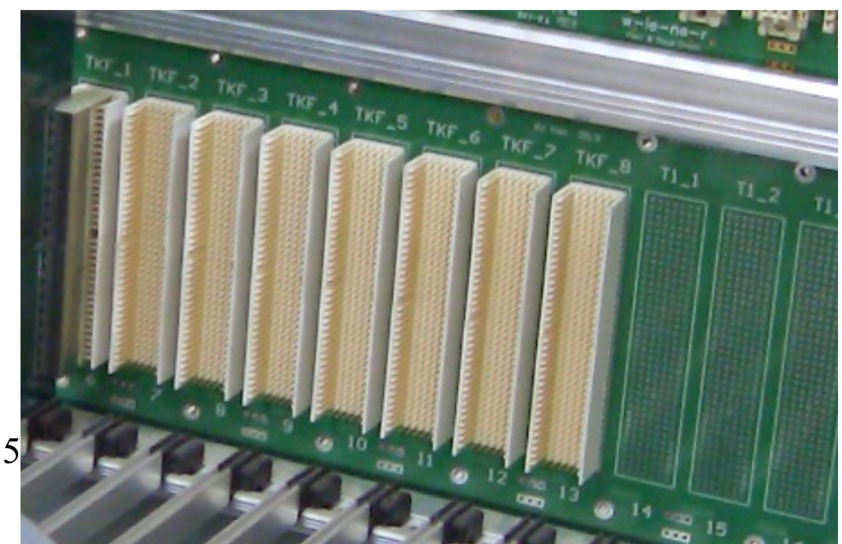


- **LTKC**（Long TracK Counter）
  receives the number of long tracks from TKF and sends the trigger conditions to global trigger
- **STKC** （Short TracK Counter）
  receives the number of short tracks from TKF and sends the trigger conditions to global trigger
- 8 layers PCB

MTB (MDC Trigger Backplane)

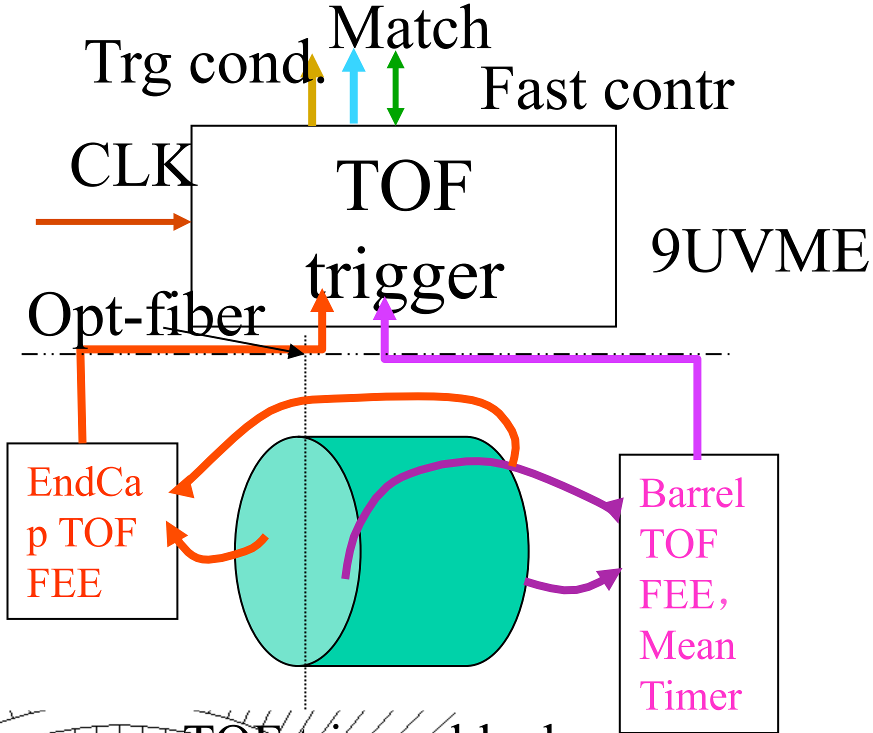
- Inter-link neighbour boards, to reduce the cables.
- 12 layers PCB
- SI & EMC

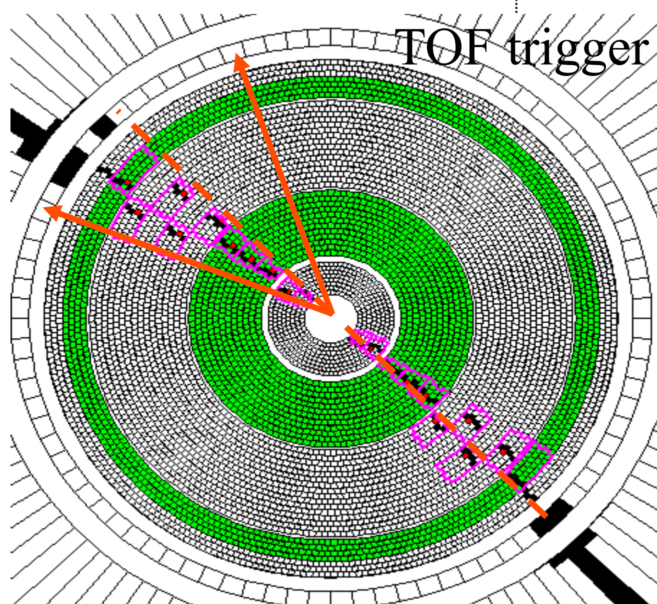




TOF 子触发系统

- 击中数
  - NBtof>=1, NBtof>=2
  - Netof>=1,Netof>=2
- 桶部背对背 TBB
  - Pt>837MeV
  - 12cells(3x2x2+1),53 °
- 端盖背对背 ETBB
  - Pt>551MeV
  - 8cells(2x2x2+1),67 °
- 径迹配对信息（TKM）：
  - TBhits(88),Tehits(48)

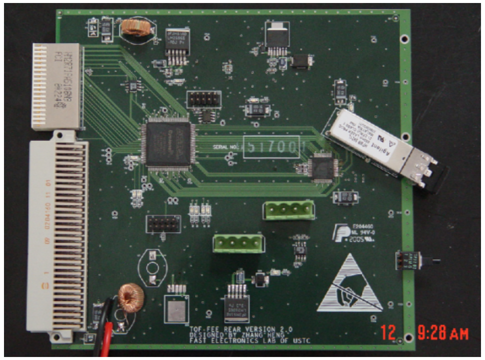




Barrel:88 Endcap:48

TOF trigger modules

- 14 FEE_Rear modules
  - Transmitting mean timer signals to trigger
  - The 2nd version has been tested
  - Self- Synchronization
- 1 TOF sub-trigger module
  - **upgradable**
  - **Firmware online modification/ reconfiguration**
  - **Dead time loss**
  - **optical fiber transmission**
    - **Minimized # of signal channels**
    - **Decreased signal loss**
    - **Decreased interference**
  - **FPGA, simple and reliable**



EMC trigger

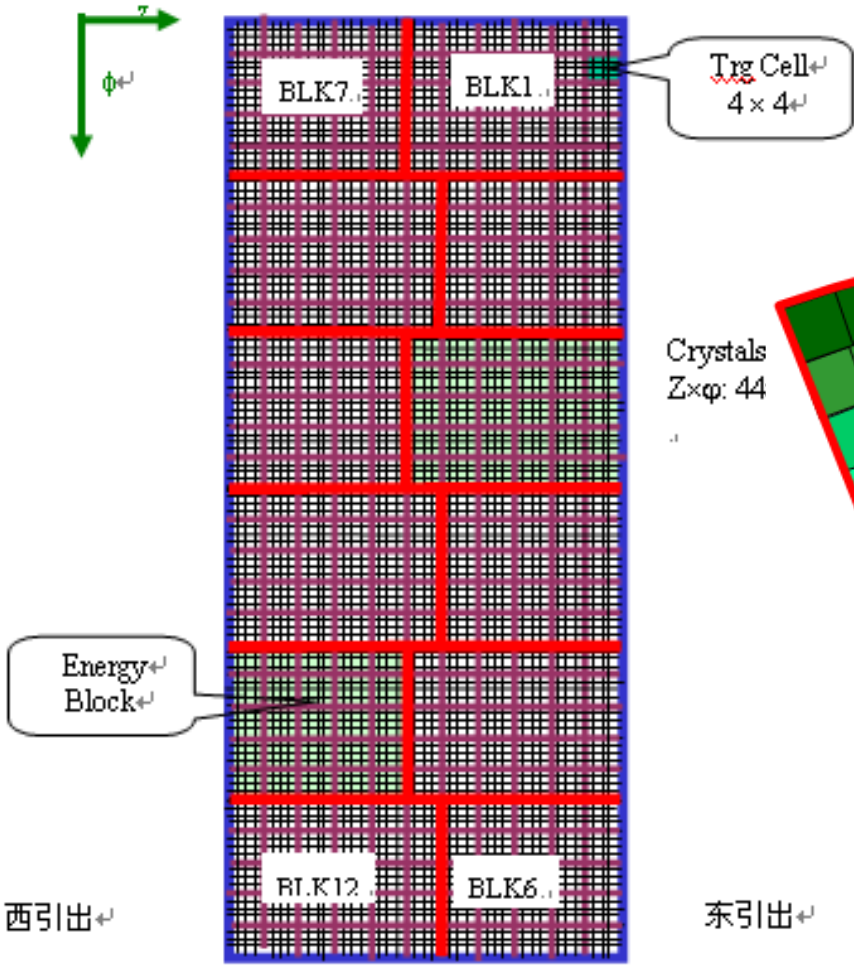


图1 桶部量能器晶体排列图

Crystals
Z×φ: 44

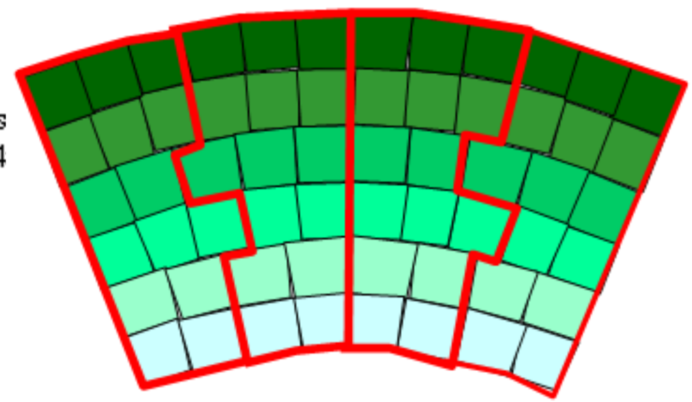
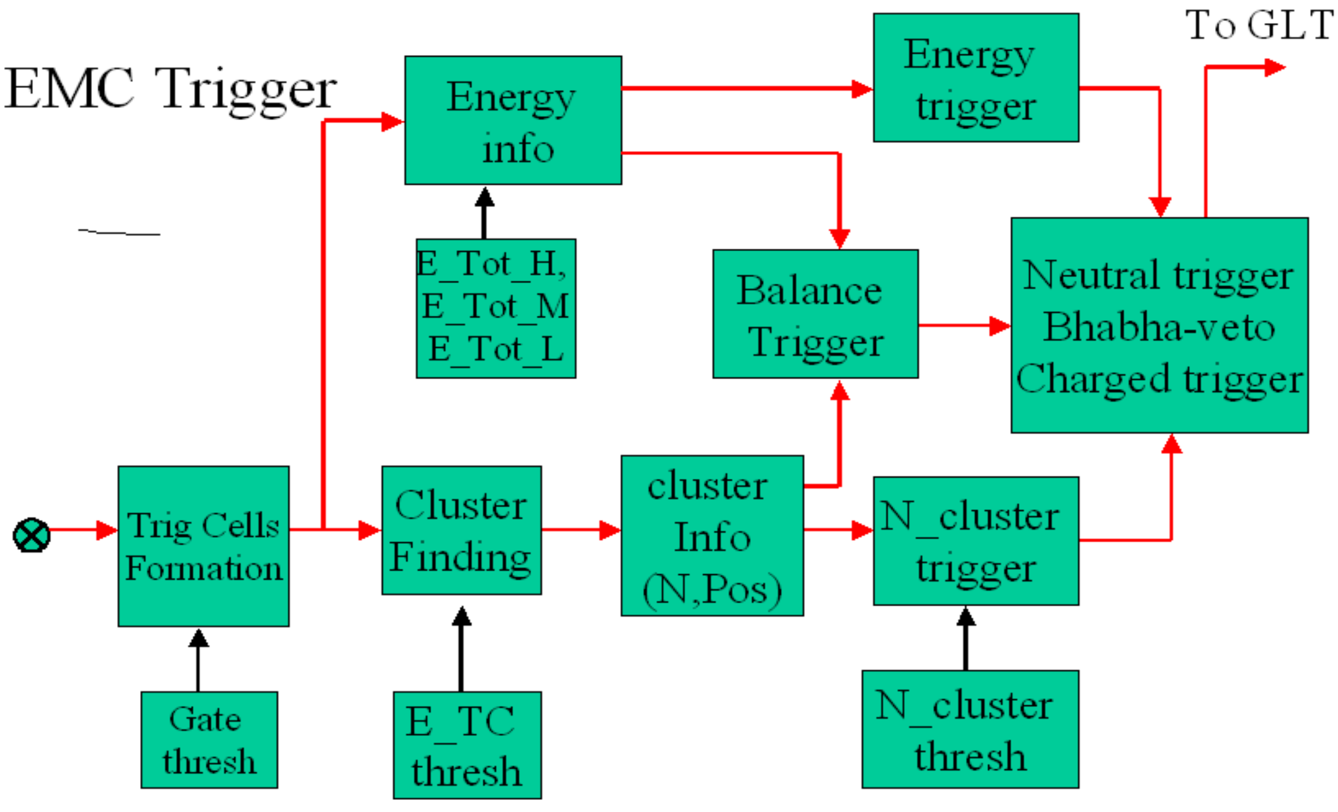


图2 量能器端部触发单元分割示意图
(单端1/8)

Crystals: 6 rings
64,64,80,80,96,96

TRG Cell:
1/32,
1 TrgCell,15 Crystals

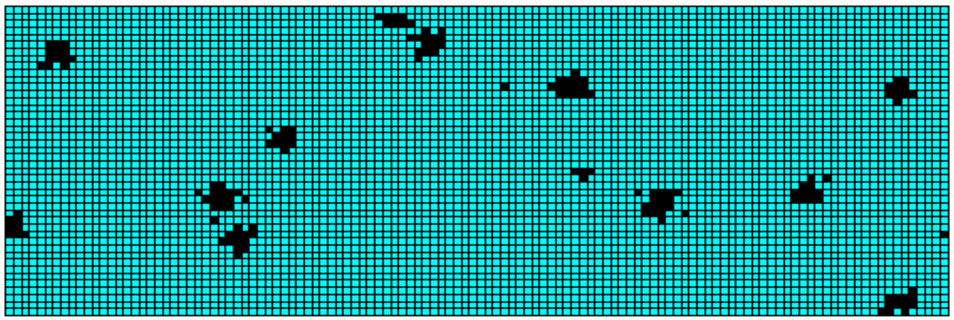
EMC Trigger



Etot,
Ncluster,
Balance,
Position in phi, theta

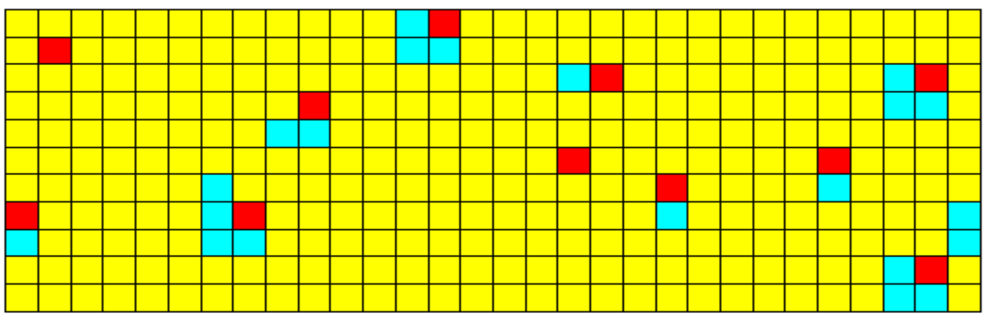
TC and Isolated Cluster finding

BEMC CRYSTAL HITS



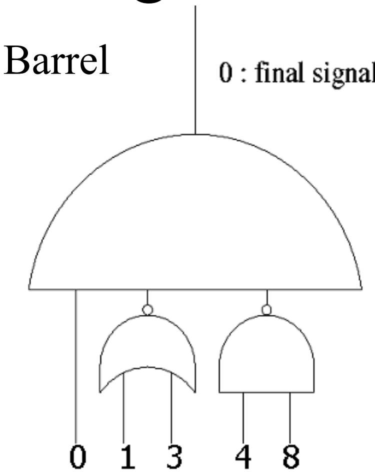
NUMBER OF CLUSTER 32. GATE THRESH 0. MEDIUM 12.
NUM OF ISO CLUSTER 11. GATE THRESH 0. MEDIUM 7.

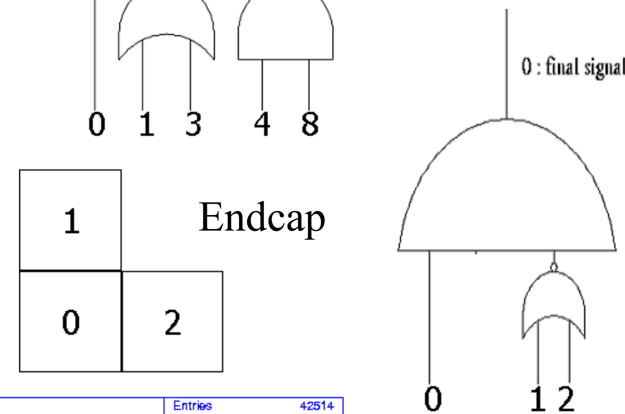
BEMC TC HITS

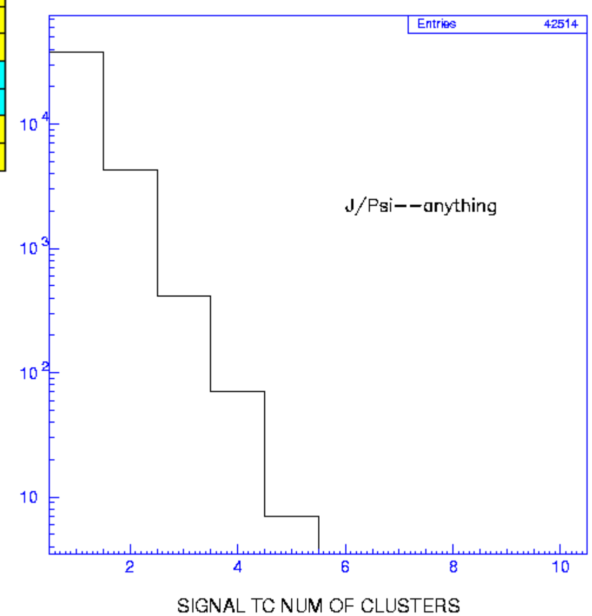


NUMBER OF CLUSTER 32. GATE THRESH 0. MEDIUM 12.
NUM OF ISO CLUSTER 11. GATE THRESH 0. MEDIUM 7.

5	1	6
2	0	3
7	4	8

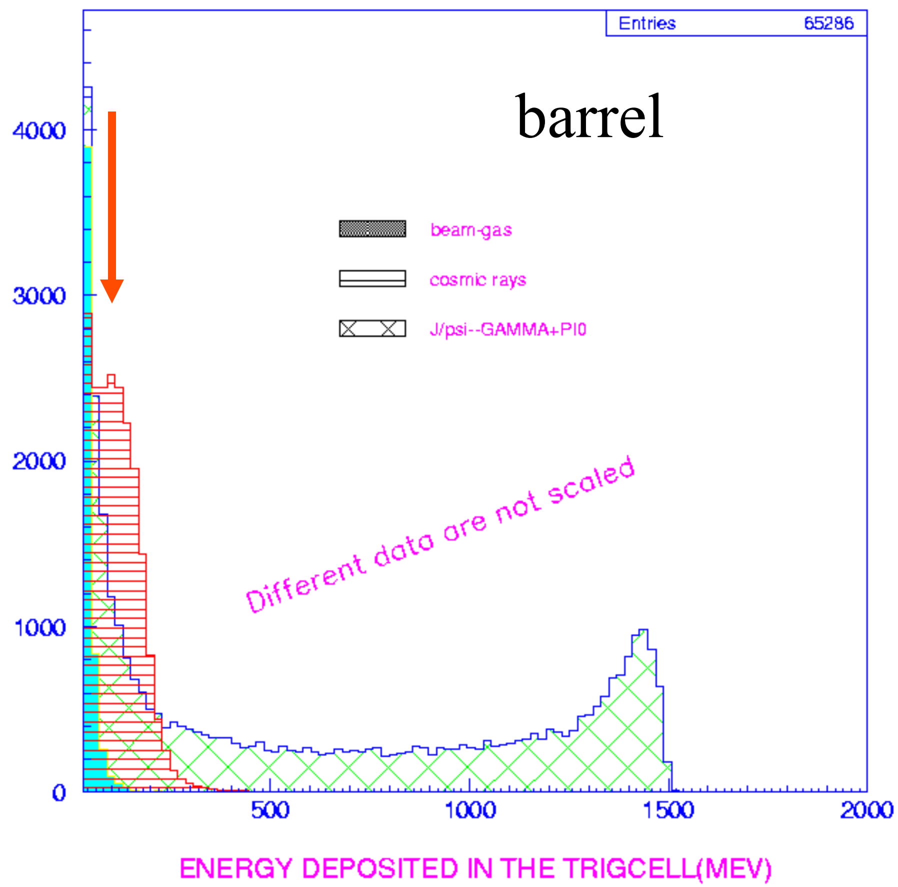


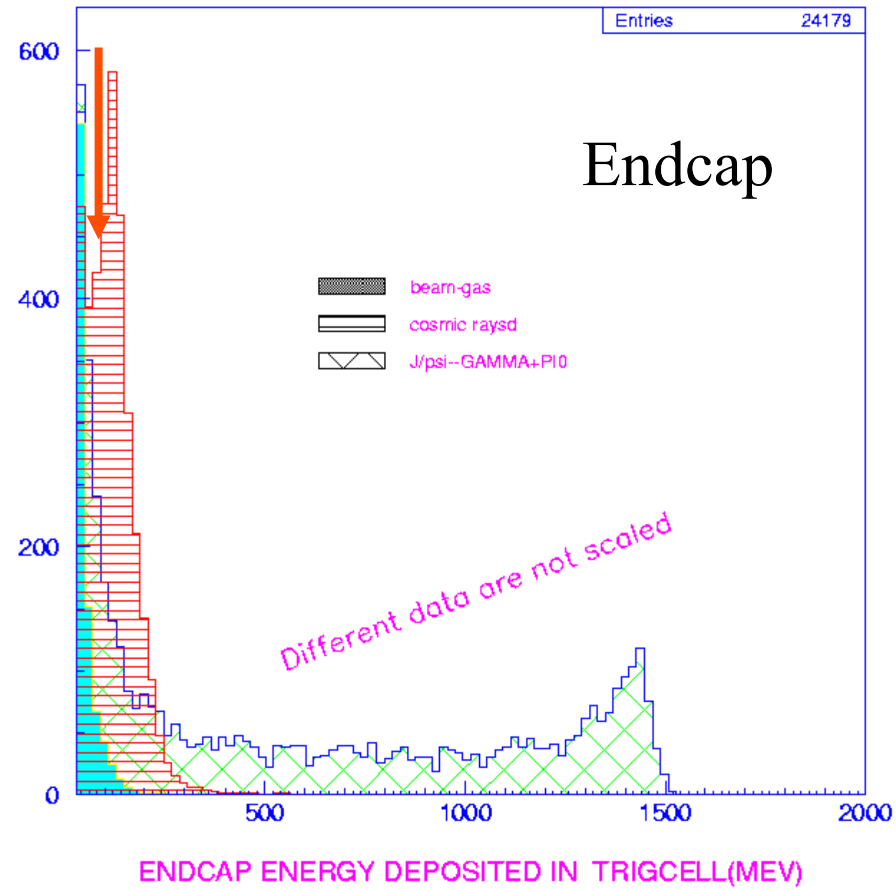




- 选取该组最右上角（即θ, φ向编号较大）中的触发单元为簇团位置。

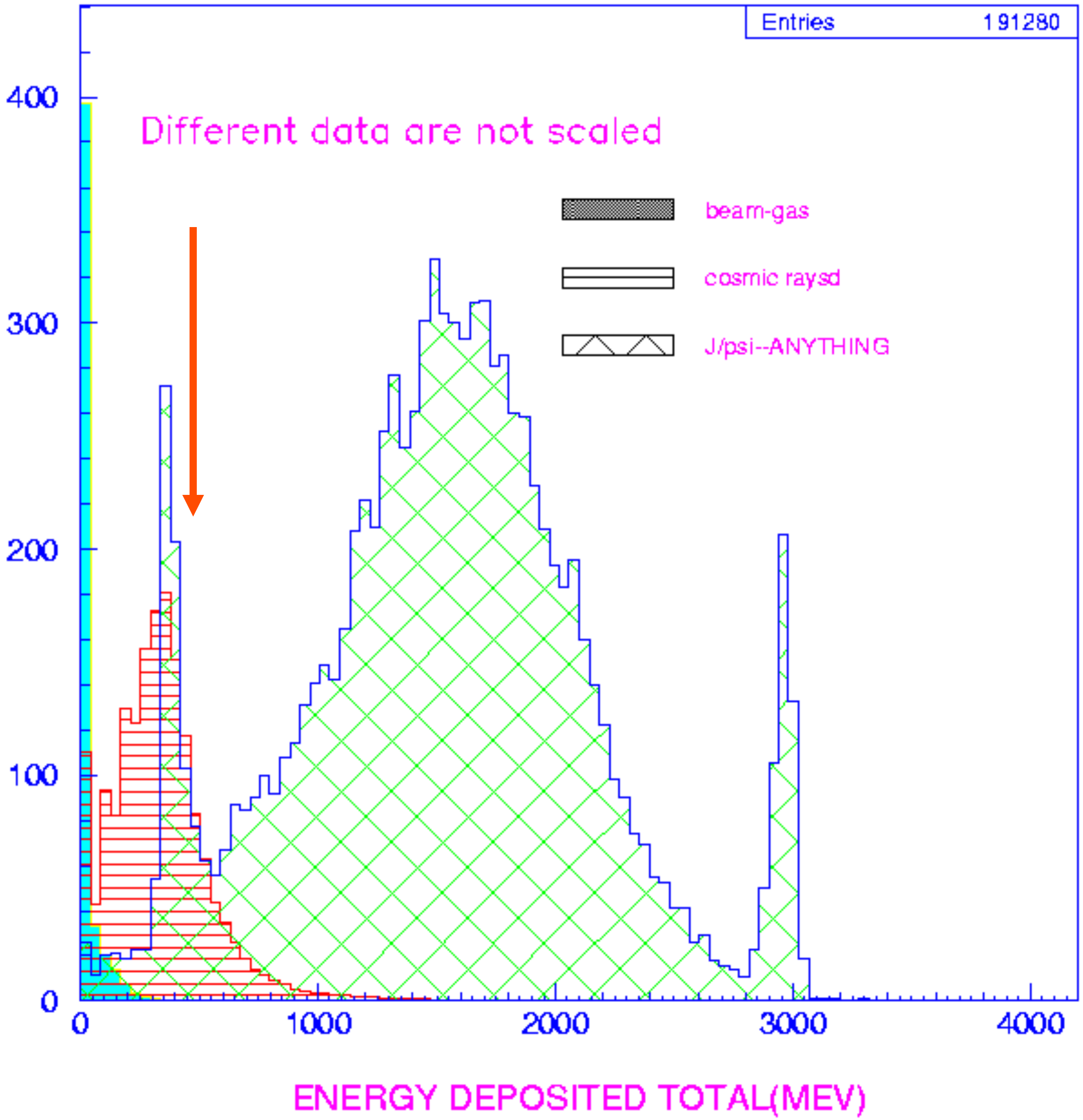
TC 阈值的选取





- 考虑信号堆积和基线涨落的限制，触发单元能量阈值确定为60—80Mev之间。
- 图中可见，束流—气体的本底的能谱集中在低能段，60—80Mev的触发单元能量阈值有能力排除在触发单元中单独沉积能量的束流本底

Total energy



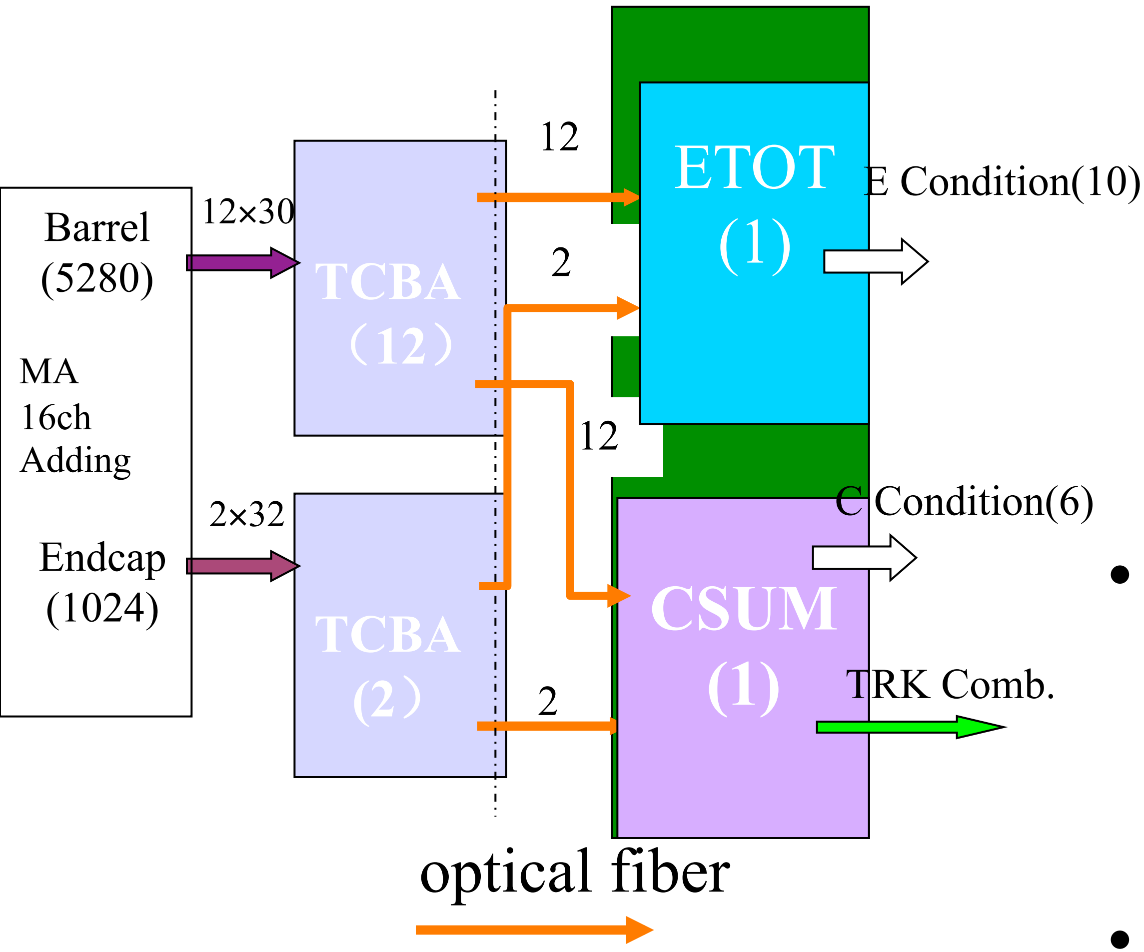
- Etot-L (~200MeV)
  Threshold for background events
- Etot-M (~800MeV)
  Threshold for neutral events
- Etot-H (~2.5GeV)
  Threshold for bhabha event

EMC 触发条件

- NClus>=1 Cluster number (>=1 for EMC timming)
- NClus>=2
- BclusBB Back to back cluster
- EclusBB
- Clus_PHI Cluster balance at φ
- Clus_Z One cluser at each half of EMC
- Diff_B Energy difference between each B half
- Diff_E Energy difference between each E half
- BL_BEMC Energy Balance between half BEMC
- BL_BLK Energy Balance of barrel blocks
- BL_EEMC Energy Balance between half EEMC
- BL_Z Z energy balance (B+E)
- Etot_L Total Energy >Thre-l
- Etot_M Total Energy >Thre-m
- BEtot_H Total energy of Barrel EMC
- EEtot_H Total energy of Endcap EMC

- To TKM:
  - Bemc(40) Eemc(48)

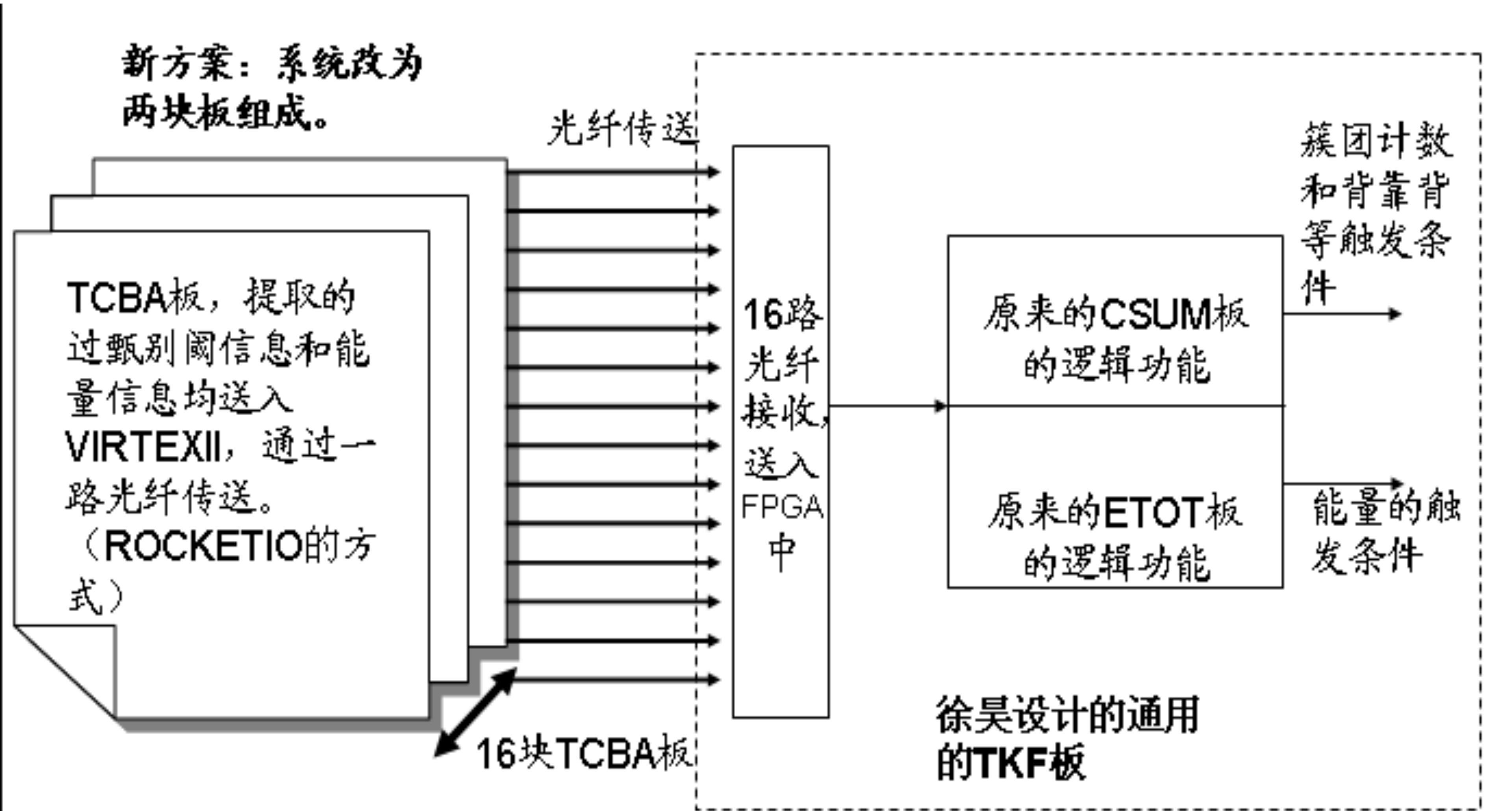
EMC sub-trigger



- TCBA:
  - CCD base line restoration
  - Input:twisted pair
  - Time extraction and cluster signal
  - Block energy sum and digitization with Flash ADC
  - Fiber transmittion
- CSUM:
  - Cluster finding
  - Cluster relative condition production
  - Condition forming
- ETOT:
  - Total Energy cut conditions production
  - Condition forming

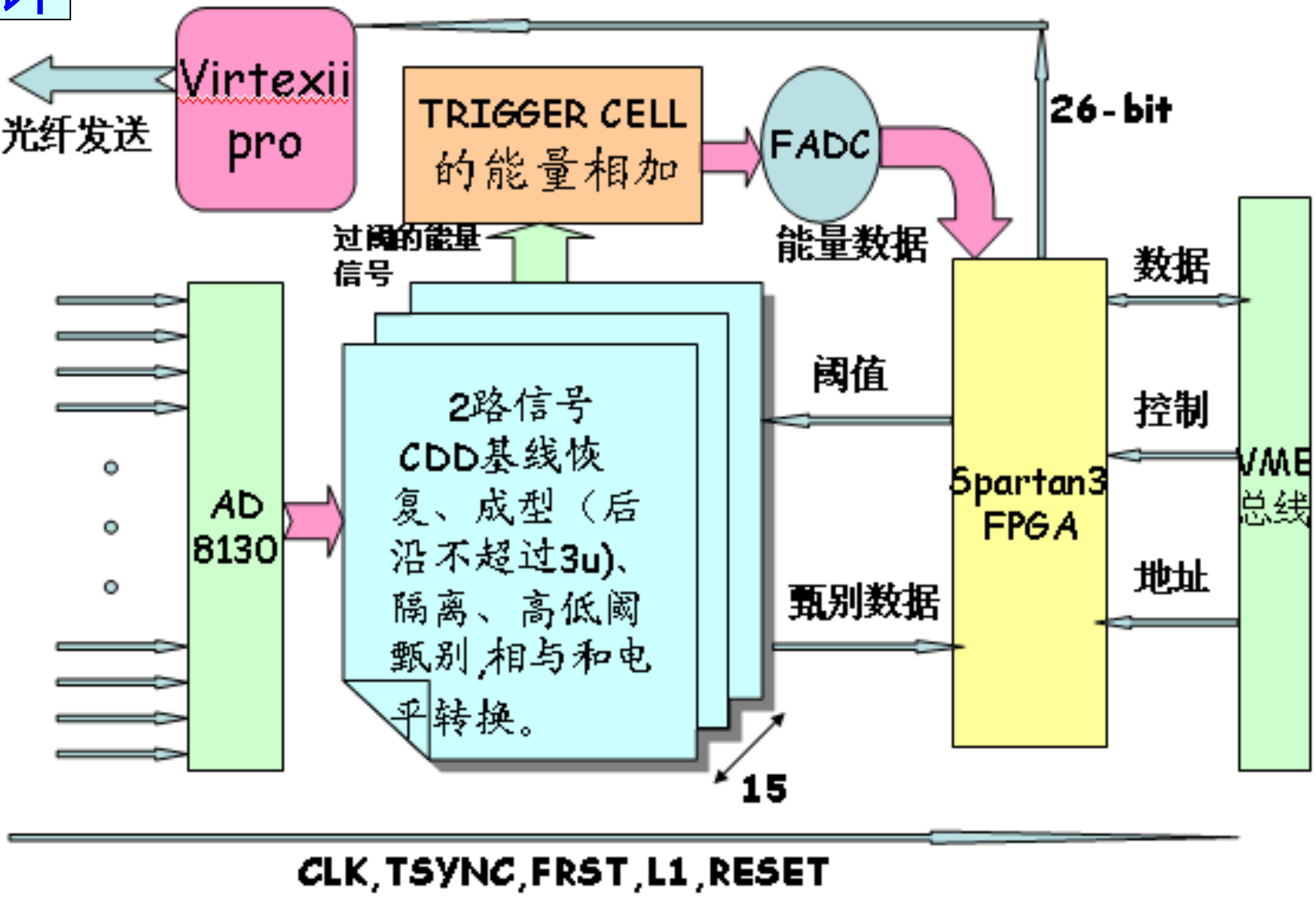
原理设计

EMC触发子系统整体硬件规划

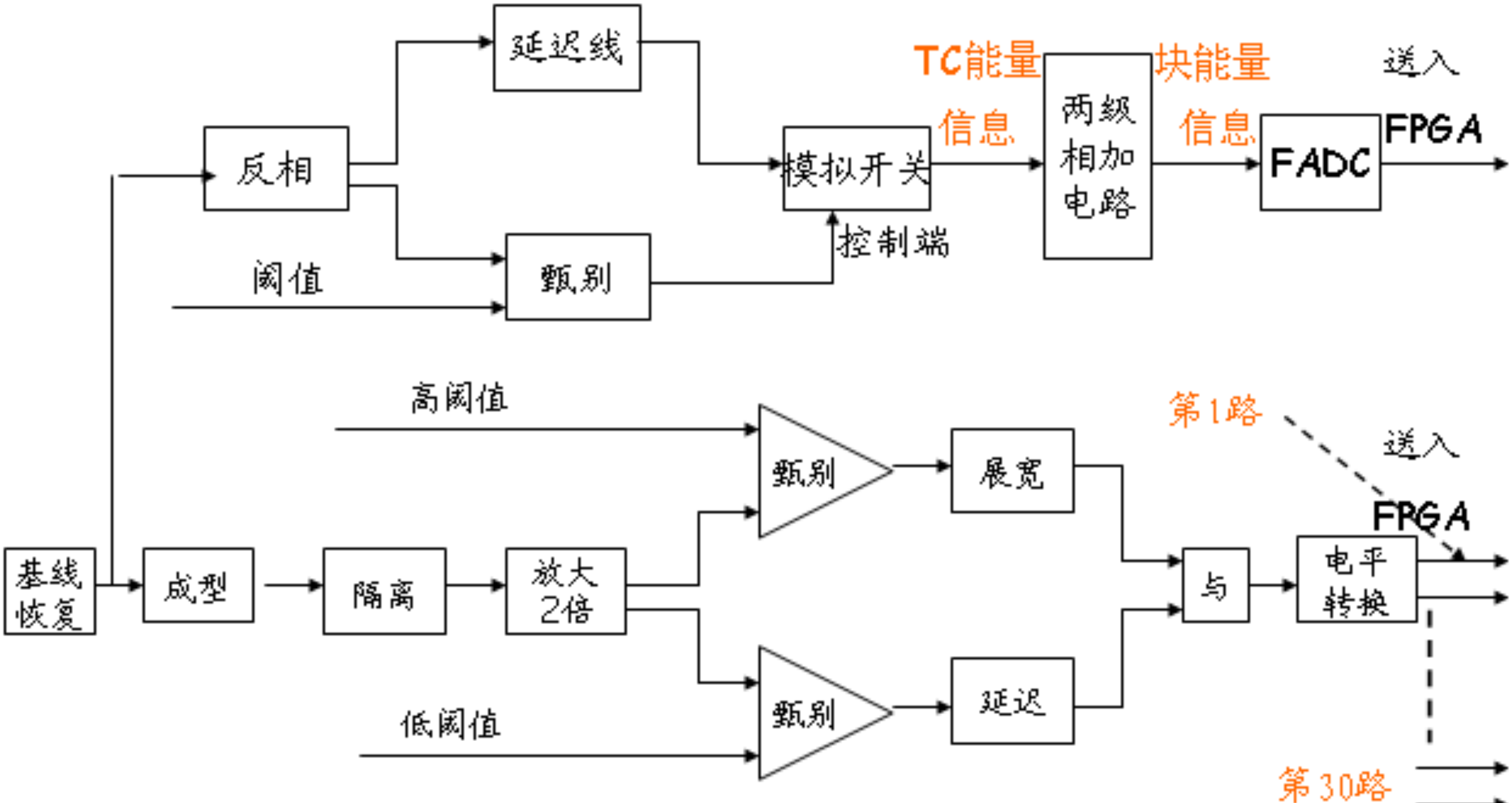


原理设计

TCBA板原理框图



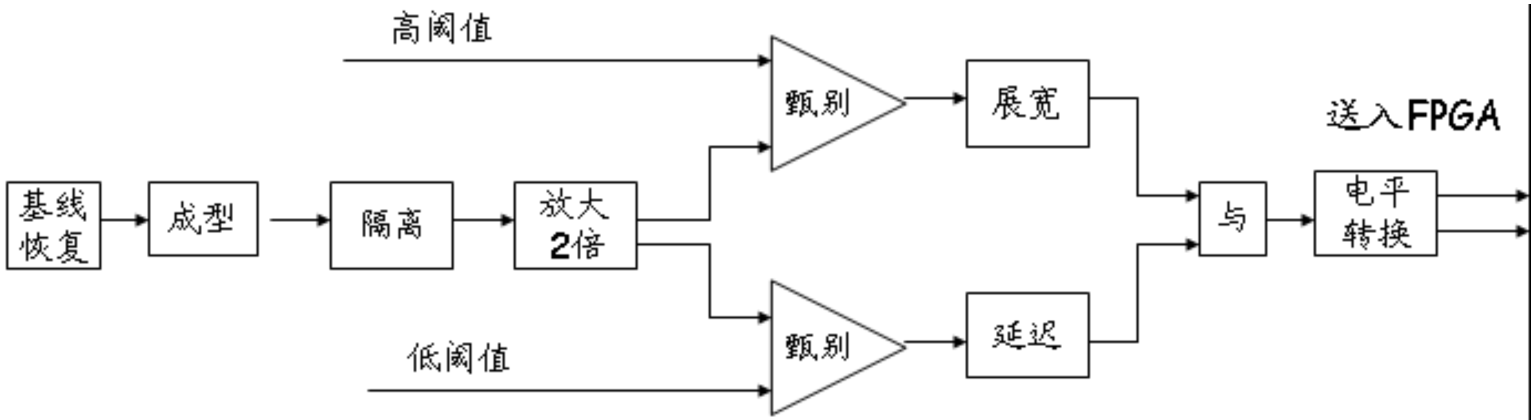
模拟部分整体原理框图


延迟线
TC能量
信息
两级
相加
电路
块能量
信息
送入
FPGA
反相
模拟开关
FADC
控制端
阈值
甄别
高阈值
第1路
送入
甄别
展宽
FPGA
基线
恢复
成型
隔离
放大
2倍
与
电平
转换
甄别
延迟
低阈值
第30路

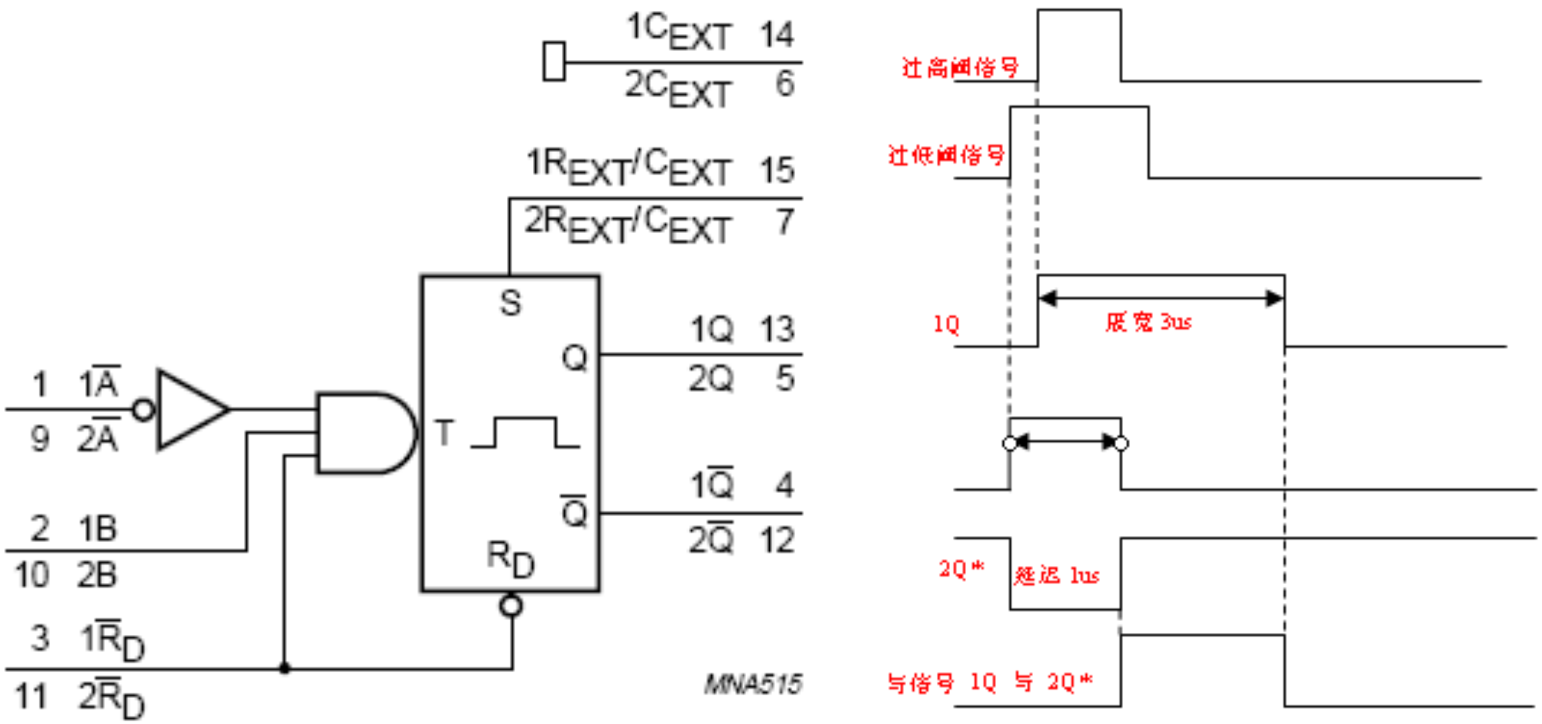
原理设计

TCBA板各部分逻辑功能的设计和实现

——时间信息提取部分的设计和实现



时间信息提取部分的原理框图

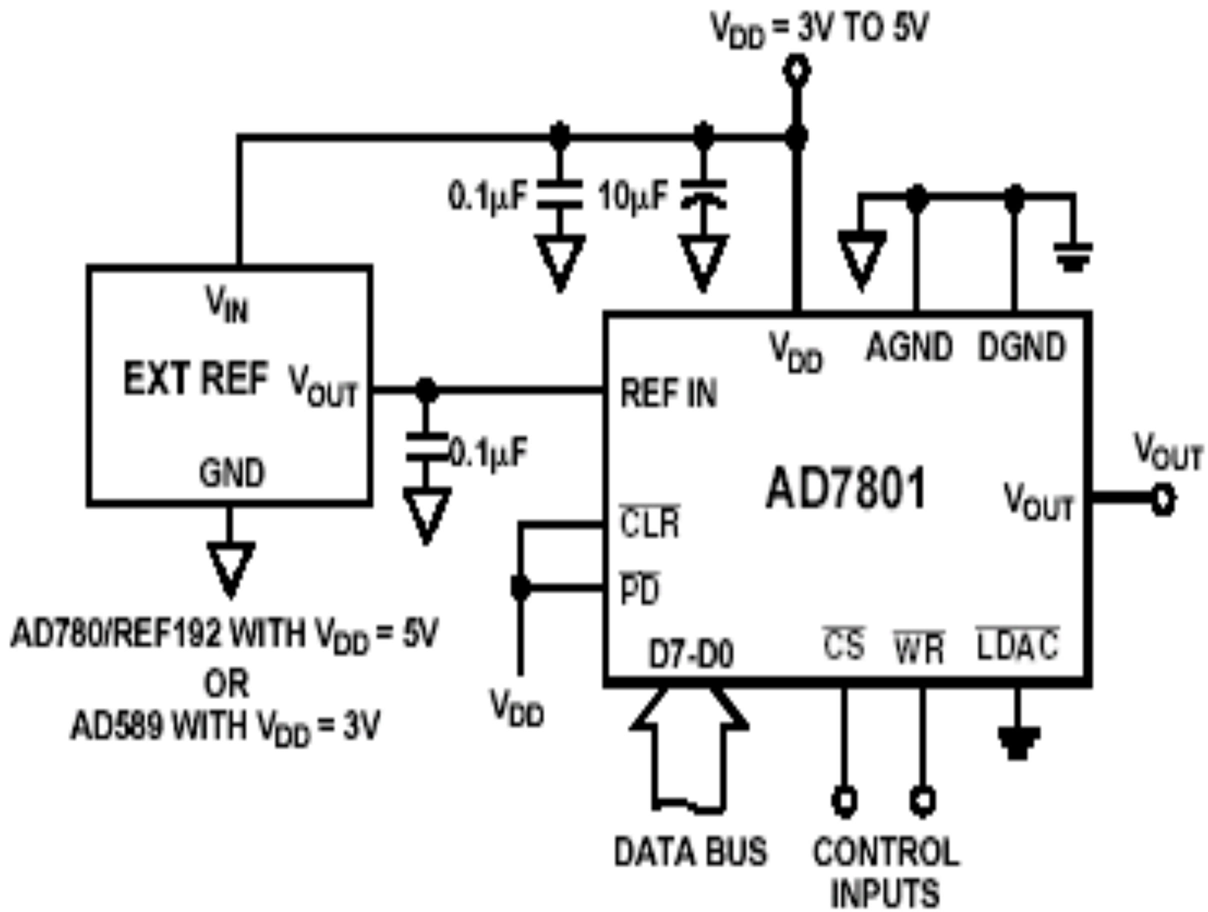


时间信息提取部分逻辑

TCBA板各部分逻辑功能的设计和实现

——阈值产生部分的设计与实现

由FPGA和DAC模块组成。板上共需要3个阈值，高阈，低阈和能量阈值，通过VME总线朝FPGA中写入合适的数字，送入DAC，转变为模拟阈值，阈值可变



DAC原理图

原理设计

TCBA板各部分逻辑功能的设计和实现

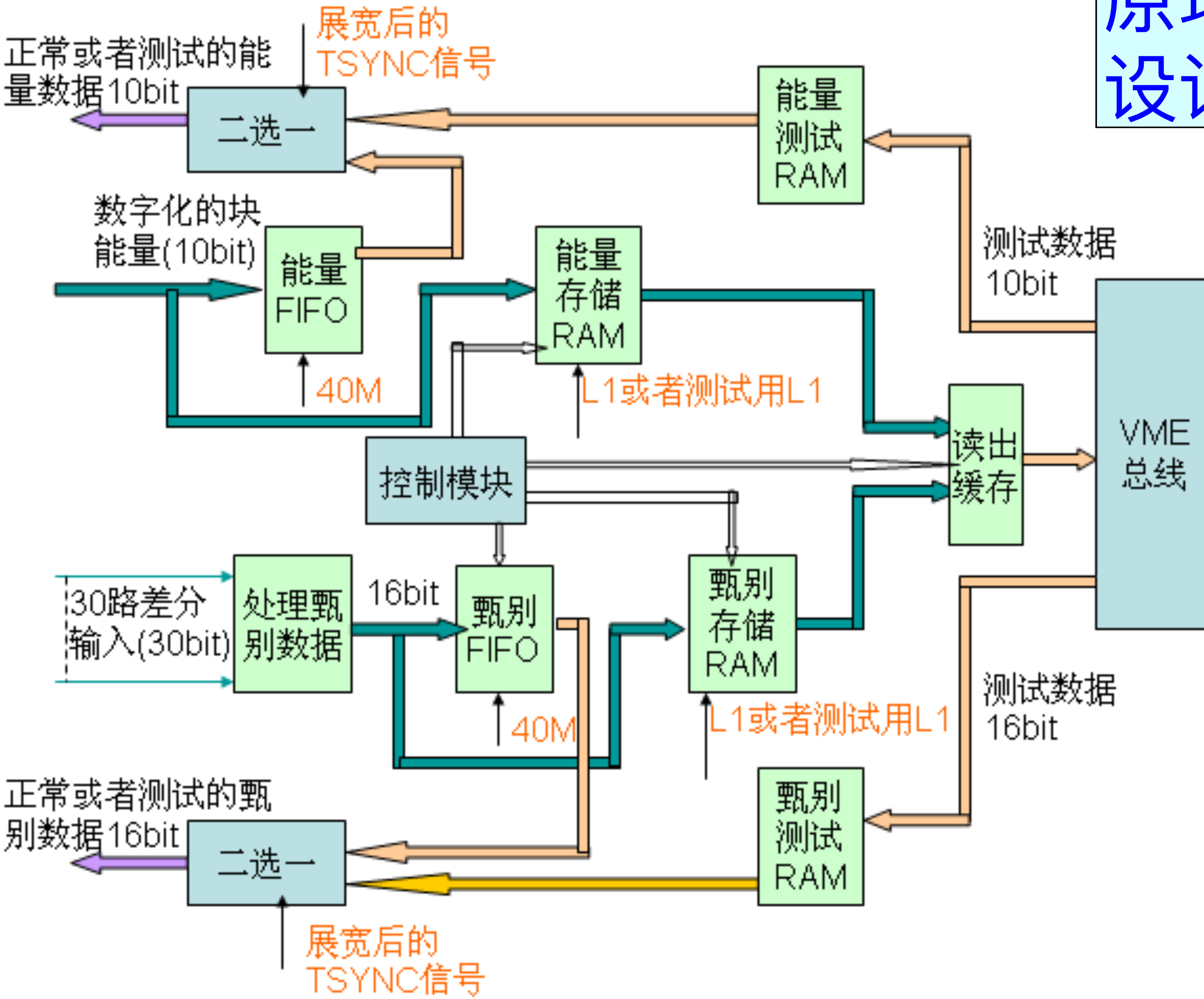
——数据的光纤发送与测试部分

数据‘并转串’由Virtexii Pro的FPGA完成。能量部分信号和甄别部分的信号，通过差分线从Sprartan3的FPGA连接到Virtexii Pro的FPGA，Virtexii Pro的片子支持ROCKETIO的光纤传输方式，内部通过8bit-10bit转换，把数据从并行变为串行，通过光纤发送，光纤收发器采用触发组通用的HFBR5921L。光纤发送FPGA选用XILINX公司的XC2VP2。

TCBA板各部分逻辑功能的设计和实现

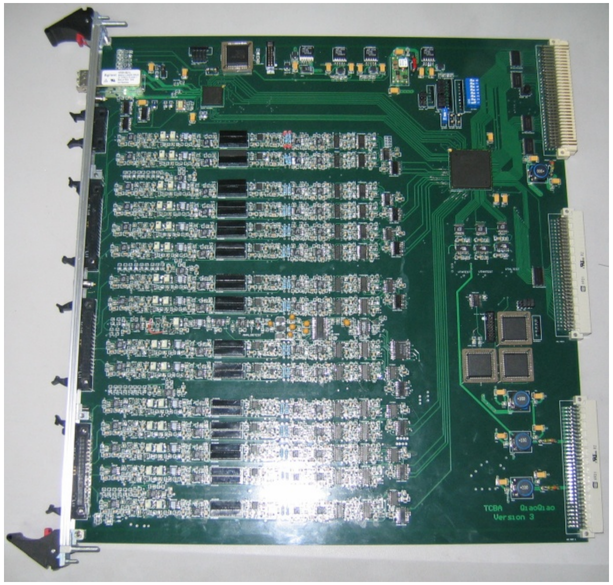
——FPGA逻辑部分（Spartan3）

原理设计



FPGA(Spartan3)的原理框图

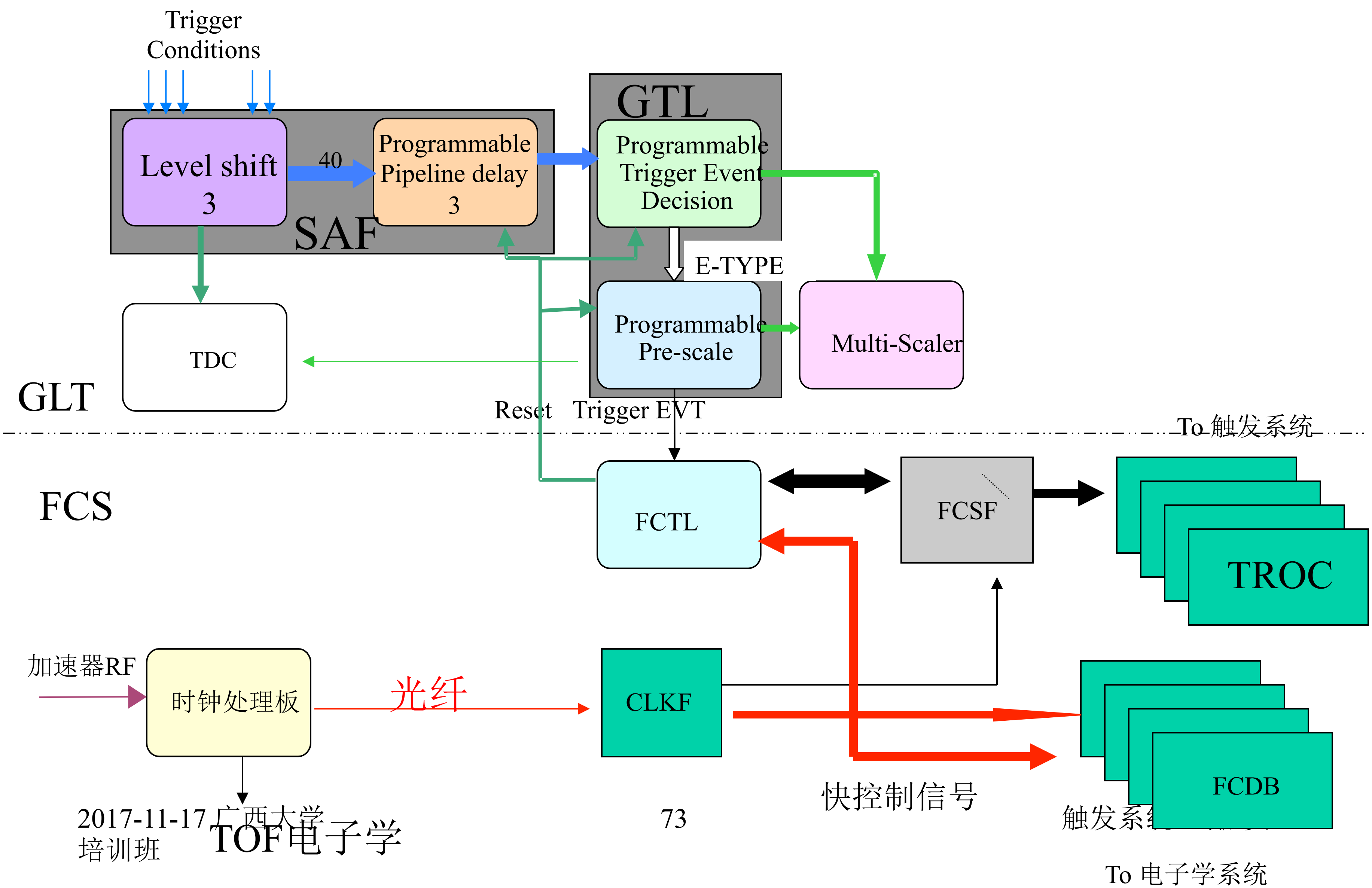
EMC sub-trigger



- TCBA

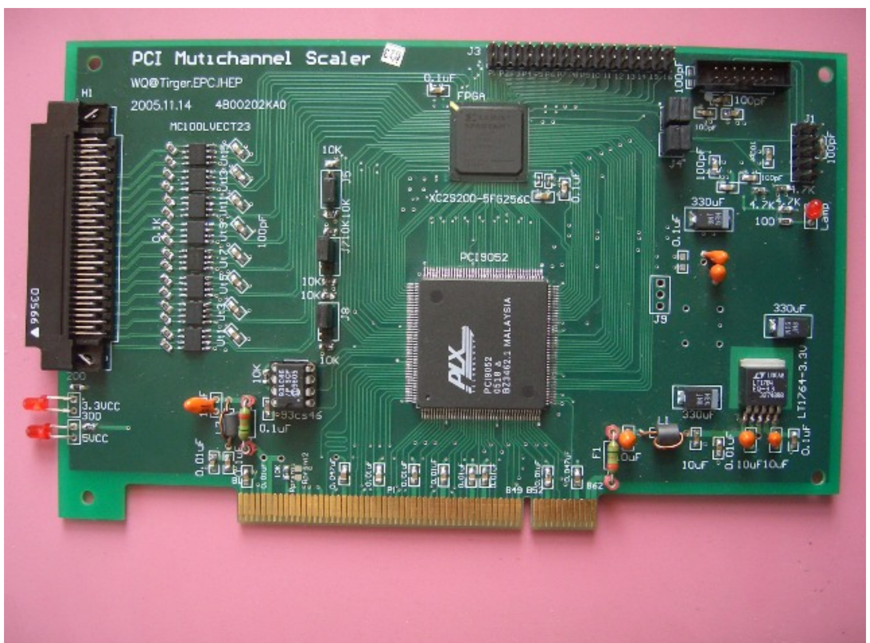
- TKF as Etot and Csum firmware

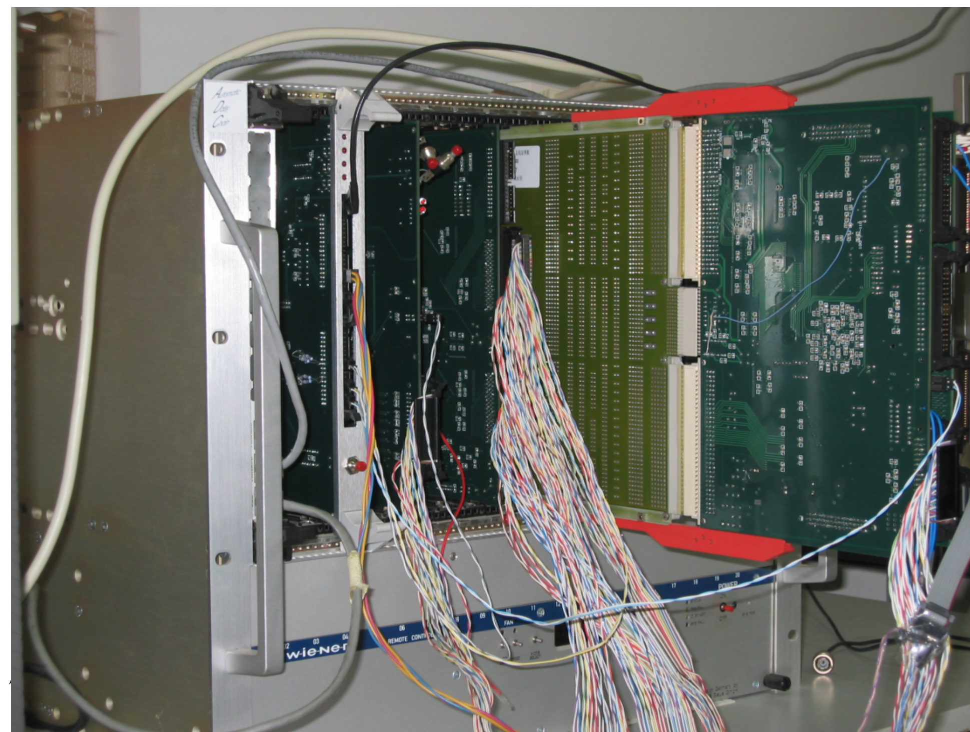
总触发GLT子系统和快控制子系统



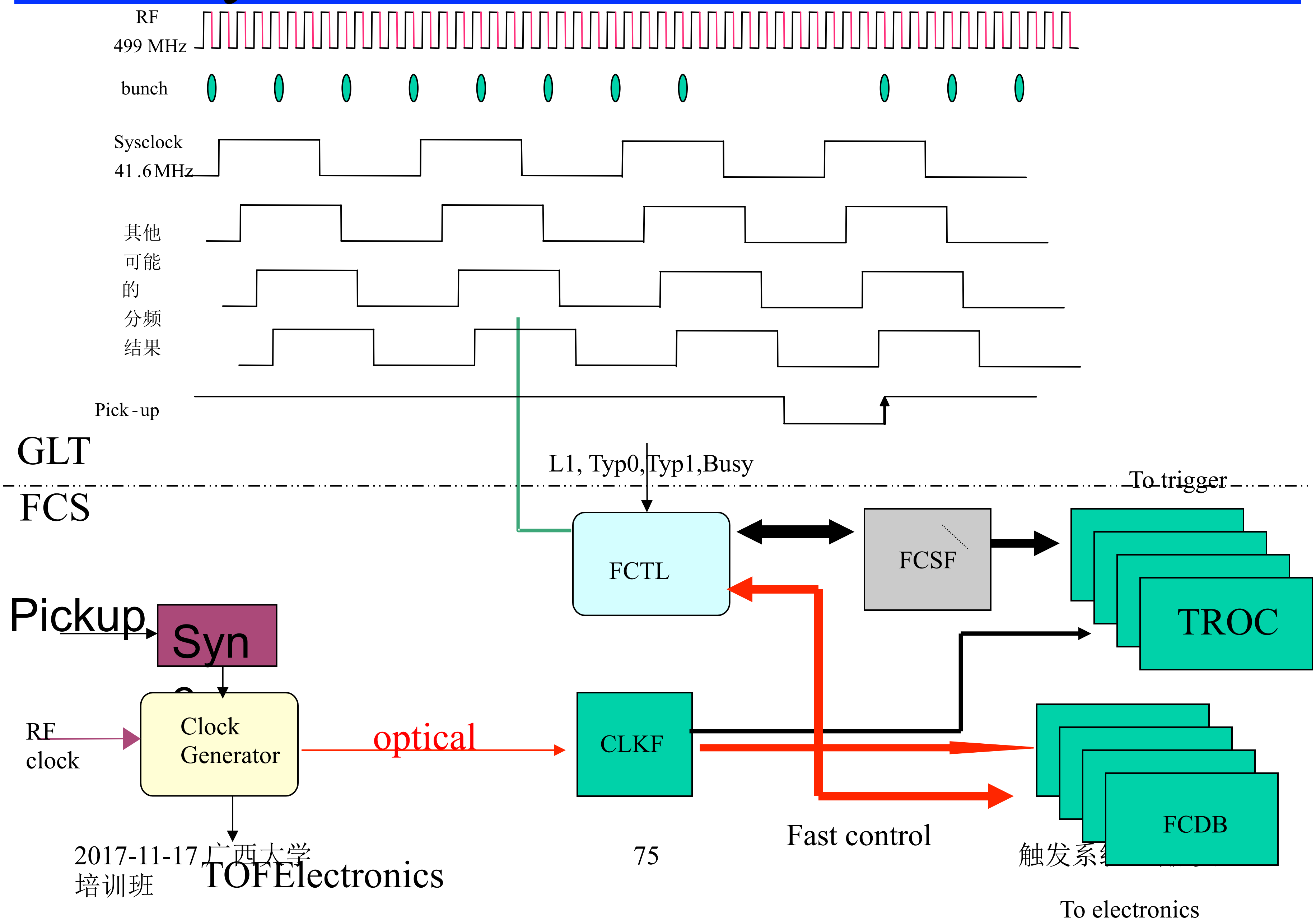
Global trigger

- 定标器
- SAF 与GTL 插件



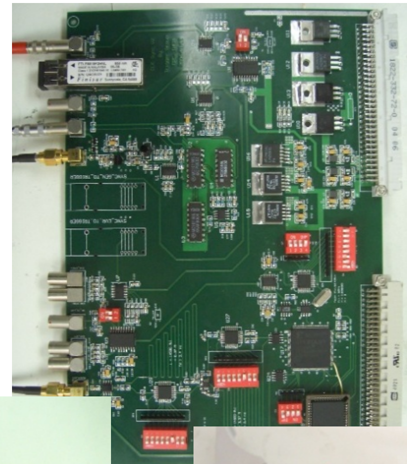


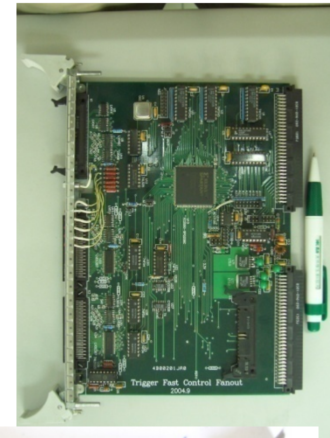
System Clock and Fast Control

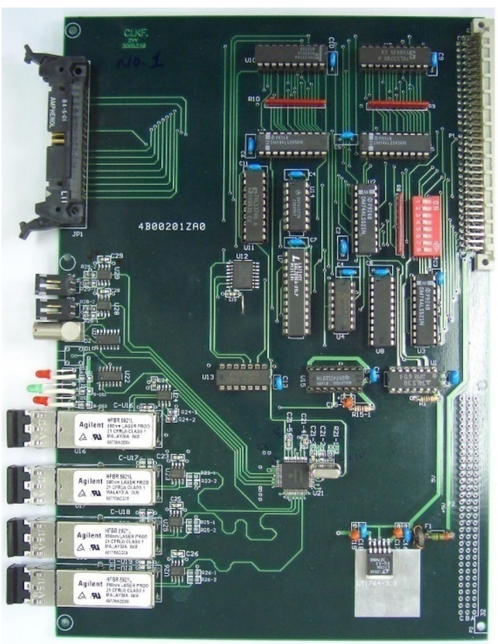


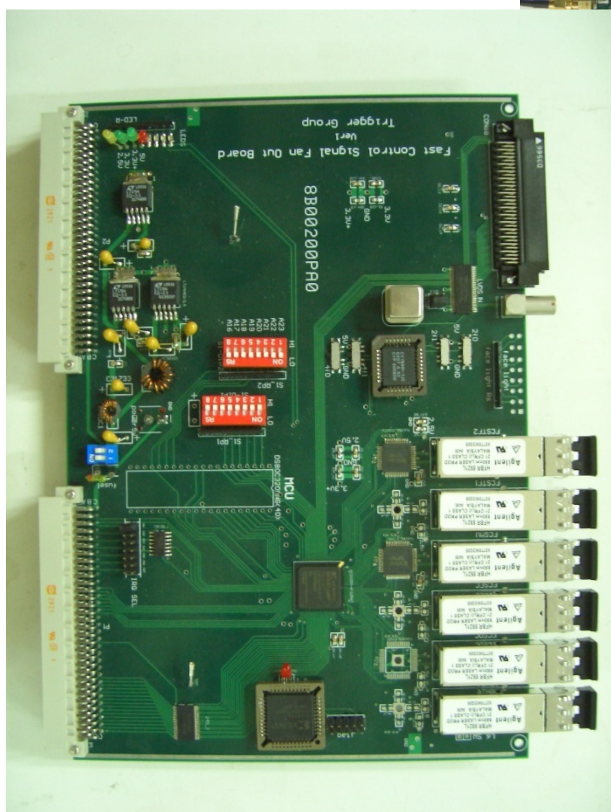
System Clock and Fast Control

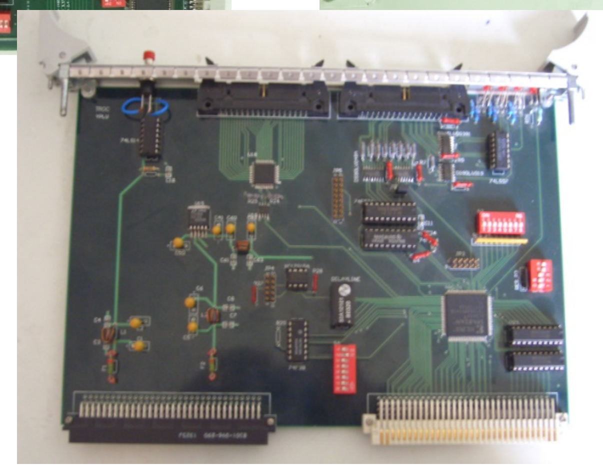
- 部分插件

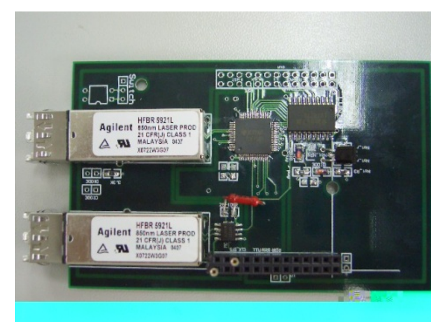






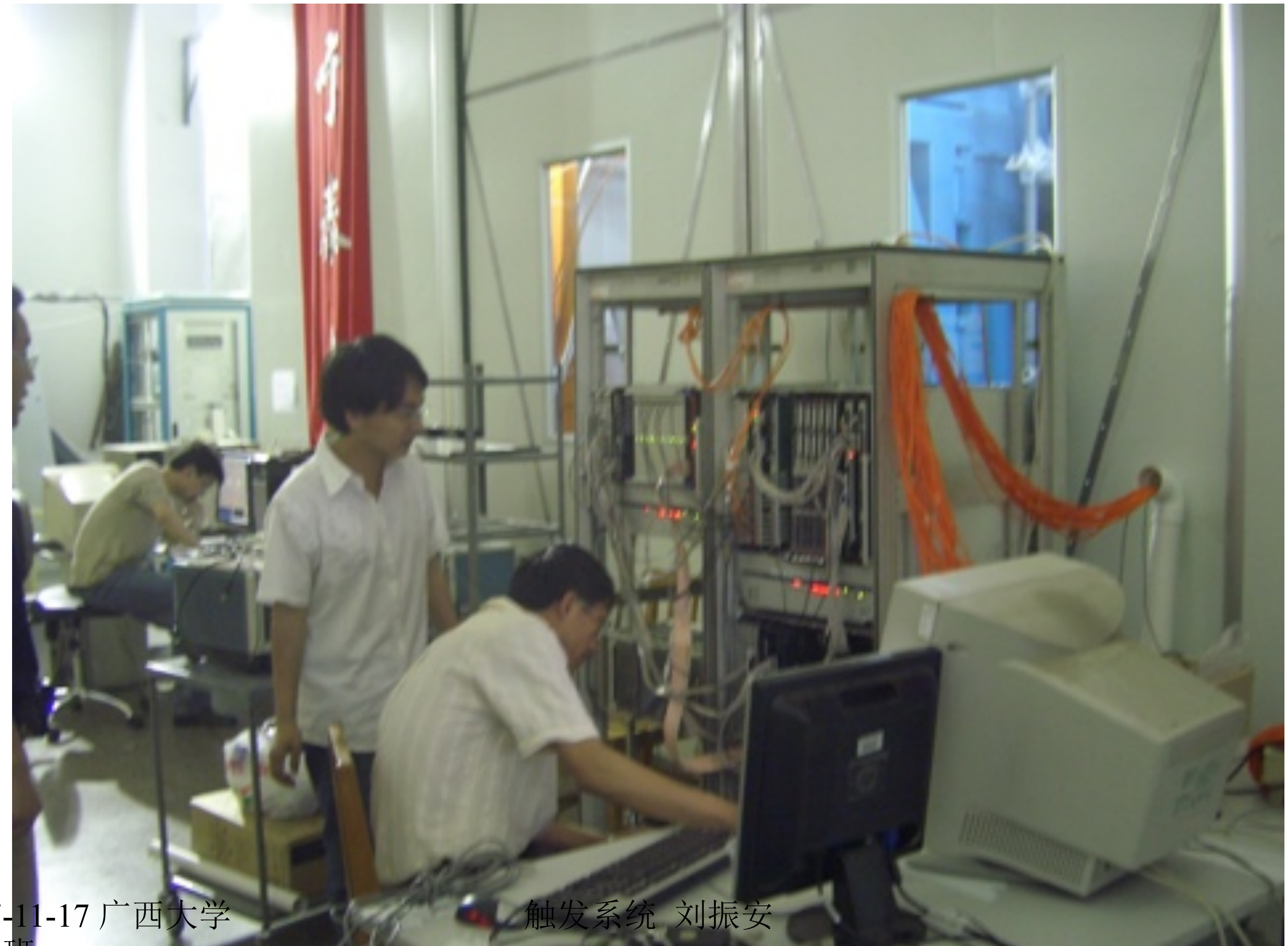




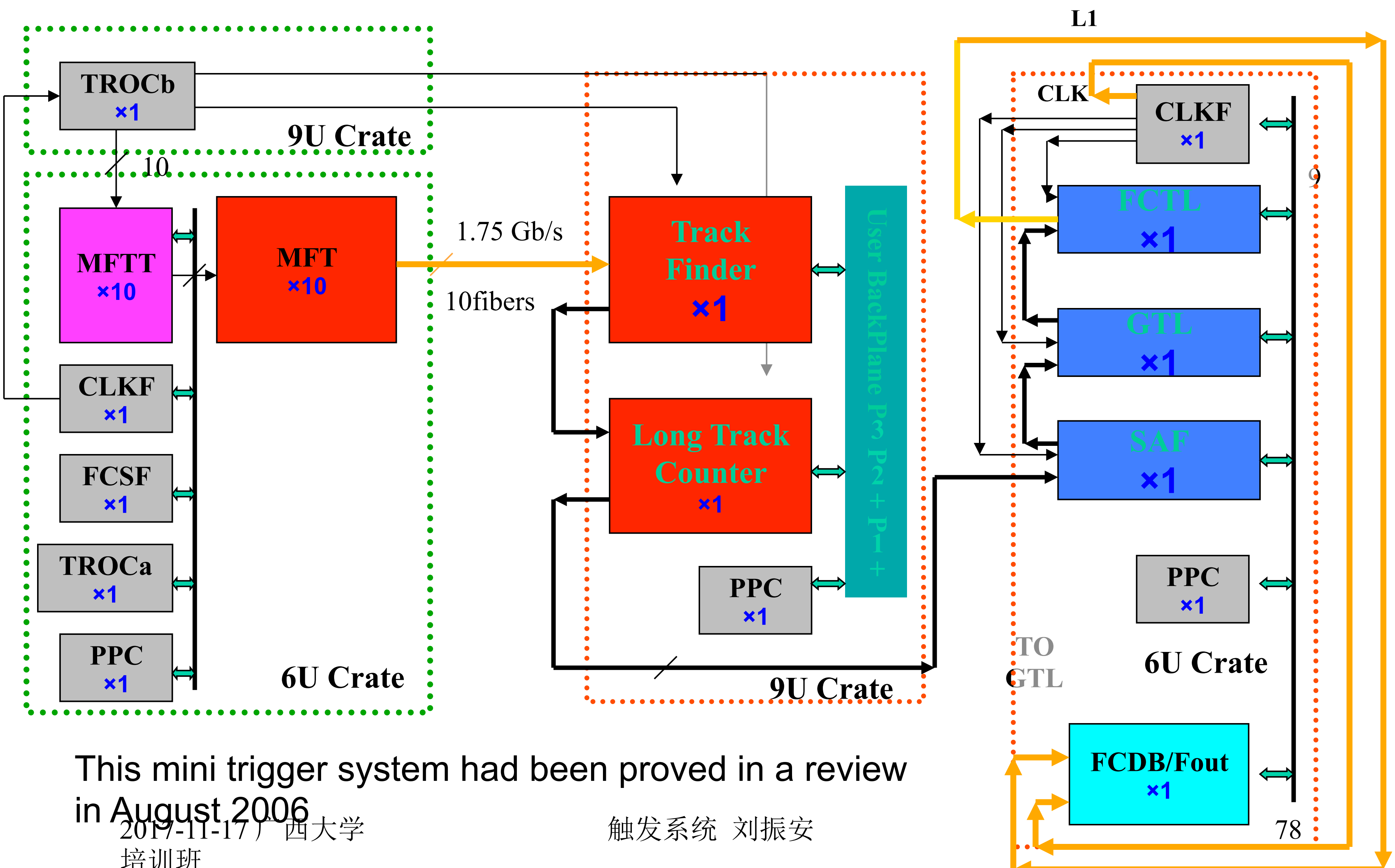


MDC宇宙线实验正在进行

希望通过宇宙线试验发现问题及时解决

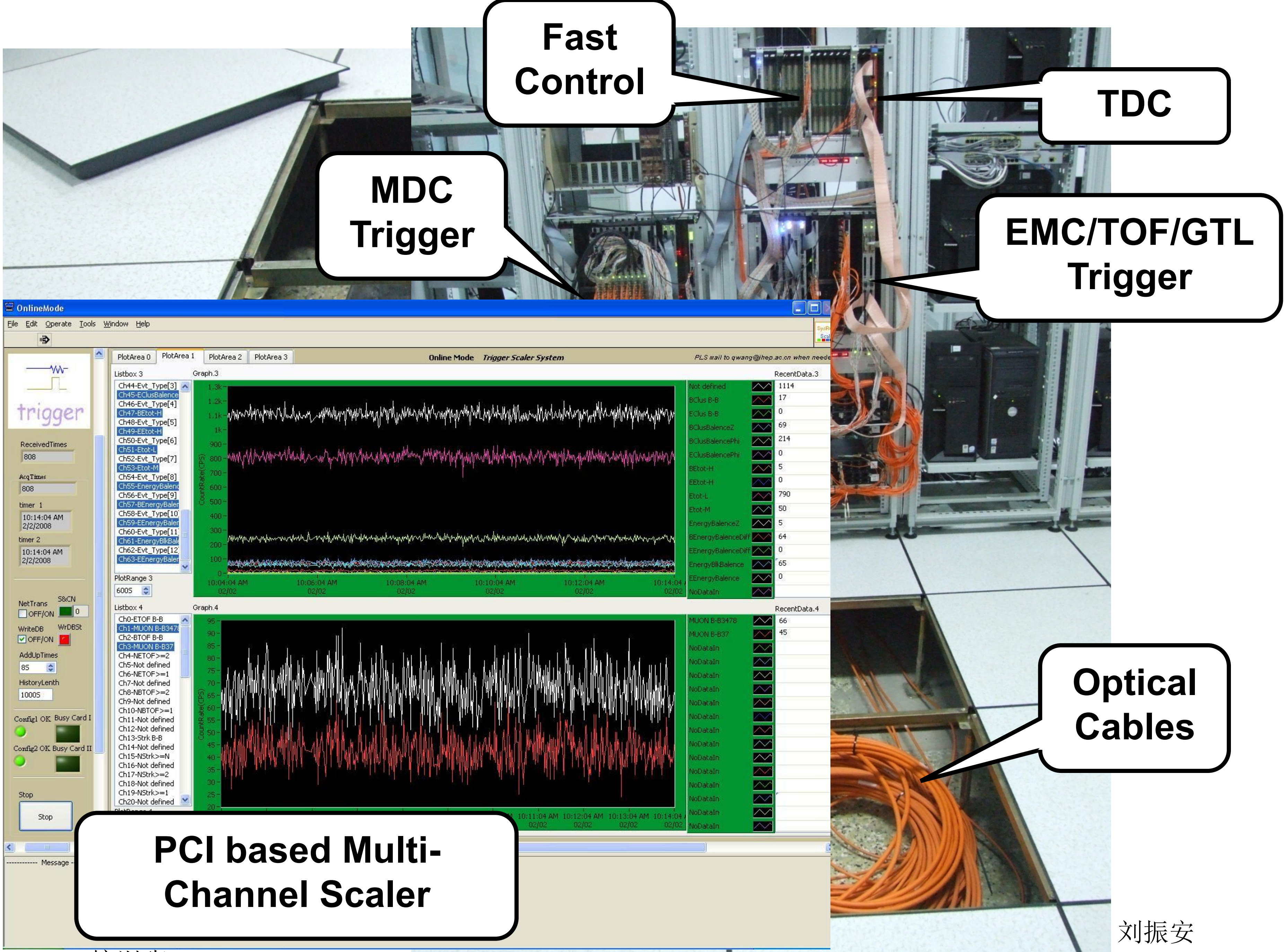


Mini trigger system



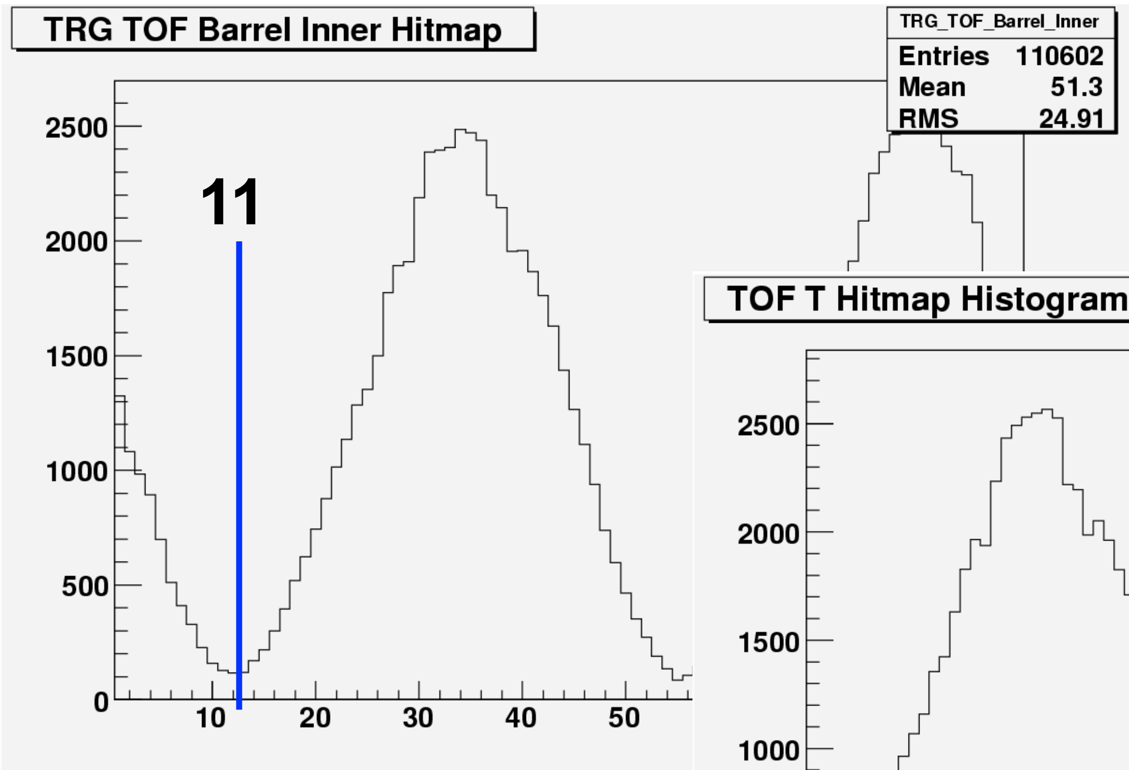
This mini trigger system had been proved in a review in August 2006

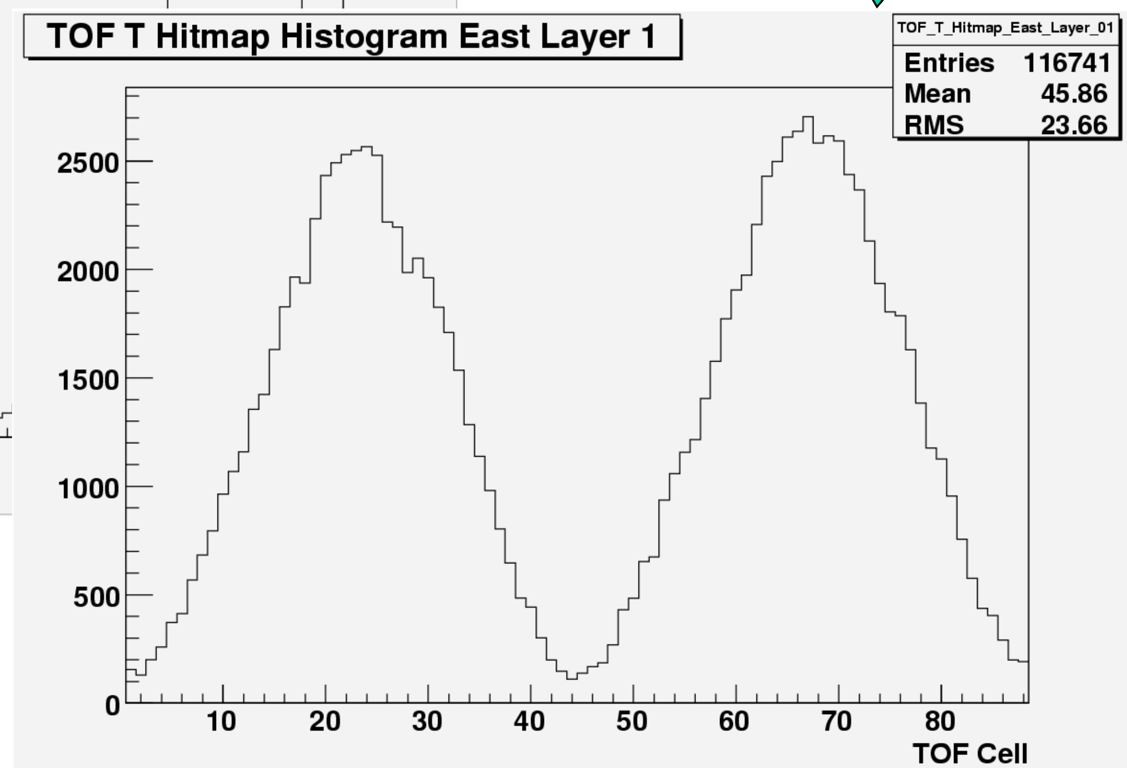
Installation


Fast Control
TDC
MDC Trigger
EMC/TOF/GTL Trigger
Optical Cables
PCI based Multi-Channel Scaler
OnlineMode
Online Mode Trigger Scaler System

TOF sub-trigger

TOF Electronics Single End

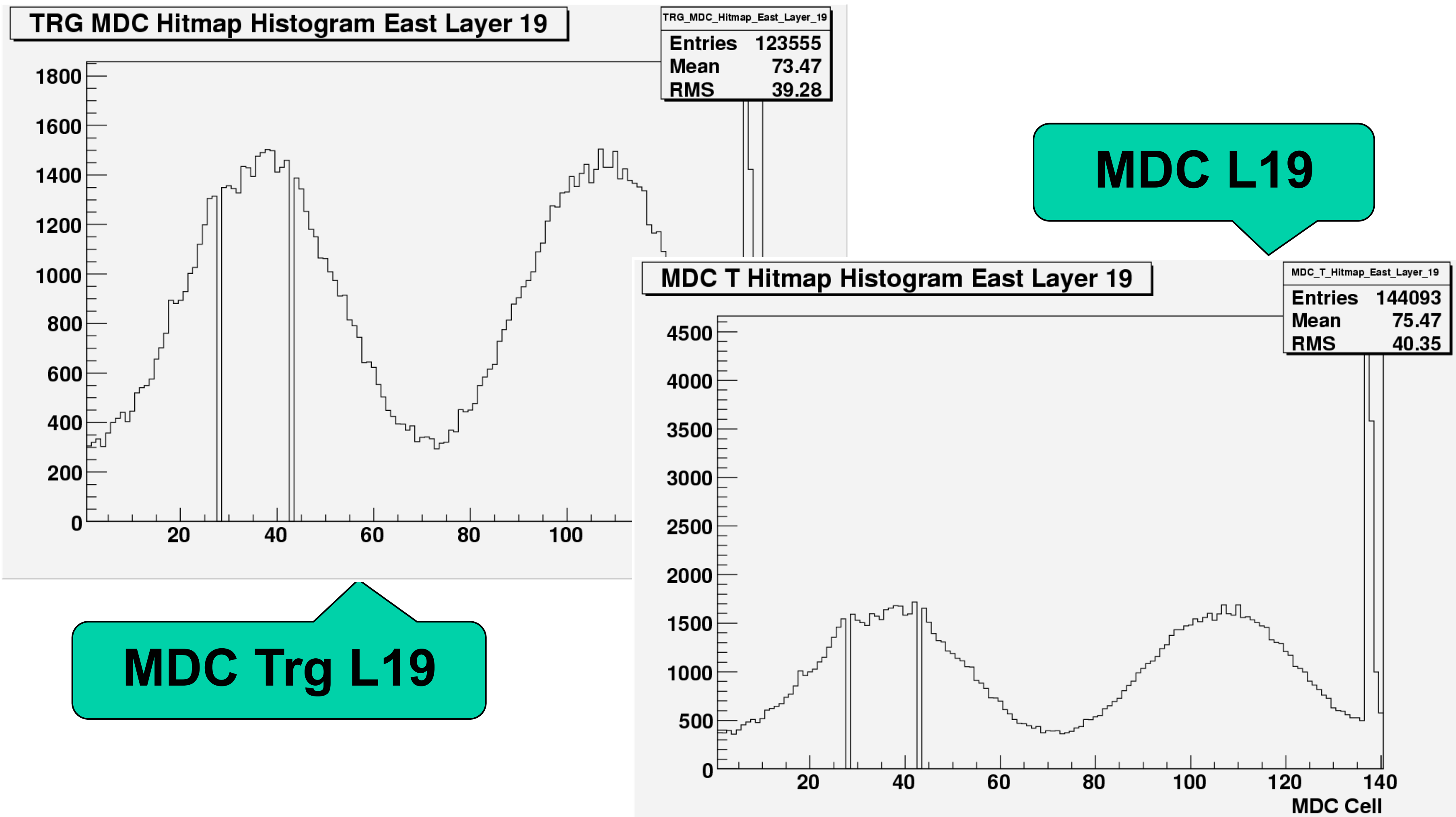




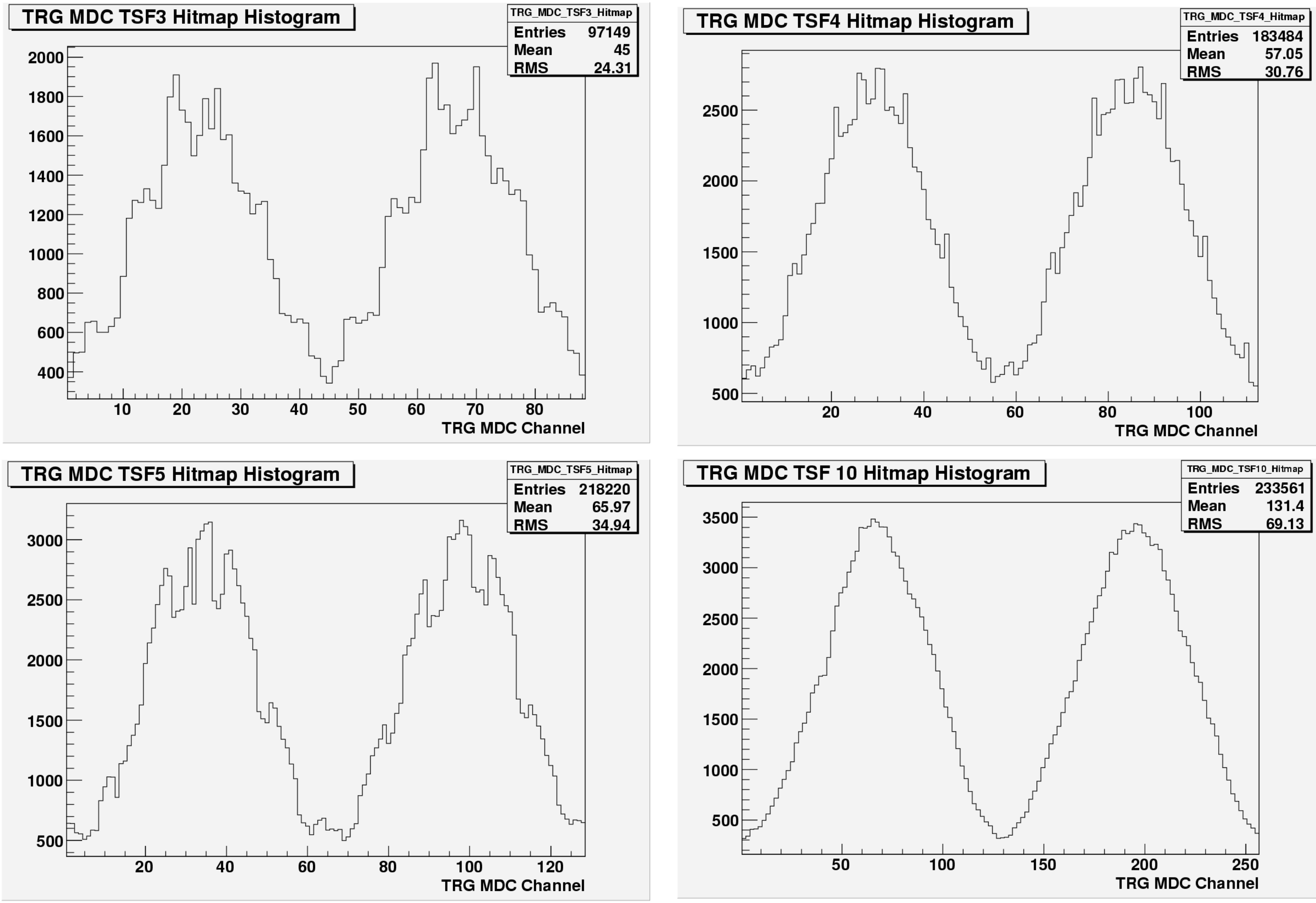
TrgTOF East && West

Hit map of TOF sub-trigger

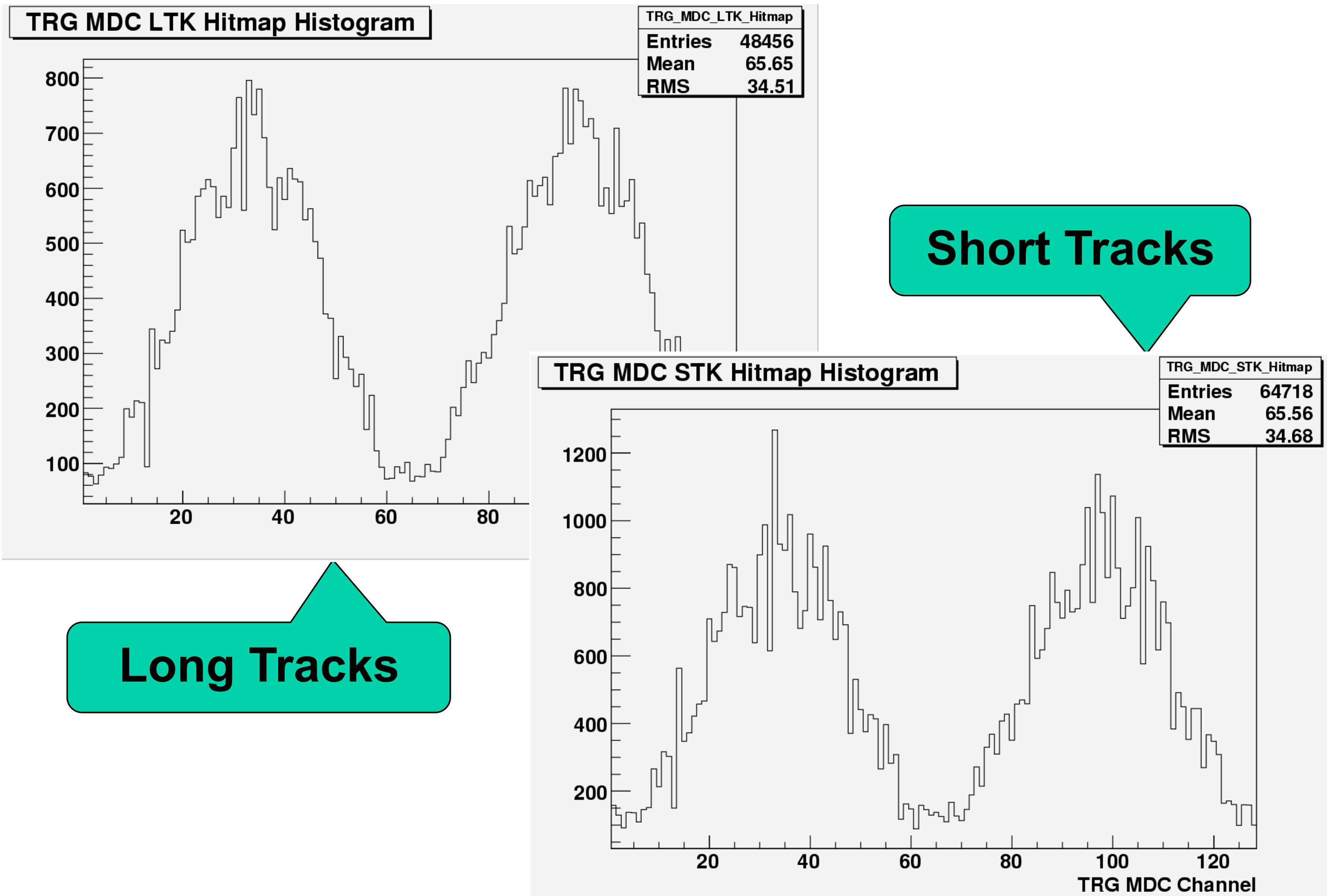
MDC sub-trigger



Hit map of MDC sub-trigger : Layer

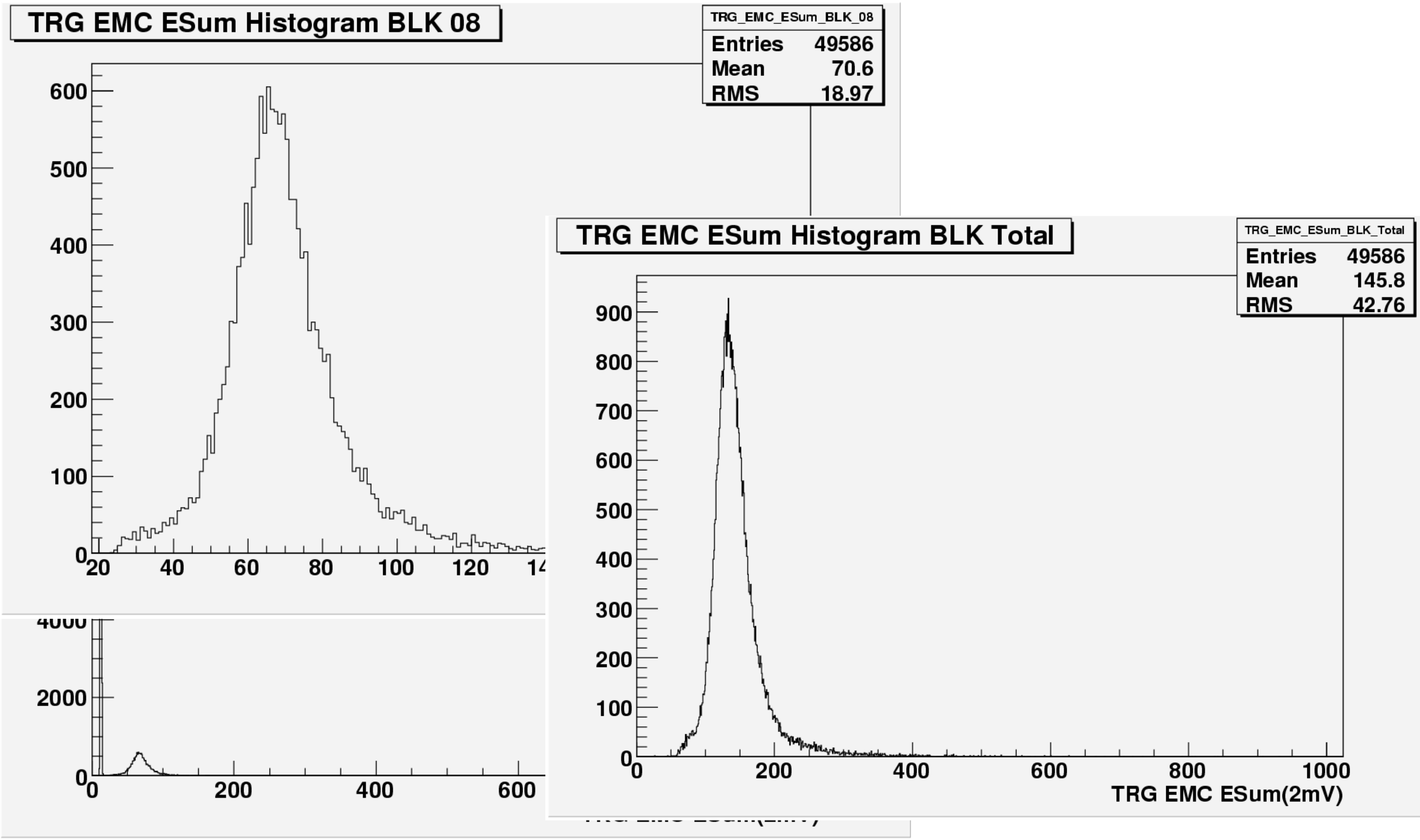


Hit map of MDC sub-trigger : TSF



Hit map of MDC sub-trigger : TRK

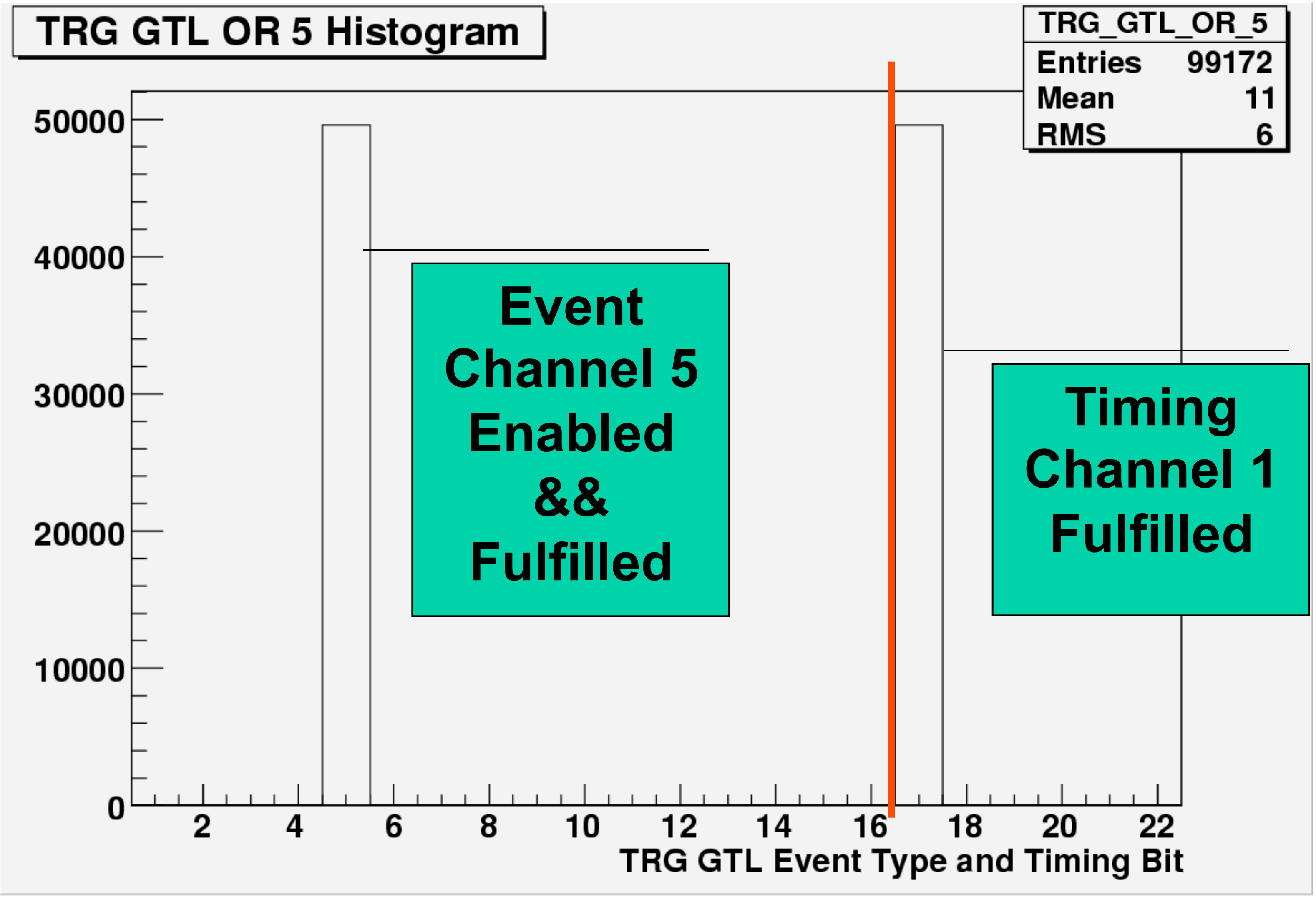
EMC sub-Trigger



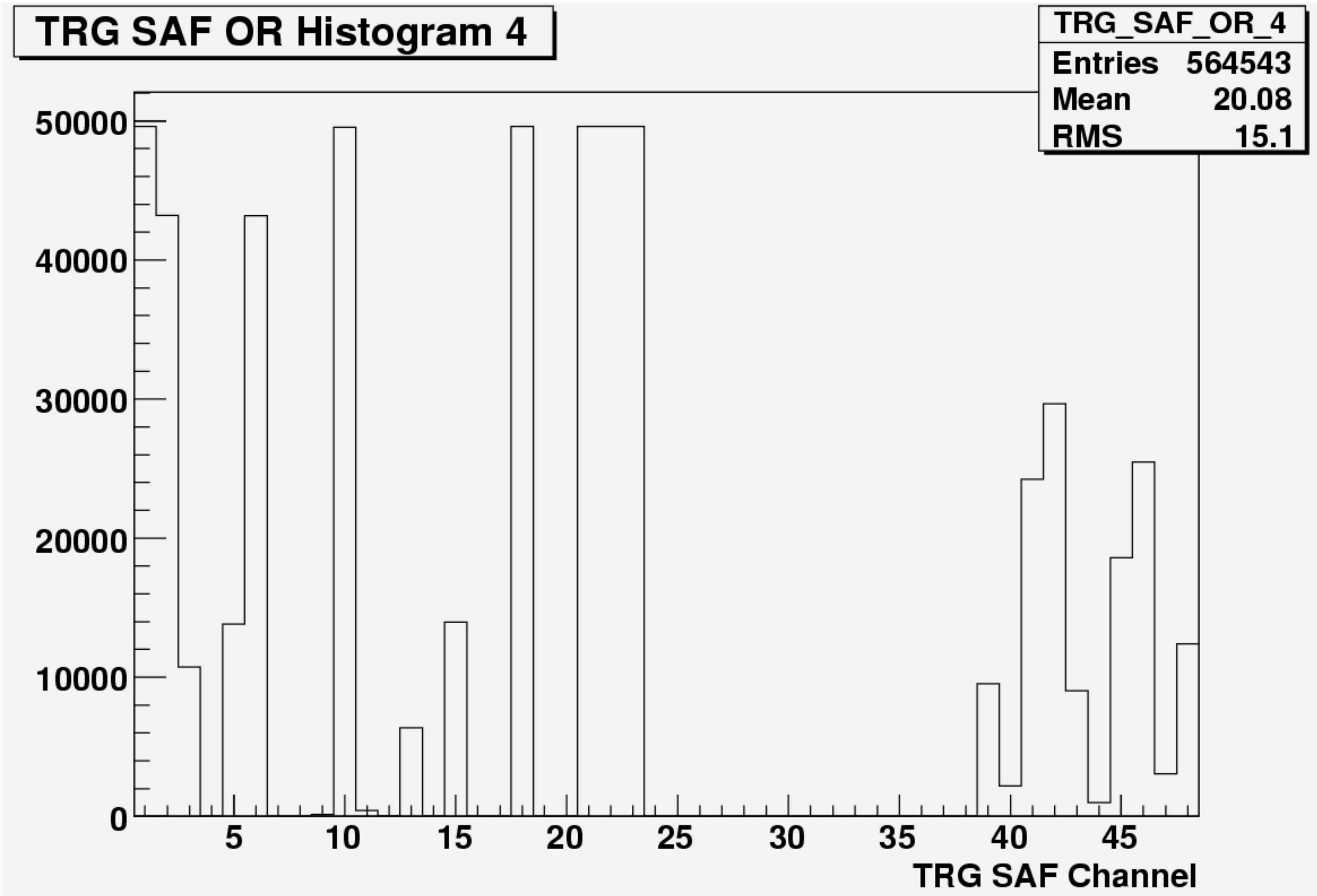
Hit map of EMC sub-trigger : Energy

Hit map of EMC sub-trigger : TC Hits

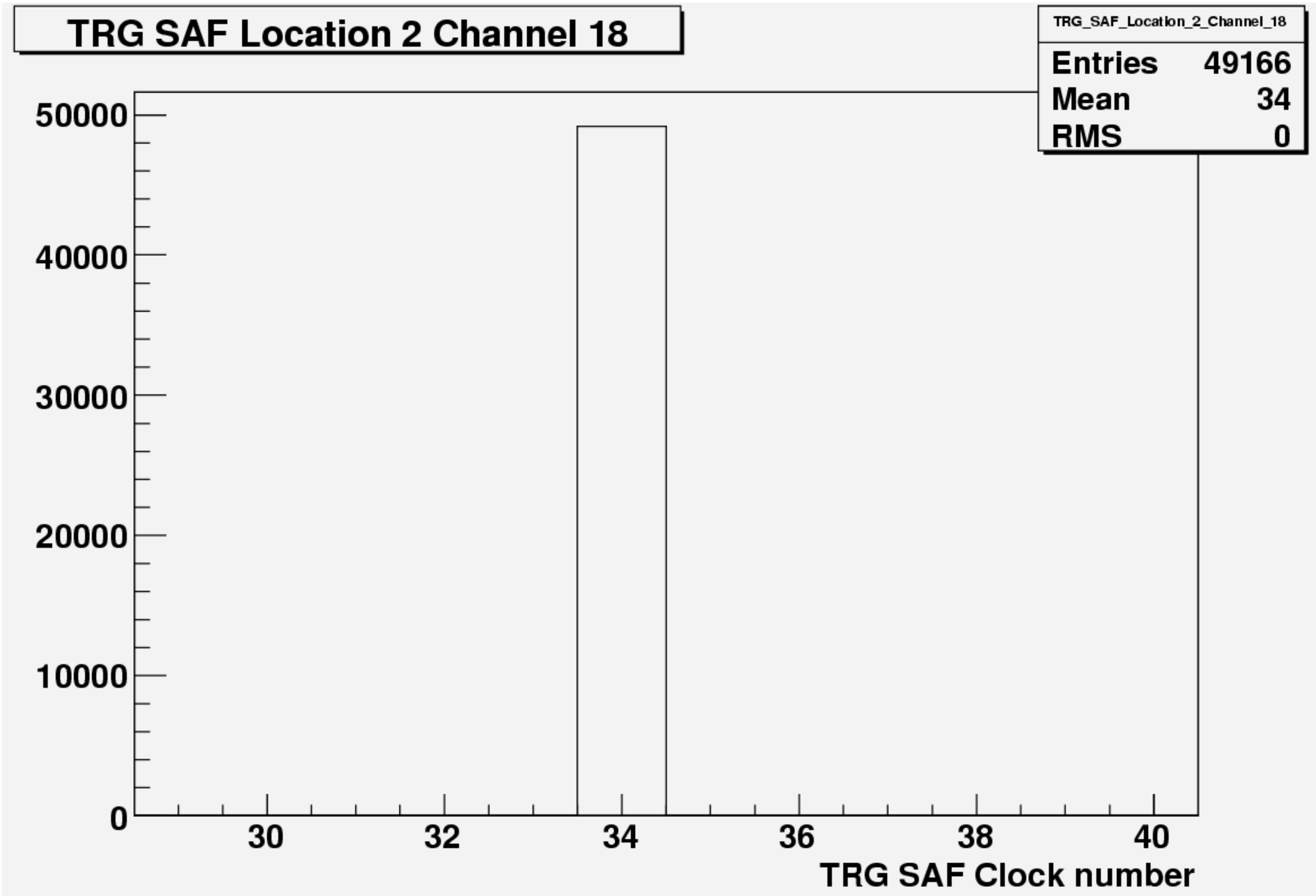
Global Trigger



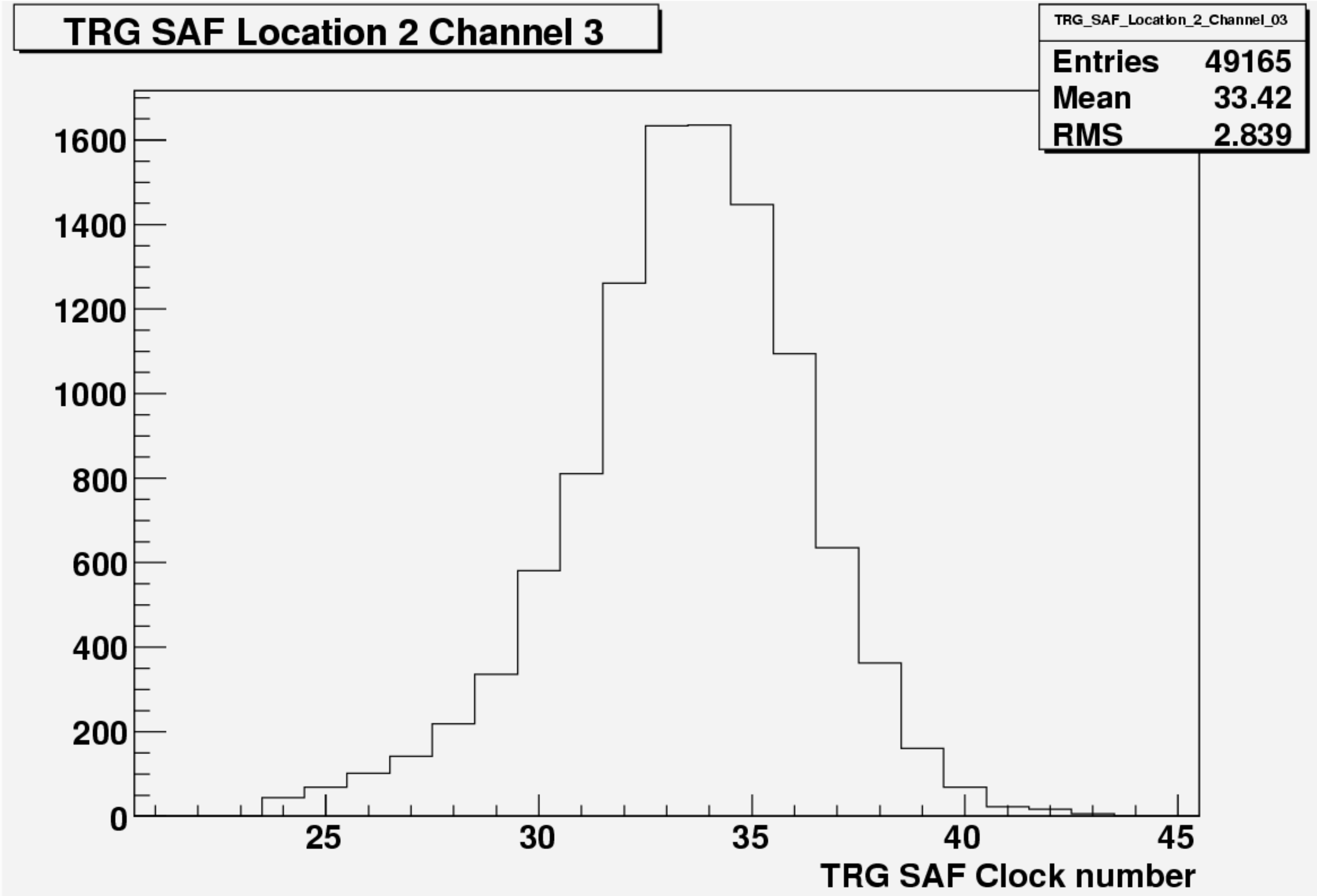
Event types and Timing types



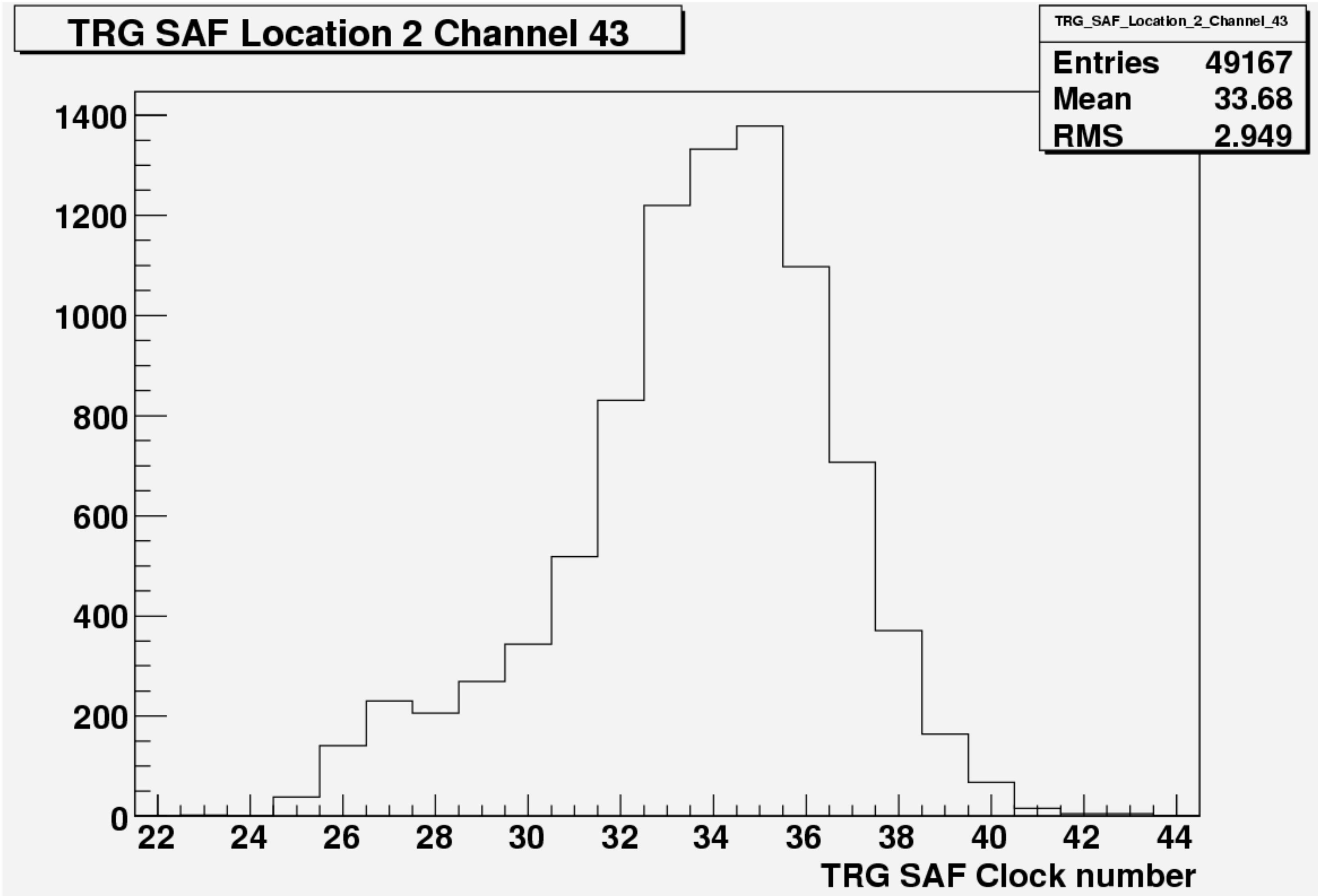
Hit map of trigger conditions



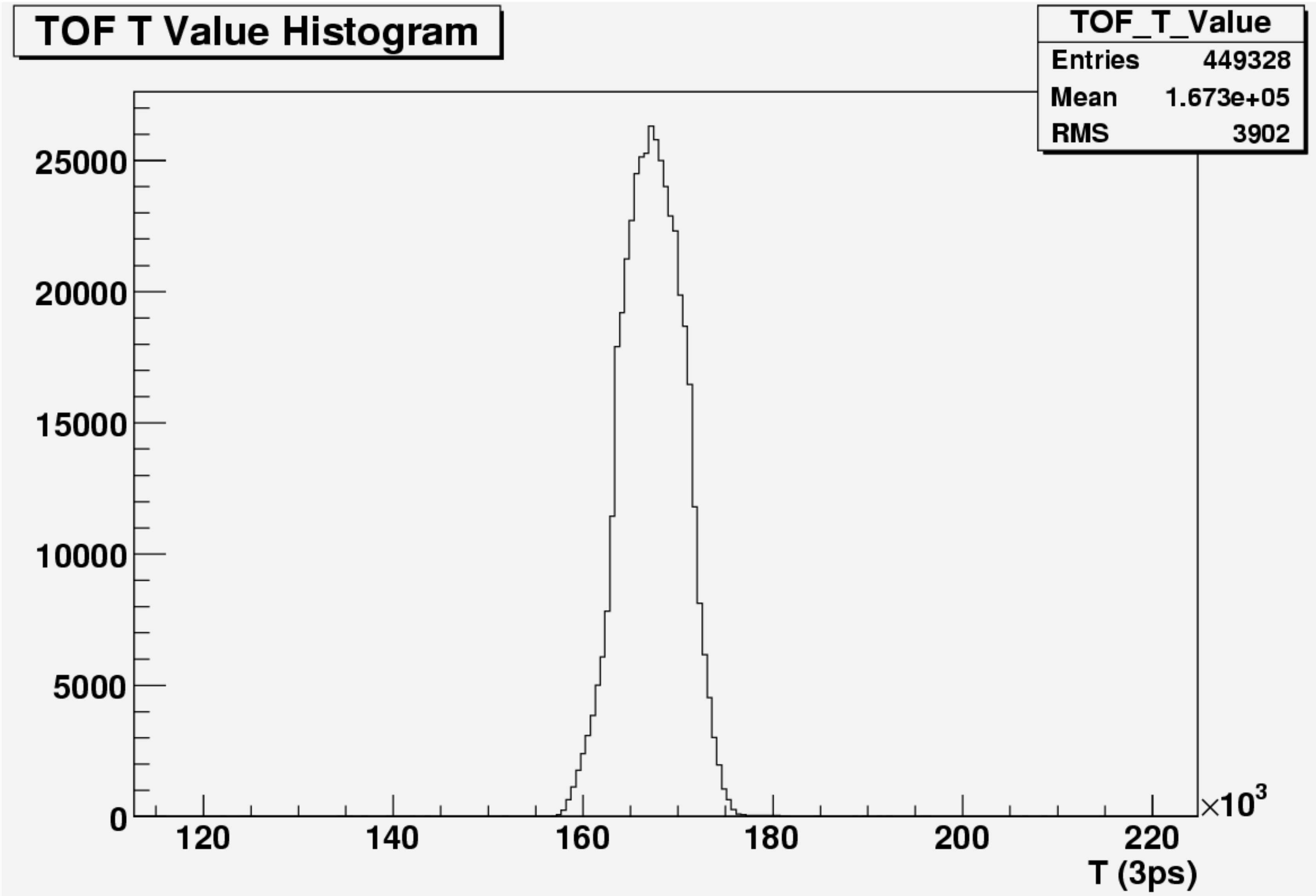
Timing alignment : BTOF-BB



Timing alignment : BClus-BB



Timing alignment : Ltrk-BB



T value of TOF electronics

BESIII触发系统小结

- 27种不同的插件通过特殊设计缩减为21种（固件不同功能不同）
- 利用了光纤隔离技术排除共地干扰
- 采用最新的FPGA芯片进行设计
- 硬件设计标准化，提高了可维护性
- 系统可重构：采用了在线下载，功能可根据需要改变
- 克服了面临的挑战与困难:
  - 条件有限（工具、软件支持等）
  - 时间紧迫，任务重
- 该系统的设计在世界上是领先的，得到认可。
- 2008年运行以来稳定运行

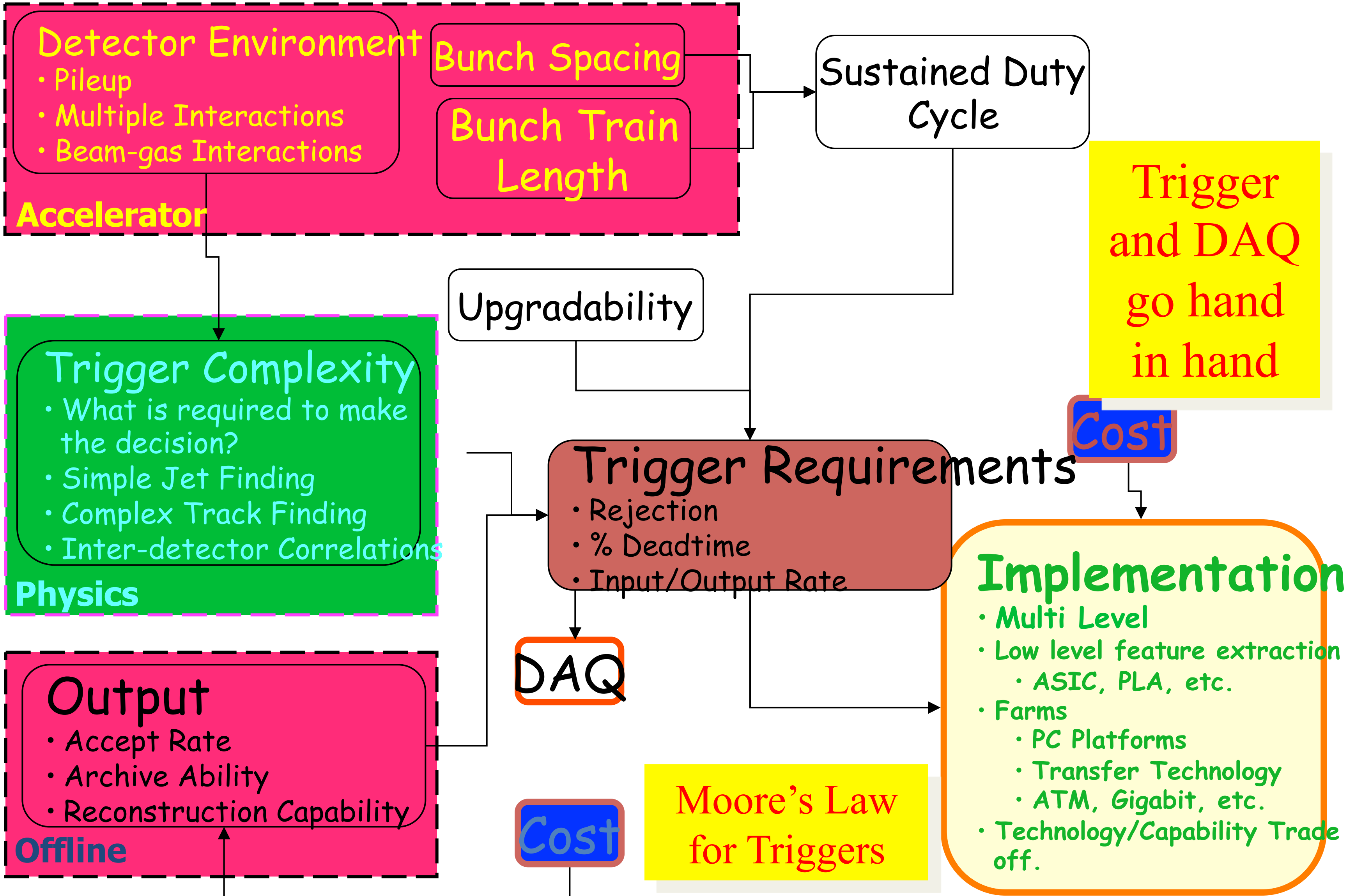
因此，我们要有信心，我们能够做出世界水平的工作。

与大家共勉

未来触发与数据获取的发展

- 其他实验的TDAQ简介
- 未来TDAQ的发展趋势
- 范例：PANDA实验

限制条件 → a multiparameters problem

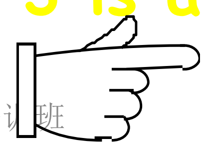


世界上各大对撞机实验参数

Exp. *Year*	Collision rate	Channel count	L1A rate	Event building	Processing. Power	Sociology
UA's *1980*	3 μsec	-	-	-	5-10 MIPS	150-200
LE *1989*	10-20 μsec	250 - 500K	-	10 Mbit /sec	100 MIPS	300-500
BESI/II *1989*	800nsec	-	15			
BaBar *1999*	4 ns	150K	2 KHz	400 Mbit /s	1000 MIPS	400
Tevatron *2002*	396 ns	~ 800 K	10 - 50 KHz	4-10 Gbit /sec	5.10^4 MIPS	500
LHC *2007*	25 ns	200 M*	100 KHz	20-500 Gbit/s	$>10^6$ MIPS	2500
BESIII *2008*	8 ns	100K	4 KHz	400 Mbit /s		
ILC *2020 ?*	330 ns	900 M*	3 KHz	10 Gbit/s	$\sim10^6$ MIPS ?	> 3000 ?

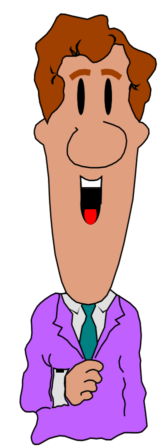
当今世界上的多级触发

- **Required rejection is orders of magnitude**
  - –Algorithms to attain required rejection are too sophisticated.
  - –Accelerator backgrounds can also contribute to the problem
    - → e^+e^- vs pp
- **Level 1 is hardware based**
  - –Crude signatures (hits, local energy deposit over threshold…)
  - –Operates on reduced or coarse detector data
- **Level 2 is often a composite**
  - –Hardware to preprocess data
    - •Some Muon processors, Silicon Triggers
  - –Software to combine
    - •Matches, Jet finders, etc.
- **Level 3 is a farm → General Purpose CPUs**

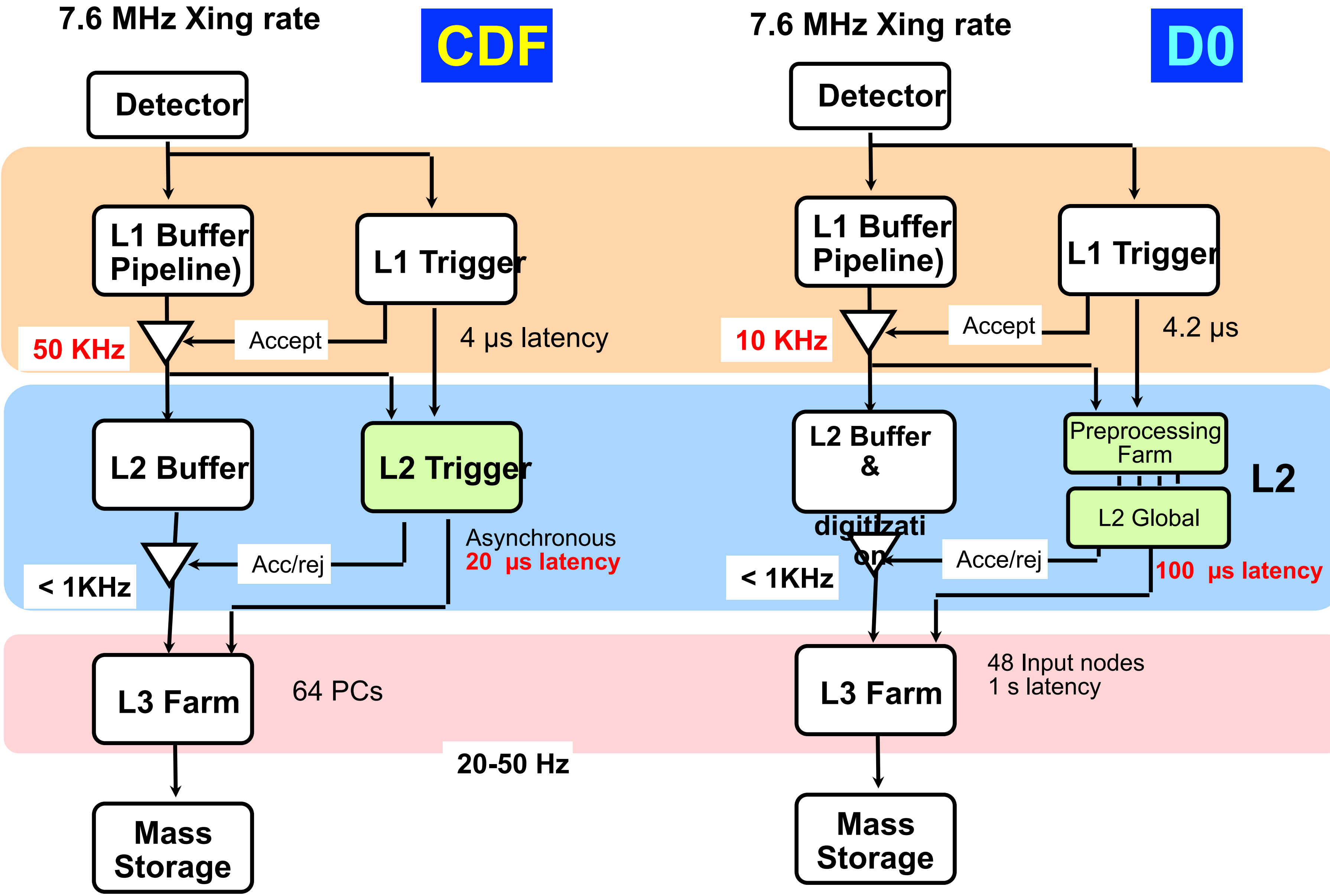


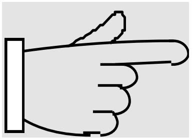
Almost every one uses this scheme

–Vary number and function of levels.



费米实验室Tevatron 触发结构 (RUN 2)





LHC上的触发判选

40 MHz

L1

- "Local" identification of high Pt objects → *use coarse dedicated data*
  - Electrons /Photons , Hadrons & Jets → Energy clusters
  - Muons → Track segments
  - Neutrinos → Missing Et

100 KHz

L2

- Particle signature (e/g,h,Jet, μ ...) → *use final digitized data*
  - Refine Pt cuts → fine granularity & track reconstruction
  - Combine detectors → Converted electron ,"Punchthrough", decays

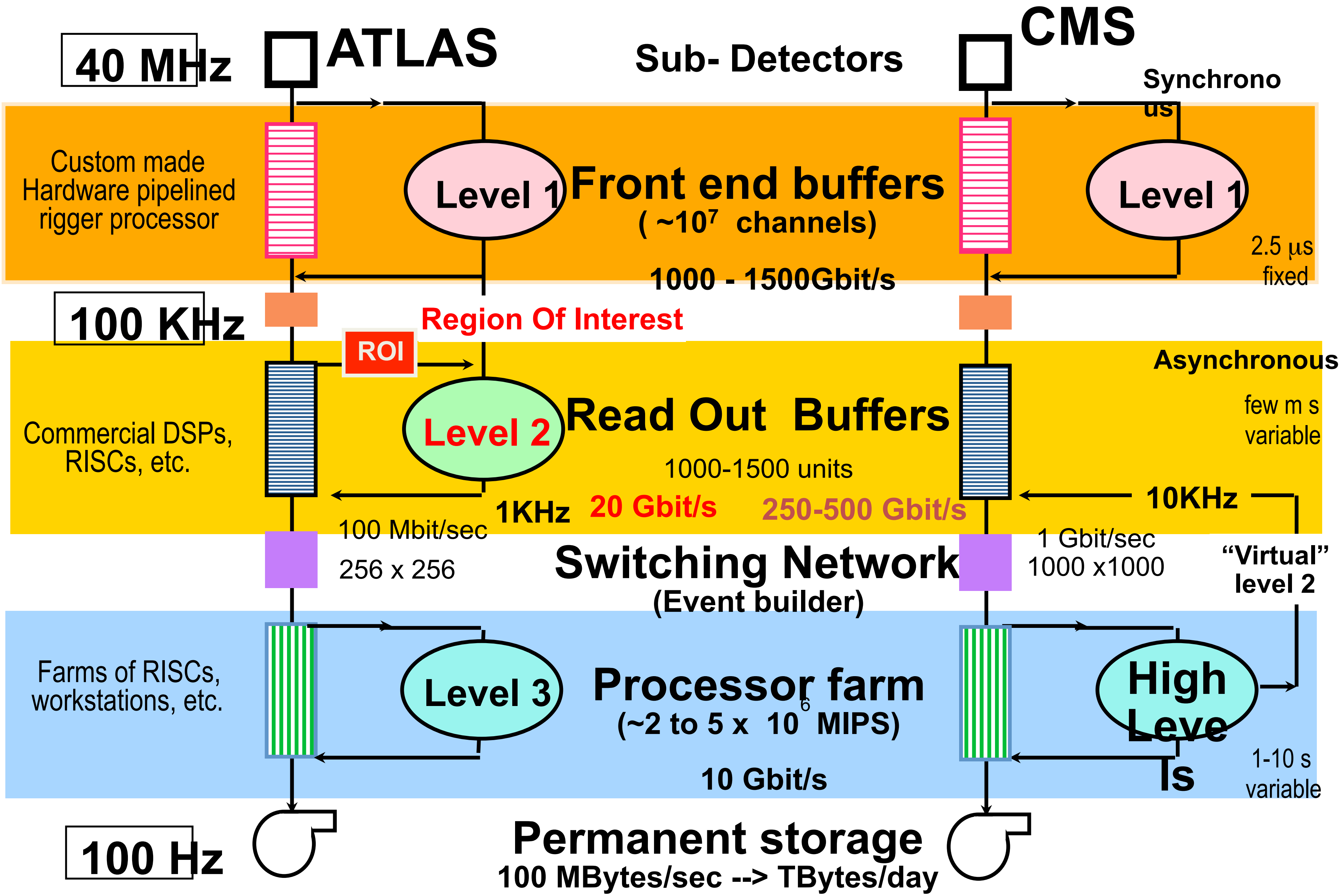
1 KHz

L3

- **Global topology** → multiplicity & thresholds

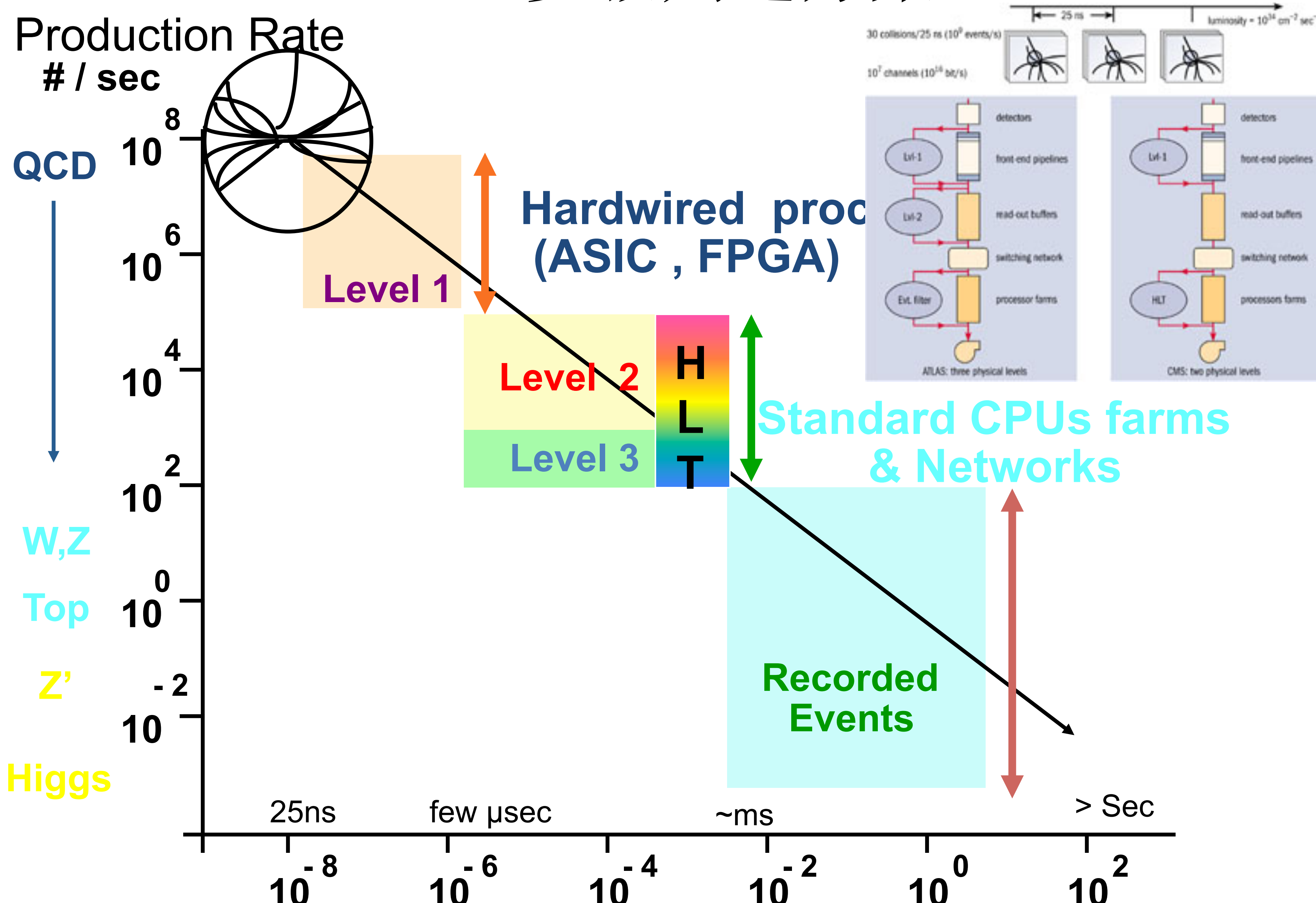
100 Hz

LHC 触发的逻辑结构



40 MHz
ATLAS
Sub- Detectors
CMS
Synchronous
Custom made
Hardware pipelined
rigger processor
Level 1
Front end buffers
(~10^7 channels)
Level 1
2.5 μs
fixed
1000 - 1500Gbit/s
100 KHz
Region Of Interest
ROI
Asynchronous
Commercial DSPs,
RISCs, etc.
Level 2
Read Out Buffers
few m s
variable
1000-1500 units
1KHz
20 Gbit/s
250-500 Gbit/s
10KHz
100 Mbit/sec
256 x 256
Switching Network
(Event builder)
1 Gbit/sec
1000 x1000
"Virtual"
level 2
Farms of RISCs,
workstations, etc.
Level 3
Processor farm
(~2 to 5 x 10^6 MIPS)
High Levels
1-10 s
variable
10 Gbit/s
100 Hz
Permanent storage
100 MBytes/sec --> TBytes/day

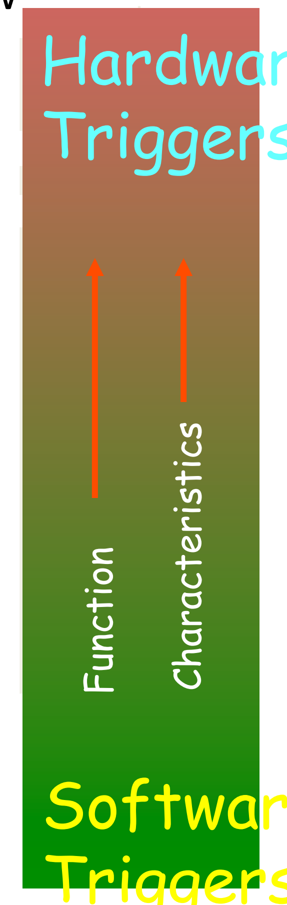
LHC 多级判选方案



Production Rate
/ sec
QCD
W,Z
Top
Z'
Higgs
10^8
10^6
10^4
10^2
10^0
10^-2
Level 1
Level 2
Level 3
HLT
Hardwired proc
(ASIC , FPGA)
Standard CPUs farms
& Networks
Recorded
Events
25ns
few µsec
~ms
> Sec
10^-8
10^-6
10^-4
10^-2
10^0
10^2
25 ns
luminosity = 10^34 cm^-2 sec^-1
30 collisions/25 ns (10^9 events/s)
10^7 channels (10^16 bit/s)
detectors
front-end pipelines
read-out buffers
switching network
processor farms
processors farms
Lvl-1
Lvl-2
Evt. filter
HLT
ATLAS: three physical levels
CMS: two physical levels

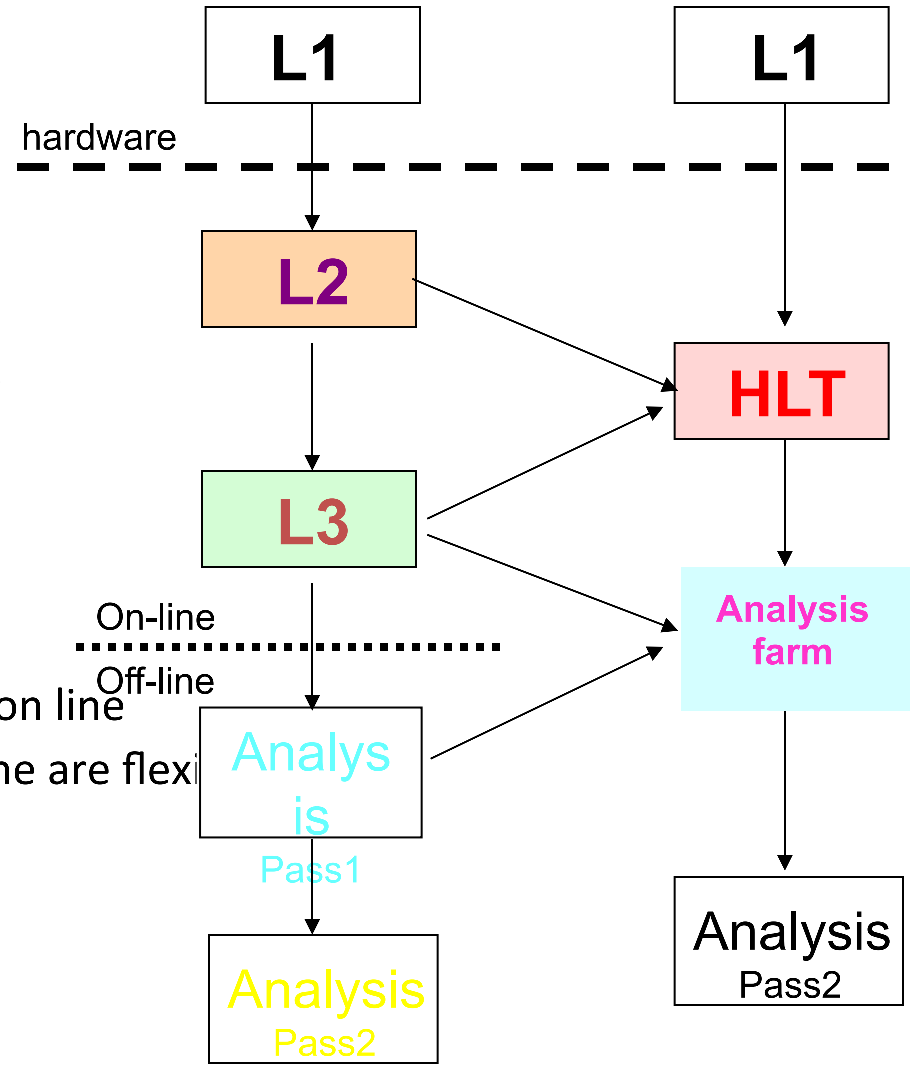
正在进行的演变 (Tevatron,LHC …)

- Higher level trigger decisions are migrating to the lower levels
  → Software Migration is following functional migration
  - Correlations that used to be done at Level 2 or Level 3 in are now done at Level 1.
  - More complex trigger (impact parameter!) decisions at earlier times (HLT) → Less bandwith out of detector?
- Boundaries
  - L2 and L3 are merging into High Levels Triggers
  - DAQ and trigger data flow are merging
  - On-line and off-line boundaries are flexible
- Recent Developments in Electronics
  - Line between software and hardware is blurring
  - Complex Algorithms in hardware (FPGAs)
  - Possible to have logic designs change after board layout
  - Fully commercial components for high levels.



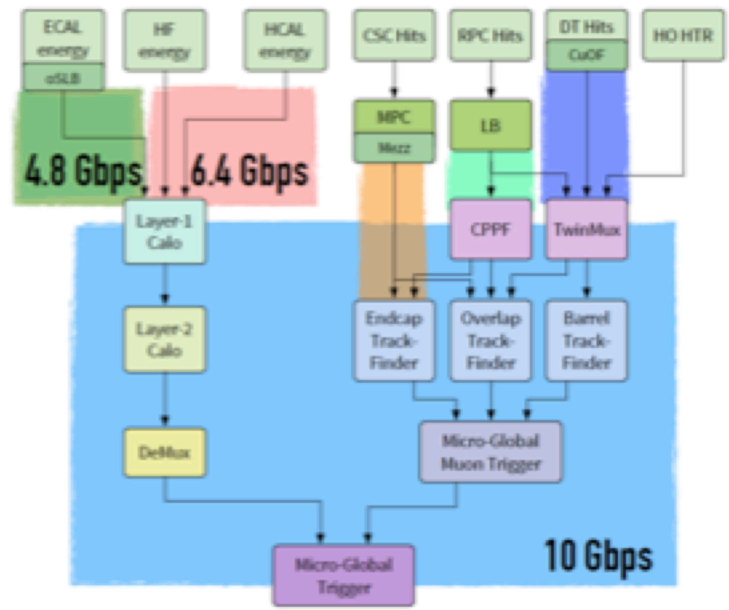
T/DAQ 结构演变小结

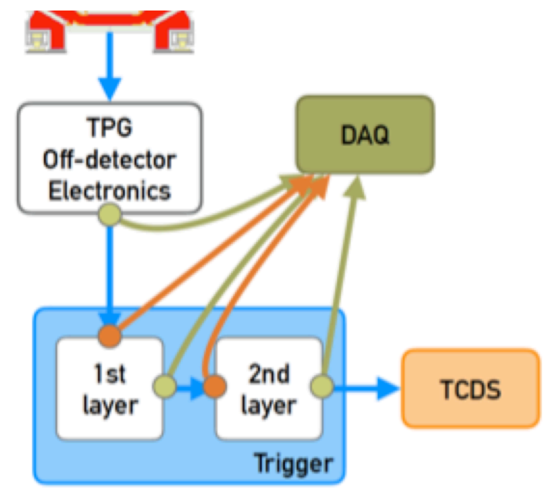
- Today
  - Tree structure and partitions
  - Processing farms at very highest levels
  - Trigger and DAQ dataflow are merging
- Near future
  - Data and control networks merged
  - Processing farm already at L2 (HLT)
  - More complex algorithms are moving on line
  - Boundaries between on-line and off-line are flexi
  - Commodity components at HLT



Key technologies

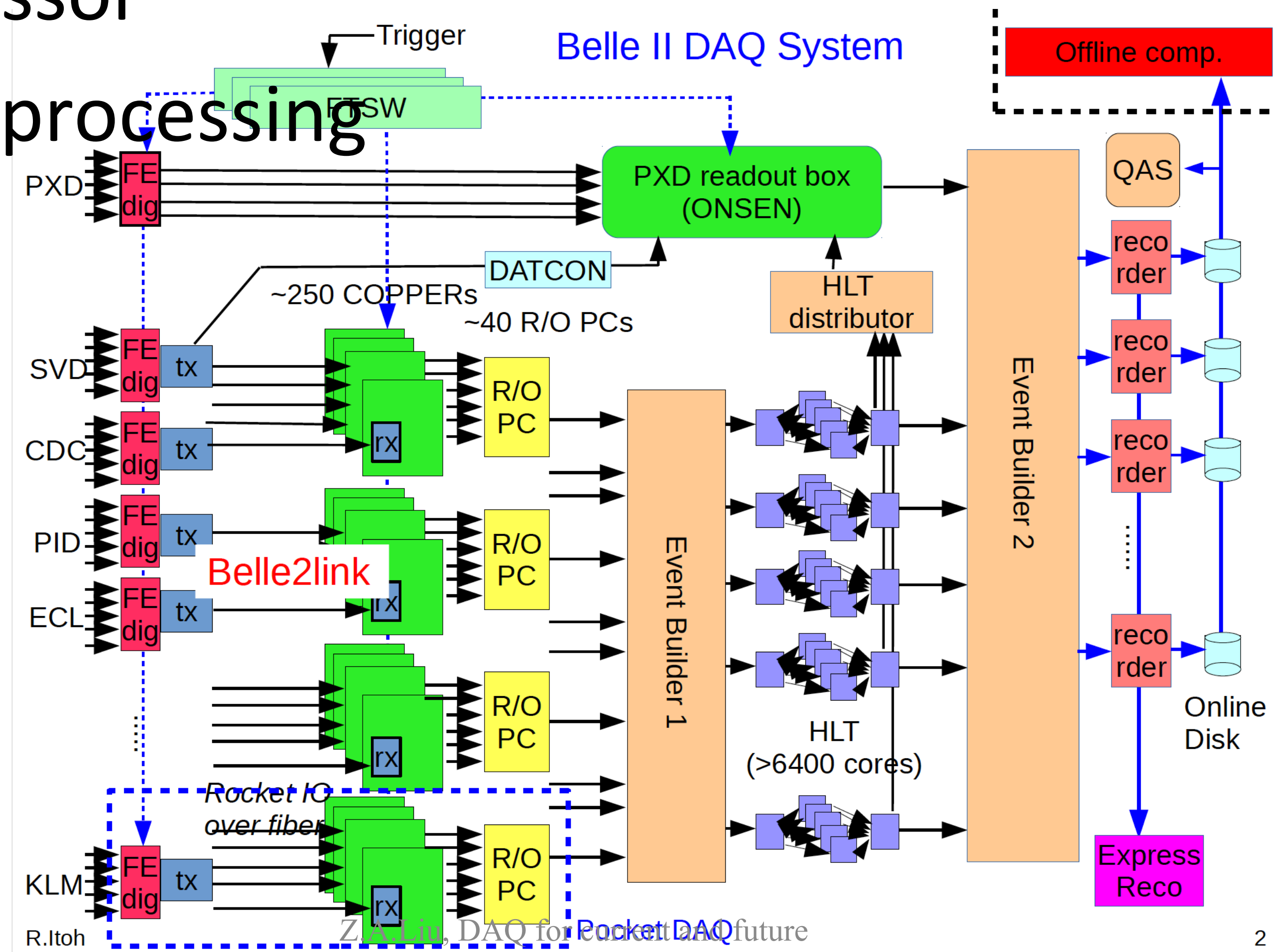
- Centralized timing and control
- Higher digitization speed and data bandwidth(1.6Gbps-6.4Gbps)
- Unified readout
- New data BUS architecture(VME to MTCA/ ATCA)
- Scalable system
- Upgradable system





Unification in Belle II

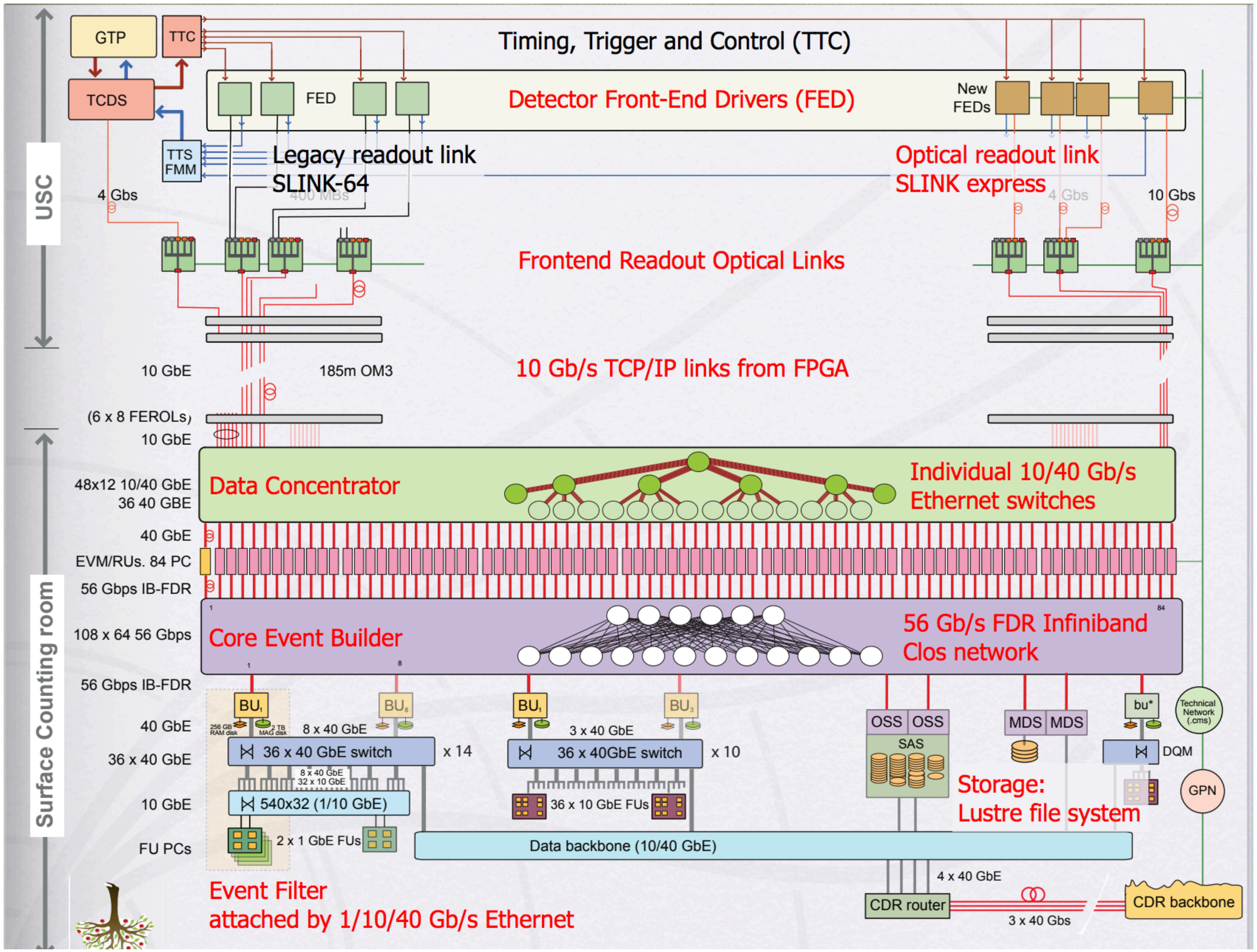
- Readout unification:Belle2link
- Processing: common processor, COPPER/new processor
- Local processing



Present CMS DAQ as example

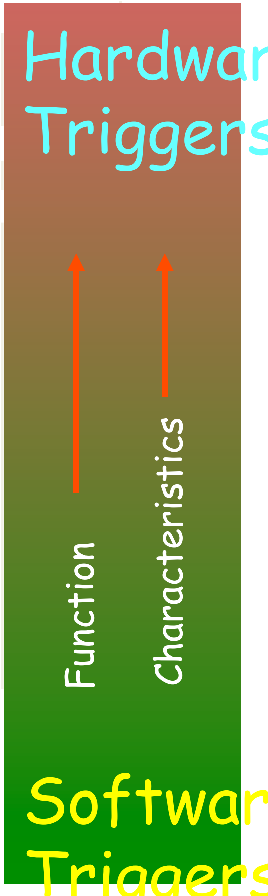
- FEE in MTCA
- 10Gbps bandwidth in data concentrator
- Networking, Ethernet
  - Not a reliable network in switched environment
  - Speed
    - 40 GbE exists on switch and NIC since ~2012
    - 100 GbE exists but still very expensive
    - 400 Gbps defined
  - High-Performance Computing (HPC) Fabric interconnect
    - Low-latency, reliable
    - Infiniband 4xFDR 56 Gbps and 4xEDR 100 Gbps available
    - New fabric interconnect forthcoming ..
      - 128 Gbps (2017-18), 200 Gbps (after 2020)
      - Integration of fabric port onto the CPU socket
  - Both technologies have switches with ~50 Tbps

CMS DAQ block diagram



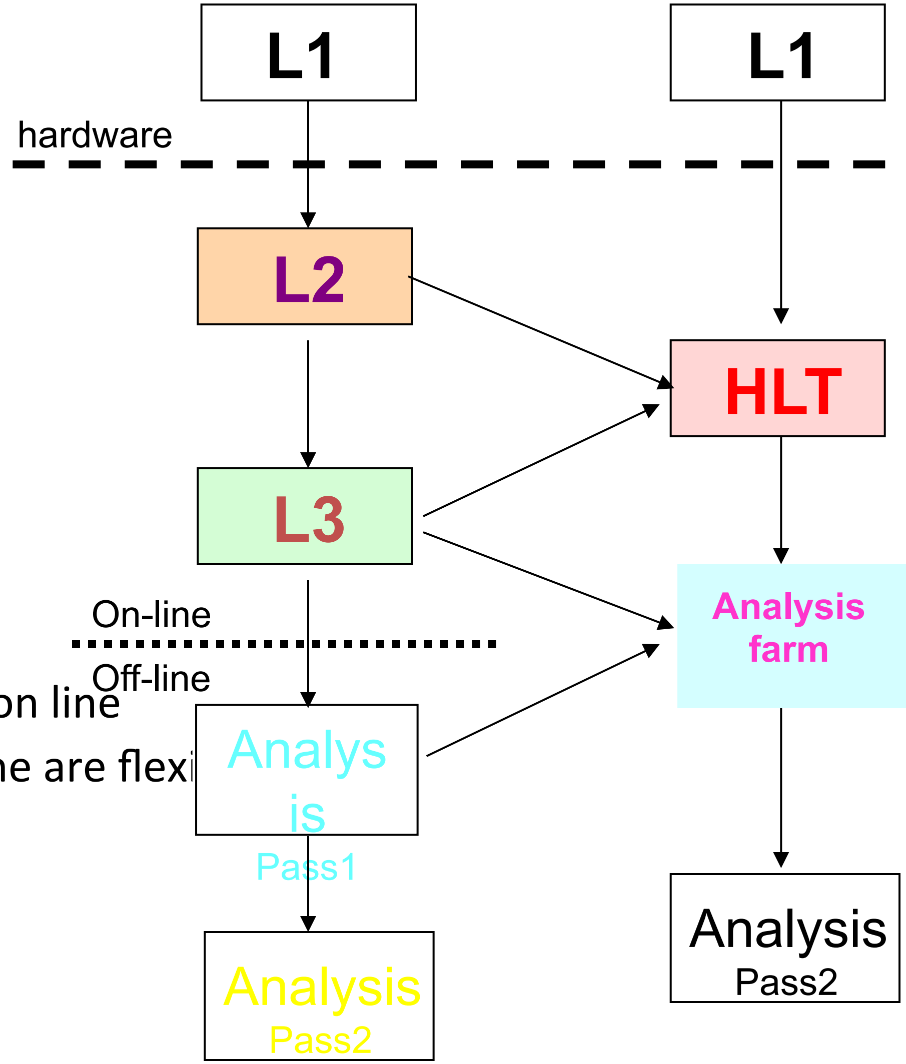
Technology evolution (Tevatron,LHC …)

- **Higher level trigger decisions are migrating to the lower levels → Software Migration is following functional migration**
  - Correlations that used to be done at Level 2 or Level 3 in are now done at Level 1.
  - More complex trigger (impact parameter!) decisions at earlier times (HLT) → Less bandwith out of detector?
- **Boundaries**
  - L2 and L3 are merging into High Levels Triggers
  - DAQ and trigger data flow are merging
  - On-line and off-line boundaries are flexible
- **Recent Developments in Electronics**
  - Line between software and hardware is blurring
  - Complex Algorithms in hardware (FPGAs)
  - Possible to have logic designs change after board layout
  - Fully commercial components for high levels.



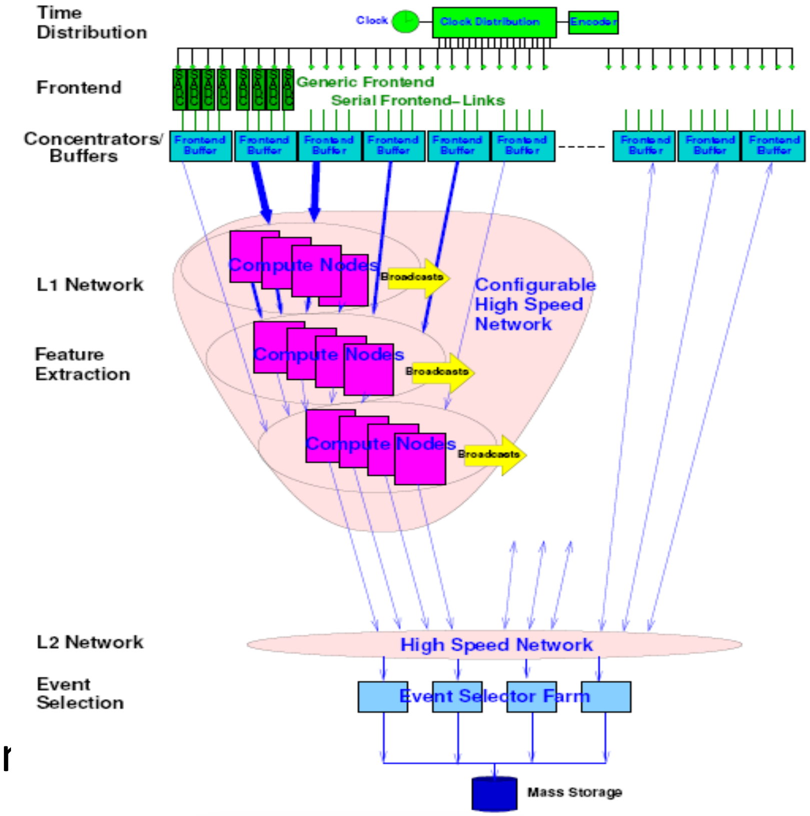
Hardware trigger less TDAQ

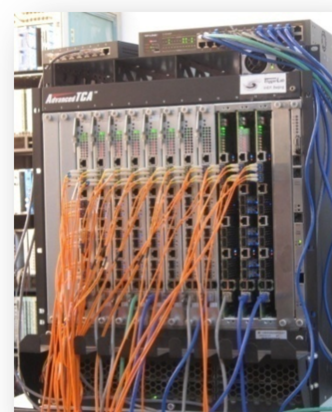
- Today
  - Tree structure and partitions
  - Processing farms at very highest levels
  - Trigger and DAQ dataflow are merging
- Near future
  - Data and control networks merged
  - Processing farm already at L2 (HLT)
  - More complex algorithms are moving on line
  - Boundaries between on-line and off-line are flexi
  - Commodity components at HLT



Hardware triggerless in PANDA Experiment

- Long time collaboration between Labs
  - TrigLab, Exp. Phys. Center,IHEP
  - II. Phy. Institut, Giessen Univ,Germany
  - Since 2006 on
    - PANDA Experiment
    - DEPFET Project
- Research
  - New Trigger and DAQ (TDAQ) Archietecture
  - Design of High Performance Compute Node(CN)
  - Firm/Software design of TDAQ with Built-Ir system on FPGA
- IHEP Responsibility
  - Responsible for Hardware Design, system test
  - Responsible for Setup of system platform
  - Participate in software development
  - Responsible and accomplishment of EMC trigger study





CN's under testing at IHEP

New standard for Physics: xTCA

- xTCA:
  - New standard after VME, CPCI, CAMAC,…
  - For machine control and measurement
  - Standands for: ATCA,MTCA,AMC, with new extentions
- IHEP is a co-founder of this new standard
  - DESY, FNAL, IHEP , SLAC
  - Cypress Point Research and Performance Technologies
- Organization
  - Coordination Committee(CCTS),PICMG
  - Officers:Chair(SLAC),Secretery(Triple Ring), Document Editor（IHEP）
  - Hardware working group (weekly meeting)
  - Software working Group(weekly meeting)
- Status
  - IHEP organized 3rd xTCA workshop in IHEP/Beijing
  - Two hardware specifications officially issued
    - PICMG 3.8
    - MTCA.4
- Reference
  - http://www.picmg.org/pdf/PICMG_Physics_Public_Web_Update_061209_R5-3.pdf

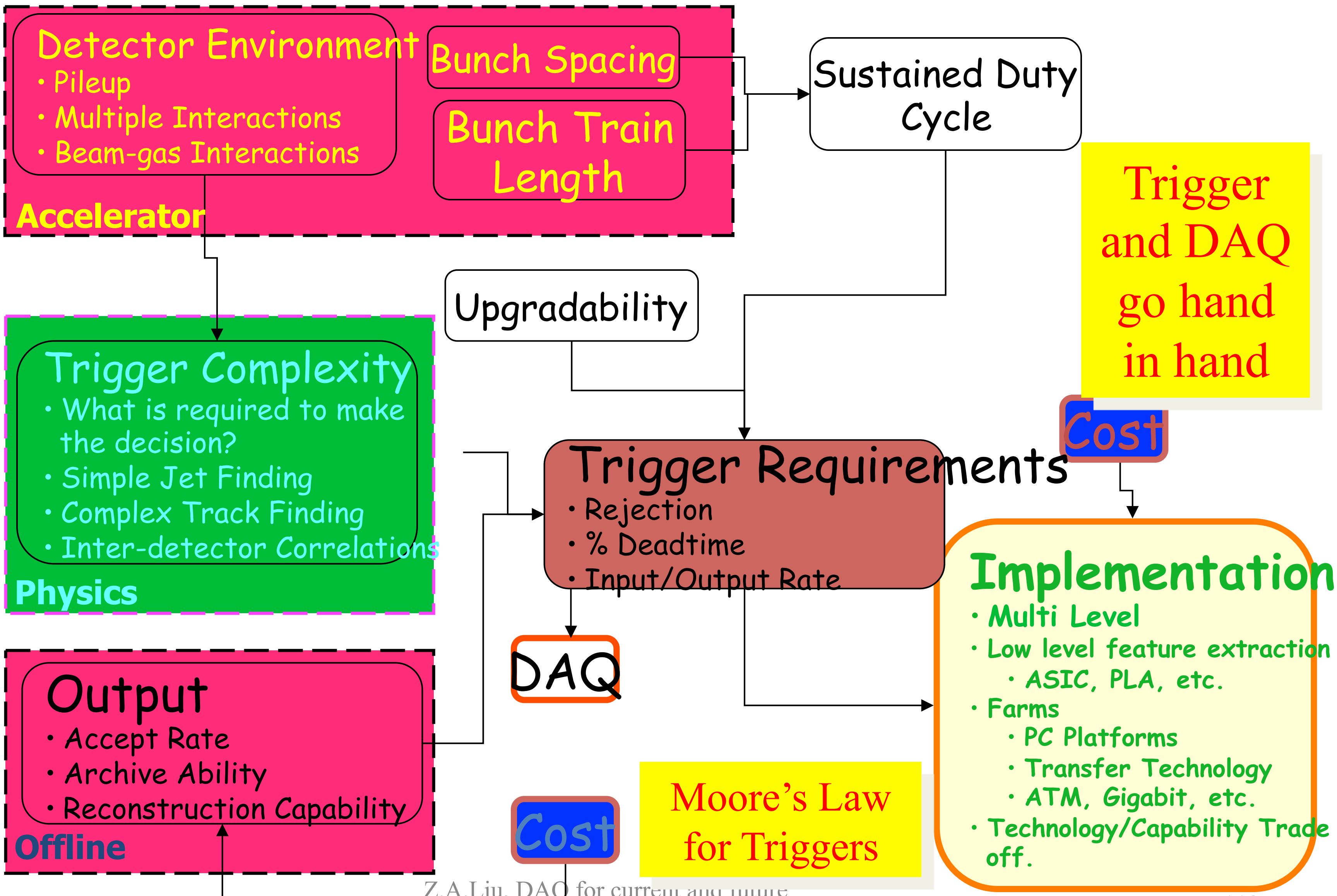
Open Modular Computing Specifications

phyTCA
xTCA™ for Physics

PICMG 3.8
AdvancedTCA Rear Transition Module

MTCA.4
MicroTCA® Enhancements for Rear I/O and Precision Timing

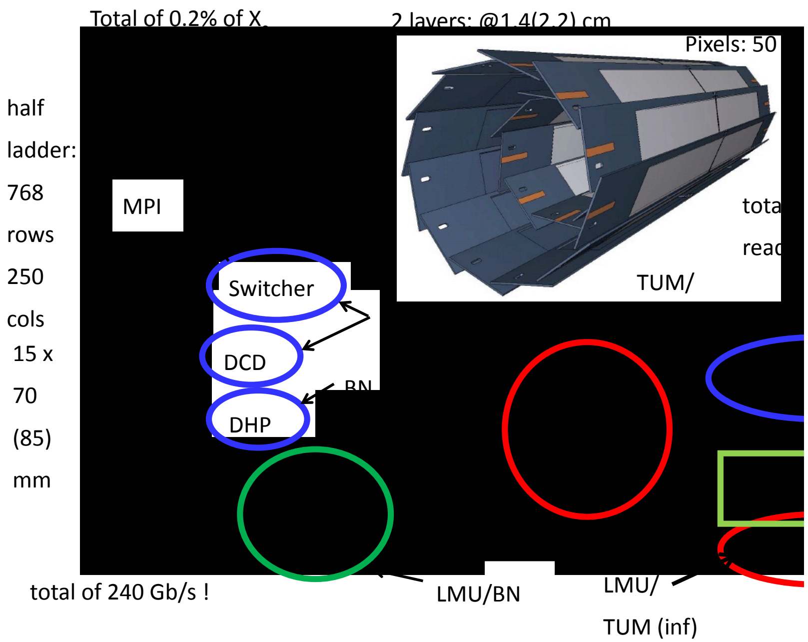
Constraints → a multiparameters problem



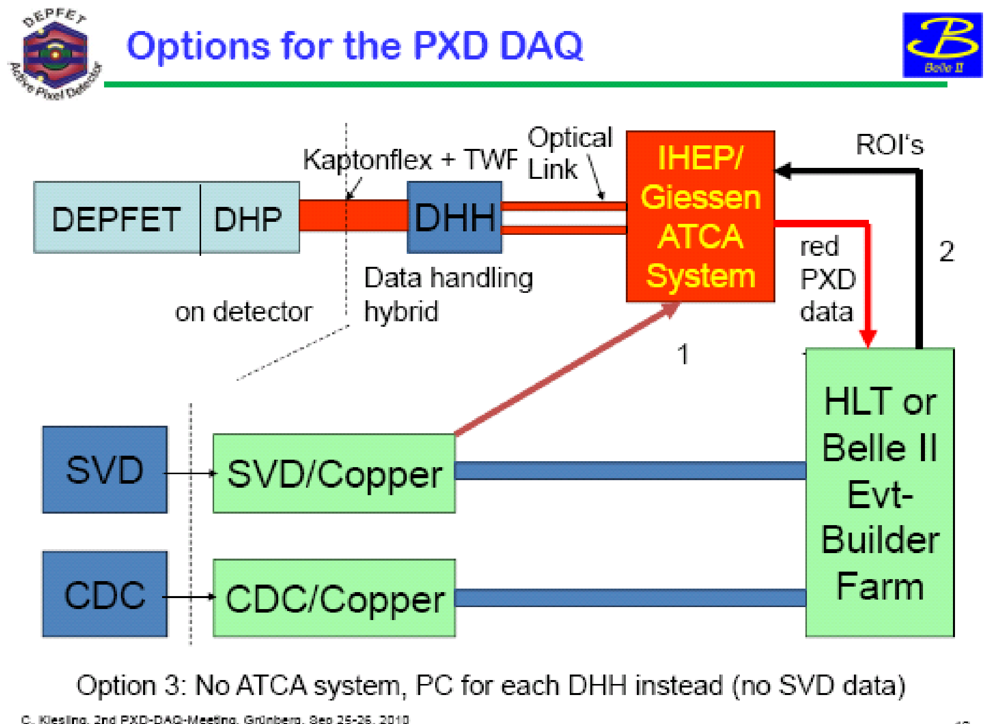
More thinking for future DAQ

- Backwards of present event building
  - Uses hardware inefficiently
  - Needs a lot of resources to transport data which is mostly unused
    - Used only for L1 trigger
    - Not processed by HLT and then discarded
  - Network b/w is used only in one direction
- Think more of a mesh (or even idea of IoT)
  - Leave data as close as possible to the detector
  - Pre-process it locally
    - Specialized processors(custom or commercial)
    - Generic CPUs
  - Access it remotely
    - Event-building on demand
  - Continuous calibrations with feedback to processors
    - Allows near offline-quality selection to reduce the event rate
    - Blurs boundary between online and offline reconstruction

Idea for Local Processing in Belle II PXD

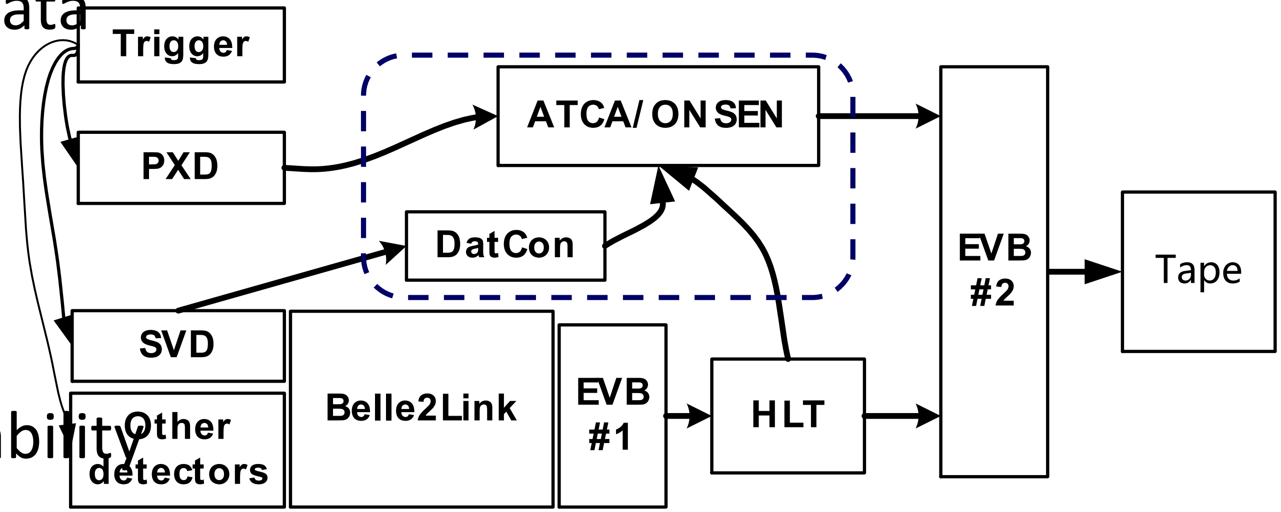


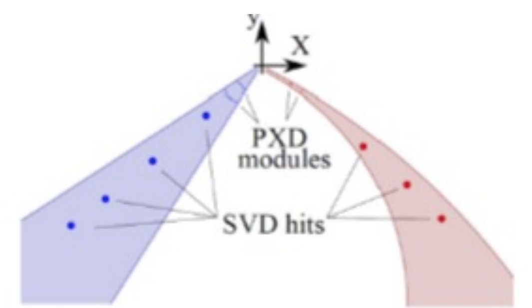
- Huge data output
  - 240Gb/s
  - >sum of Belle II others
- Reduction 1/10

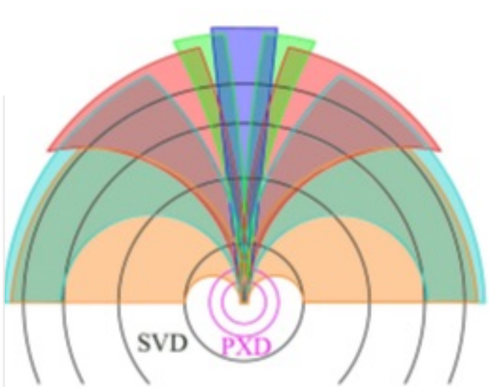


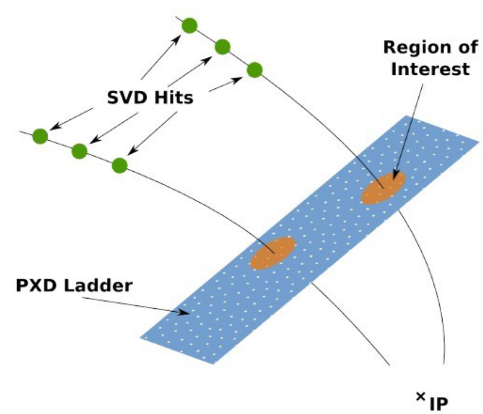
Principle of reduction

- PXD reduction
  - Based on HLT result
  - Help with SVD data
  - Tracking back
  - ROI searching
  - Data extraction
- Difficulties
  - Computing capability
  - Algorithms
  - 5s data buffer



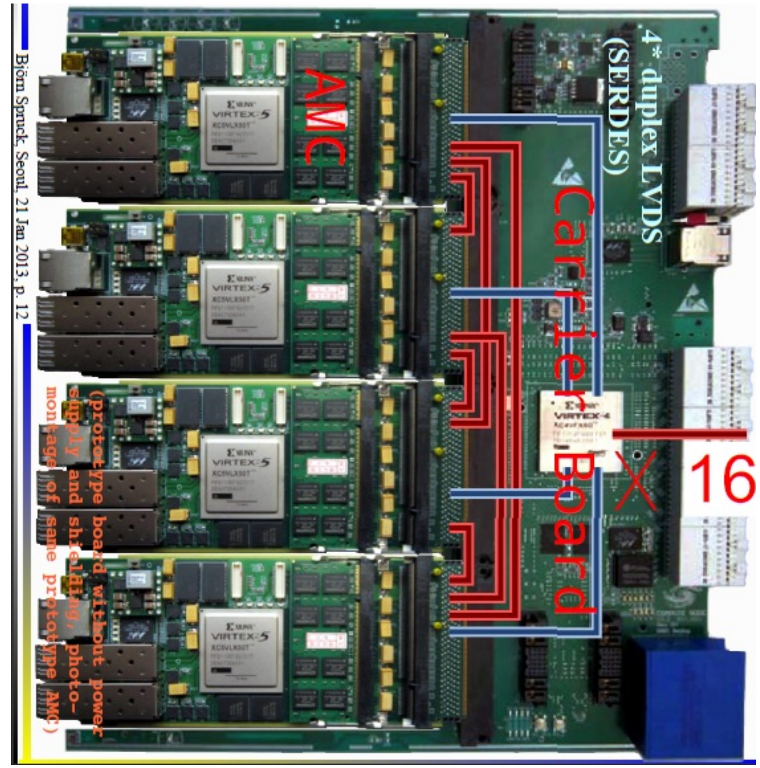


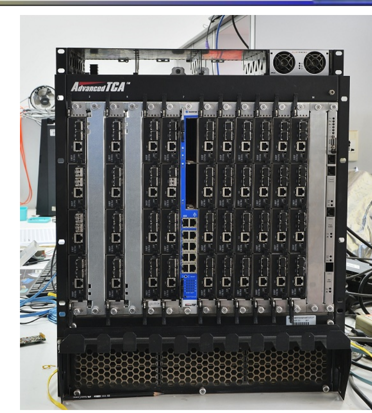




Key parts of PXD-reduction

- ONSEN/PXD-DAQ
  - Firmware(Giessen Uni)
  - Hardware(IHEP Beijing)
    - 1 ATCA Shelf
    - 2 shelf managers
    - 1 Power Supply
    - 10 Compute Node(CN)
      - 1 ATCA Carrier(PICMG3.8)
      - 1 Power Board
      - 4 xFP/AMC cards
      - 5 MMCs





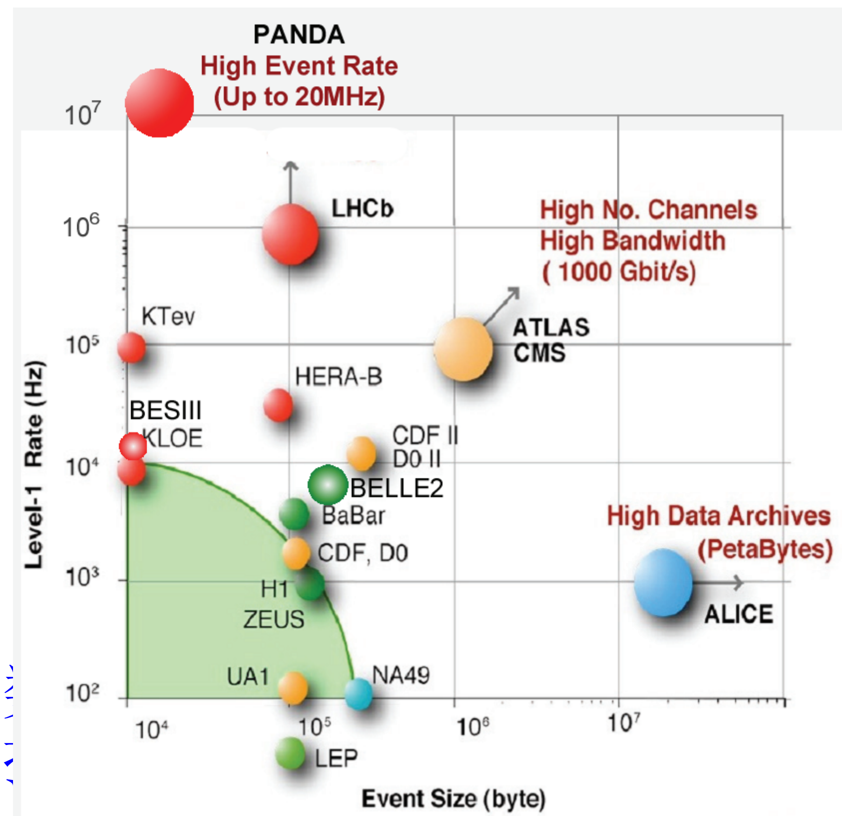
小结

- 简单介绍了触发系统的基本概念
- 以BESI/II/III实验为例介绍触发原理
- 简介了TDAQ未来的发展趋势

Backups

范例：PANDA实验对TDAQ系统

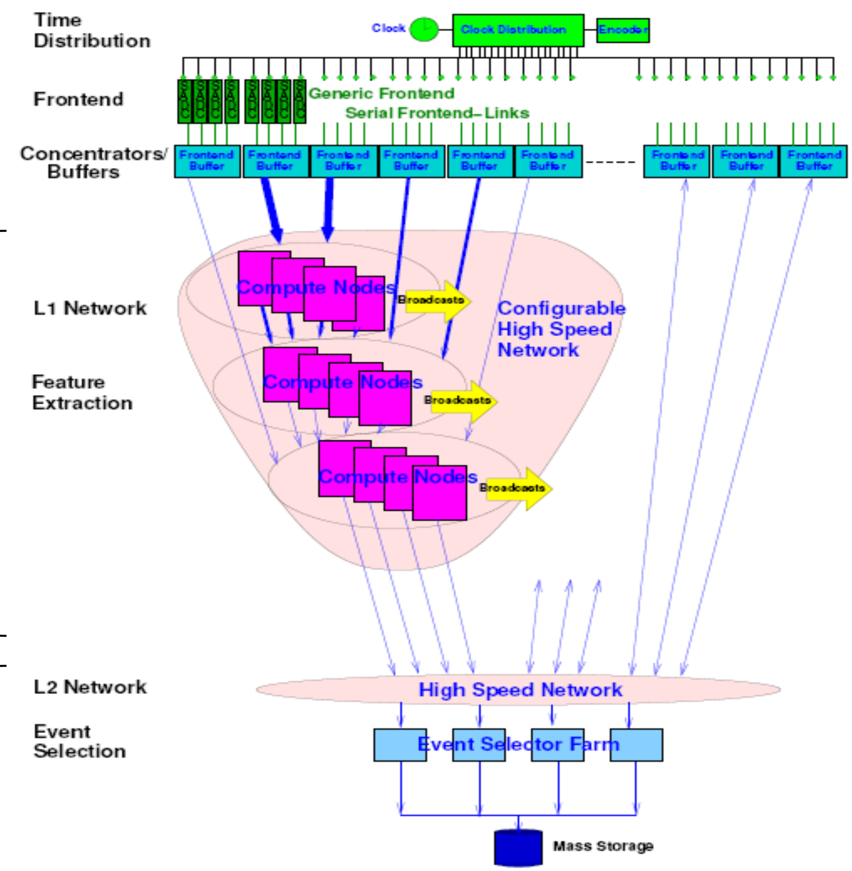
- 要求
  - 预计打靶所产生反应事例率在20MHz（预留50MHz的处理能力)，通过前端电子学进行初步的噪声压低及数据筛选，事例大小在4kB到8kB（处决于最终探测器的选择），TDAQ系统需要处理的数据通量达到200GB/s;



在线触发与 … 据传输、大数据量缓
存及快速数 …

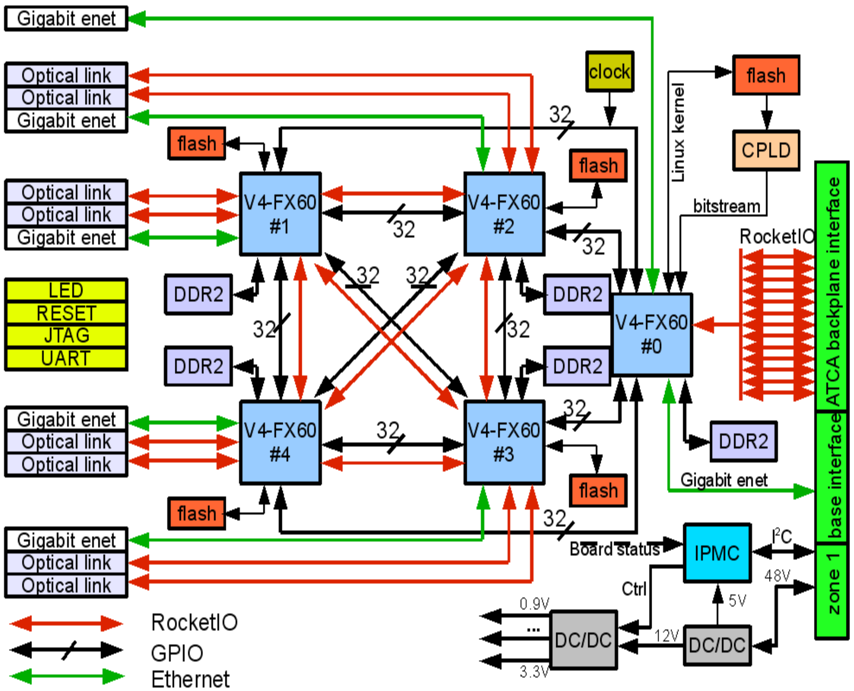
PANDA触发与数据获取系统体系结构

采用**自触发前端电子学及数据推动**的结构(**Self-triggered Data Push Architecture**)，没有独立的触发数据通路，采用打**全局时间戳**的办法来对齐事例，同时解除了对触发**Latency**的限制.



- L1:特征提取：来自前端的数据被打上精确的时间戳(Timestamp)后送入公共数据缓冲区；若干高性能的计算节点（Compute Node）通过高速串行传输技术组成可重配置的高速互联网络，采用多种特征提取手段挑选出感兴趣的物理信息；
- L2:事例重建与筛选：L1提取的物理信息在L2进行基本事例重建，通过事例筛选来压缩数据量，经过L2的数据最后存储进海量存储设备供离线数据分析；

通用硬件平台—计算节点（高能所设计）



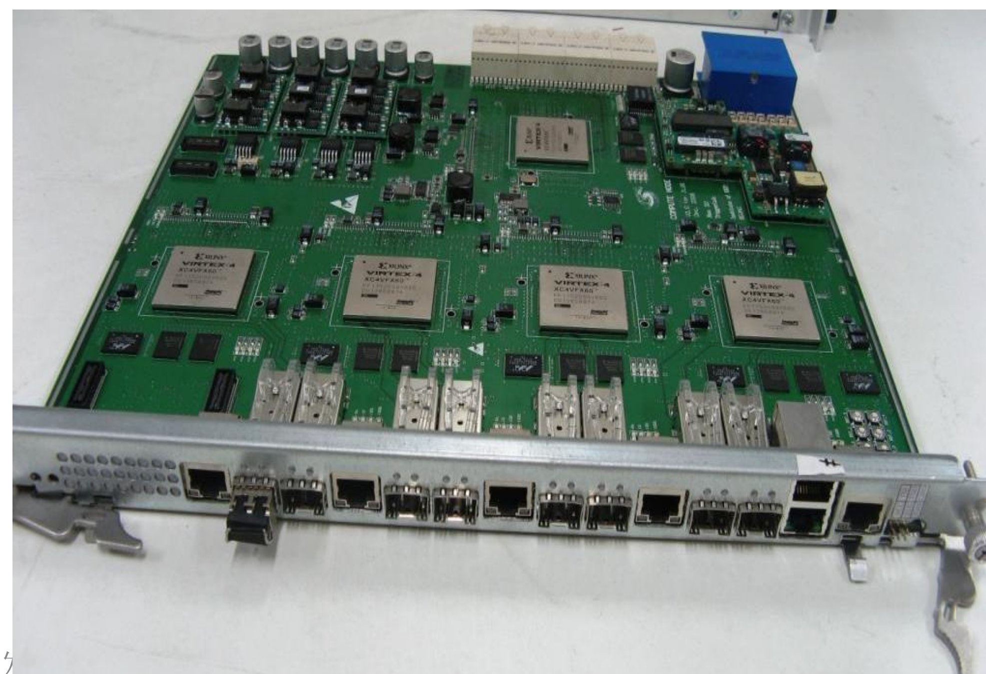
它是构成**PANDA TDAQ**系统的核心模块，具有以下特点：

大容量数据处理能力

- 5x (Virtex4 FX 60 FPGA + 2GB DDR2)

高数据传输带宽

- 6 个千兆网口(包括背板的)
- 8 个光纤口(到3.125Gbps)
- 13个RocketIOs通过背板与同机箱内的其他板进行点对点的互联



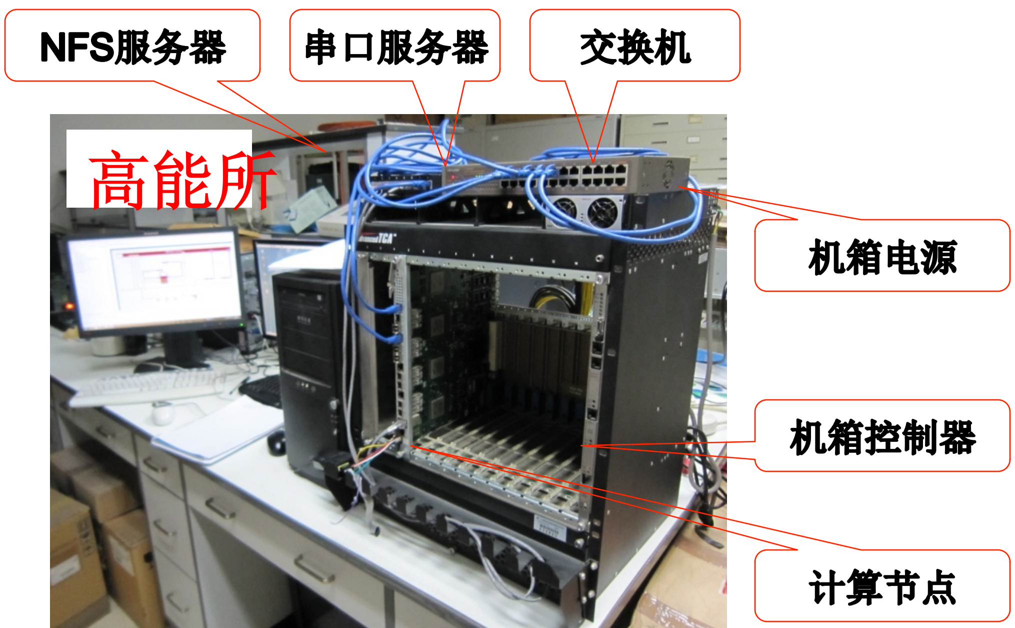
嵌入式设计方式

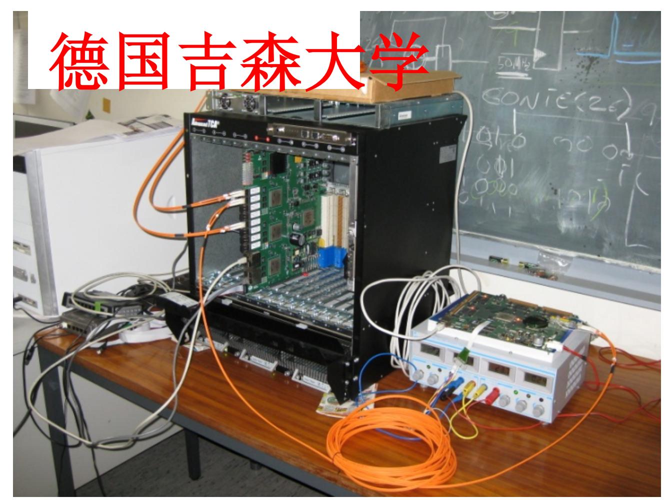
- 通用的系统+专用的数据处理模块

智能平台管理

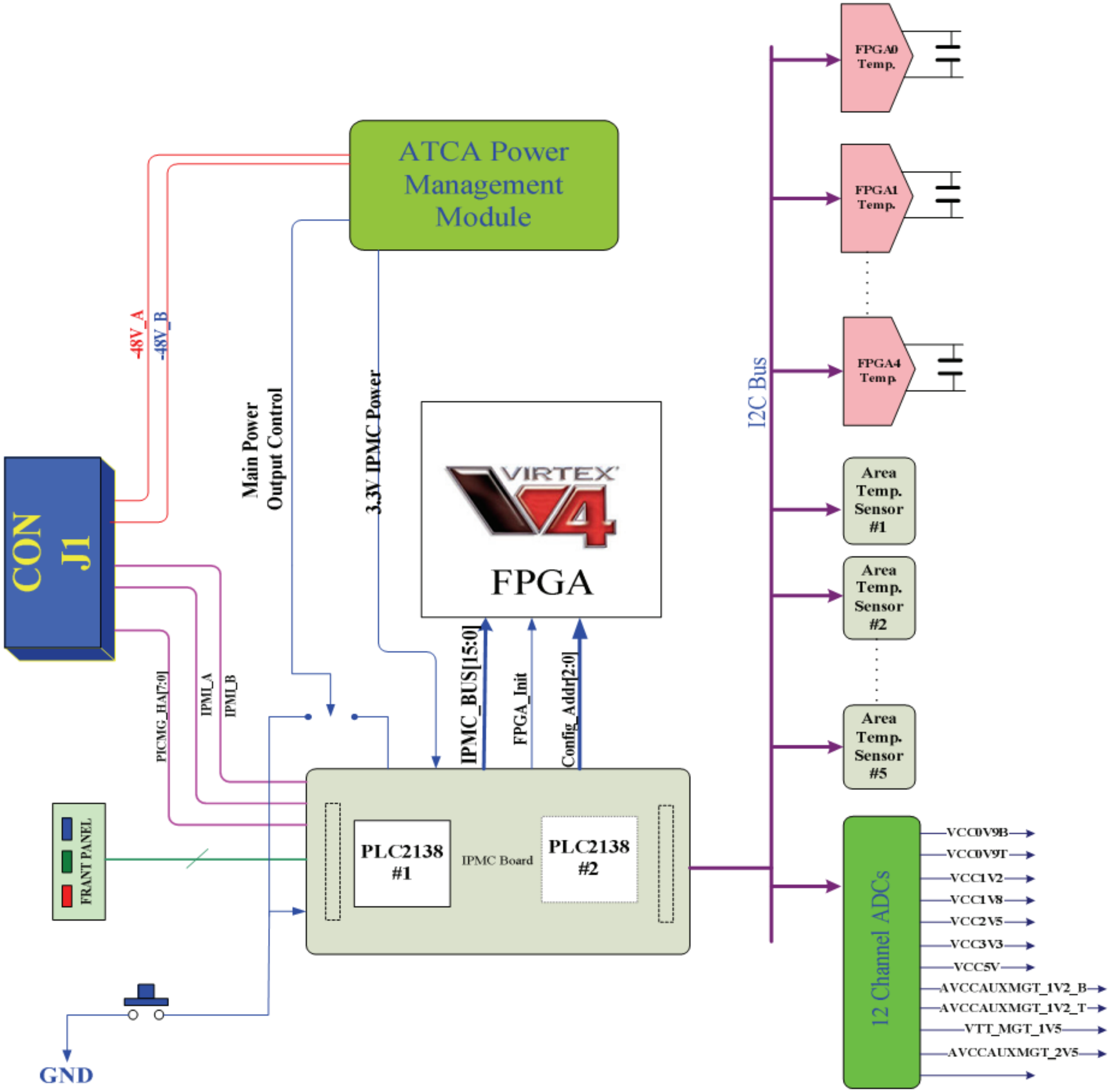
- 基于板上IPMC子板与机箱控制器的通信来实现系统监测及管理功能

通用高性能硬件平台



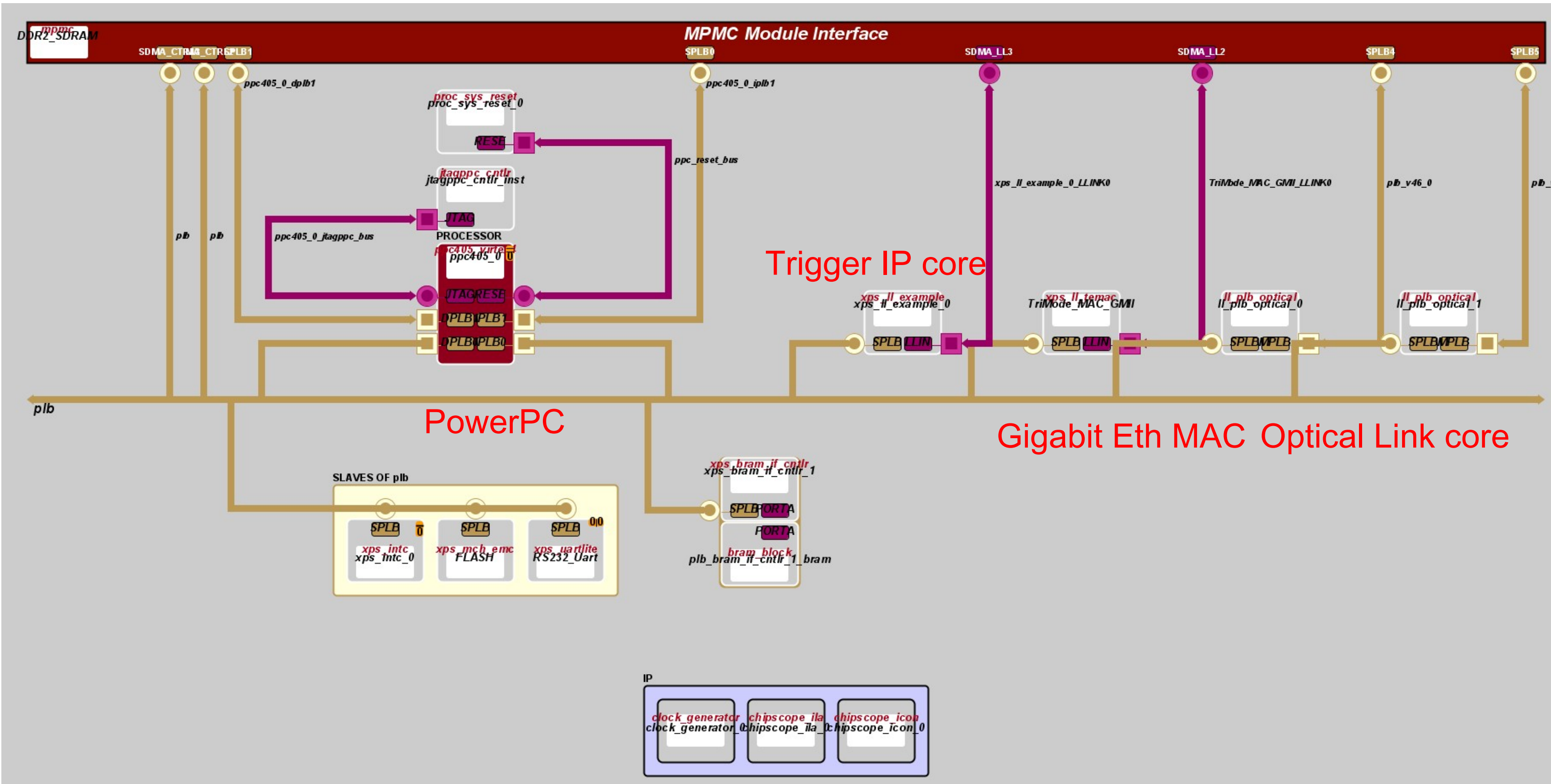


通用硬件平台—计算节点



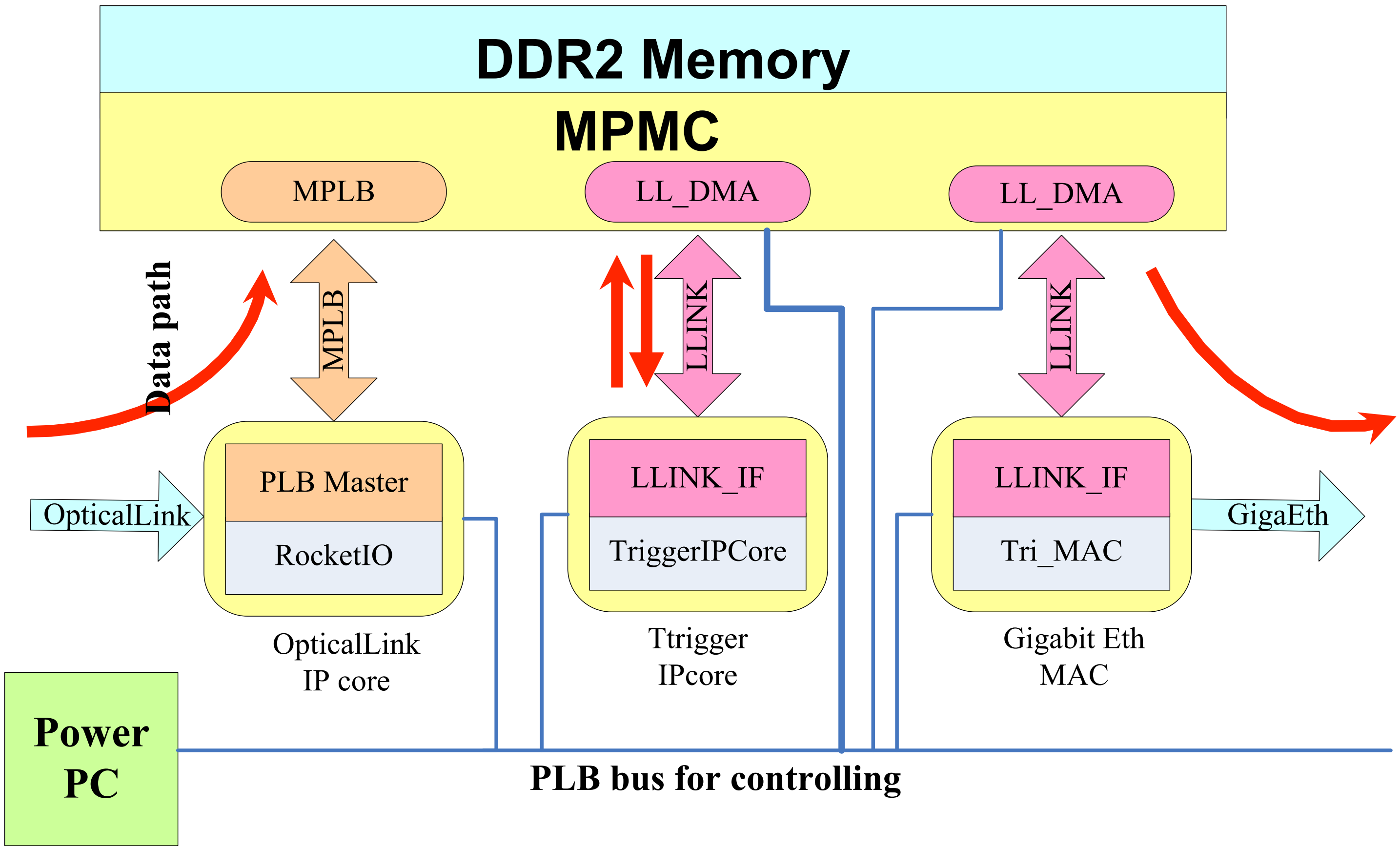
- 板级监测
- 控制管理

System on Programmable Chip



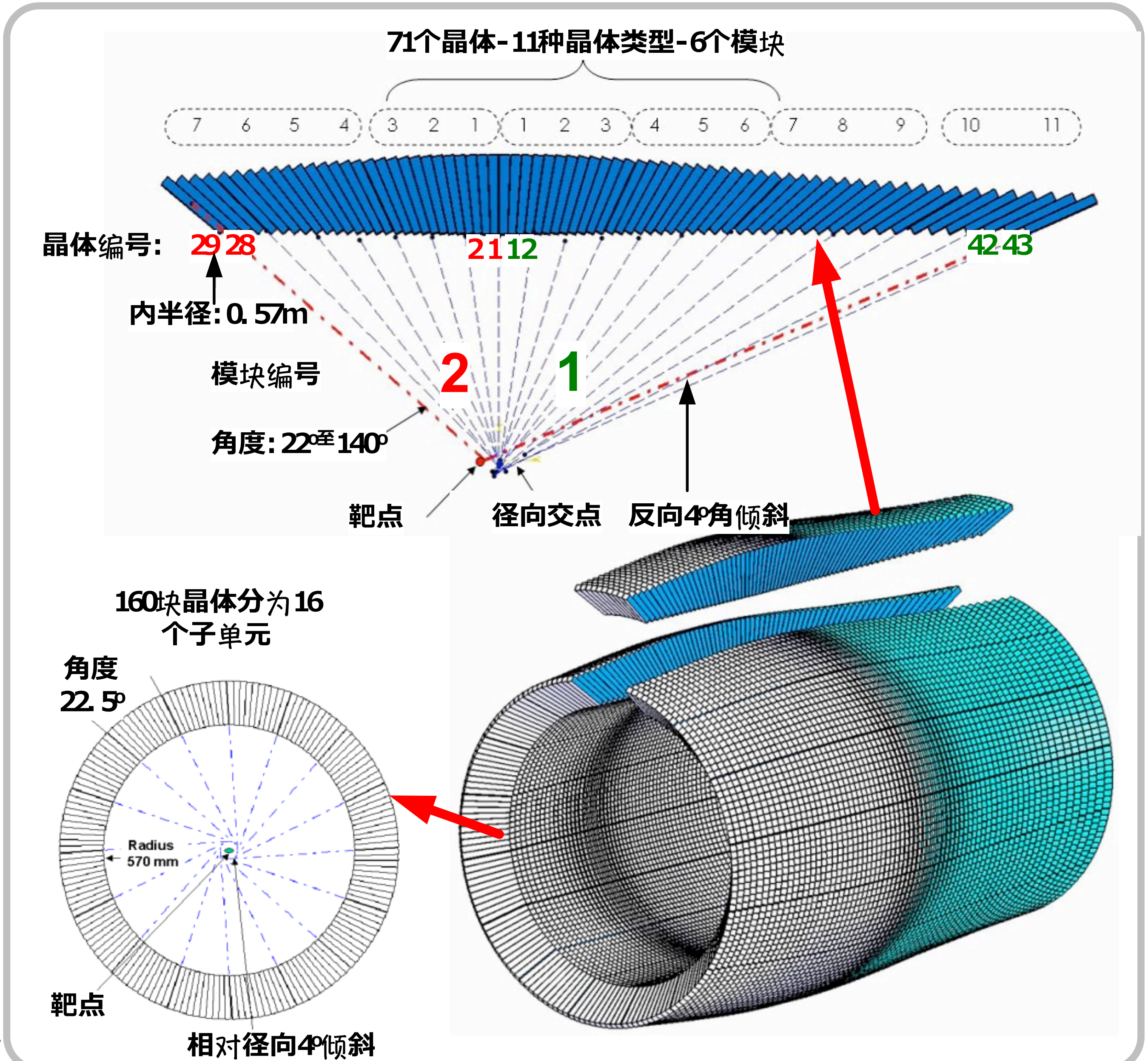
- 基于Xilinx FPGA内嵌的PowerPC硬核和一些开源的IP和构建一个通用的硬件系统,移植开源Linux来实现系统管理以及UDP/TCP 协议栈的处理
- 在线触发算法设计成专用IP核以及基于多端口内存控制器实现片上数据交换模块

数据流的问题



- 从高速光口接收到的粗数据在DDR2内缓存（通过PLB主设备：低延时，高带宽）
- 数据从DDR2发送到触发算法IP核以及处理结果写回DDR2（通过LocalLink DMA设备，更加灵活，高带宽）
- 结果通过Gigabit Ethernet送出（通过UDP/TCP，标准设计）

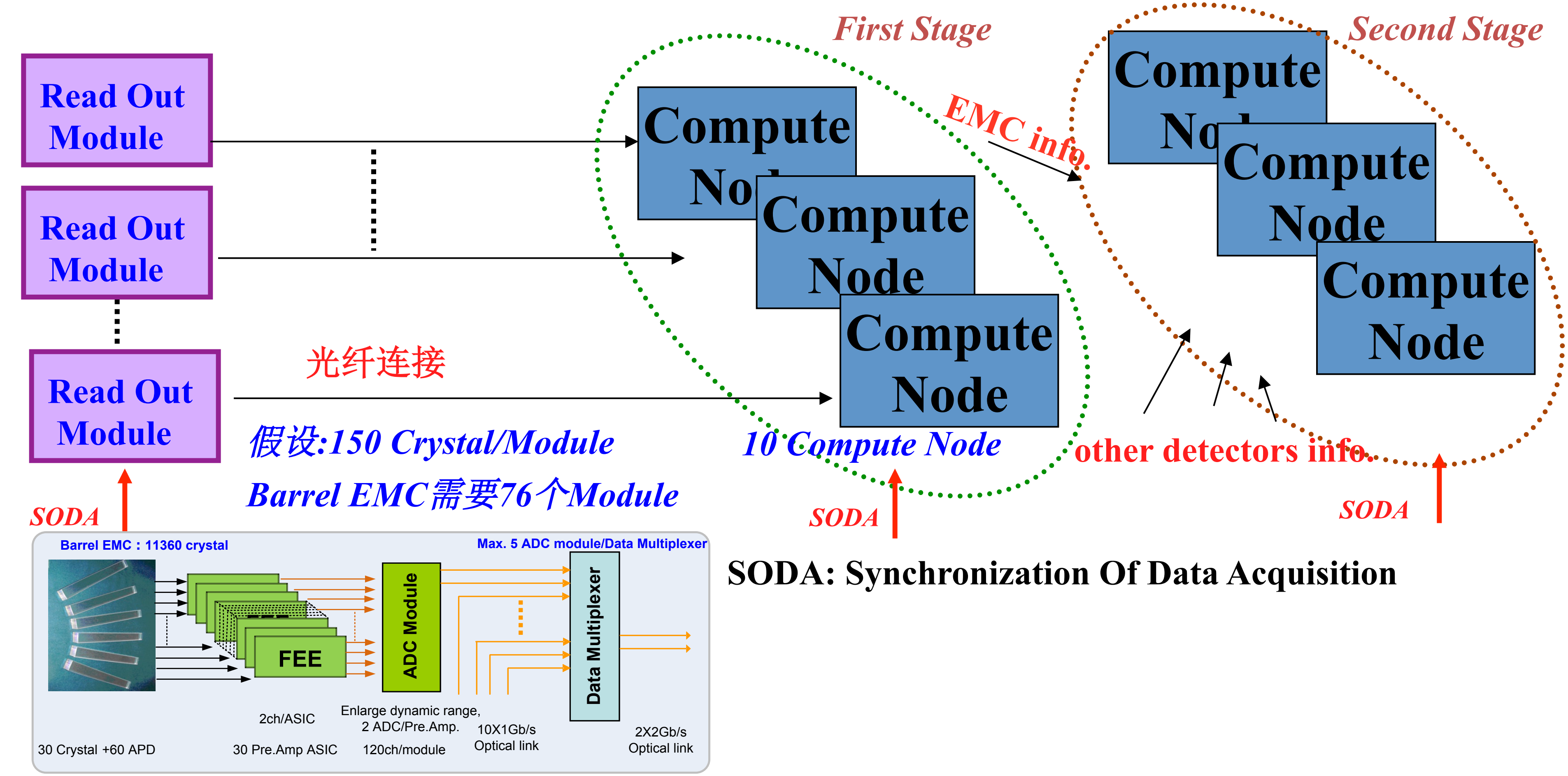
EMC探测器



Barrel EMC:

11360块晶体

EMC TDAQ系统框图



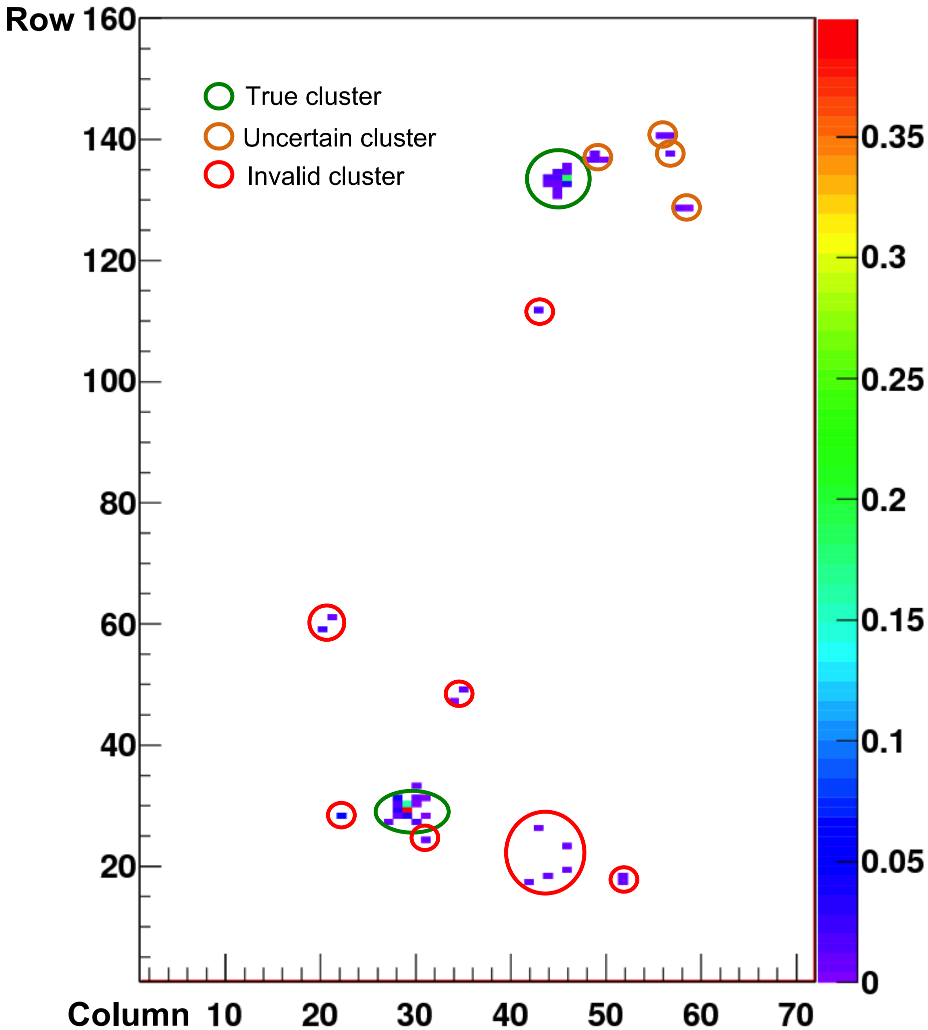
任务

1. Signal Feature extraction (Time, Amplitude)
2. Data Zero suppression

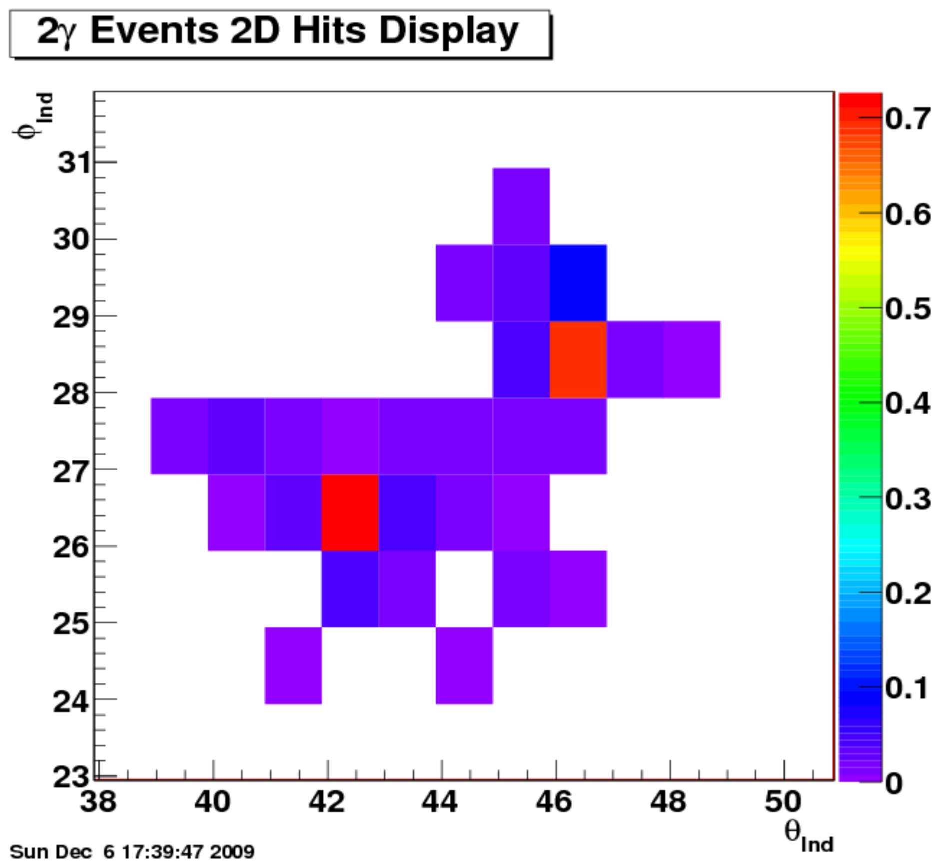
1. Clustering
2. Cluster Properties extraction
3. Pattern recognition

1. Correlation
2. Physical parameters calculation
3. Event building

簇团重建需要解决的问题



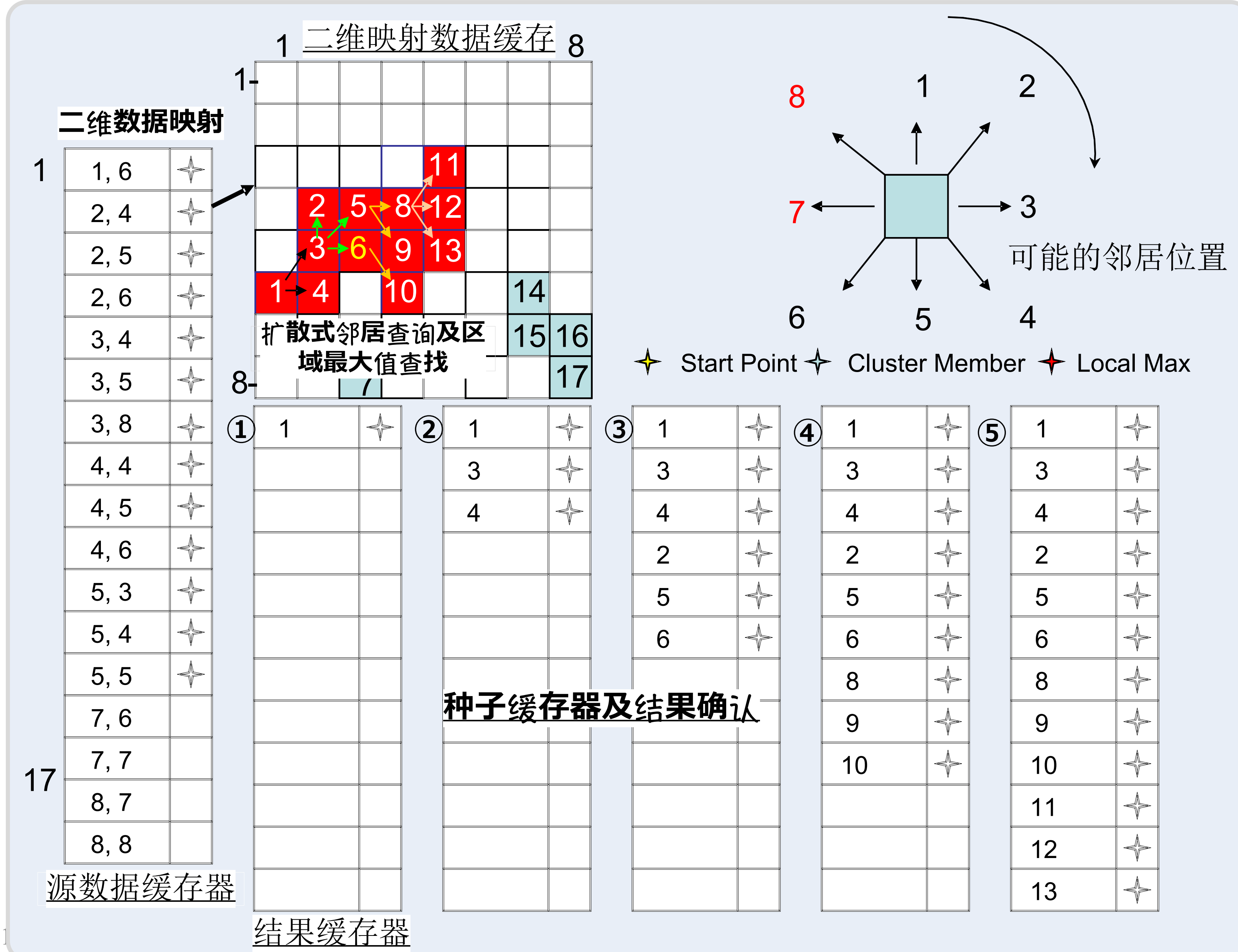
- 簇团查找



- 重叠簇团的处理
- 重建簇团信息:能量,位置

- 在线簇团重建：速度，效率

二维簇团查找算法


二维数据映射
二维映射数据缓存
1
8
1-
8-
11
2 5 8 12
3 6 9 13
1 4 10 14
15 16
17
扩散式邻居查询及区域最大值查找
1, 6
2, 4
2, 5
2, 6
3, 4
3, 5
3, 8
4, 4
4, 5
4, 6
5, 3
5, 4
5, 5
7, 6
7, 7
8, 7
8, 8
1
17
源数据缓存器
结果缓存器
种子缓存器及结果确认
①
②
③
④
⑤
1
3
4
2
5
6
8
9
10
11
12
13
可能的邻居位置
Start Point
Cluster Member
Local Max

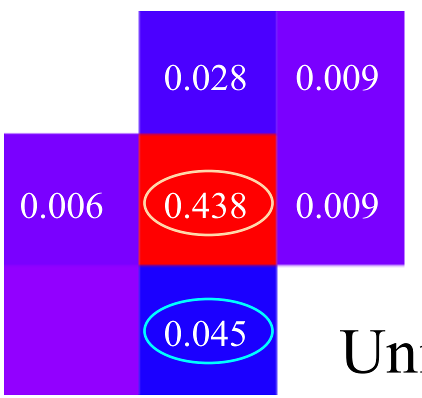
寻找区域最大值

为了避免找到假的区域最大值，需要选择更加严格的判选条件

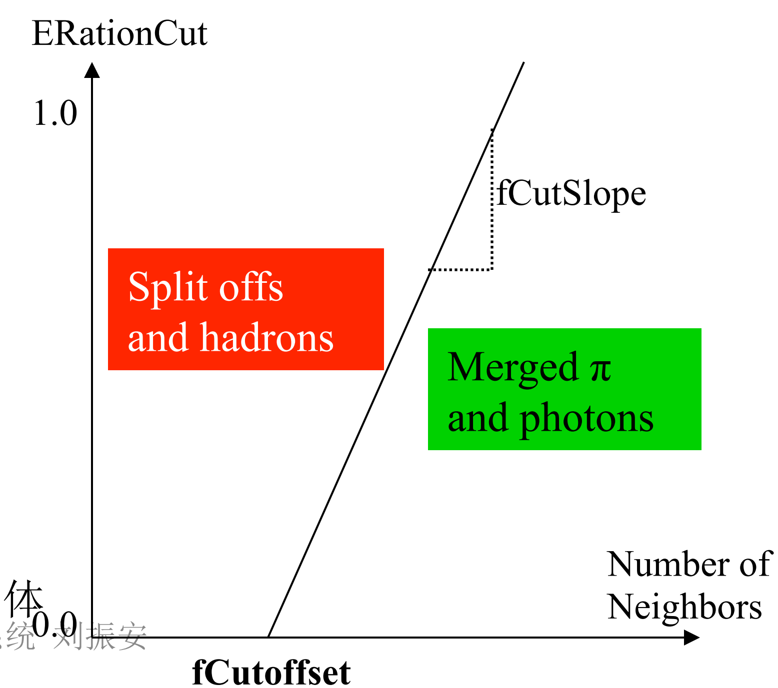
- ✓ Eseed>20MeV
- ✓ ERatio<ERatioCut

$$ERatio = \frac{MaxEofNeighbors - fERatioCorr}{MaxE - fERatioCorr}$$

$$ERatioCut = fCutSlope \times (NumberofNeighbors - fCutoffset)$$



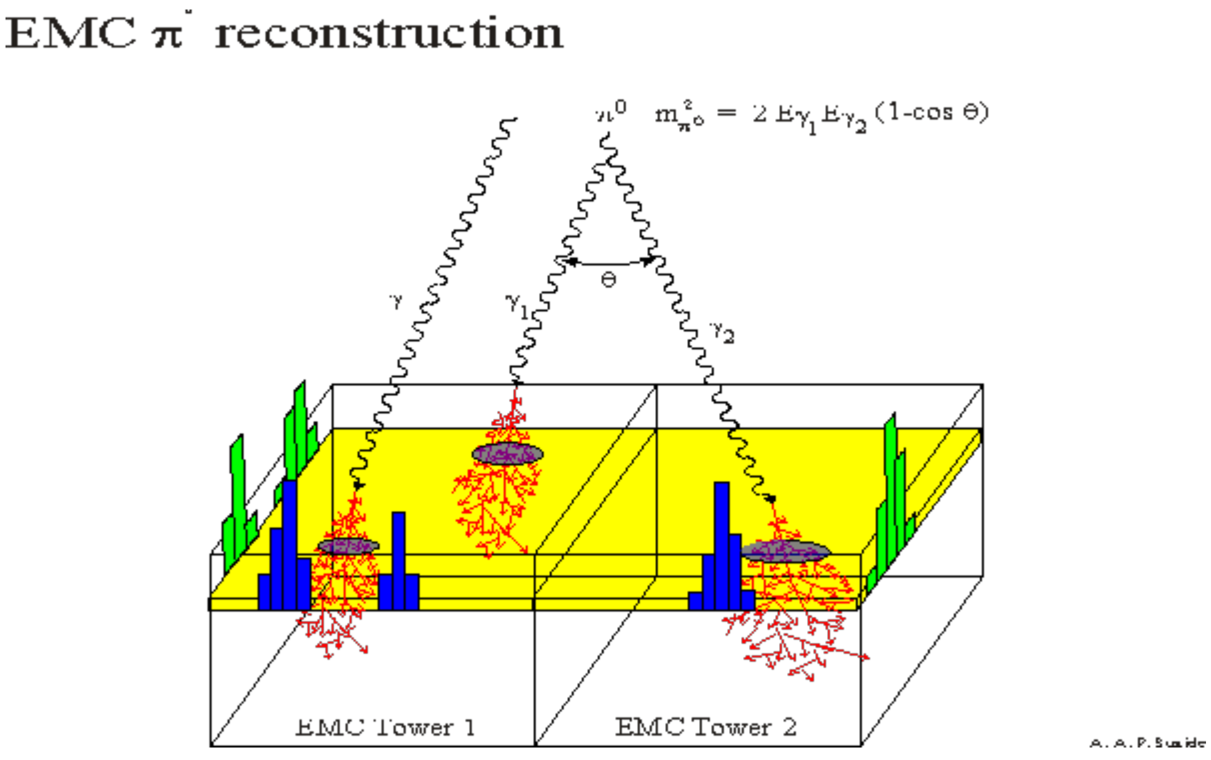
Unit: GeV



一个模拟的簇团有一个区域最大值以及6个相邻晶体

簇团位置计算

- 带电粒子必须提供簇团位置来与径迹探测器做匹配；
- 光子位置重建准确性对 π_0 质量的重建影响特别大；



$$Wi = Ei$$

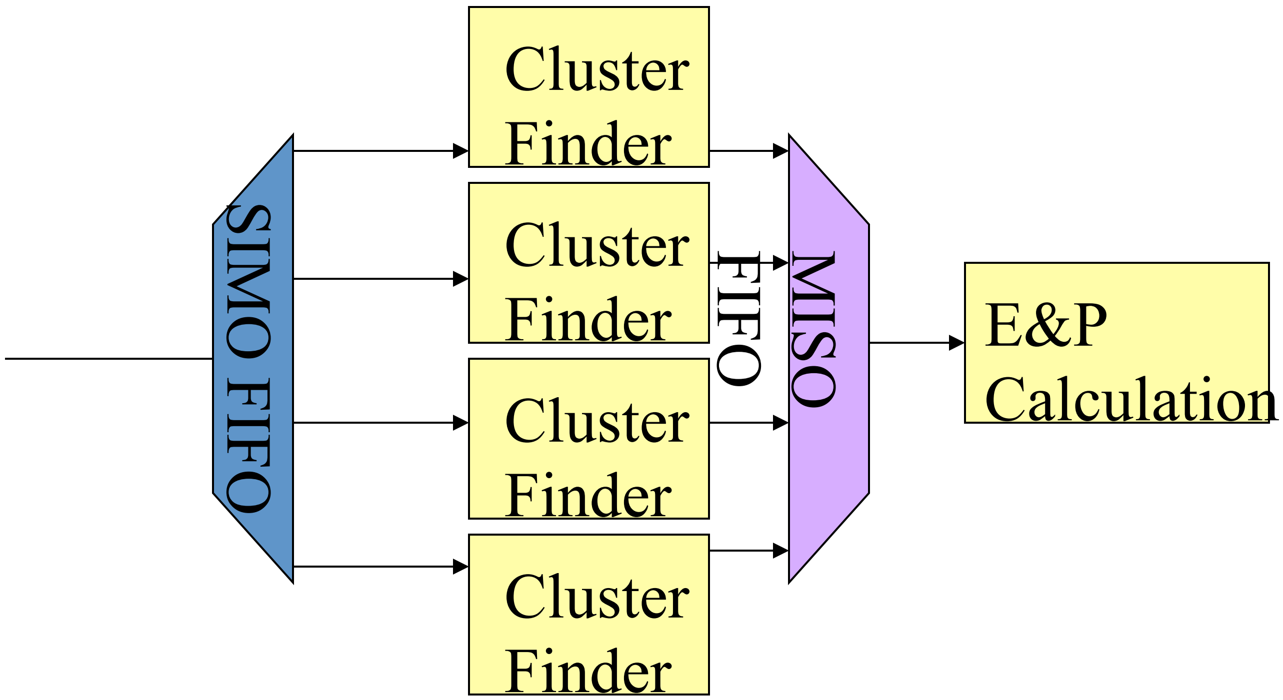
权重

$$Xcal = \frac{\sum_i Wi * Xi}{\sum_i Wi}$$

线性权重位置计算

适合V4Fx60 FPGA的设计

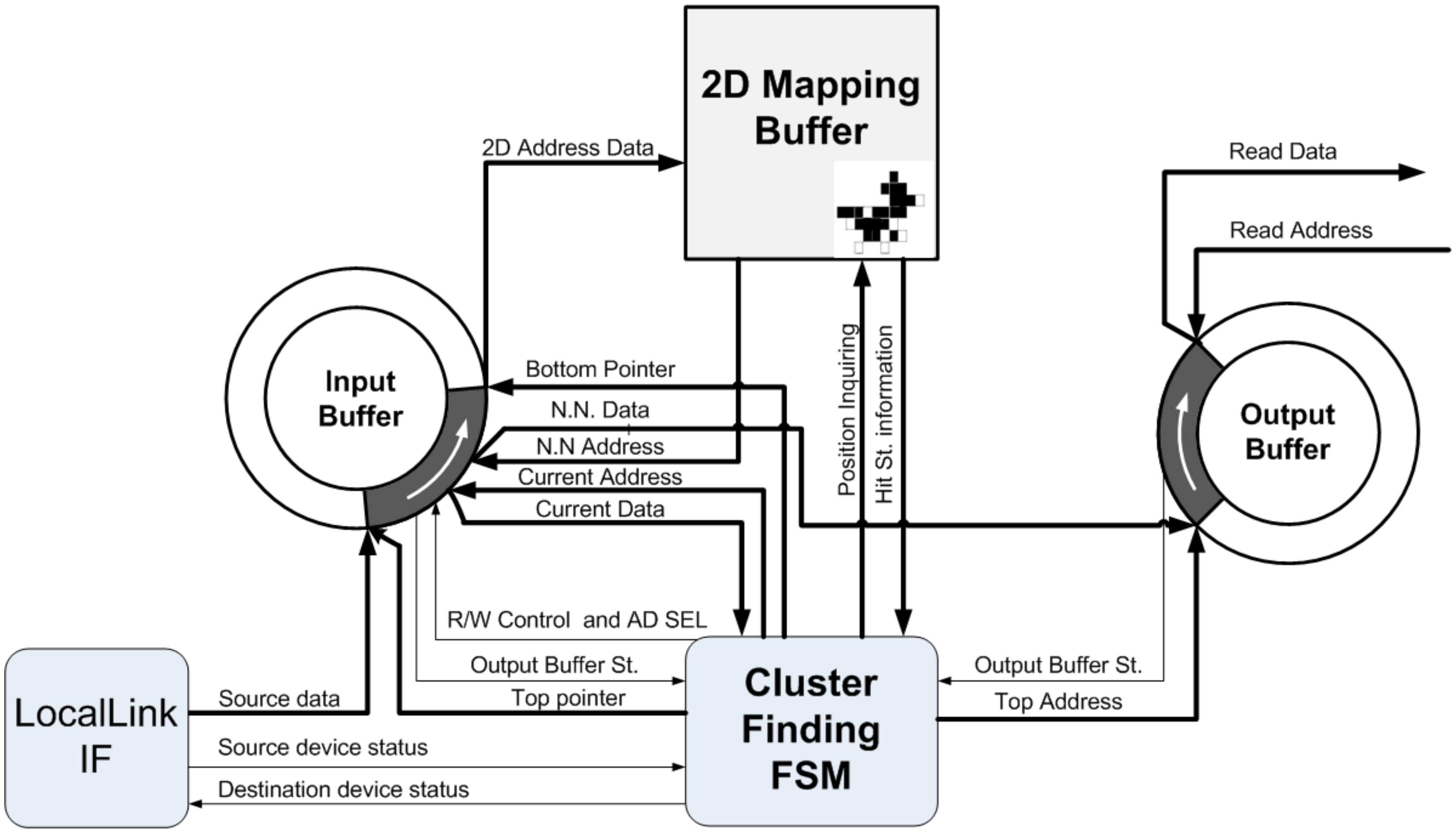
•能量/位置计算模块速度较快，能完全流水线运行
•从资源使用量上看，这是最优的配置



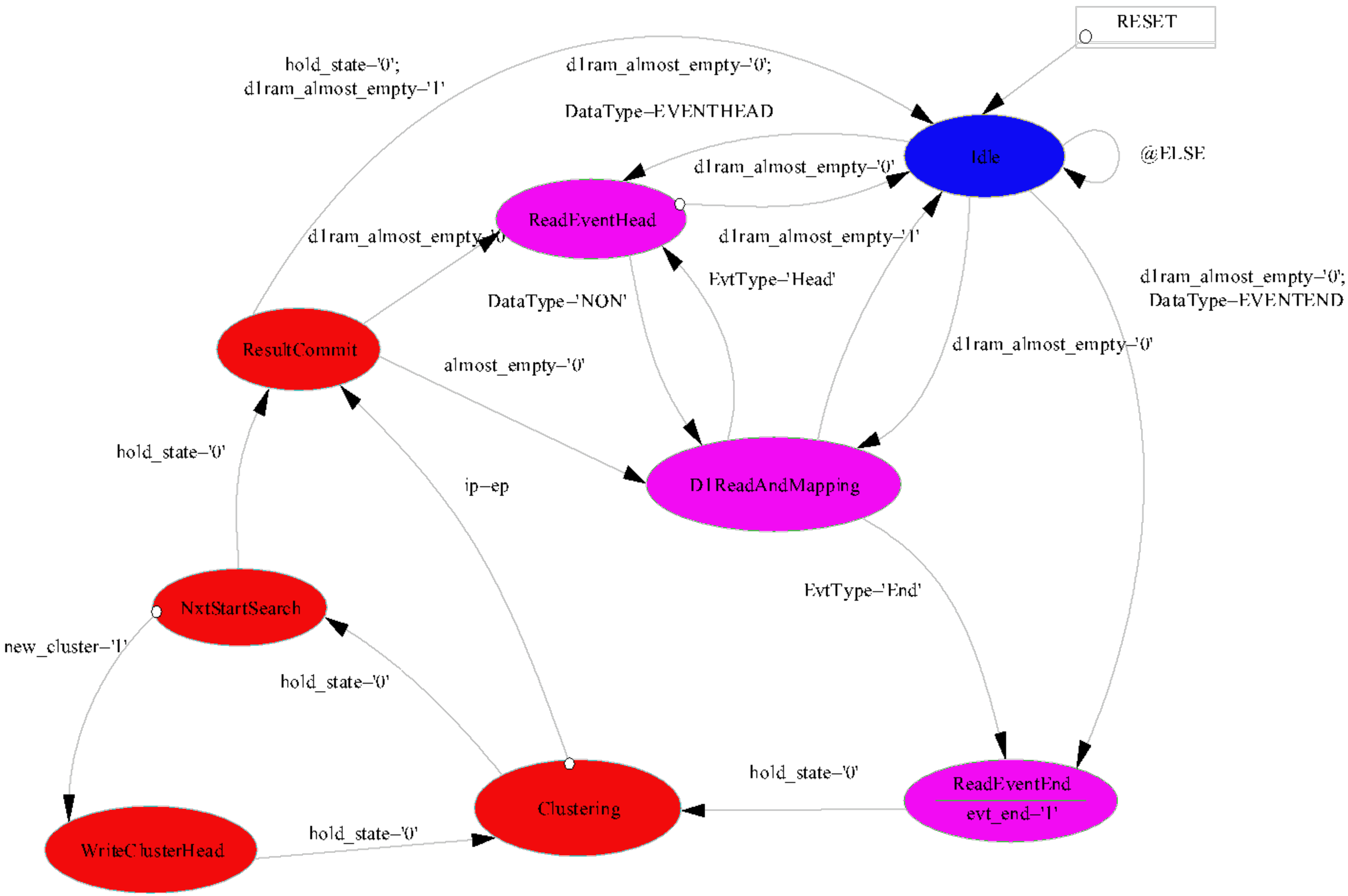
- 4 Cluster Finder + 1 Energy and Position Calculation

400KHz Events/FPGA=>1.6MHz/CN

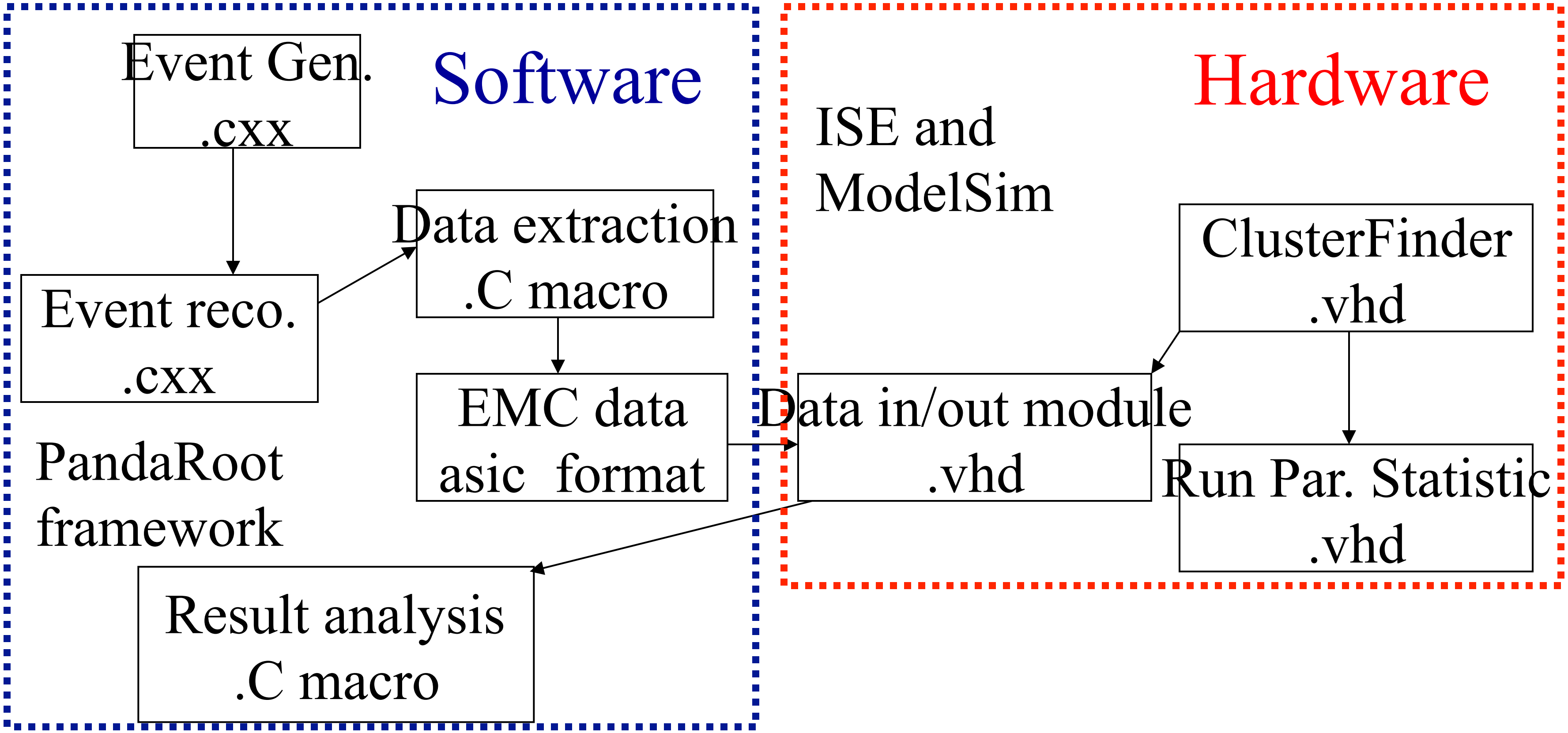
Cluster Finder 模块框图



簇团查找有限状态机

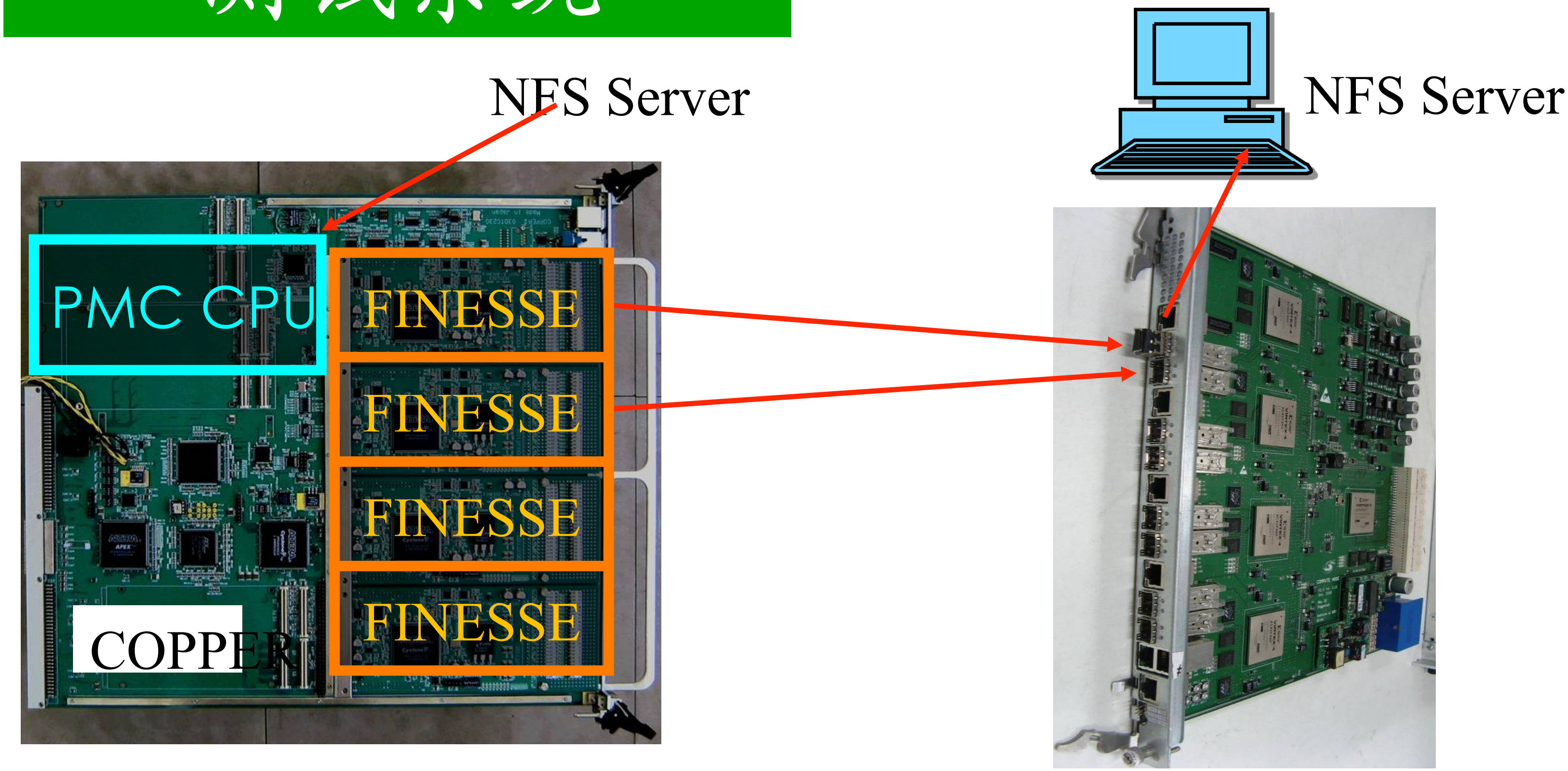

RESET
Idle
@ELSE
hold_state='0';
d1ram_almost_empty='1'
d1ram_almost_empty='0';
DataType=EVENTHEAD
d1ram_almost_empty='0'
ReadEventHead
d1ram_almost_empty='0'
d1ram_almost_empty='1'
EvtType='Head'
DataType='NON'
d1ram_almost_empty='0';
DataType=EVENTEND
d1ram_almost_empty='0'
ResultCommit
almost_empty='0'
D1ReadAndMapping
hold_state='0'
ip=ep
EvtType='End'
NxtStartSearch
new_cluster='1'
hold_state='0'
hold_state='0'
ReadEventEnd
evt_end='1'
Clustering
WriteClusterHead
hold_state='0'

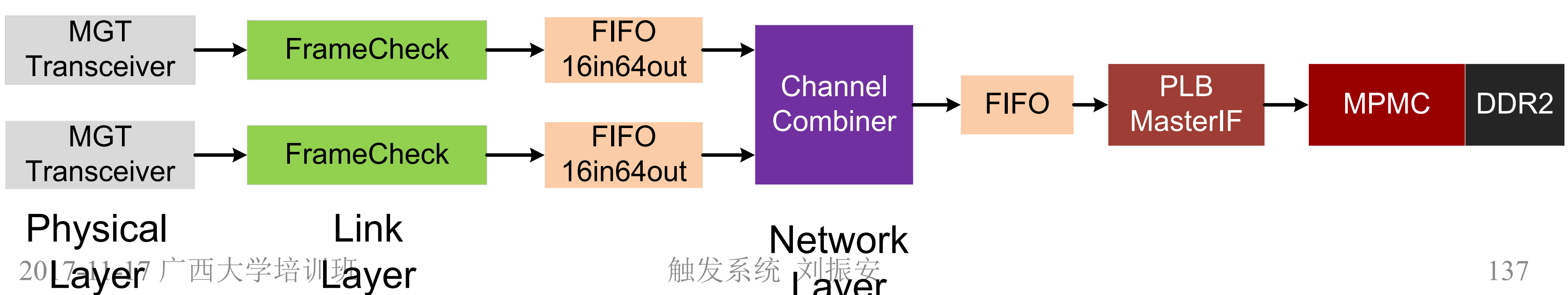
逻辑验证方法



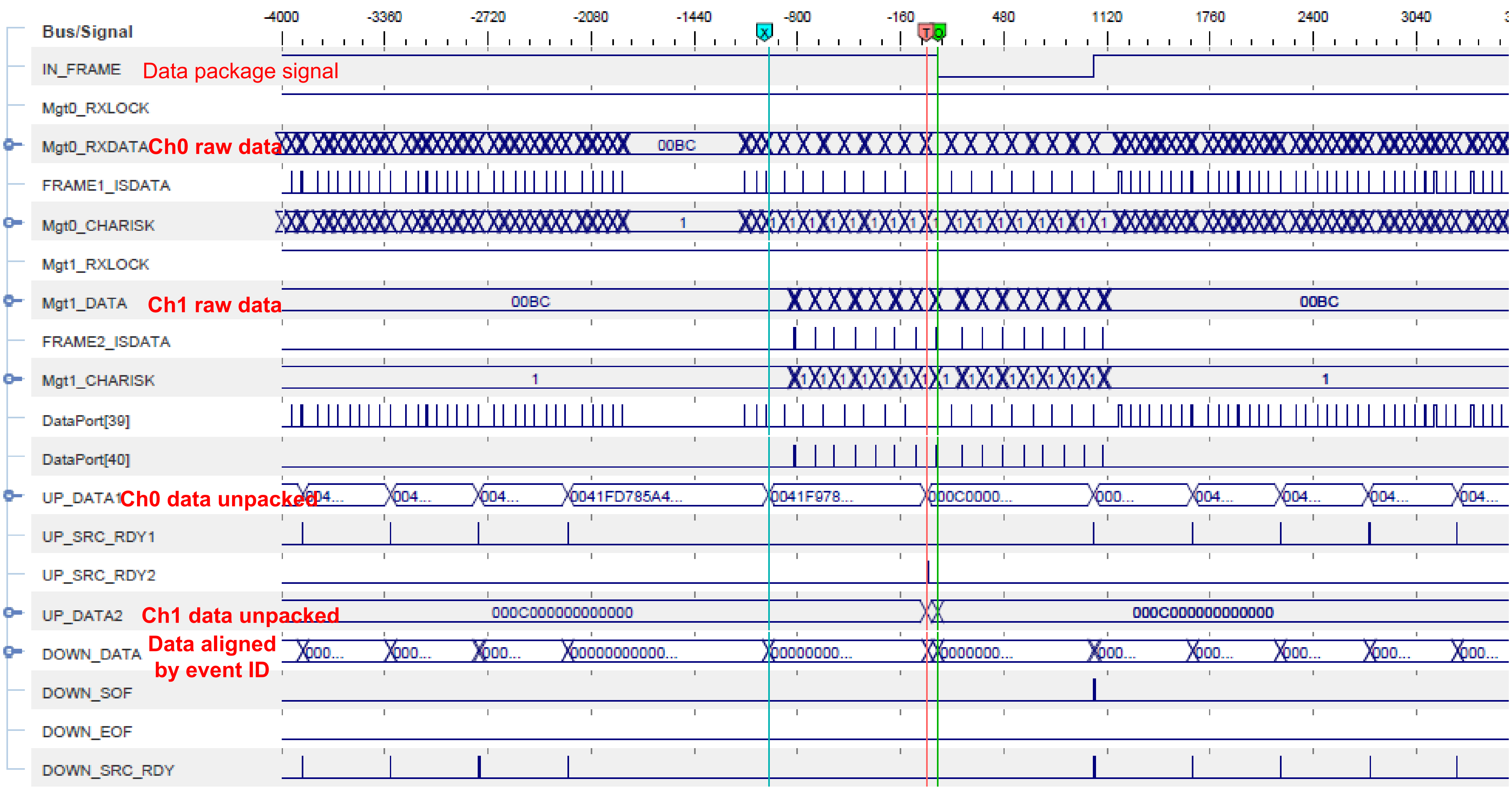
Software
Hardware
Event Gen.
.cxx
Event reco.
.cxx
Data extraction
.C macro
EMC data
asic format
PandaRoot
framework
Result analysis
.C macro
ISE and
ModelSim
ClusterFinder
.vhd
Data in/out module
.vhd
Run Par. Statistic
.vhd

测试系统


NFS Server
NFS Server
PMC CPU
FINESSE
FINESSE
FINESSE
FINESSE
COPPER


MGT
Transceiver
MGT
Transceiver
FrameCheck
FrameCheck
FIFO
16in64out
FIFO
16in64out
Channel
Combiner
FIFO
PLB
MasterIF
MPMC
DDR2
Physical
Layer
Link
Layer
Network
Layer

Chipscope 截图



文件传输测试

```
##################################################
##                                              ##
##      Compute Node Ver2 Application Programs  ##
##  OpticalLink Received Data Through DDR2 Memory ##
##                                              ##
##################################################
-- Entering main() --
XIntc init successful
XIntc start successful
intr controller enabled
ll_plb_optical intr enabled in the intr controller
Reg0 is: 2000000 Reg1 is: 4000000

The 0 th Daq Run
Data transmission finished
CLK cycles needed for 1024 KByte Data Transmission: 1300889748 Cyc, Transmit Speed: 236 KByte/s
Received Data Checking .......
|A:2000000|D:00000000||A:2000004|D:00000000||A:2000008|D:00080030||A:200000C|D:00000000||A:2000010|D:0041FD60||A:2000014|D:634FB3B0|
|A:2000018|D:0041F960||A:200001C|D:634FEDB0||A:2000020|D:0041FD68||A:2000024|D:604FCAD8||A:2000028|D:0041F968||A:200002C|D:607FE370|
|A:2000030|D:0041F568||A:2000034|D:604DC400||A:2000038|D:0041F168||A:200003C|D:604DD0D8||A:2000040|D:00420170||A:2000044|D:5D50D6D8|
|A:2000048|D:0041FD70||A:200004C|D:5D4FD2F0||A:2000050|D:0041F970||A:2000054|D:5D4FC0F0||A:2000058|D:0041F570||A:200005C|D:5D4DF400|
|A:2000060|D:0041FD78||A:2000064|D:5A4FDD28||A:2000068|D:0041F978||A:200006C|D:5A4FCCA0||A:2000070|D:000C0000||A:2000074|D:00000000|
|A:2000078|D:0008043C||A:200007C|D:00000000||A:2000080|D:0041D8F0||A:2000084|D:9546CCA0||A:2000088|D:0041D8F8||A:200008C|D:9146EFC8|
|A:2000090|D:0041D4F8||A:2000094|D:9145D2F0||A:2000098|D:0041E100||A:200009C|D:8D48CCA0||A:20000A0|D:0041D900||A:20000A4|D:8D47C050|
|A:20000A8|D:0041D500||A:20000AC|D:8D47CEC0||A:20000B0|D:0041D100||A:20000B4|D:8D45E9C8||A:20000B8|D:0041CD00||A:20000BC|D:8D43CCA0|
|A:20000C0|D:0041E108||A:20000C4|D:8948CCA0||A:20000C8|D:0041DD08||A:20000CC|D:8947E378||A:20000D0|D:0041D908||A:20000D4|D:895FE150|
|A:20000D8|D:0041D508||A:20000DC|D:896FFBF8||A:20000E0|D:0041D910||A:20000E4|D:8646FA00||A:20000E8|D:0041D510||A:20000EC|D:8645D6D8|
|A:20000F0|D:00202010||A:20000F4|D:F4788CA0||A:20000F8|D:000C0000||A:20000FC|D:00000000||A:2000100|D:00080838||A:2000104|D:00000000|
|A:2000108|D:0041E0F0||A:200010C|D:954ADD78||A:2000110|D:0041DCF0||A:2000114|D:956FEEB8||A:2000118|D:0041D8F0||A:200011C|D:9546E8A0|
|A:2000120|D:0041E4F0||A:2000124|D:9549C050||A:2000128|D:0041E0F8||A:200012C|D:9148EFC8||A:2000130|D:0041DCF8||A:2000134|D:9147C488|
|A:2000138|D:0041D8F8||A:200013C|D:9147D730||A:2000140|D:0041D4F8||A:2000144|D:9145FDE8||A:2000148|D:0041F4F8||A:200014C|D:914DCCA0|
|A:2000150|D:0041E100||A:2000154|D:8D48EFC8||A:2000158|D:0041E0E8||A:200015C|D:9948EFC8||A:2000160|D:0041DCE8||A:2000164|D:9957DDA0|
|A:2000168|D:0041E0E0||A:200016C|D:9D48D6D8||A:2000170|D:0041DCE0||A:2000174|D:9D47D6D8||A:2000178|D:000C0000||A:200017C|D:00000000|
|A:2000180|D:00080C34||A:2000184|D:00000000||A:2000188|D:004154D0||A:200018C|D:A426AFC8||A:2000190|D:004150C8||A:2000194|D:A827E160|
|A:2000198|D:00414CC8||A:200019C|D:A824FA00||A:20001A0|D:004154C0||A:20001A4|D:AC26FA00||A:20001A8|D:004150C0||A:20001AC|D:AC759458|
|A:20001B0|D:00414CC0||A:20001B4|D:AC2EBA18||A:20001B8|D:004148C0||A:20001BC|D:AC2386A0||A:20001C0|D:004154B8||A:20001C4|D:B027C748|
|A:20001C8|D:004150B8||A:20001CC|D:B025FCC0||A:20001D0|D:00414CB8||A:20001D4|D:B0269340||A:20001D8|D:004148B8||A:20001DC|D:B023D0D8|
|A:20001E0|D:004154B0||A:20001E4|D:B427E378||A:20001E8|D:004150A8||A:20001EC|D:B8258CA0||A:20001F0|D:000C0000||A:20001F4|D:00000000|
|A:20001F8|D:0008103C||A:20001FC|D:00000000||A:2000200|D:002044F0||A:2000204|D:9580F3B0||A:2000208|D:002040F0||A:200020C|D:957FDD28|
|A:2000210|D:00203CF0||A:2000214|D:957FC4D8||A:2000218|D:002048F8||A:200021C|D:9181E378||A:2000220|D:002044F8||A:2000224|D:9182FE38|
|A:2000228|D:002040F8||A:200022C|D:91FFE598||A:2000230|D:00203CF8||A:2000234|D:917FE378||A:2000238|D:002034F8||A:200023C|D:917CDAC0|
|A:2000240|D:00204900||A:2000244|D:8D81E760||A:2000248|D:00204500||A:200024C|D:8D80FA00||A:2000250|D:00204100||A:2000254|D:8D7FCAD8|
|A:2000258|D:00203D00||A:200025C|D:8D7ECB28||A:2000260|D:00203900||A:2000264|D:8D7DCCA0||A:2000268|D:00204508||A:200026C|D:8980CCA0|
|A:2000270|D:00204108||A:2000274|D:897FD6D8||A:2000278|D:000C0000||A:200027C|D:00000000||A:2000280|D:00081450||A:2000284|D:00000000|
|A:2000288|D:00427D18||A:200028C|D:826F8CA0||A:2000290|D:00427518||A:2000294|D:826D8CA0||A:2000298|D:00427920||A:200029C|D:7E6EAFC8|
|A:20002A0|D:00427528||A:20002A4|D:7B6DCCF0||A:20002A8|D:00427128||A:20002AC|D:7B6CD2F0||A:20002B0|D:00426D28||A:20002B4|D:7B6B5728|
|A:20002B8|D:00426928||A:20002BC|D:7B6AF3B0||A:20002C0|D:00427530||A:20002C4|D:776DFA00||A:20002C8|D:00427130||A:20002CC|D:777CA908|
|A:20002D0|D:00426D30||A:20002D4|D:776B4CA8||A:20002D8|D:00426530||A:20002DC|D:776BDDC8||A:20002E0|D:00427938||A:20002E4|D:746EAFC8|
```

Event head

Event data

Event end

Thanks