LHC实验研讨会
L1触发系统工作进展报告

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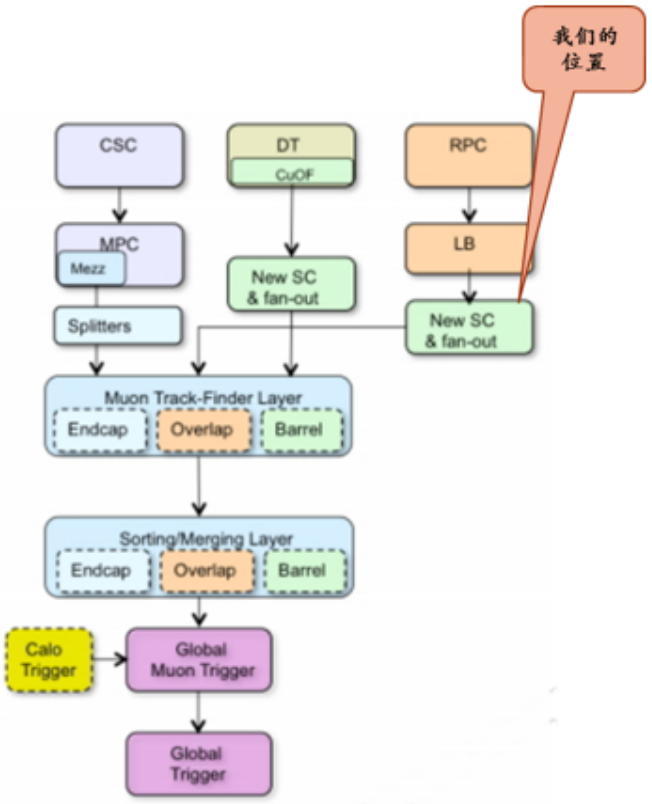
中科大，合肥

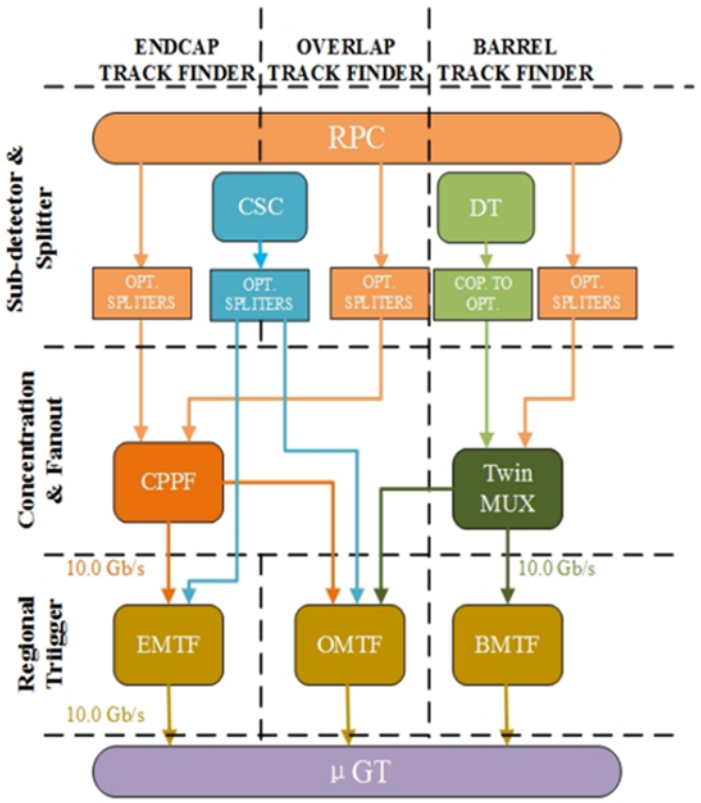
内容

- 2017年的任务
  - CPPF软件功能的优化
  - CPPF 控制软件SWATCH的开发
  - CPPF系统在 904楼的调试
  - CPPF在 Point 5的安装与调试
- 2017年的重大进展
  - CPPF 参与CMS宇宙线
  - CPPF系统正式参加 CMS运行取数
- 近期任务
  - 数据分析CPPF Unpacker的开发
  - 新型处理器的研制

高能所任务：μ子L1触发升级CPPF系统研建

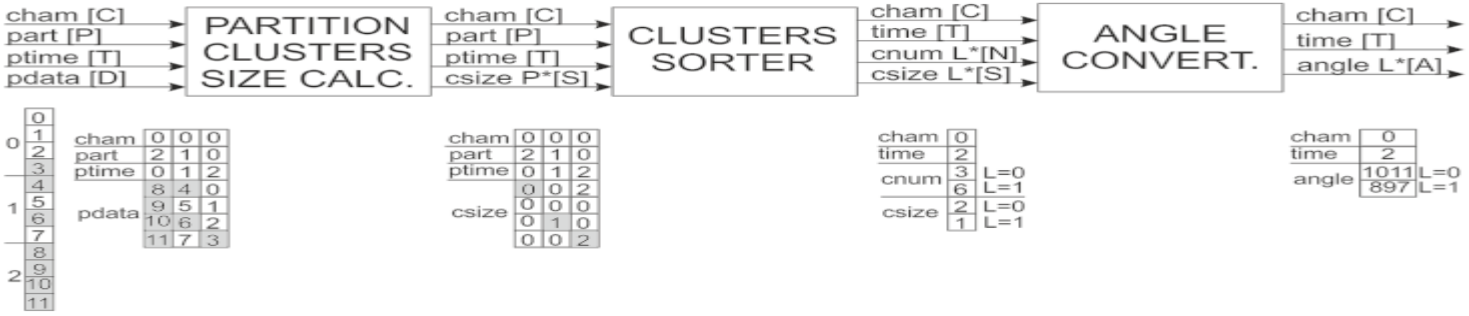


升级后的L1触发系统



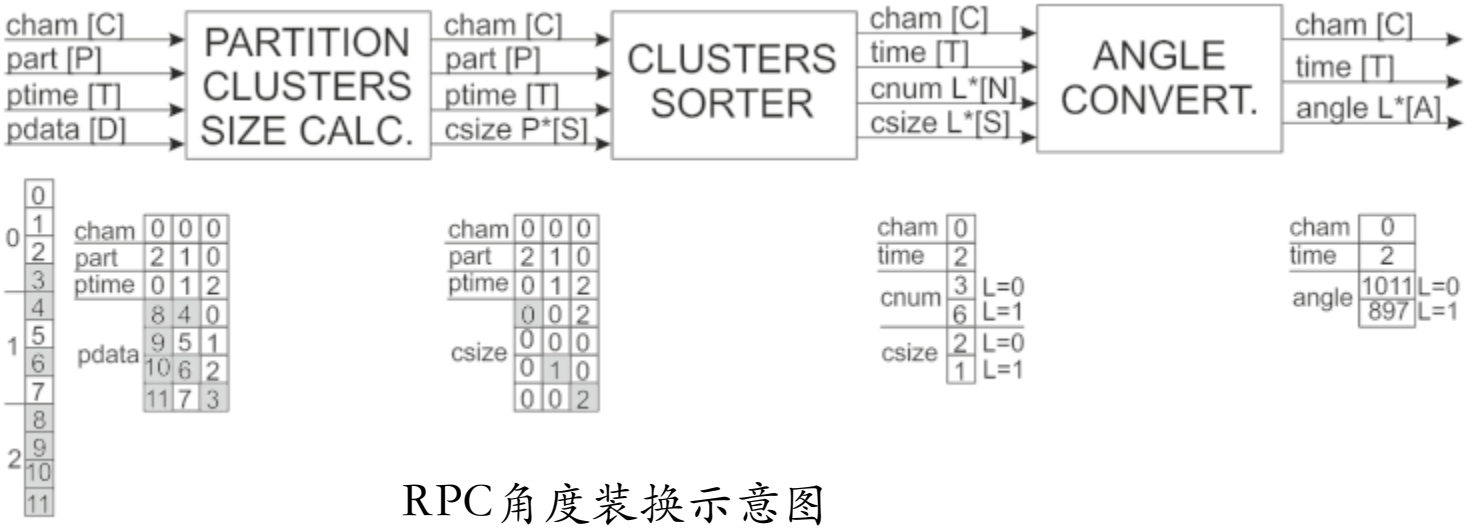
TwinMUX: concentration for Barrel DT and RPC

CPPF: Concentration, Pre-Process, Fan-out system for Endcap/ overlap RPC



CPPF软件功能的优化

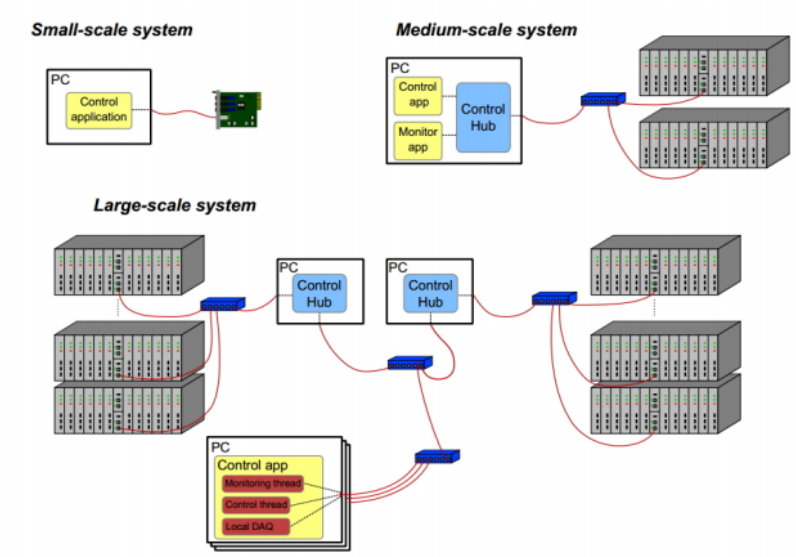
- 功能
  - RPC数据的解压缩
  - 找寻击中CLUSTER
  - 计算角度与转换
  - 1.6Gbps 转 10 Gb
  - 结果输出给径迹匹配



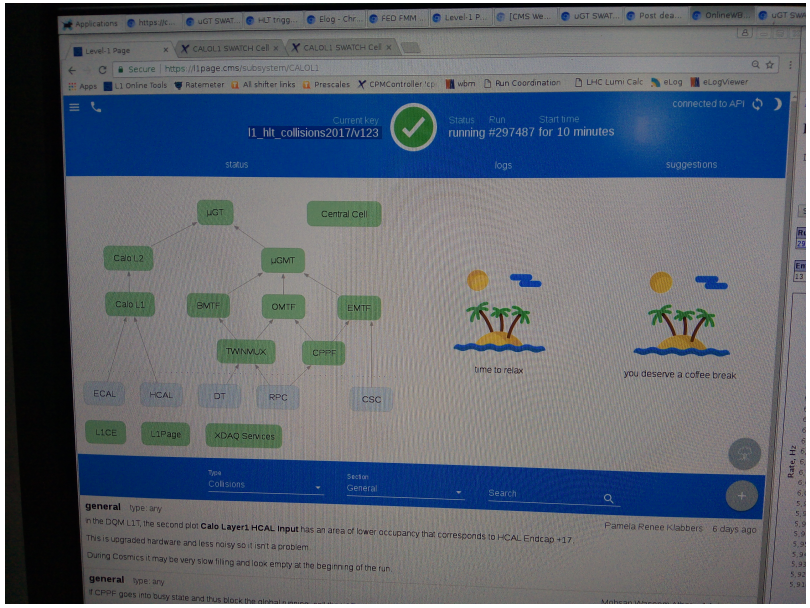
RPC角度装换示意图

CPPF 控制软件SWATCH的开发

- IPbus协议
  - 针对CMS实验，CERN开发的一款基于UDP的可靠以太网传输协议，实现对μTCA机箱的远程控制。
  - 基于IP访问硬件设备，采用A32/D32总线标准



基于Ipbus的μTCA机箱控制系统拓扑结构图



- 控制架构
  - μHAL：C++ Micro Hardware Access Library，提供访问FPGA固件中寄存器和RAM的接口
  - XML语言定义寄存器和RAM的地址
  - 采用Python脚本的方式控制CPPF插件
  - CPPF 融入CMS架构

```
<node description="ctrlFPGA" fwinfo="endpoint" class="ctrlFPGANode">
    <node id="ctrl_reg"    address="0x0" fwinfo="endpoint;width=1"/>
    <node id="ram"   address="0x10" size="1024" mode="block" fwinfo="endpoint;width=2"/>
```

CPPF系统在 904楼的调试

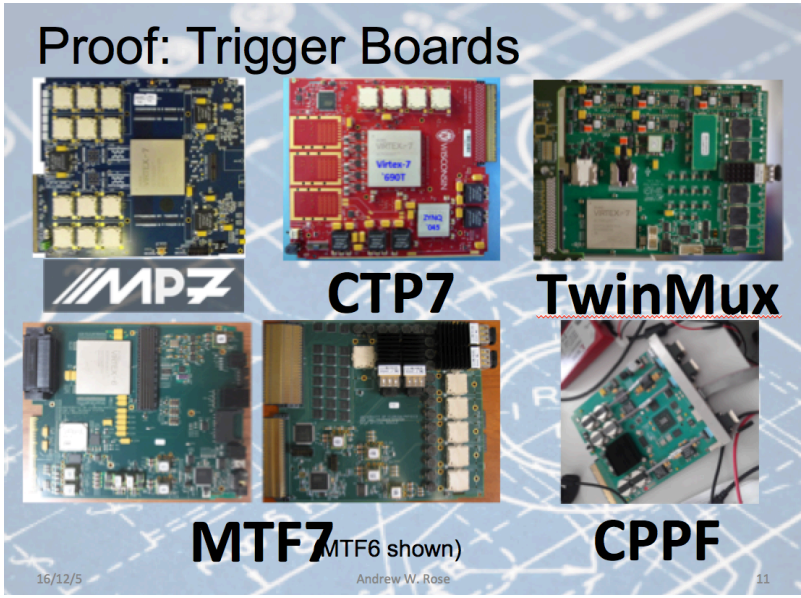
- 进入CMS系统集成前总体验证
  - 与探测器的联调
  - 数据解压缩验证
  - 多通道数据对其验证
  - 触发实现与数据浓缩
  - CPPF SWATCH控制功能验证
  - CPPF CMS SWATCH整体集成验证

CPPF在 Point 5的安装与调试

- 2017年3月16日
  - 完成了系统集成
  - 和联调测试
- 2017年4月30日
  - CPPF 加入CMS系统运行
  - 开始宇宙线取数实验
- 2017年6月20号
  - CMS合作组会中认可CPPF系统软硬件工作正常

2017年的重大进展及意义

- 中国组在LHC合作中可以发挥重要作用
  - MTCA设计是我们高能所的强项
    - CMS Phase I触发升级只有5种新插件，高能所独立承担了CPPF的设计
    - 提出设计思路，并命名CPPF系统，承担建造任务
    - CPPF满足MTCA新标准(高能所参与发起制定）
  - 敢于提出我们的方案
    - 系统初始设计为12块 CPPF插件后改进为8块CPPF插件
    - IO口部分使用，资源充足
- 体会
  - 时间紧任务重（2013年起只有3年多的时间）
  - 有辛苦（4个版本设计）
  - 被质疑（通过充实完备的实验方案与数据证明我们）
  - 有成功的喜悦，辛苦是值得的
  - 感谢高能所领导们对工作的无保留支持



升级最新进展

- Mu触发的数据验证
  - CPPF unpackor开发
  - CPPF emulator开发
  - 高能所的任务，但协调困难
  - 刚刚派程立波赴 CERN
- CMS 二期升级

Phase II升级最新

- 获邀做三次报告
  - 2016.12
  - 2017.3
  - 2017.4

ATCA System for Belle II –
Development of A General Purpose Compute Node for TDAQ system

Zhen-An Liu, IHEP, China
CMS Phase II L1 Trigger Workshop
CERN, Switzerland
Dec.6-7 2016

Progress Report on CMS Trigger Upgrade

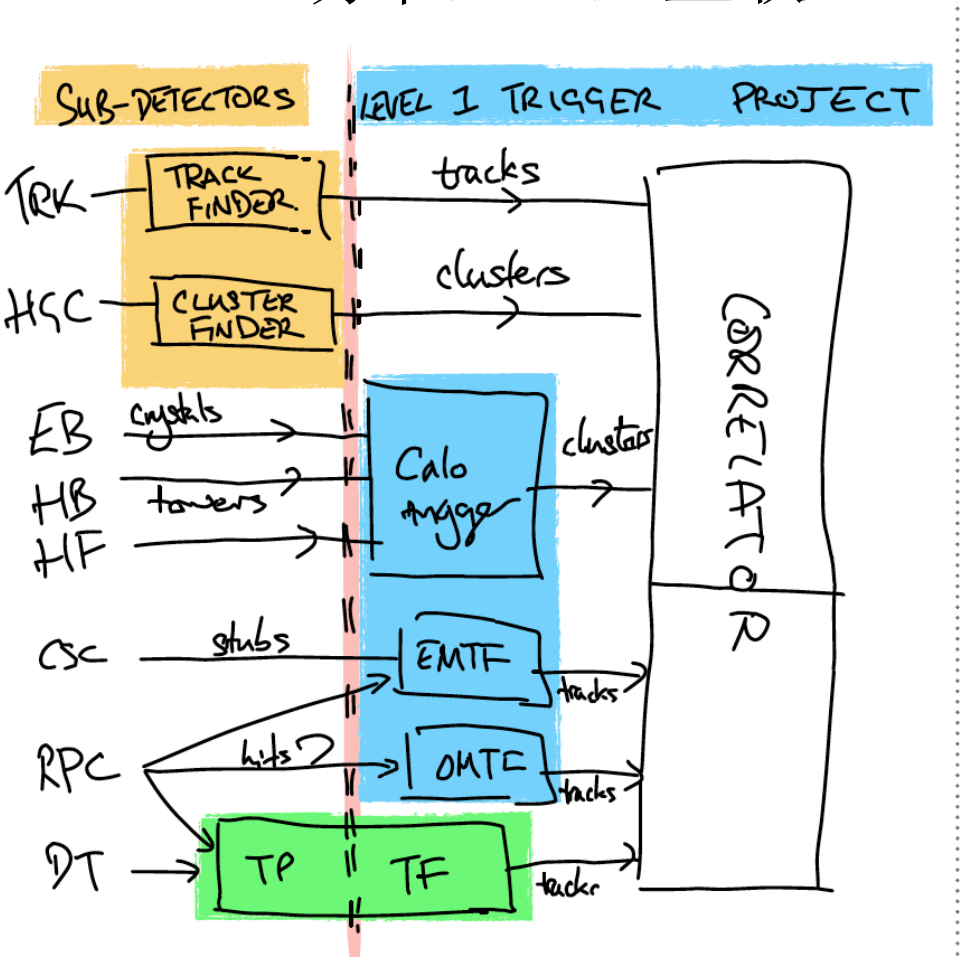
Zhen-An Liu, Jingzhou Zhao
LHC Phase II upgrade Vidyo Meeting
Mar. 2 2017

ATCA/xTCA Hardware R&D in IHEP Beijing

Zhen-An LIU
TriggerLab, IHEP Beijing
CERN, CMS Phase II L1 Trigger Workshop
Apr. 26 2017

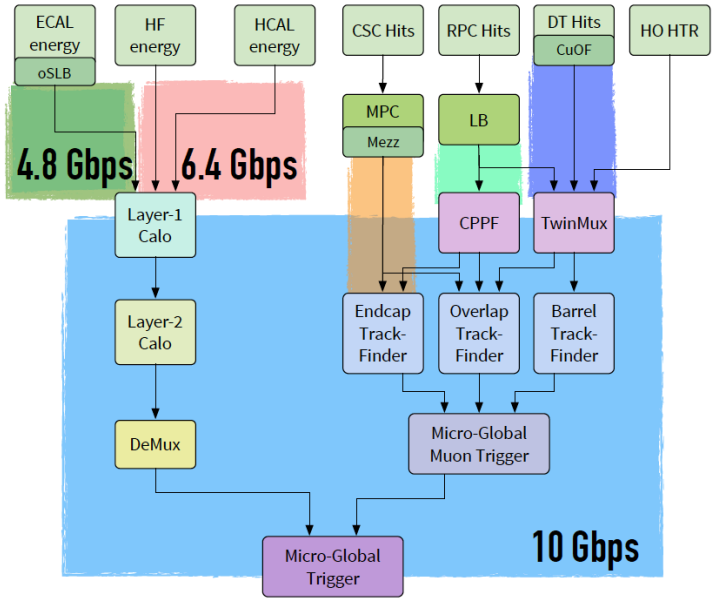
主要研究几个方面的技术

- 系统架构
  - MTCA还是ATCA？（功率，IO，互联）



数据链数据吞吐率

- 现在是多种，最高10Gbps,未来 26Gbps?



Phase1 Trigger

Optical Links

- Standard rate/protocol within trigger borders
  - 10 Gpbs, 8b/10b encoding, asynchronous
- Heterogeneous TPG to L1 links
  - ECAL: 4.8 Gbps, sync
  - HCAL, HF: 6.4 Gbps, sync
  - DT: 480 Mbps, sync
  - RPC: 1.6 Gbps, sync
  - CSC: 3.2 Gbps, sync
- Link firmware sharing where appropriate/possible

L1 & TPGs: Standardise link protocols

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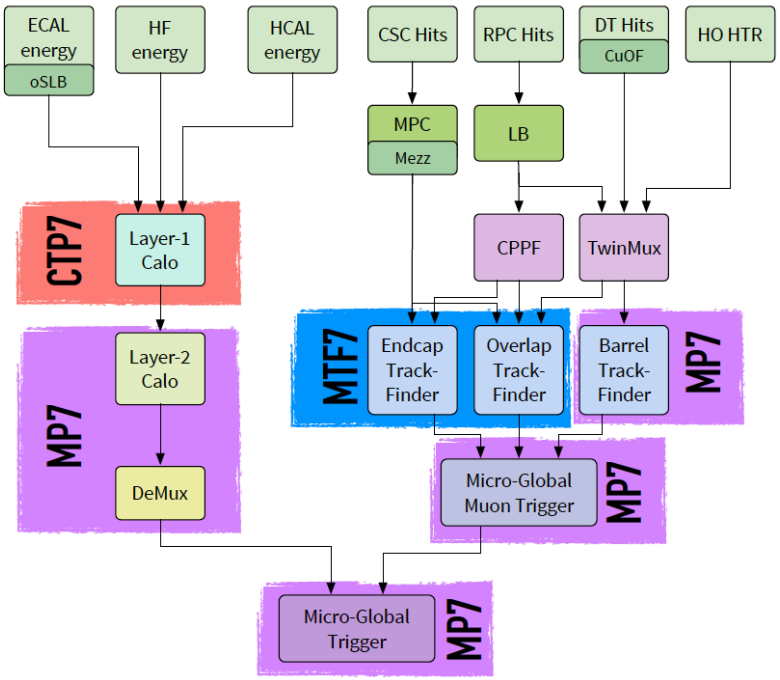
硬件研发通用性，减少插件种类



Phase1 Trigger

HARDWARE & FIRMARE

- Drastically **increased uniformity** compared to Legacy trigger.
- 6 hardware platforms
  - MP7, CTP7, MTF7
  - AMC502, TWINMUX, CPPF
- **AMC13** : Crate-level Clock/TTC distribution and local EVENT building
- Integration and commissioning time significantly reduced by firmware sharing.

Promote hardware & firmware standardisation across L1

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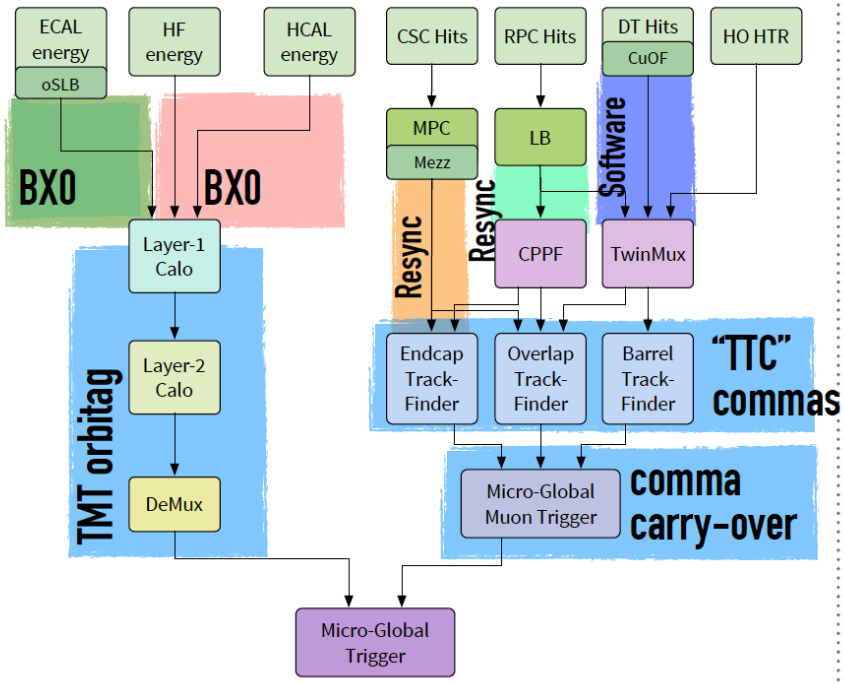
Phase I 同步回顾



Phase1 Trigger

System-level Synchronisation

- No unique strategy
  - TPGs either send inject a BX0 marker in data or 'on request' special patterns.
  - Intra-L1 subsystem links are aligned exploiting the 10G link protocol (commas)
    - Multiple strategies (carry over, injection)
- Uniformity enforced (somehow) at software level
- Lack of common strategy.

L1T & TPGs: Standardise synchronisation procedure

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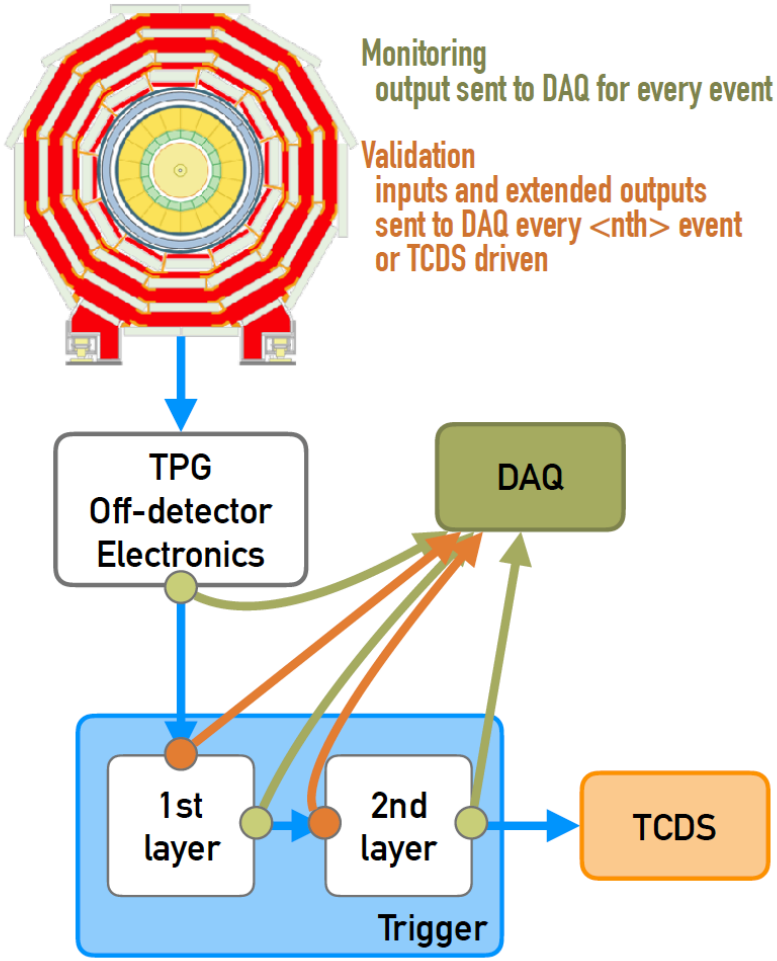
Phase II 研发原则实现统一同步、触发、DAQ



Monitoring & Validation data in Phase 2

- Crucial for debugging and commissioning
- Particularly crucial for TPGs performing clustering/tracking i.e. HGCal/Tracker
- Truly effective only if synchronously sent by L1 & TPGs alike.
- **Starting proposal**
  - Monitoring: L1 & TPGs to send 1BX of output data at every event
  - Validation Events: Every <n> L1As; L1 & TPGs to send extended output (5BX?). L1 systems send inputs.

L1& TPGs: agree on monitoring and validation data definition and implementation

高能所在CMS触发系统二期任务

- 预研
  - 2017年5月
    - Hardware R&D Contributions to Interim Document
      --Some inputs from Zhen-An of IHEP Beijing, China
      - Schedule
      - Key technologies
      - Demonstrator
- 设计
  - 高能所CMS组决定不参加 Tracker触发了
  - HGCal 触发（困难：没有联系人了解讨论技术问题）
  - 继续参加Mu upgrade设计
    - 探测器两端读出
    - 电子学增加幅度信息
    - 预触发（Imad talk at IHEP Nov. 5-9/CEPC workshop)
  - DTC设计

小结

- 2017年取得了重大成绩，完成了CPPF系统
  - 建造
  - CMS 系统集成
  - CMS宇宙线取数
  - LHC对撞数据取数
- 在进行的任务
  - CPPF Unpacker,Emulator的开发
  - 完成了CMS phase II L1 upgrade高能所的预研计划
  - 讨论新Mu探测器的新型读出对应的新预触发设计

backups

Schedule (IHEP Beijing)

- *Final hardware designs (partial if any) will be in decided by CMS after 2020/2022
- *Prototype hardware (if any) between 2018-2020 with key technology demonstration
- *Hardware R&D will continue based on present ATCA/xTCA development aiming key technologies

关键技术研究

The technologies and challenges that we will seek to address in the R&D period can be summarized as:

- Study on the advantage and disadvantage of pluggable module, i.e. ATCA/xTCA carrier module with AMC processor compatible PICMG 3.8 specifications. Signal integrity for 10G+ with connectors
- Study on the advantage and disadvantage of input/output with RTM module including capabilities and/or limitations of optics and connectors.
- Influence of power modules on the carrier board to the heat resistance in the airflow route in an ATCA shelf.
- Crosstalk inside FPGA in high speed data transmission in some cases.
- Experience of designing hardware moving from Virtex FPGA to Ultrascale/Ultrascale+ as key module.

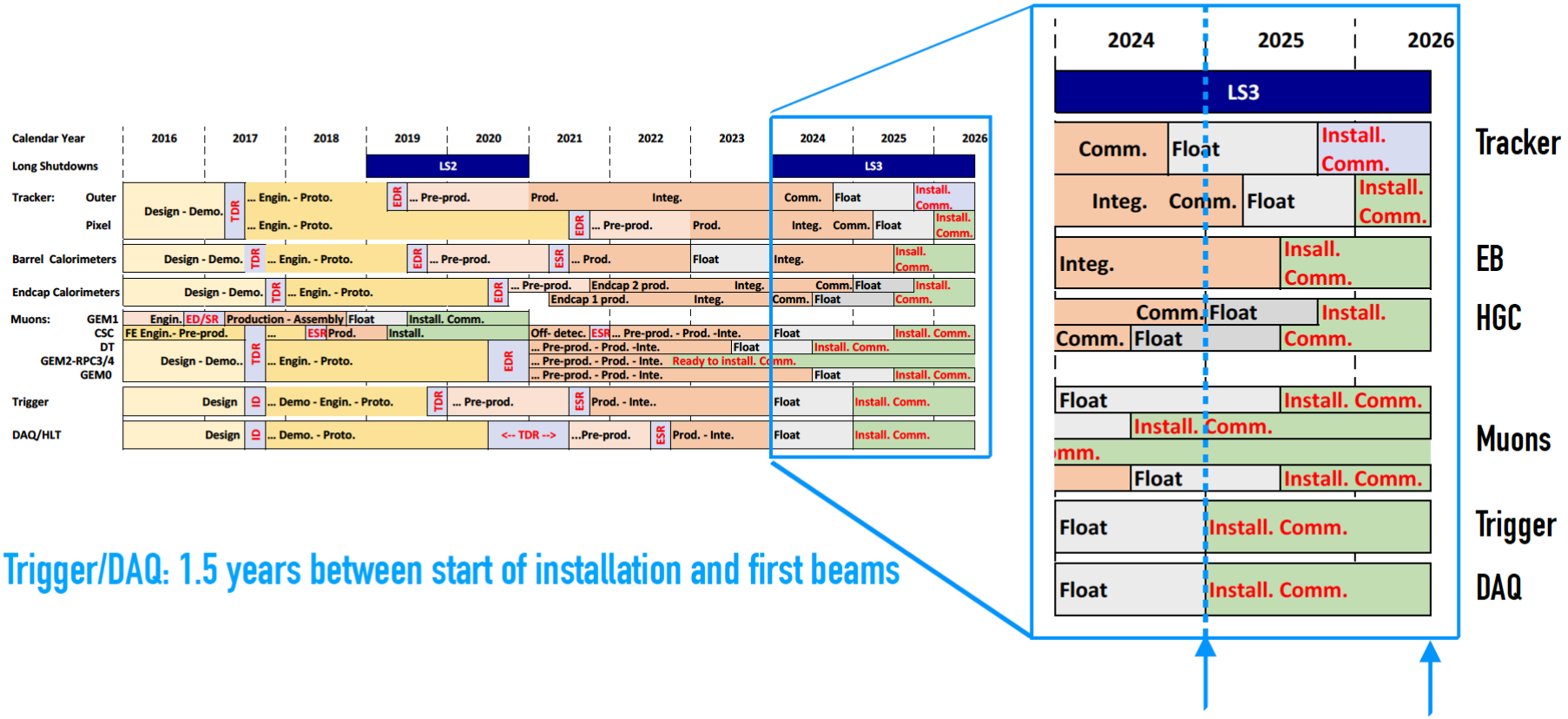
Modularity system is popular and necessary in most of cases but higher speed 10G+ make the signal integrity a problem especially with connectors so these studies are important and necessary(item 1,2). Applications with Belle II showed that some of the power modules on the carrier board and processor AMC module block the airflow which make the head resistance high. In the Belle II application we met also some problem with some channel inside FPGA which we doubt due to the crosstalk inside FPGA, and this study should continue. And transition from Virtex FPGA to Ultrascale and Ultrascale+ is a must for a design of in 5 years. These studies should be made in accordance with prototype designs. We will first use Ultrascale FPGA, and later use Ultrascale+.

Demonstrators

- IHEP demonstration will be mainly in modularity one as a basis, that is AMC as a processor, ATCA frame with routine and control as carrier, and RTM as auxiliary IO channels. IO bandwidth will be increased with prototypes aiming a 26G. Higher possibilities will be depends on the test results. Ultrascale will be used for the first prototype in 2017 and move to Ultrascale+ later in 2018+. Some tests in Belle II application might be possible to better understanding the possible problems. Final demonstrator will be well coordinated with CMS joint work as outcome of CMS R&D before moving to final design.

CMS 触发 PhaseII计划

A BRIEF LOOK AT THE PHASE 2 SCHEDULE



Trigger/DAQ: 1.5 years between start of installation and first beams

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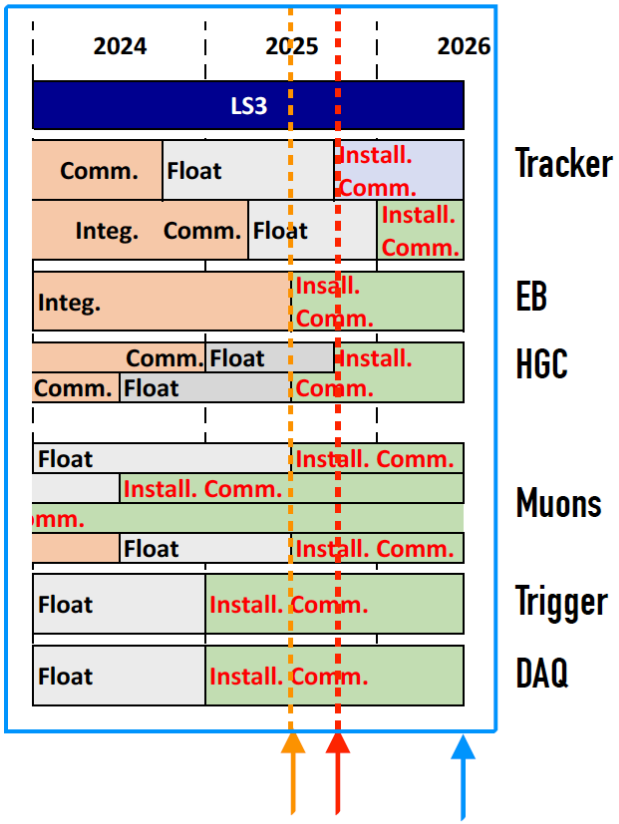
触发二期关键因素

A BRIEF LOOK AT THE PHASE 2 SCHEDULE

- Timeframe similar to **Phase1 upgrade**:
  - Installation/Commissioning: Start of 2015 to mid 2016.
  - Heavily relied on upon the stability of TPG and DAQ/TCDS.
- **Phase-2**
  - TPG detectors installation/commissioning starts **6-9 months before beam**.
  - **Tracker, HGCal**: new detectors, never in the trigger before, performing complex TP computations



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