

Silicon Tracker in HERD and the ion beam test result of ladder with IDE1162 chips

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Outlines

- Silicon Tracker for HERD
- New ladder with IDE1162 chips
- Ion beam test and preliminary result
- Summary



Silicon Tracker for HERD

Main function of STK

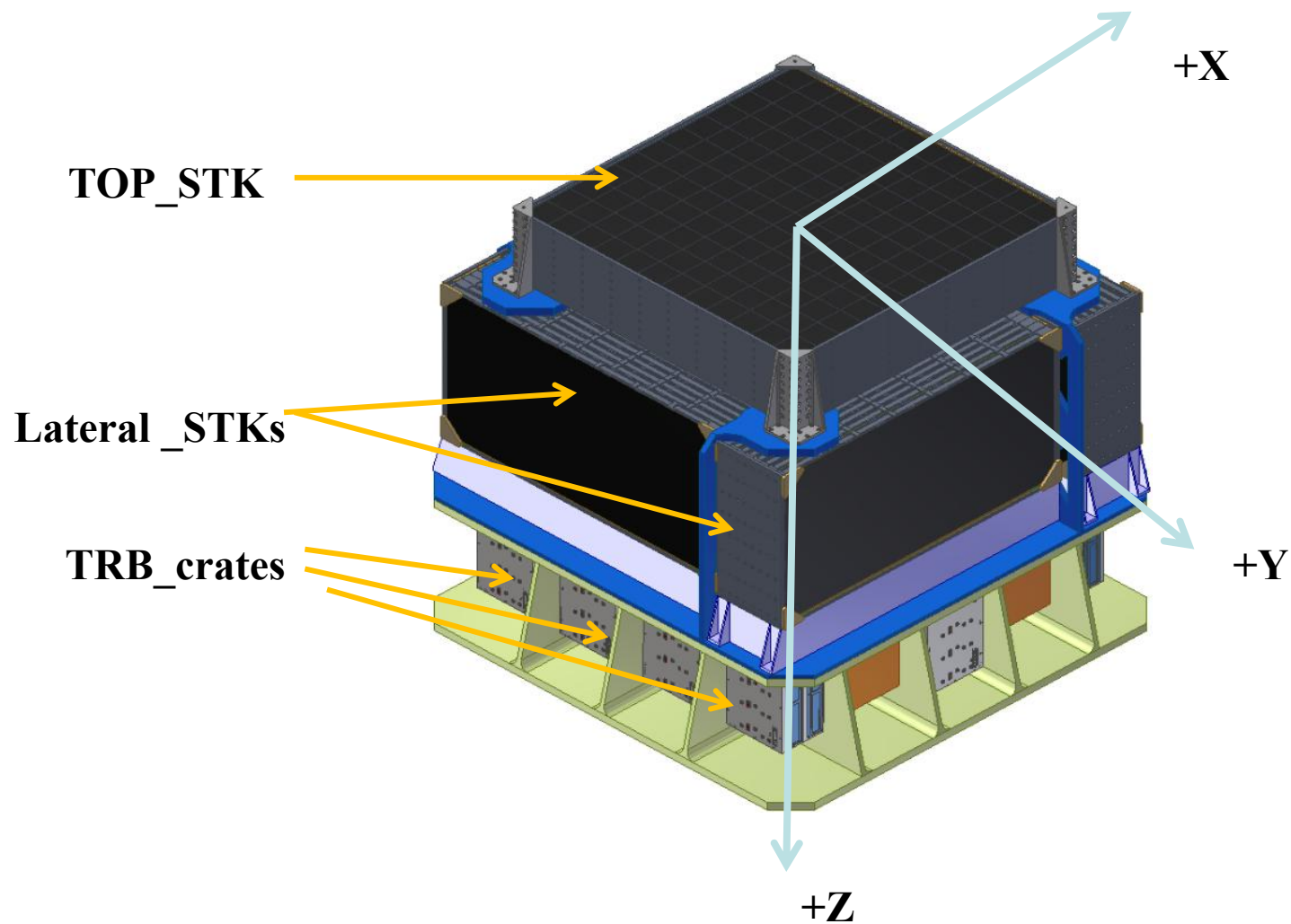
- I. Particle tracking
- II. Gamma-ray converter&imaging
- III. Charge measurement

STK	Specification
FOV Coverage (ECAL)	>80%
Charge measurement	Z=1~20 (26) (charge resolution <10%@Z=1)
Layers	6 (X, Y) for both Top_STK and 3(X,Y) for Lateral_STK
Angular resolution	~0.1 deg@10GeV
Gamma pair-production Material	LYSO crystals or Tungsten layers (55% pair production @10GeV gamma-ray)
Dead time	<2ms
Operating mode	External trigger (Internal trigger for calibration)



Silicon Tracker for HERD

STK Layout and configuration



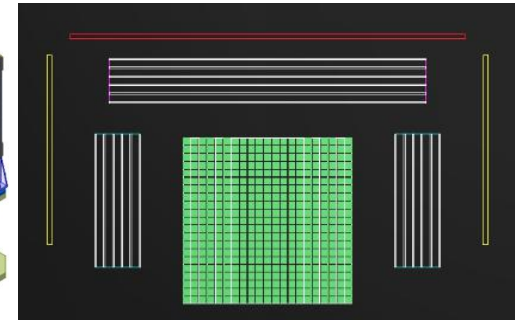
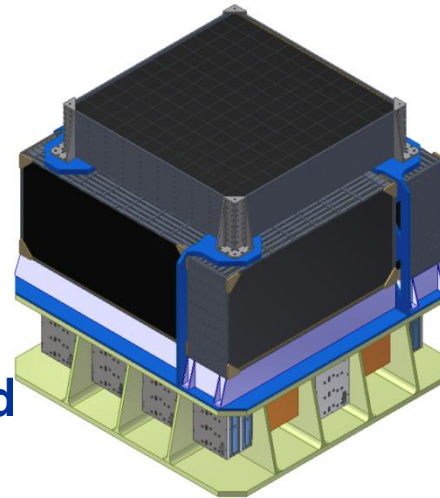


Silicon Tracker for HERD

STK Layout and configuration

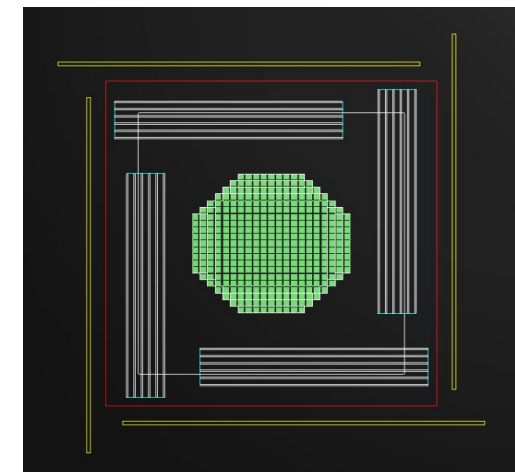
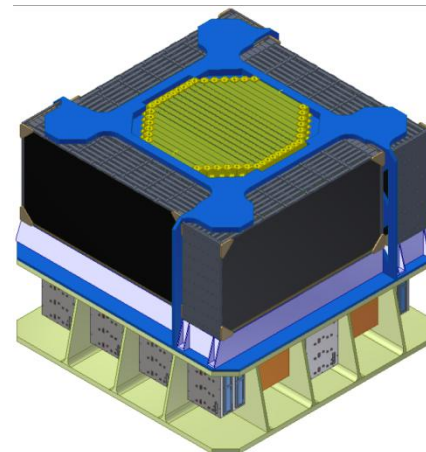
■ Top_STK

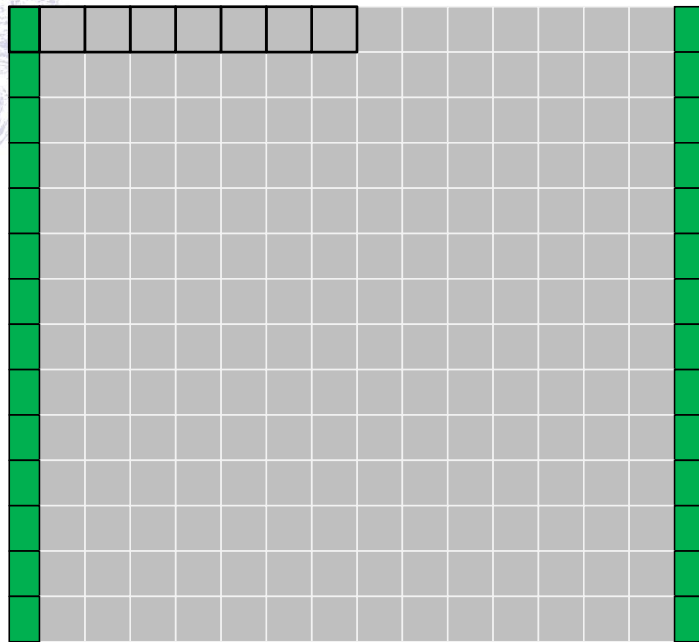
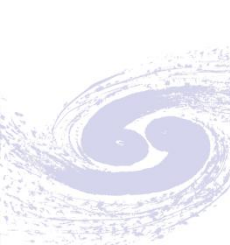
- 6 Layers of X&Y SSDs with LYSO
- 133cm*133cm (active area)
- 28 ladders on each X or Y plane and each ladder has 7 SSDs



■ 4*Lateral_STK

- 3 Layers of X&Z or Y&Z SSD
- 95cm*66.5cm (active area)
- *10 ladders on X or Y plane and each ladder has 7 SSDs
- *14 ladders on Z plane and each ladder has 5 SSDs

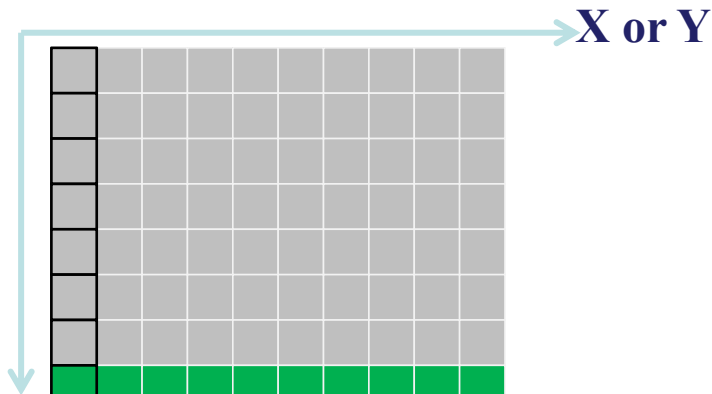




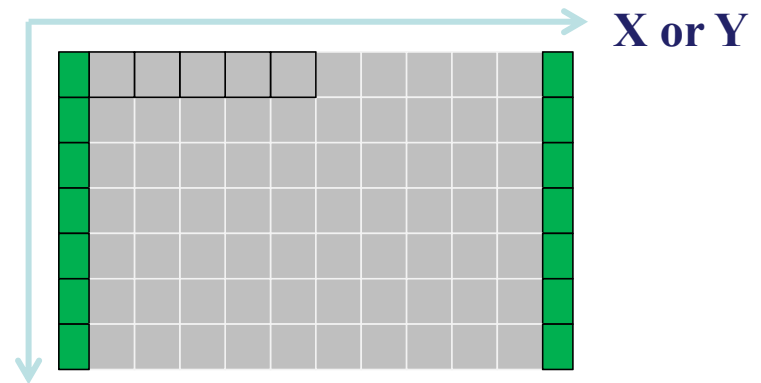
ladder layout on the Silicon Plane

Top_STK: 14*14 SSDs /each X or Y layer

	Top_STK	Lateral_STK
ladders	336	72*4=288
Sum up	624	



+Z
Lateral_STK- Z layer: 7 SSDs *10
one side readout



+Z
Lateral_STK- X or Y layer: 5 SSDs *14
two side readout



Silicon Tracker for HERD

STK Design – inherit from DAMPE STK, but more challenge!

	DAMPE STK	HERD STK
Single-sided Silicon micro-strip Detector (SSD)	Size: 95 x 95 x 0.320 mm ³ Pitch: 121 um	the same
Ladder	4*SSDs in a daisy chain	7*SSDs and 5*SSDs
Tracker Front-end Hybrid (TFH)	6*IDE1140 chips (0~200fC, Z=1~6) Analog output	New ASIC: Much higher dynamic range for charge measurement (Z=1~26) if needed, Digitalization, Zero compression; HCC-ASCI control chip
Tracker Readout Board (TRB)	ADC board, FPGA control board, (ASIC control, Data compression) Power supply board	FPGA control board (configure HCC, Data storage and transmission, more simple than DAMPE) Power supply board
Mechanism	Plane: CFRP+HoneyComb	Bigger plane
Thermal issue	85W , easy for sun synchronous orbit	? W (depend on power consumption of ASIC chips) Complicate thermal environment for space station



Silicon Tracker for HERD

new ASIC

Large Dynamic range (0~5.6pC) for
charge measurement(Z=1~26),

low noise (rms<0.3fC) for Z=1(MIPs)

Digitalization and zero compression

Low power consumption

Radiation hardening

(similar to IDE1140)

•

We should customize a new ASIC!



New ladder with IDE1162 chips

We chose IDE1162 to test the high-Z response of SSD

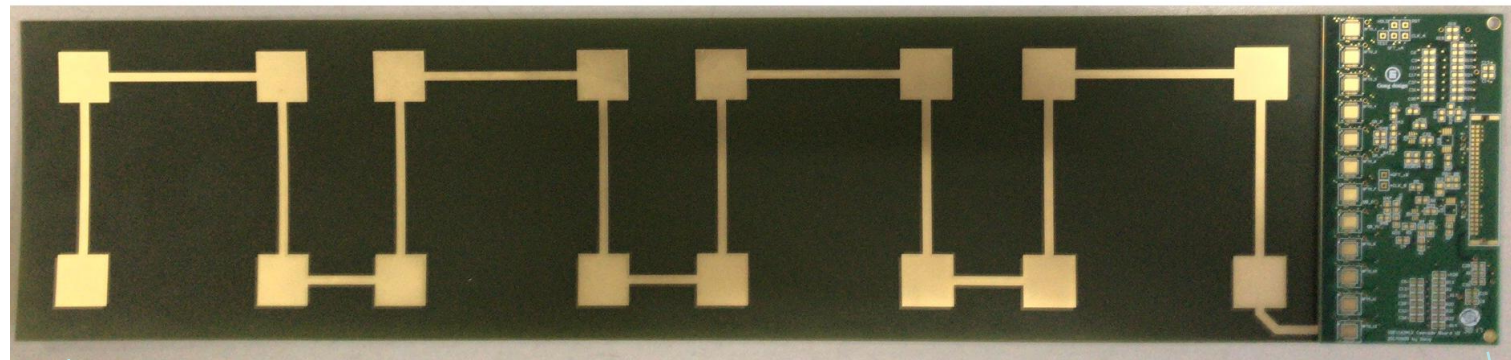
	IDE1140(VA140)	IDE1162
Number of inputs	64	32
Input charge range	$\pm 200\text{fC}$ (Z<6 r/o, ,Z<10 float)	$\pm 1.5\text{ pC}$ (Z<14 r/o, Z<24 float) Z>1
Shaping time	5 μs to 8 μs	2 μs to 2.5 μs
Equivalent Noise Charge (ENC)	98e ⁻ + 6.5e/pF	1900e ⁻ + 2e/pF
Outputs	Multiplexed pulse height	Multiplexed pulse height
Test and calibration	Internal calibration circuit	Internal calibration circuit
Other function	/	/
Power consumption	0.29mW/channel	1.78mW/channel

- Compared with VA140, IDE1162 has a large dynamic range but higher noise.



New ladder with IDE1162 chips TFH design and production

- We made a TFH hybrid board with 12 IDE1162 chips connected in a daisy chain

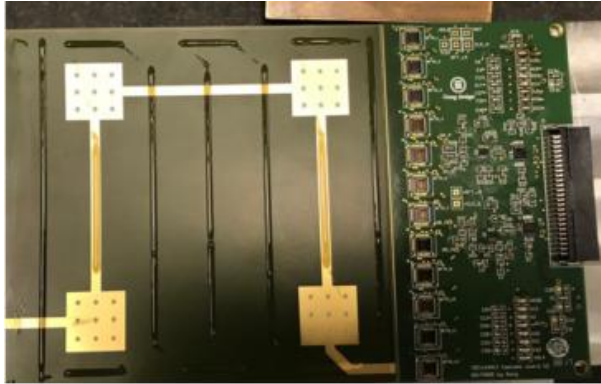


Flex Board for silicon microstrip detectors mounting and High Voltage (9.5 x 9.5 cm² from 6 inch wafer, 320μm thick from Hamamatsu)

IDE1162 ASIC *12



New ladder with IDE1162 chips **ASIC and SSD assemble**



Silicon micro-strip detectors gluing

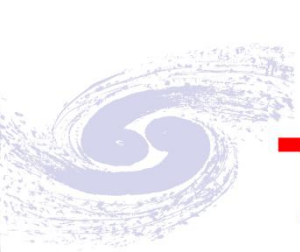


Sense assembly



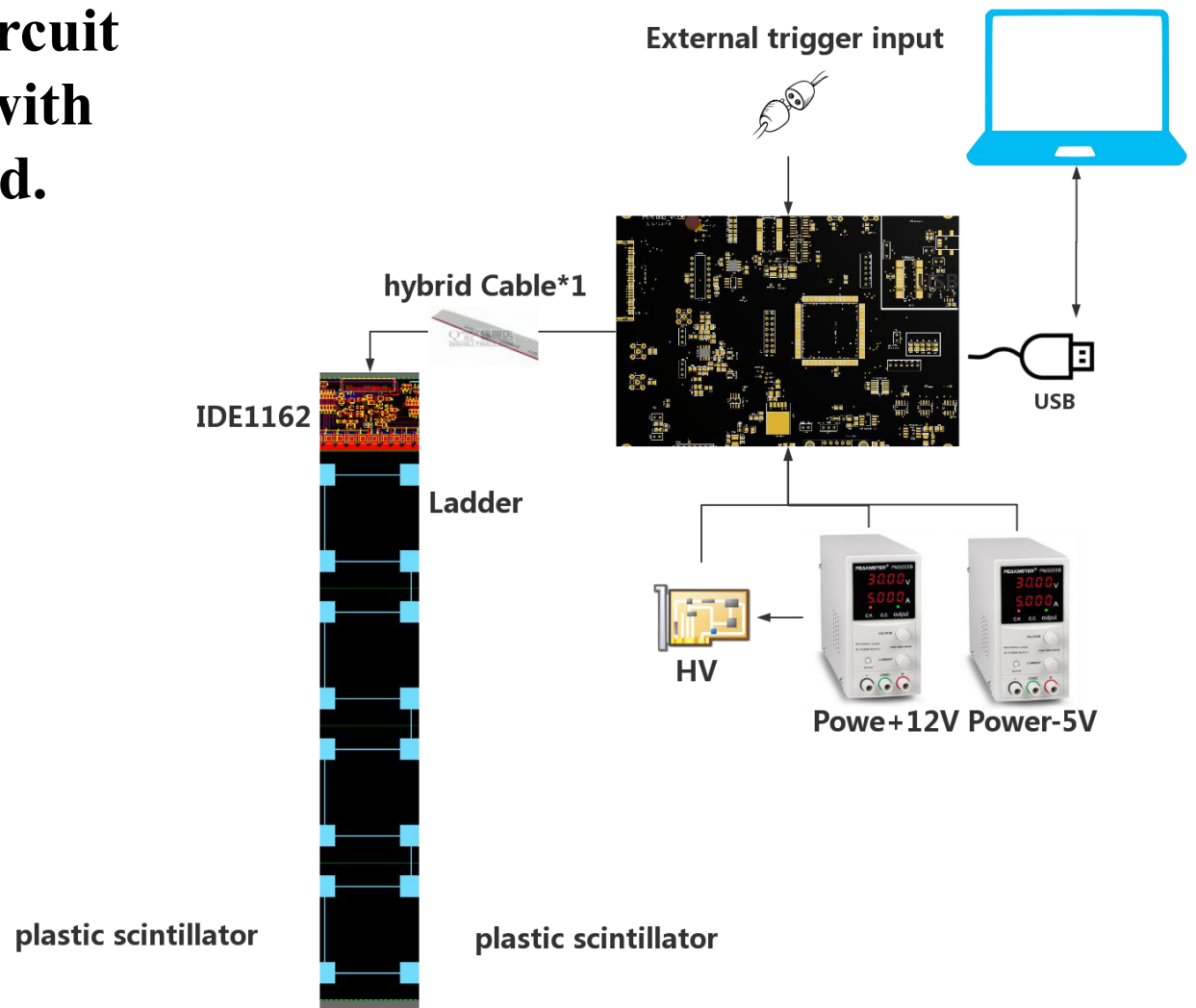
wire bonding

Many thanks to Giovanni and other colleagues in Perugia University!



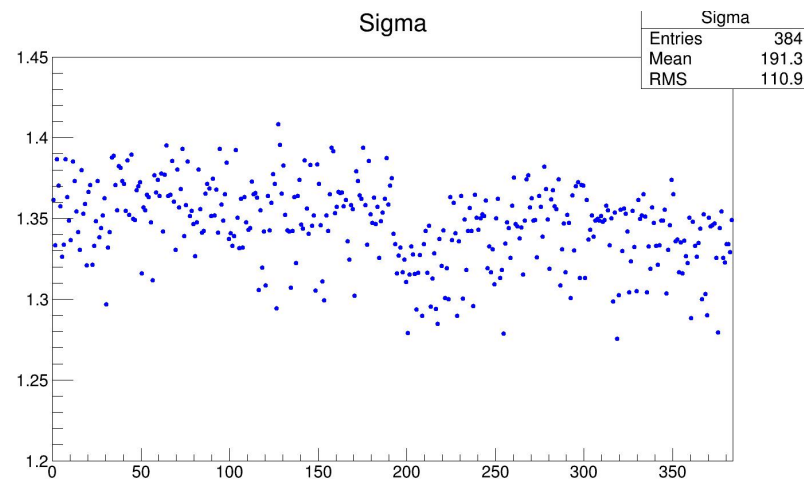
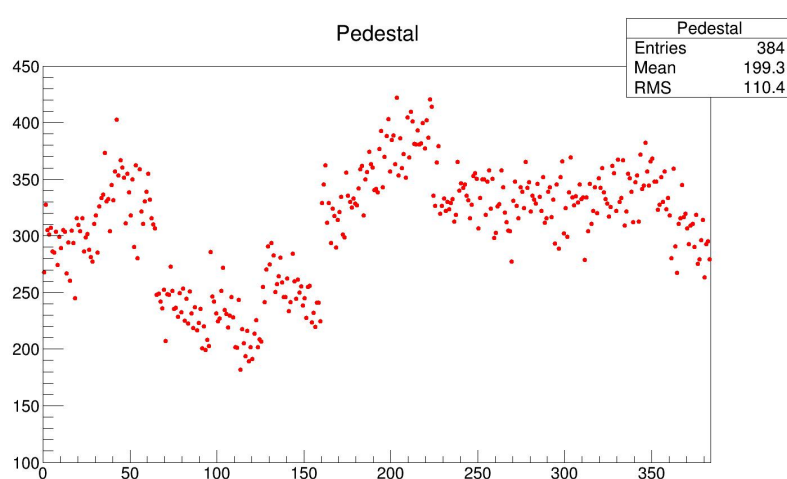
New ladder with IDE1162 chips TFH design and production

**IDE1162 readout circuit
inherit Mini_TRB with
FPGA code modified.**





New ladder with IDE1162 chips Pedestal and noise



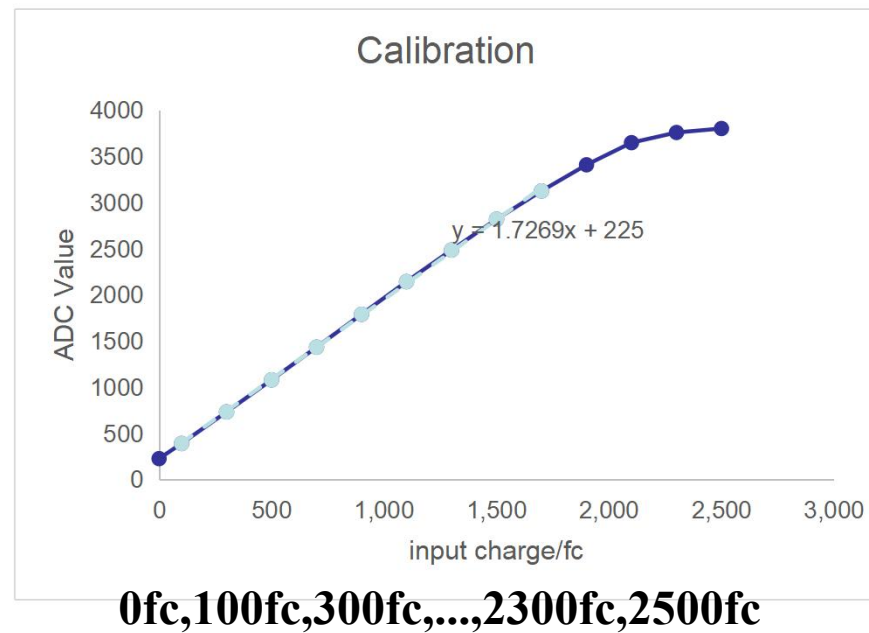
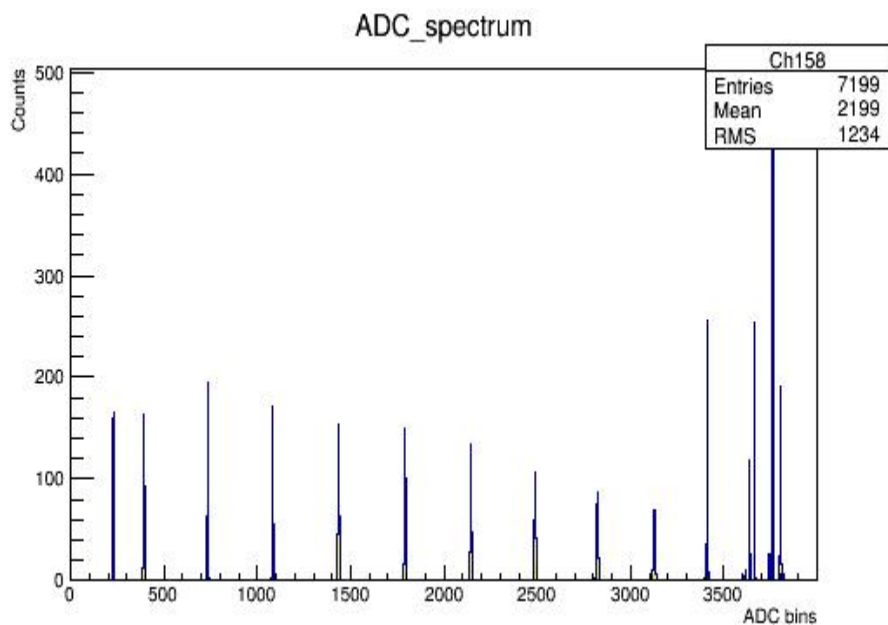
Pedestal and RMS after common noise subtraction

RMS = 0.78fC (0.58fC per ADC)



New ladder with IDE1162 DAC Calibration

■ DAC calibration by charge injection



<1.6 pC is linear

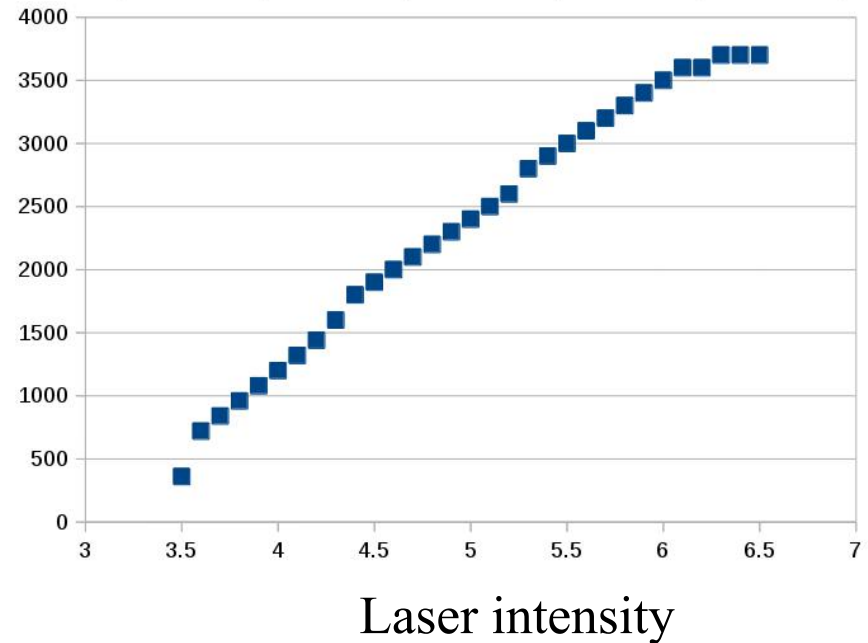
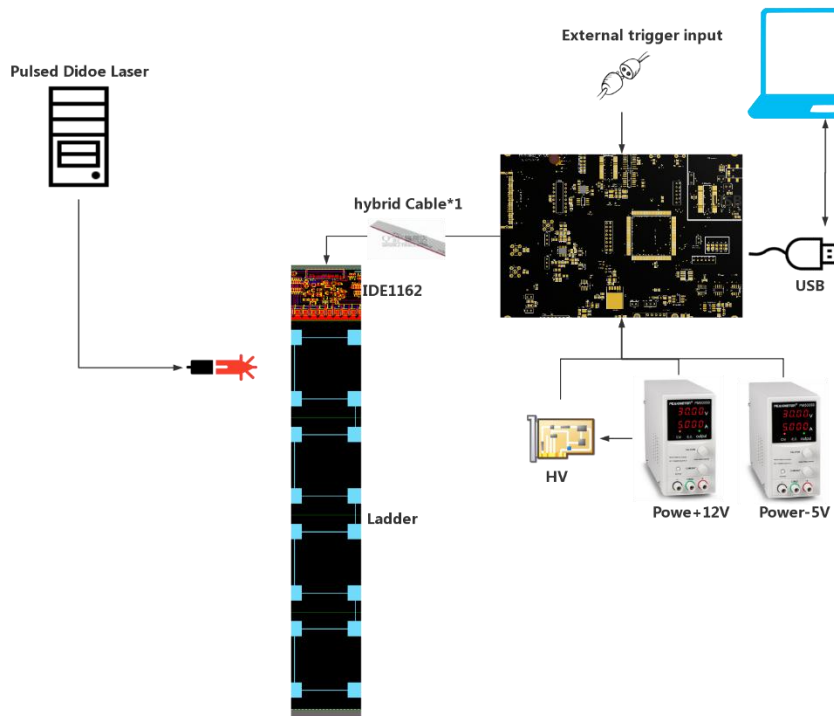
1% integral linearity for positive charge



New ladder with IDE1162

Ladder test with Laser

(in Perugia University)

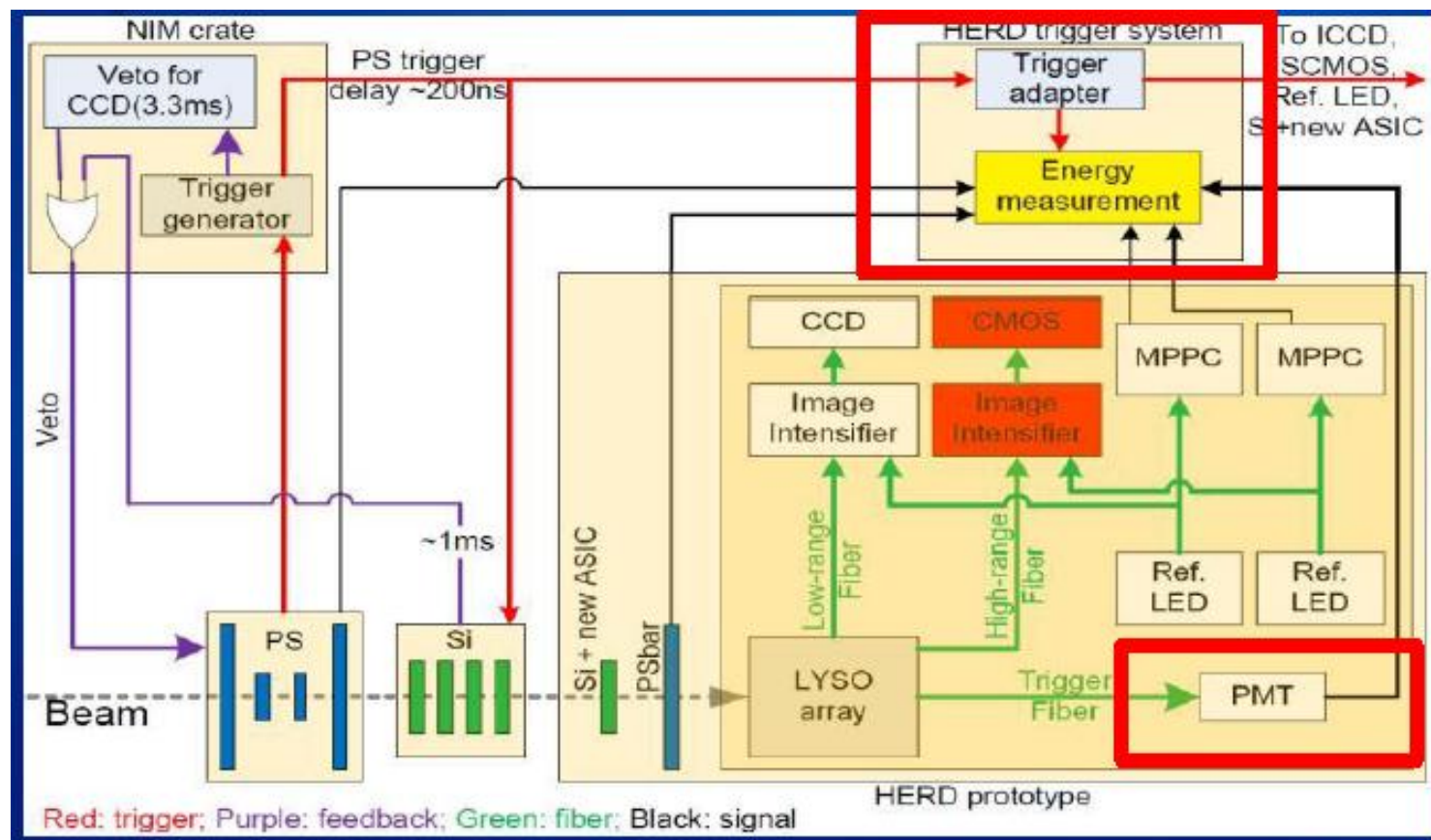


Hard to accurately measure the linearity of the entire Ladder with laser.



Ion beam test preliminary result

Trigger system setup

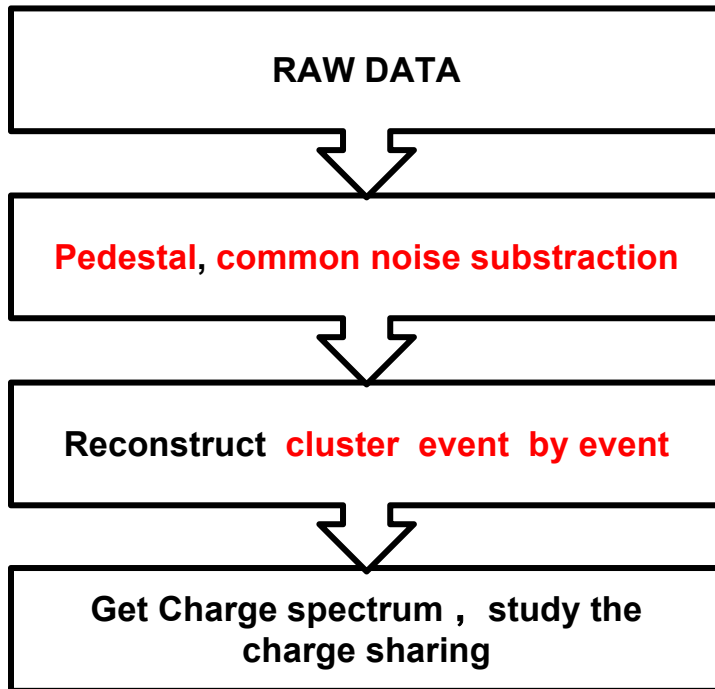




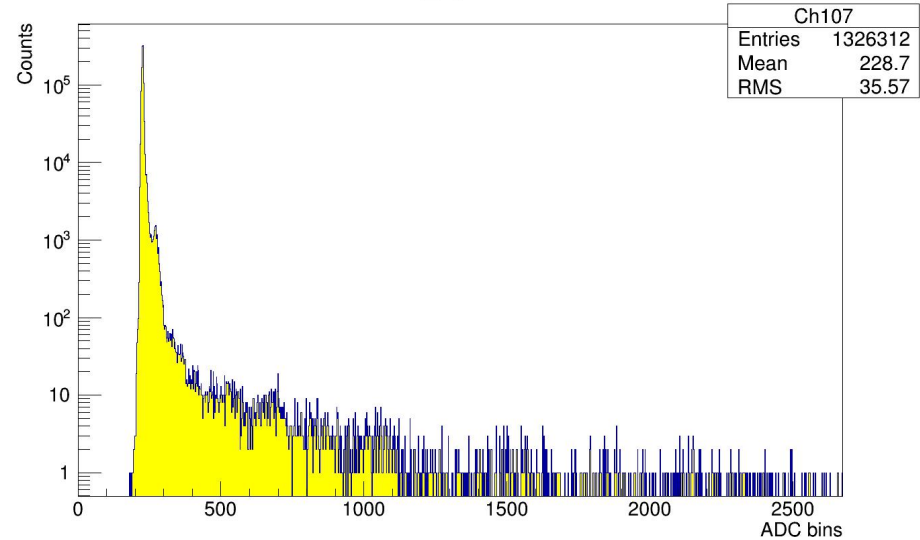
Ion beam test preliminary result

Result from Beam Test

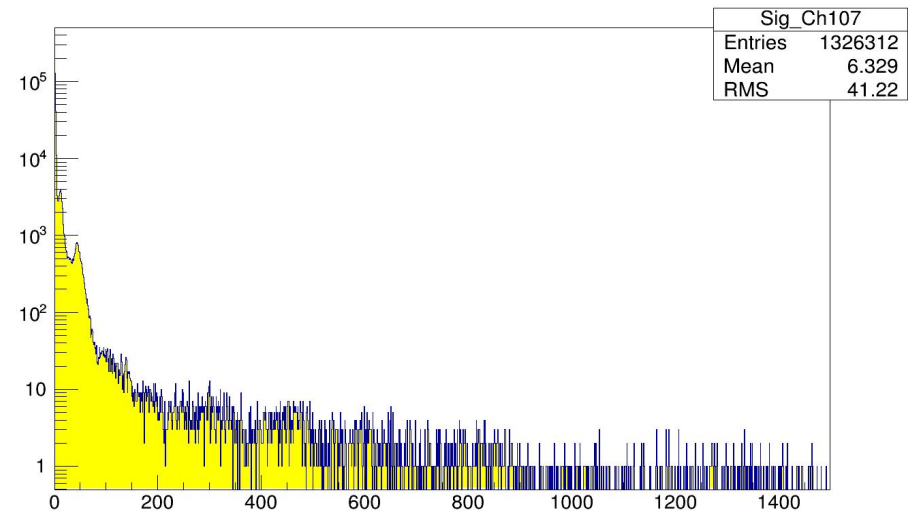
■ Preliminary data analyzing



ADC_spectrum



RawADC-Pedestal-CN





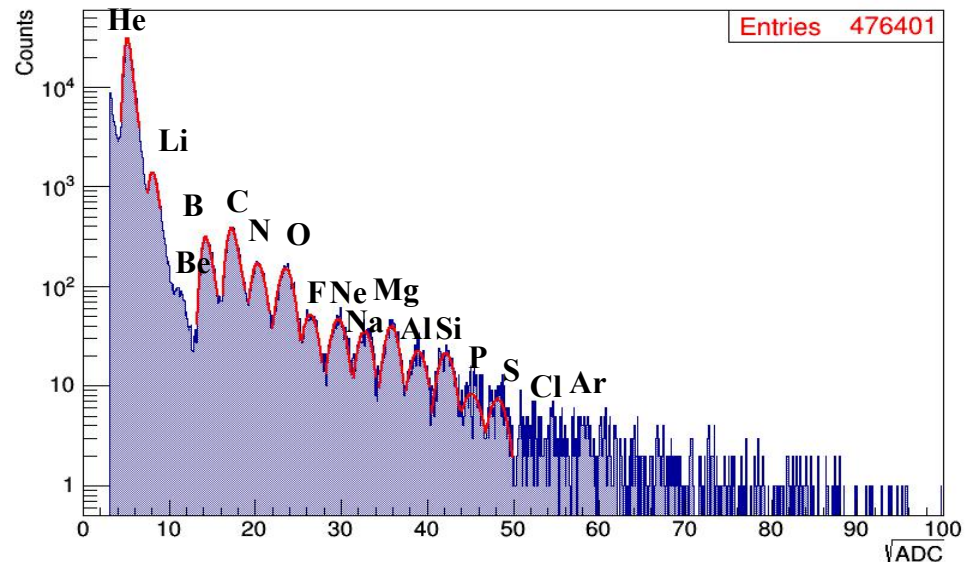
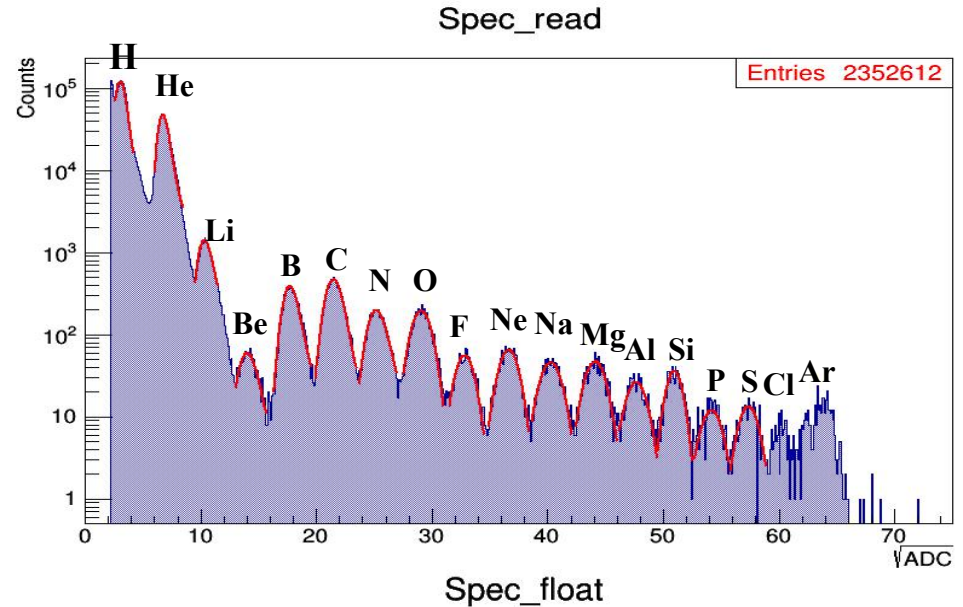
Ion beam test preliminary result

ADC Charge spectrum

□ r/o strip/float cluster ADC charge spectrum

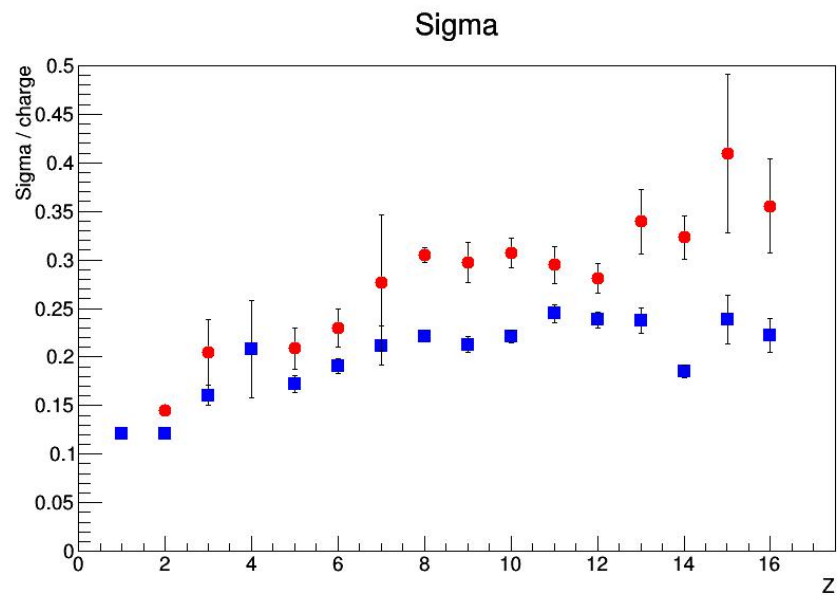
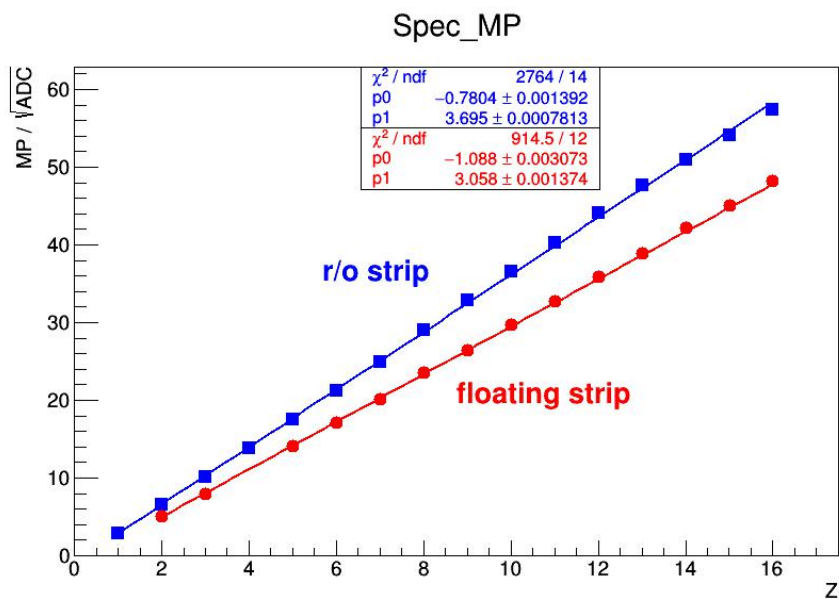
□ Preliminary analysis results

- When the r/o strip is hit, the lowest case is $Z=1$ can be detected
- When the float strip is hit, can only detect $Z \geq 2$
- Up to $Z=16$ (in linear) or higher Z particles





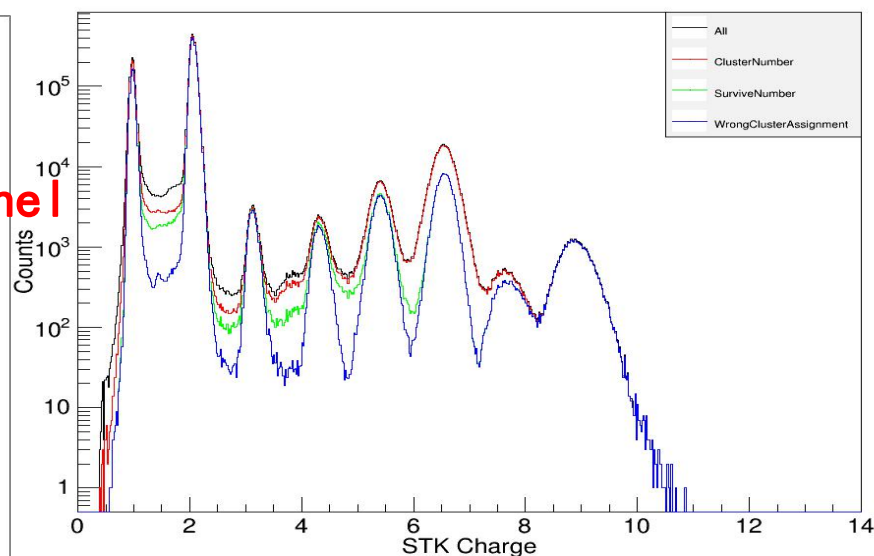
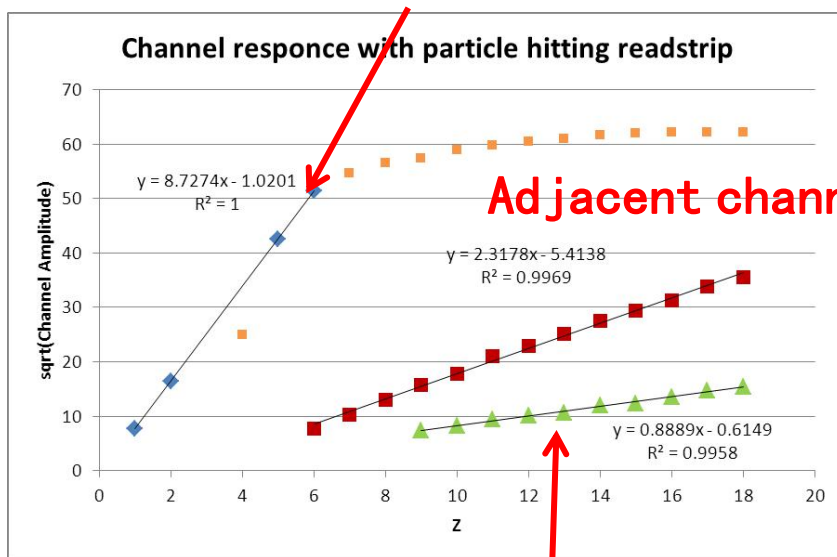
Charge response linearity and resolution





Compared with DAMPE-STK

Hit bar saturation ($Z > 5$)

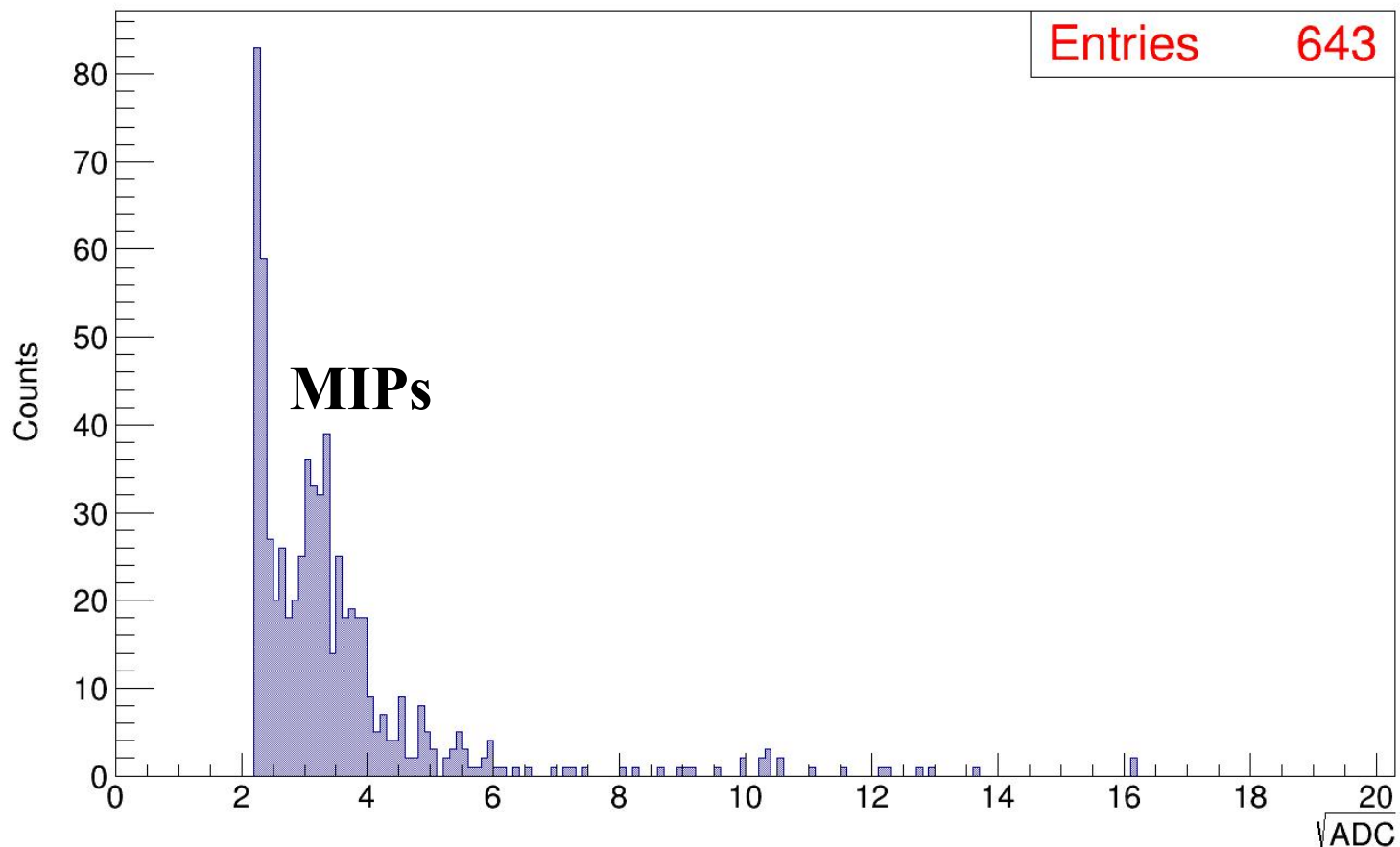


Interval of one channel



Ladder test with cosmic ray after BT

ADCSpec_read





Summary

- A customized ASIC is needed for STK to measure high-Z(1~26) Cosmic-rays.
- We design and produce a new ladder with higher dynamic-range ASIC – IDE1162(~1.6pC) .
- The beam test result of new ladder showed that the charge response was linear up to Z=16, but the noise was higher than expected.

An aerial photograph of a large, circular, multi-layered structure, possibly a well or a large hole, with a blue sky background. The structure consists of several concentric rings of earth and rock, with a dark, circular opening in the center. The surrounding area is a mix of brown and tan earth, with some sparse vegetation. The sky is a clear, bright blue.

Thanks!