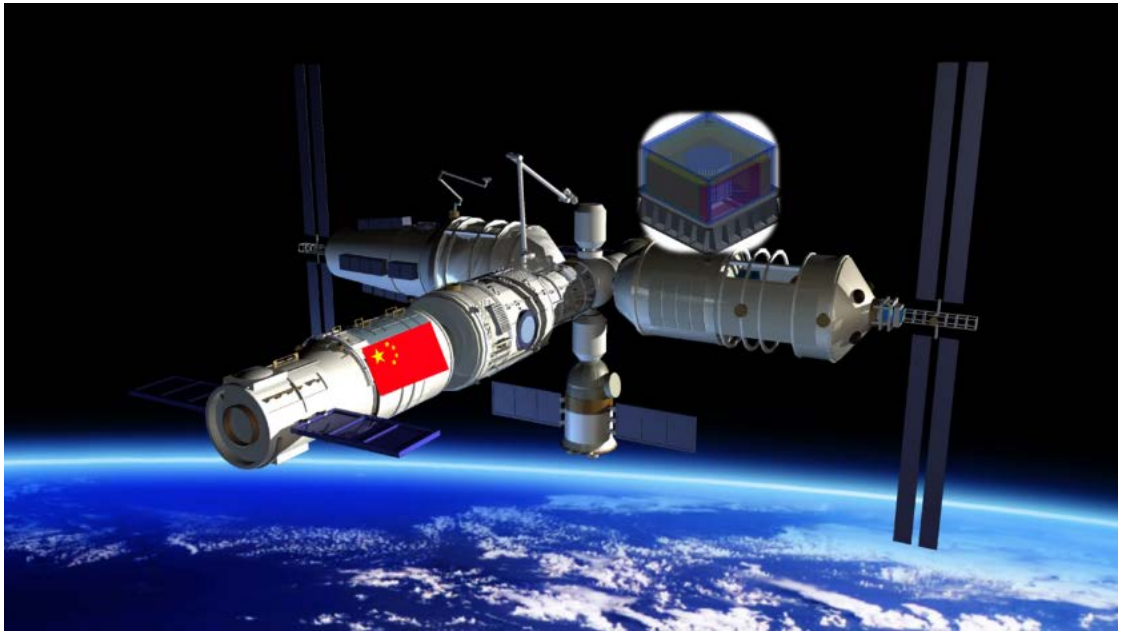
6TH HERD INTERNATIONAL WORKSHOP

R&D activities on Fiber Tracker (FIT)



STATUS AND PLAN

27th March 2018

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Introduction

- Scintillating fiber tracker has been used in space
  - CALET: 1 mm^2x44.8 cm, 7168 fibers, 8 x-y layers, 64-ch MAPMT readout
- Large area high precision SciFi trackers in HEP
  - UA2: ø=1 mm, 62k fibers, CHORUS: ø=0.5 mm, 1.3M fiber, D0: ø=0.835 mm, 80k fibers, K2K: ø=0.692, 275 K fibers, …
  - Mu3e: small SciFi tracker/TOF being produced in Geneva
  - LHCb SciFi for run 3 upgrade (installation Dec. 2018)
    - ø=0.25 mm, SiPM readout, 560 m^2 detector surface, 590 k channels, 10,000 km fibers, 1300 fiber mats (13 cm x 2.5 m)
    - 4 mat winding centers, including one in at EPF Lausanne
- HERD fiber tracker (FIT) can profit the synergy with LHCb and Mu3e
  - Technology is mature for space application
  - Production capability easily available

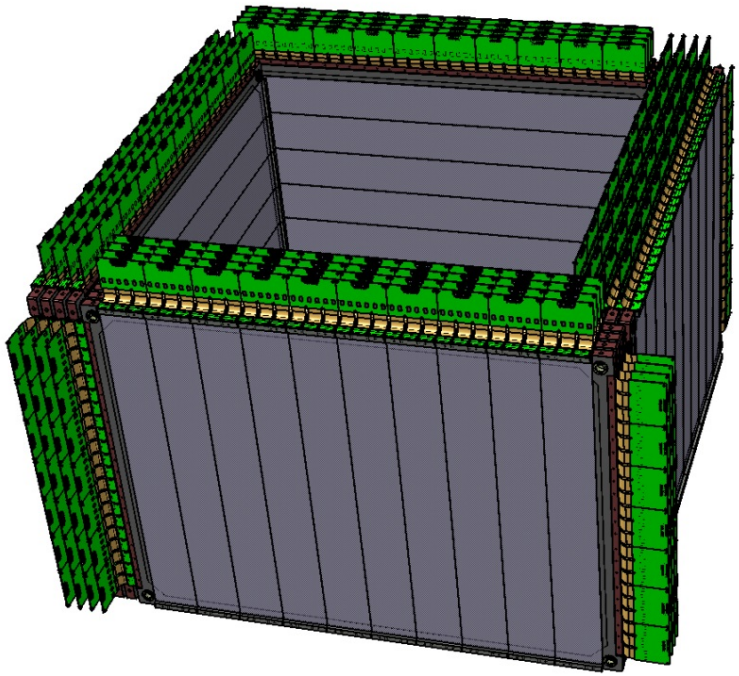
Why a fiber tracker

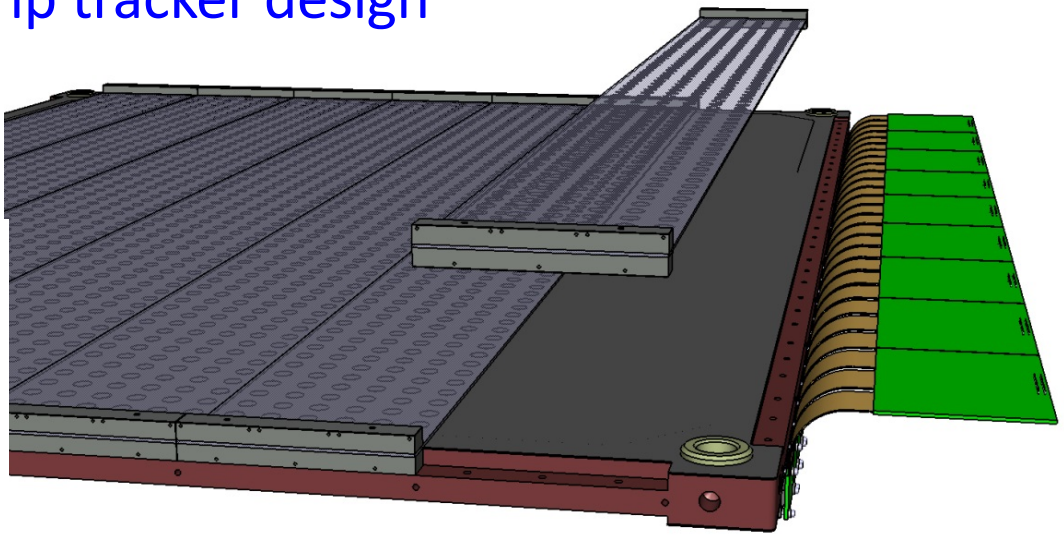
- Depending on applications, the spatial resolution is similar to the one of silicon strip detectors.
- Simpler to build long detector (of e.g. 1 m).
- FEE can be placed on one side of the detector module, even if it is long.
- Simpler to place the FEE outside of the support tray.
- Reduced dead area (no gap between sensors, no dead area on the silicon detector, FEE placed outside of support tray).
- No wire bonds on the detectors, thus the distance between support trays can be smaller than for silicon detectors.
- Lighter trays.

- Still the design needs to go through the space qualification process.

Fiber Tracker proposal

- Proposal to use scintillating fibers on the four lateral sides of the tracker detector.
  - Based on the silicon strip tracker design





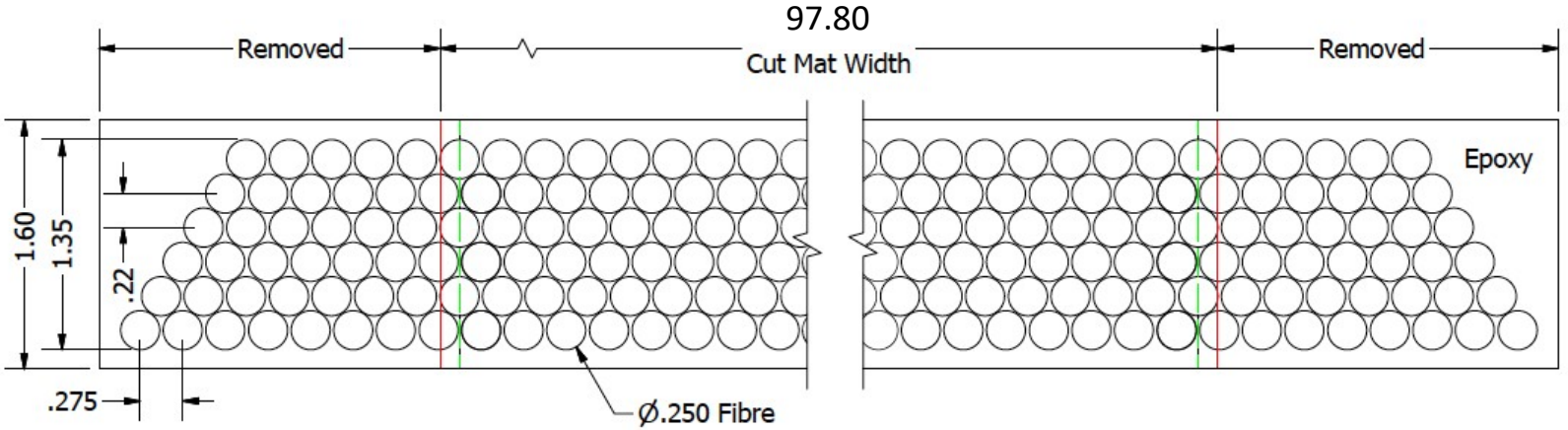
Detailed description in the presentation on mechanical design

FIT: 4 x/y-z SciFi layers

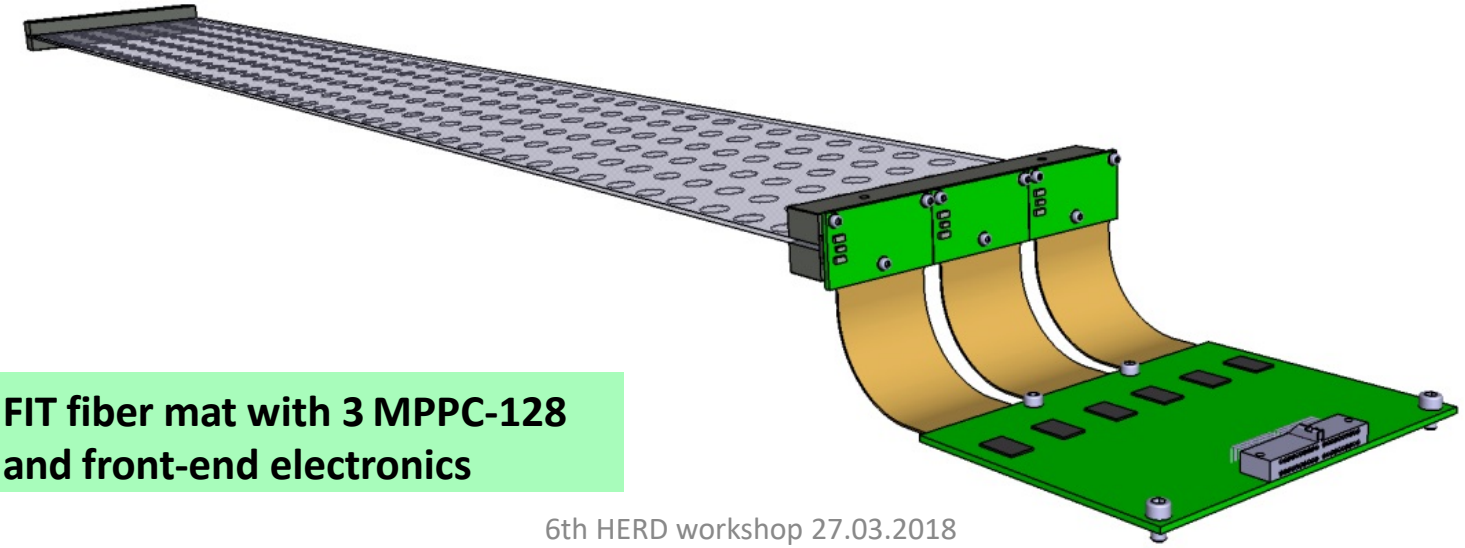
Using Scintillating Fibers for the side tracker

- Sensitive area ~ 100 cm x 70 cm: can fit this size with 3-MPPC array fiber mats
  - Fiber mat width: 97.8 mm
    - MPPC array size 32.54 mm, gap between chips 0.11 mm, gaps between mat: 0.15 mm: 3x(32.54 +0.11) = 97.8+0.15 = 97.95 mm
  - Panel size
    - xy: width (7 mats) = 685.65 mm, length = 100 cm (long)
    - z: width (10 mats) = 979.5 mm, length = 70 cm (short)
  - Fiber mat thickness: 6 layers of 250 μm fibers + glue, ~1.7 mm
- Layout
  - Minimal: 4 x-y, 22 mm layer spacing, 272 mats (112/160 long/short)
    - 816 MPPC arrays, ~104k channels
    - 560 km fiber (assume 2.5 km for 1m of mat)
  - Robust: 5 x-y, 22 mm layer spacing, 340 mats (140/200)
    - 1020 MPPC arrays, ~130k channels, 700 km fibers

Fiber mats



- HERD mat: 97.80 mm width + 200 μm inter-mat gap to match for 3 SiPM
  - MPPC size 32.54±0.05 mm, gap between chips 110 μm ⟹97.84 mm



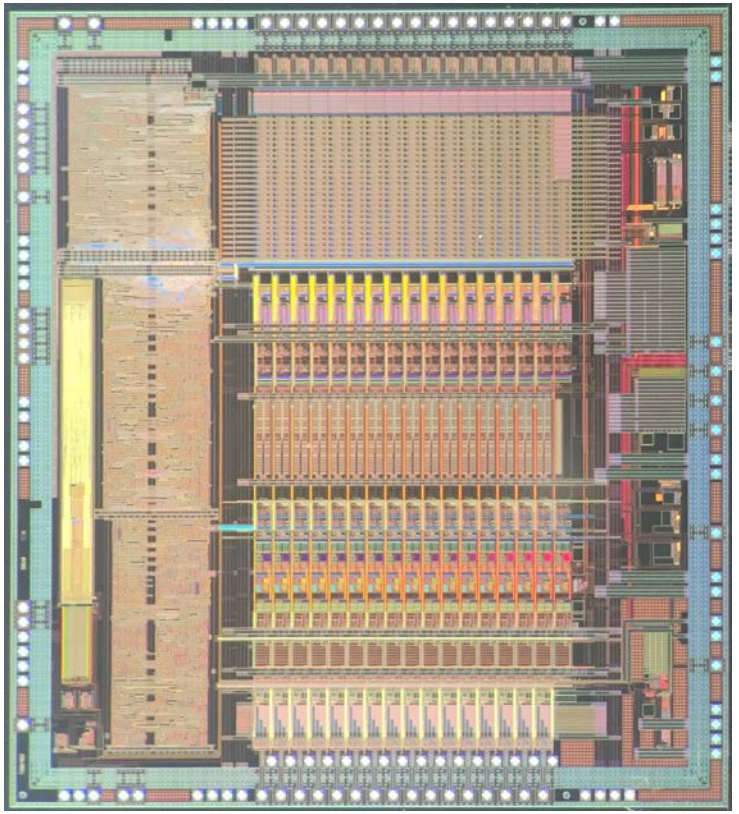
FIT fiber mat with 3 MPPC-128 and front-end electronics

Test and study activities

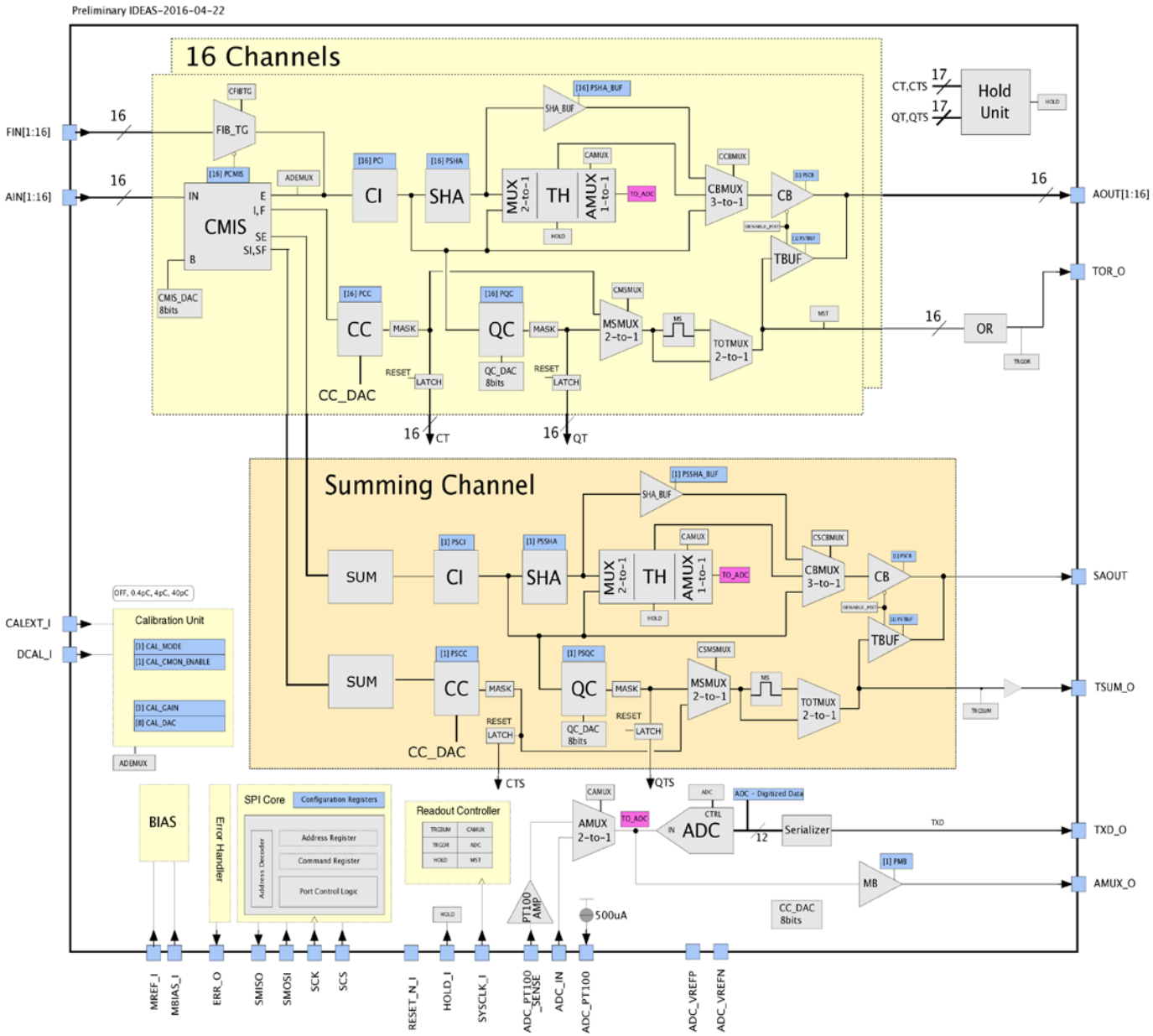
- Production of test modules.
  - Two modules assembled in 2017, more will be produced in 2018.
- Performance tests.
  - Beam tests, cosmics, LED, radioactive source…
- Mechanical design studies.
  - Production of test trays.
  - FEA simulations.
- Design and production of test front-end electronics.
  - Two types of ASICs are used: VATA HDR 64 and SIPHRA.
- Space qualification tests.
  - Thermal, thermal-vacuum tests, vibration tests foreseen in 2018.
  - A thermal vacuum setup is under development at UniGE.
- Detector simulations.

SIPHRA ASIC

- SIPHRA = “Silicon Photomultiplier Readout ASIC”
- New ASIC from IDEAS for space applications
- The circuit has been designed under contract from the ESA with support from the Norwegian Space Center and the University of Geneva.
- 16 input channels, designed for PMT or MPPCs.
- Possibility to readout positive or negative charges
  - More functionalities for negative charges
- **12-bits ADC included.**
- One line to readout and digitize one PT100 temperature sensor.
- One single power voltage of 3.3 V.
- 16 mW power consumption, i.e. 1 mW per channel.

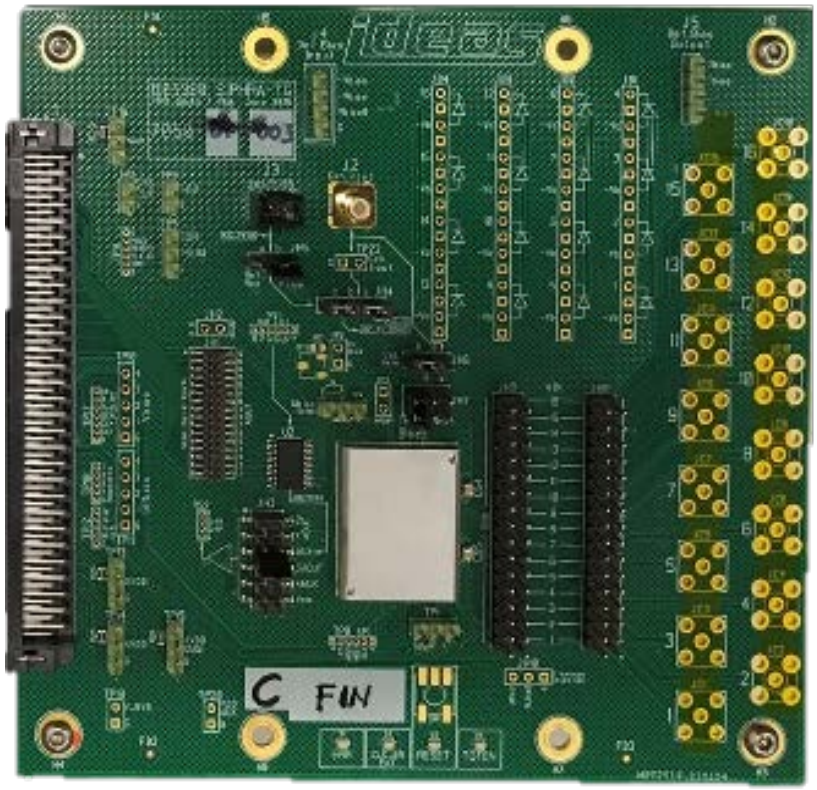


SIPHRA ASIC: block diagram



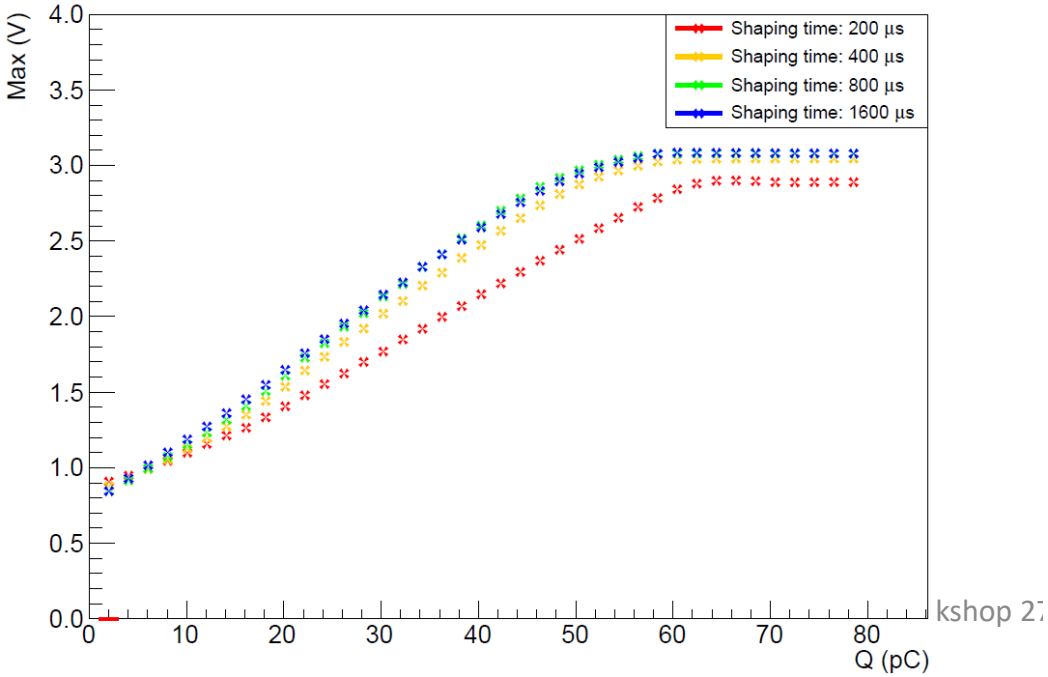
SIPHRA test board

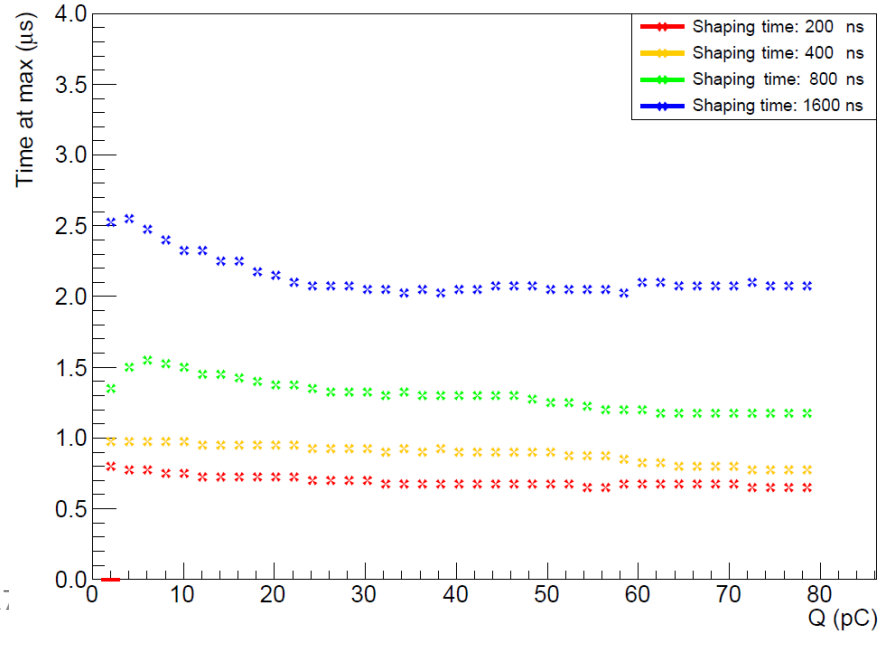
- Test board allows to test all functionalities of the SIPHRA chip.
- The SIPHRA needs to be bonded either for negative input charge, or for positive input charge.
- DAQ board developed at UniGE.
- IDEAS has implemented a ZIF connector for our MPPC board.
  - ➢ We can use the test board as a front-end development board.



SIPHRA tests: gain calibration

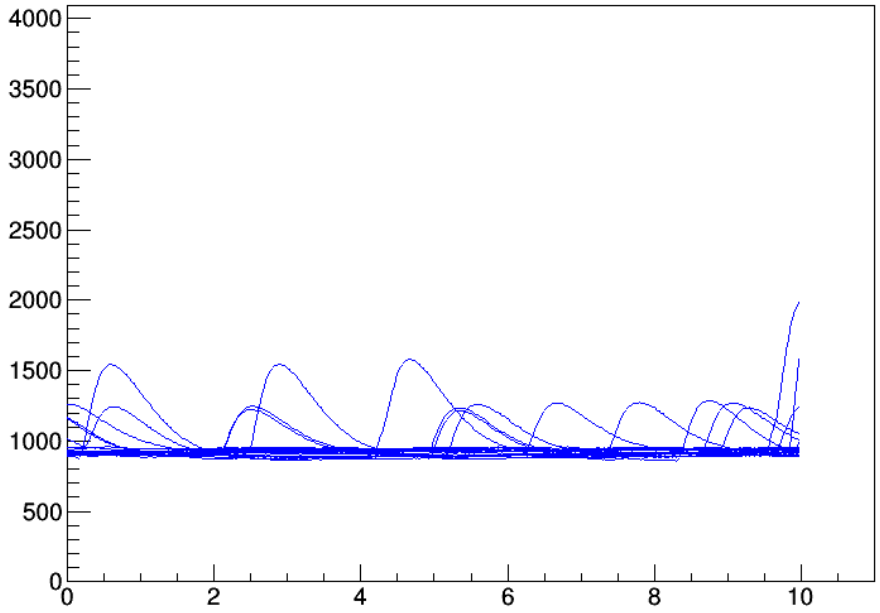
- Gain calibration tests have been done to study the various gain and shaping time settings of the SIPHRA.
  - A test charge is sent to one of the 16 channels, and the time response of the channel is recorded during a 10 µs time interval (25 ns sampling).
  - The maximum values as well as the peaking time are computed.

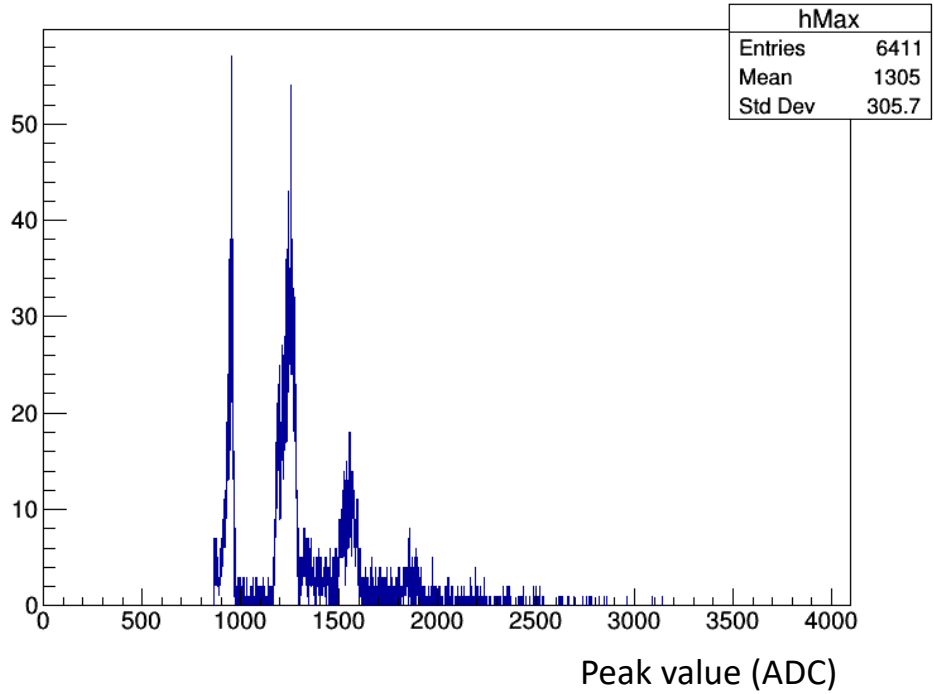




SIPHRA tests: signal sampling with SiPM

- A SiPM array is connected to the test board.
- The time response of a selected channel is recorded during 10 μs with 25 ns sampling.
- Maximum value of signal is recorded.





Comments

Next steps:

- Beam test from April 11th to April 18th
  - First tests with SIPHRA ASIC, in parallel with VATA front-end.
  - Various SIPHRA configurations will be tested, in particular the internal ADC mode will be studied.
- Production of new modules, to prepare the space qualification of the design.
- Prepare a front-end with 6 VATA HDR 64 (to readout three SiPM arrays).
- Prepare a front-end with 6 SIPHRAs (to readout 96 channels).