Brief Introduction To MOSFET Device

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MOSFET : metal-oxide-semiconductor field-effect transistor

Si 基绝缘栅场效应晶体管(IGFET)

The most important class of FETs: the Si-based insulated-gate field-effect transistor (**IGFET**) is the origin of the term metal-oxide-semiconductor field-effect transistor, or **MOSFET**.

For ease of fabrication and reproducibility, however, a current practice is to use degenerately doped polycrystalline Si (poly-Si), which is highly conductive, instead of metal for the gate. In n-channel devices, n+ poly-Si is used for the gates, and p+ poly-Si is used for p-channel devices.

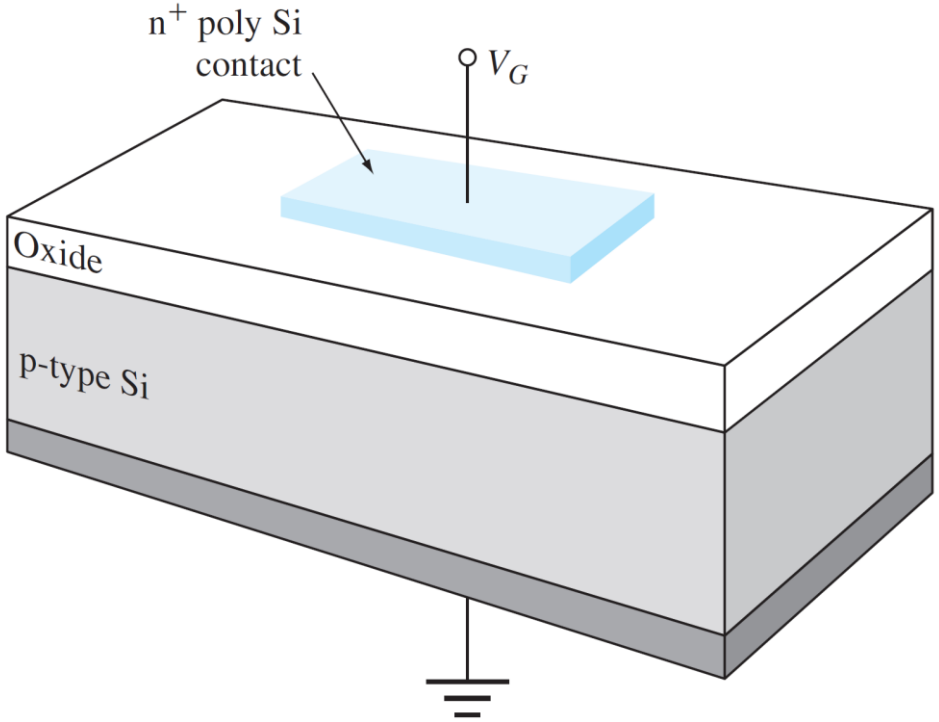
Although the term **IGFET** is a more accurate description , the practice common in the industry is to use the more common term **MOSFET** to describe this class of devices.

The basic principles of the MOSFET

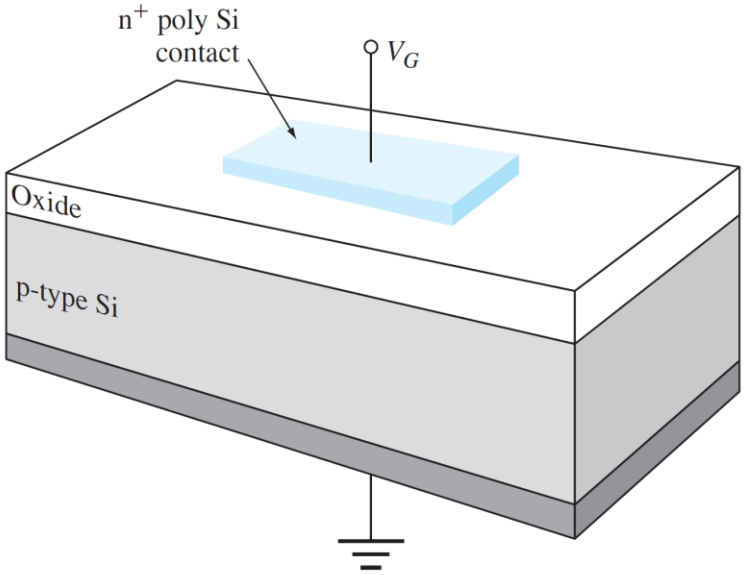
- **MOS capacitors:** MOS电容

To illustrate how the **MOSFET** channel is formed, a brief qualitative description of **MOS capacitors** is presented.

Consider an ideal MOS capacitor (**MOSC**) with the structure of Figure. This capacitor consists of a degenerate n+ Si gate, a thin layer of (insulating) oxide separating a gate from a p-type substrate.

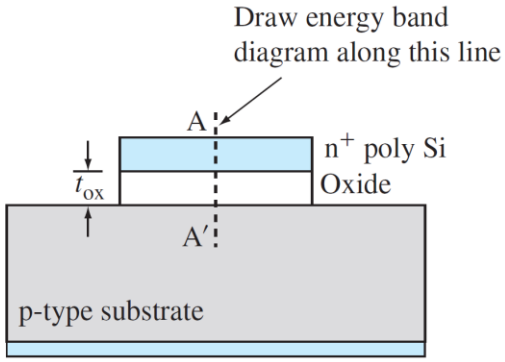


重掺杂n+材料-绝缘氧化层-p型硅基底结构致使p型硅基底中出现了弱反层，即表现为n型硅。



(a)

physical structure of an n+-Si/oxide/p-Si MOS capacitor

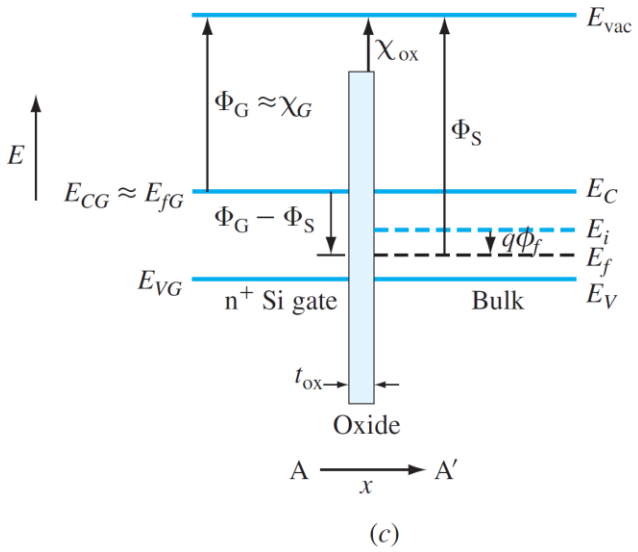


(b)

cross section

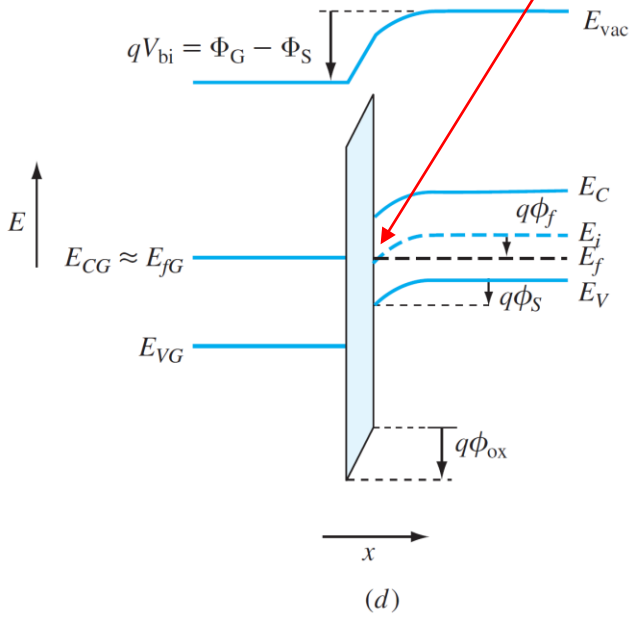
Note that the surface of the p-type substrate near the oxide interface has become weakly inverted!

弱反型



(c)

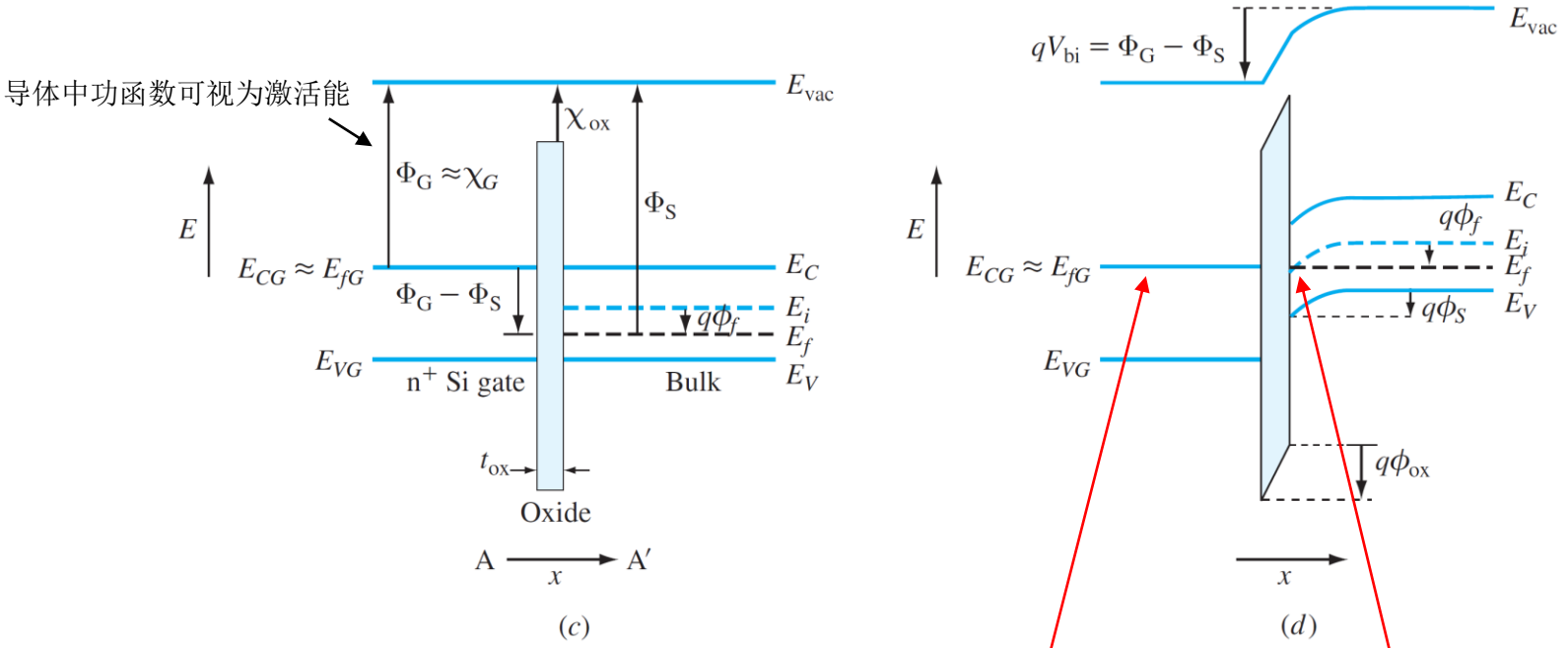
the energy band diagram under charge neutrality



(d)

the energy band diagram at equilibrium

two heterojunctions 异质结
*one between the polysilicon gate and the insulator
*another between the insulator and the semiconductor substrate.

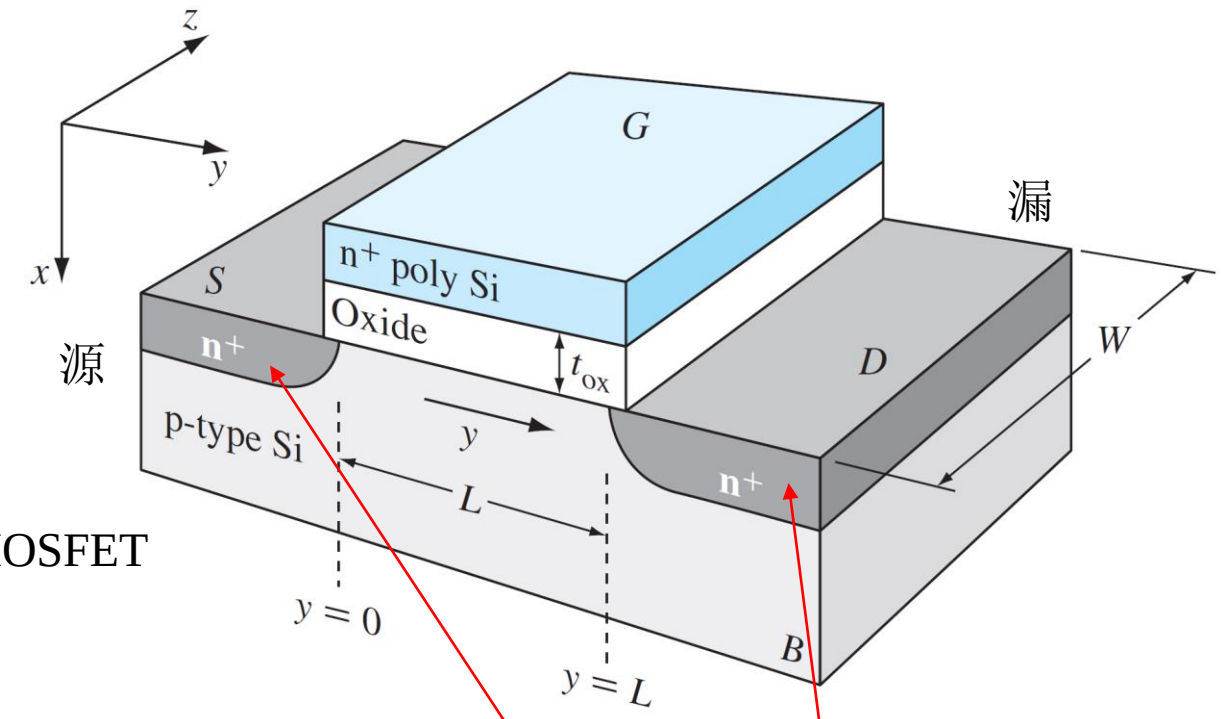


To achieve equilibrium, electrons flow (through an external circuit) from the gate to the semiconductor substrate, causing the Fermi levels to line up. The resulting (equilibrium) energy band diagram is shown in **Figure d**. We see that the bands bend, and a built-in voltage results. Some of the voltage is dropped across the oxide and some across the semiconductor. Furthermore, the bulk semiconductor now has a depletion region near its surface—it is depleted of majority carriers, which are holes in this case, since the material is p type.

The total built-in voltage is

$$V_{bi} = \frac{\Phi_G - \Phi_S}{q} = \phi_{ox} + \phi_S$$

- **MOSFET:**



n 沟硅基MOSFET

A schematic of an n-channel MOSFET is shown in Figure . It resembles the MOS capacitor just discussed except that there are source and drain regions of n+ Si at opposite sides of the gate region. Since electrical connections are made to gate, source, drain, and substrate, a MOSFET is a **four-terminal** device. Often, however, the substrate is connected to the source, and the MOSFET is then considered to be a three-terminal device. The symbols W and L represent the width and length of the channel.

- **MOSFET at equilibrium**

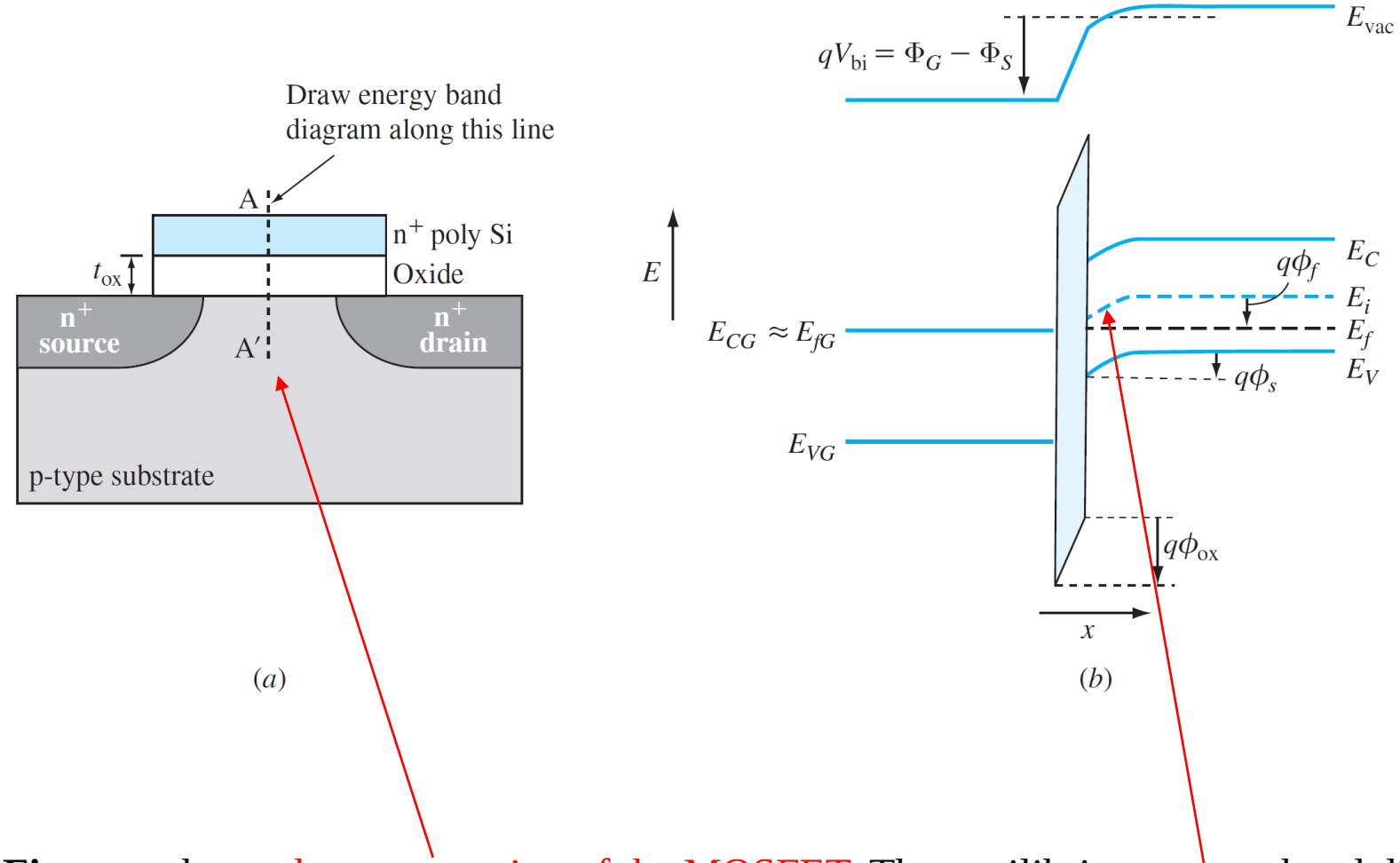
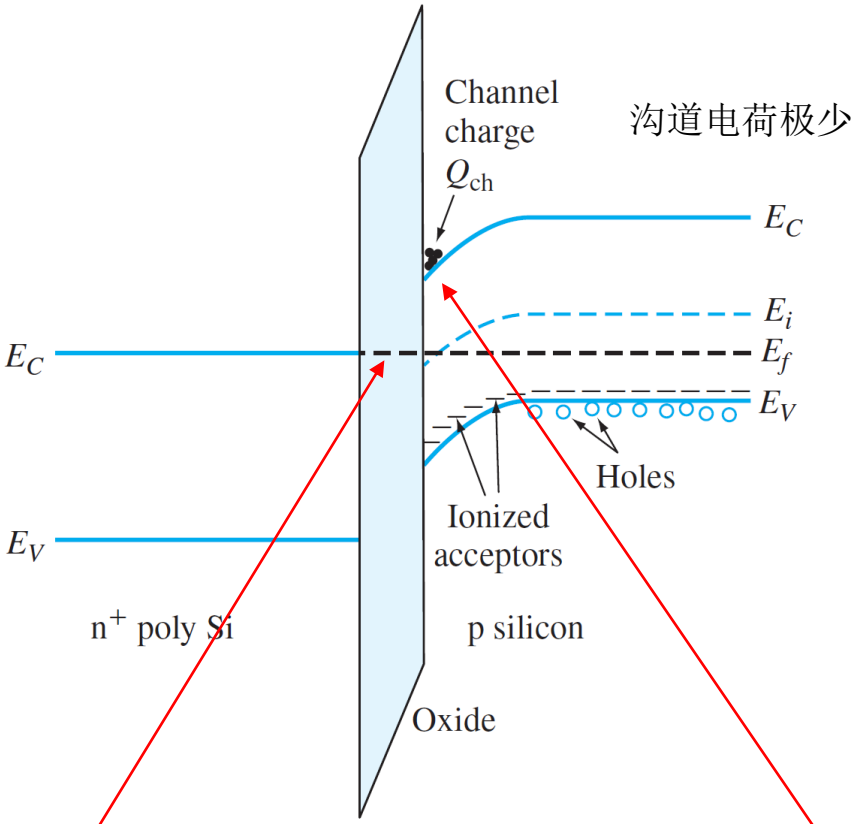
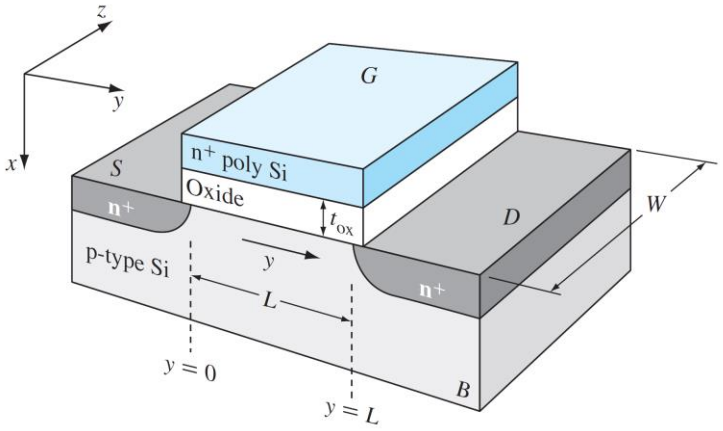
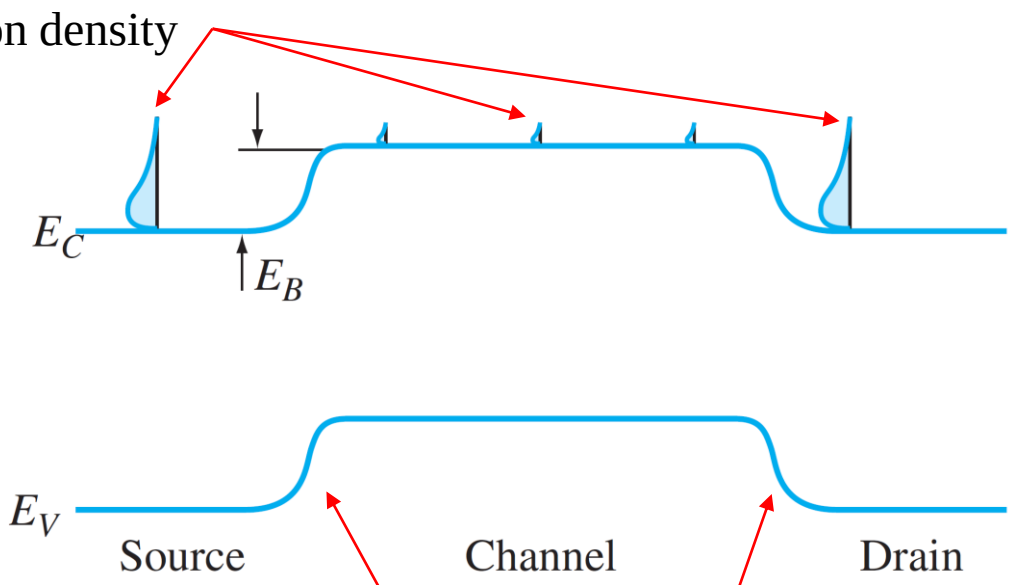


Figure a shows the cross section of the MOSFET. The equilibrium energy band diagram along the cut A-A' normal to the gate is shown in **(b)**. From the figure, it appears as though there is no n-type channel from source to drain in this device. From the energy band diagram for this structure, we can determine whether a channel in fact exists.



The equilibrium energy band diagram of Figure(b) on last page is repeated in Figure on this page, which also indicates the charge in the Si. It can be seen from the figure that the Fermi level is still close to the intrinsic level near the semiconductor-oxide interface. In other words, while a channel does exist, it has a low conductance, since it contains few electrons. Because the electron concentration in the channel is so low, for an applied drain-to-source voltage, only a miniscule current can flow between source and drain. This device is said to be in the subthreshold region.（亚阈值区或亚阈值态）





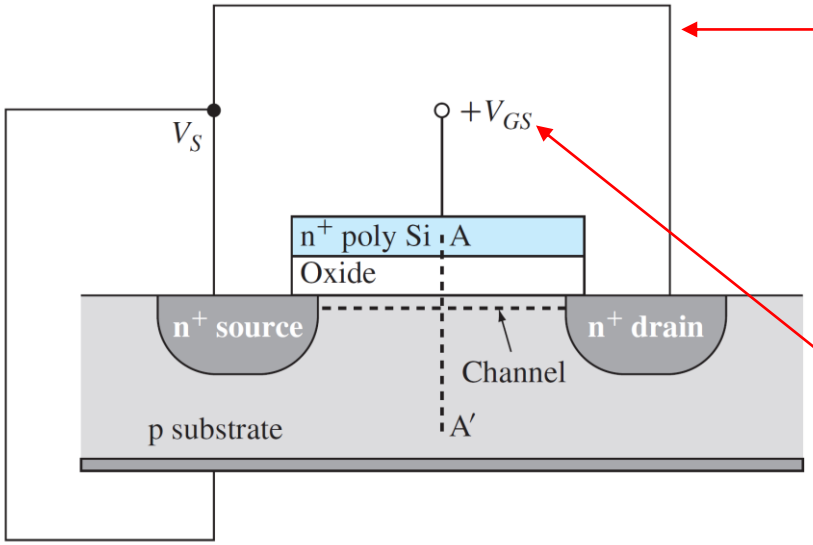
正如上一张PPT给出，由于沟道中的电子浓度太低，源和漏之间可以视为不导电。

The source and drain are doped n+, but the induced channel is only weakly n type. The resulting difference in the electron concentration creates a modest (n+n) potential energy barrier at either end of the channel. Figure shows the equilibrium energy band diagram along the channel instead of across it. Since the electron density function $n(E)$ decreases exponentially with increasing energy, the barrier E_B is still large enough that only a small electron concentration exists in the channel.

Thus, the induced channel is n type but the channel conductivity is negligible.

In the next page, we will see how changing the gate voltage affects the barrier height and thus the channel conductance!

- **MOSFET not at equilibrium（Under bias）**



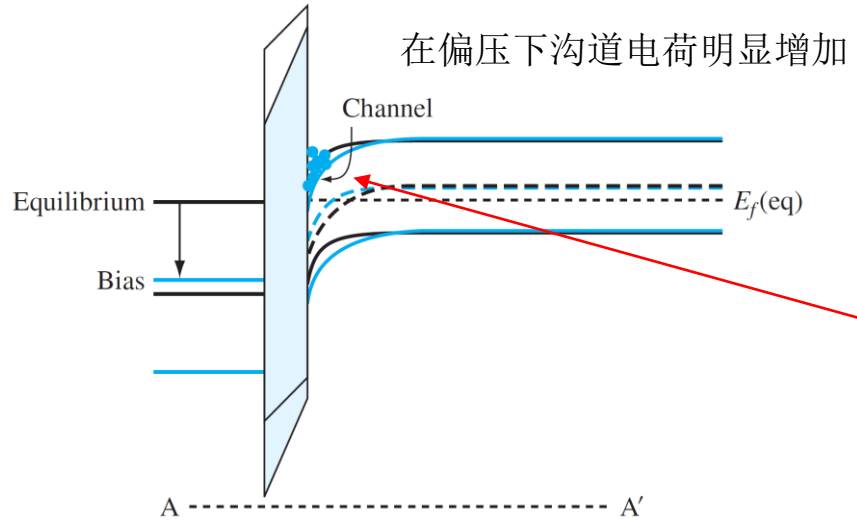
(a)

In here , just only consider the case for $V_{DS} = 0$

*the gate-source voltage V_{GS} and the drain-source voltage V_{DS}

Connect the source to the drain electrically, such that those two terminals are at the same potential, as shown in **Figure (a)**

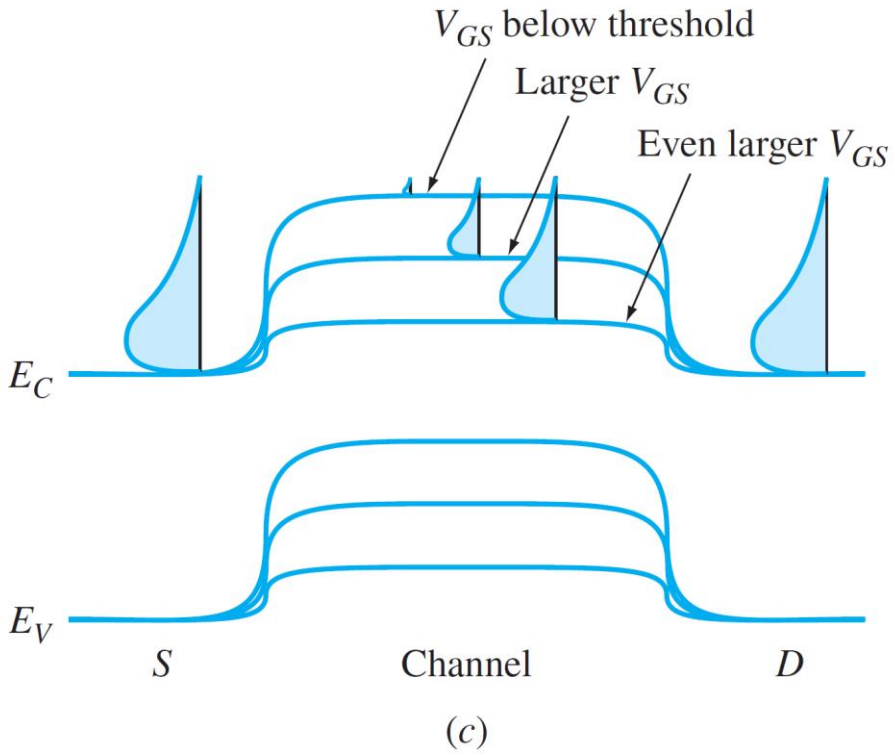
The effect of applying a positive gate voltage is to lower the channel energy



(b)

Under bias, the conduction band edge bends down toward the Fermi level. The surface is now more strongly n type than before, and thus more strongly inverted. There are now more electrons in the channel, increasing its conductance.

The channel has been “enhanced!”

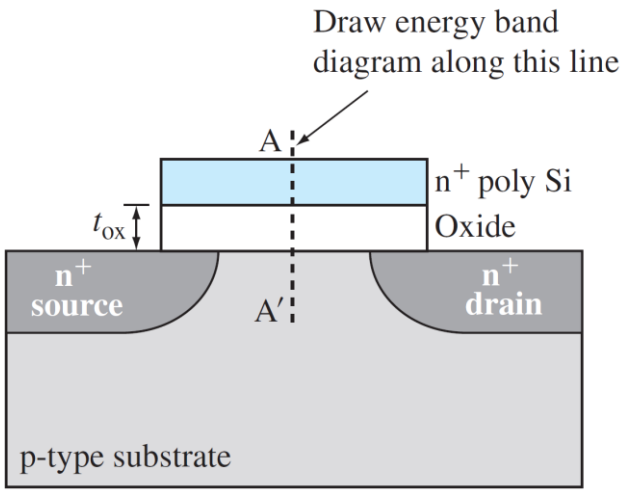


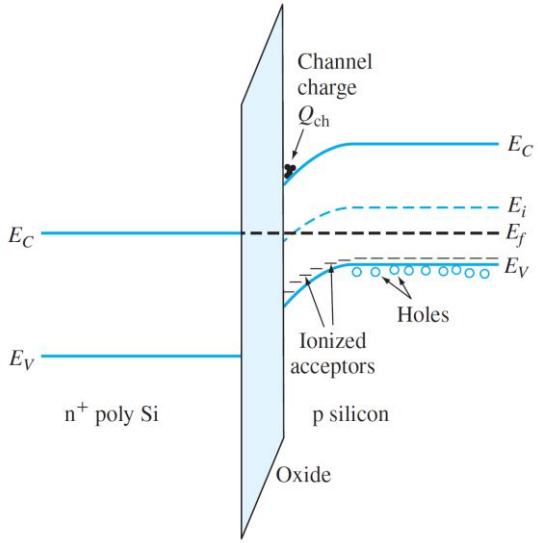
偏压下由于沟道中的电子浓度大幅增加，源和漏之间可以导电。

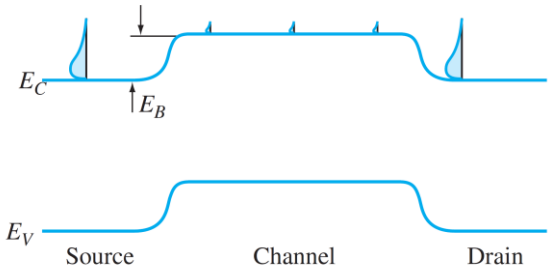
Another way to look the **Figure (c)**, which shows the energy band diagram along the channel for three different gate voltages.

For V_{GS} near threshold, the energy barrier between source and channel at the Si surface, E_B is fairly high. Few electrons appear in the channel and its conductance is low.

As V_{GS} increases above threshold, the barrier decreases. More electrons are able to enter the channel, and thus its conductivity increases.

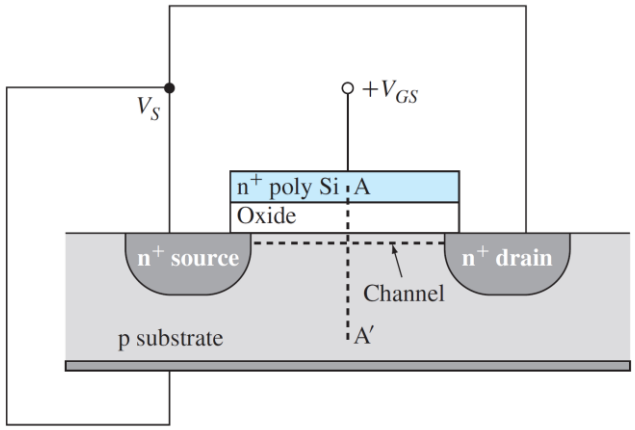


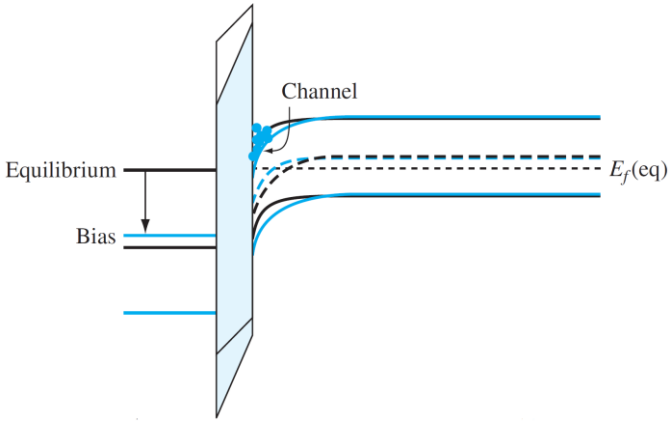


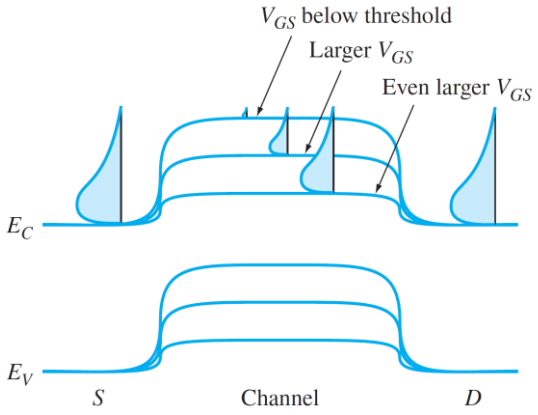


MOSFET at equilibrium

MOSFET under bias







- **CMOS : complementary MOSFETs** 互补型 MOSFET - CMOS

Currently, most integrated circuits use both n-channel and p-channel devices, hence the term complementary MOSFETs, or CMOS.

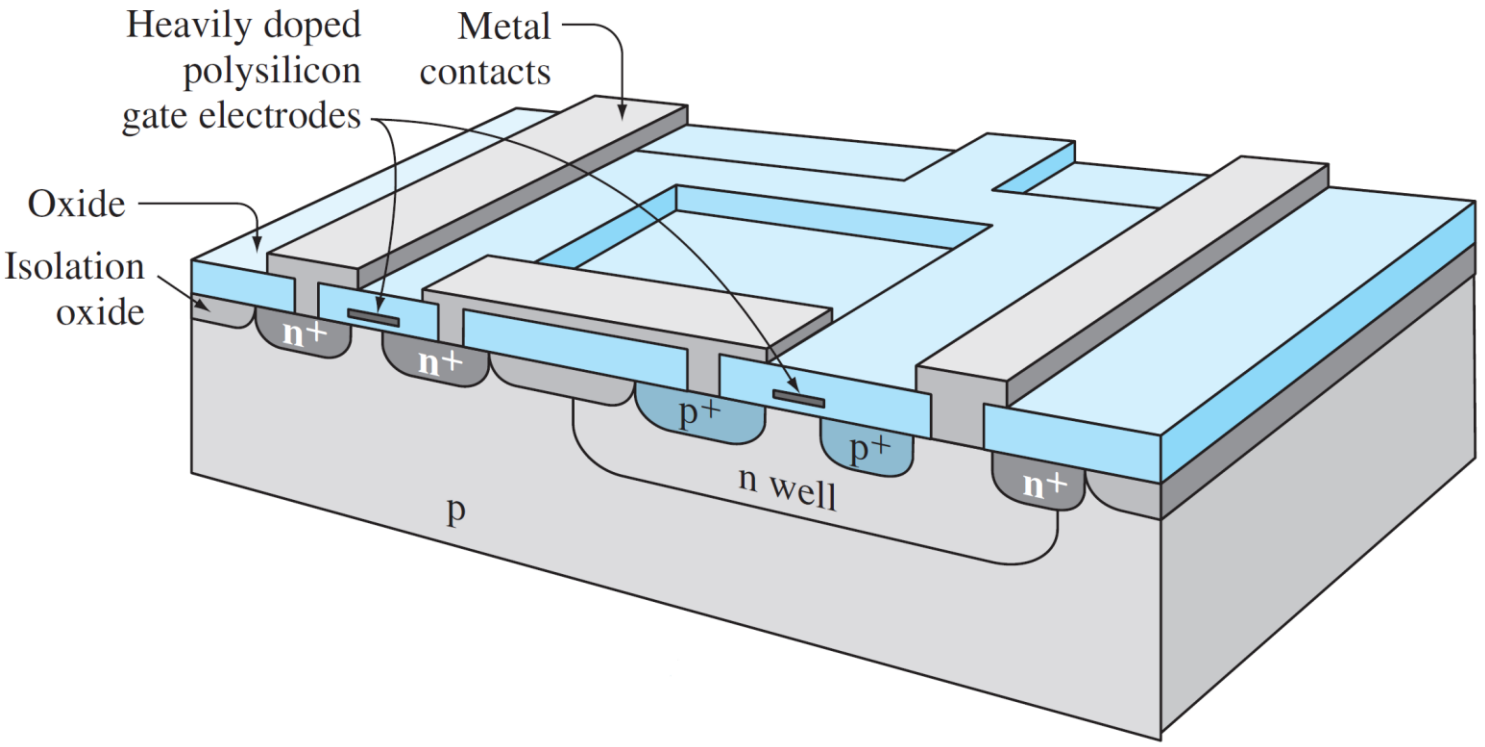


Figure shows the schematic cutaway view of a CMOS inverter using the so-called n-well technology. **The n well is ion-implanted into a p-type substrate.** The p-channel device is fabricated in the n well while the n-channel FET is fabricated directly into the p substrate.

Thanks !

Ref:

[1]Fundamentals of Semiconductor Devices 2nd Edition (auth.)-Betty Anderson -McGraw Hill Education Publishing (2017)
[2]Evolution of Silicon Sensor Technology in Particle Physics 2nd Edition (auth.)-Frank Hartmann -Springer International Publishing (2017)