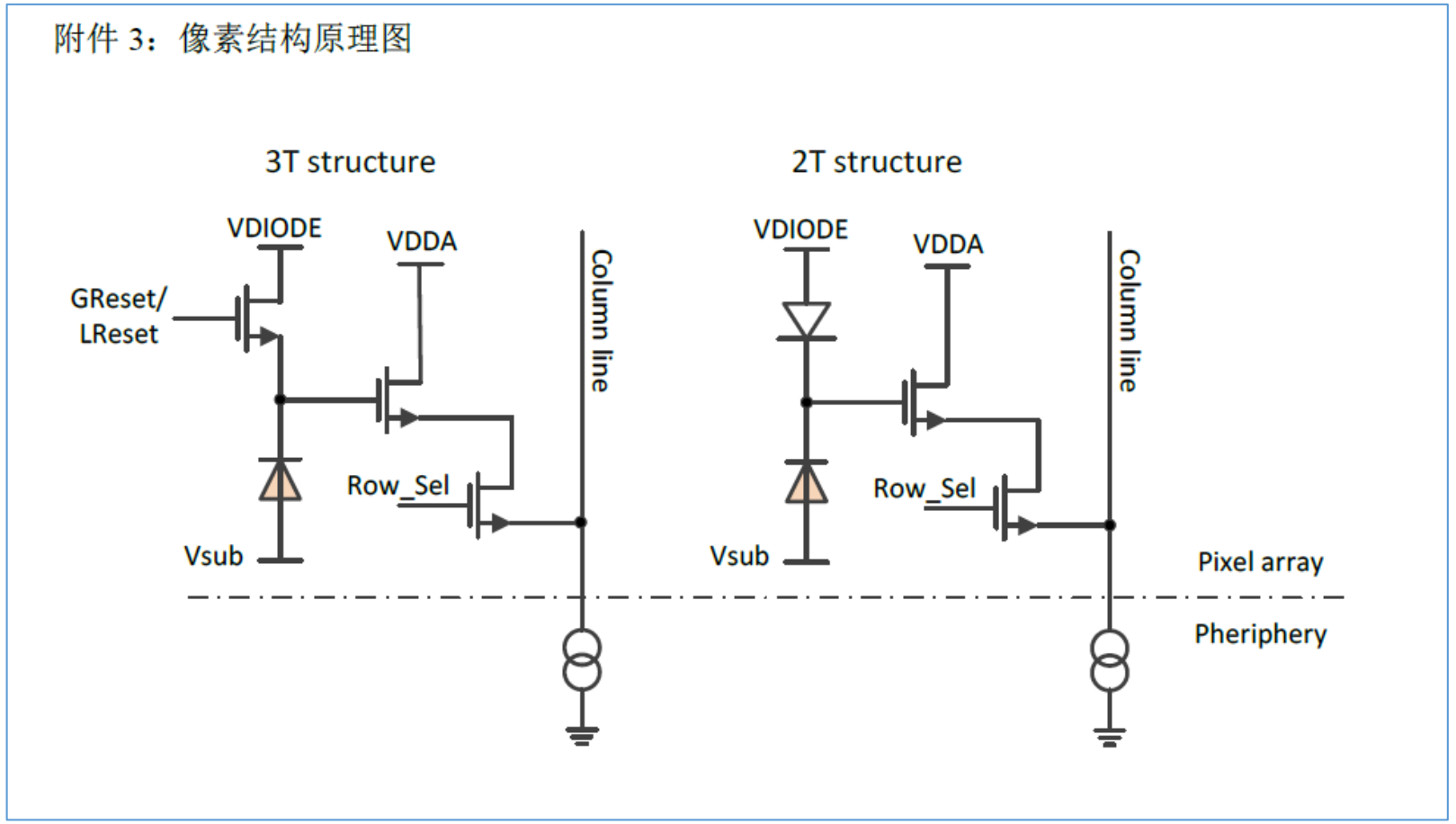
Some tips regarding the CMOS circuit

-- Based on my personal learning (&knowledge) to understand the function of the JadePix1

Special topic @ 05/11/2018

From the manual of CPS (JadePix1)



Topic 1 What is 2/3/4 T?

-- Number represents the number of transistor (MOSFET) in the APS (per pixel)

-- Tips: Active pixel sensor (APS) <==> Passive pixel sensor

<-- Amplified the signal via a transistor or not

[Reference]

“Design and Implementation of a CMOS imager with active column for SPR-based sensors”, by Arnoldo Salazar Soto

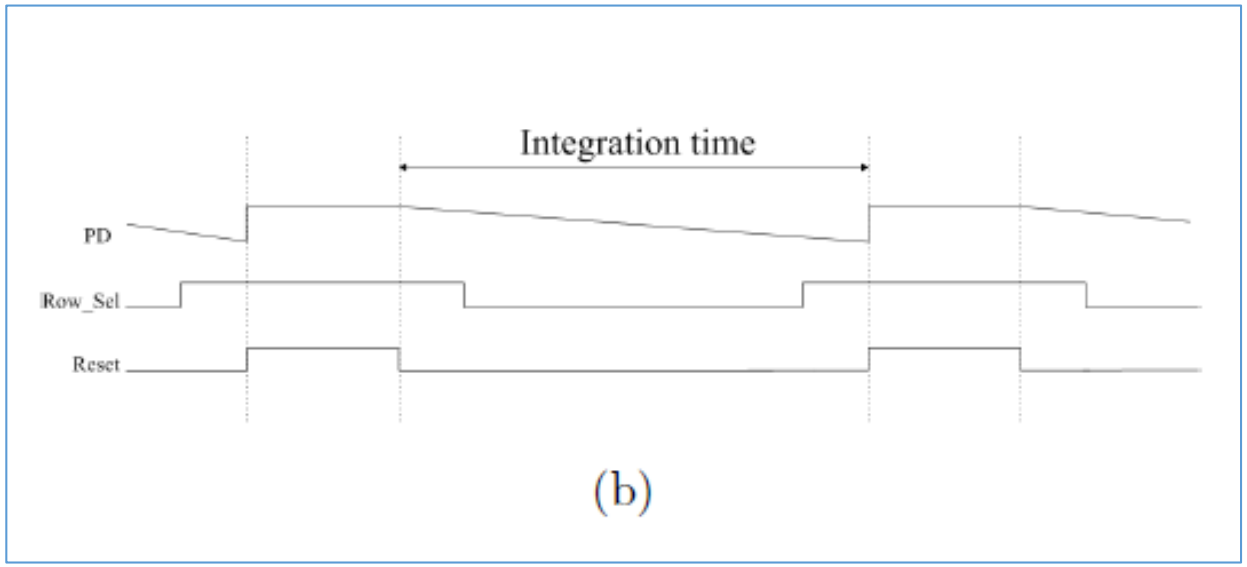
“CMOS Image Sensors: Electronic Camera-On-A-Chip”, by Eric R. Fossum, IEEE Transactions on Electron Devices, Vol44, No. 10, October 1997

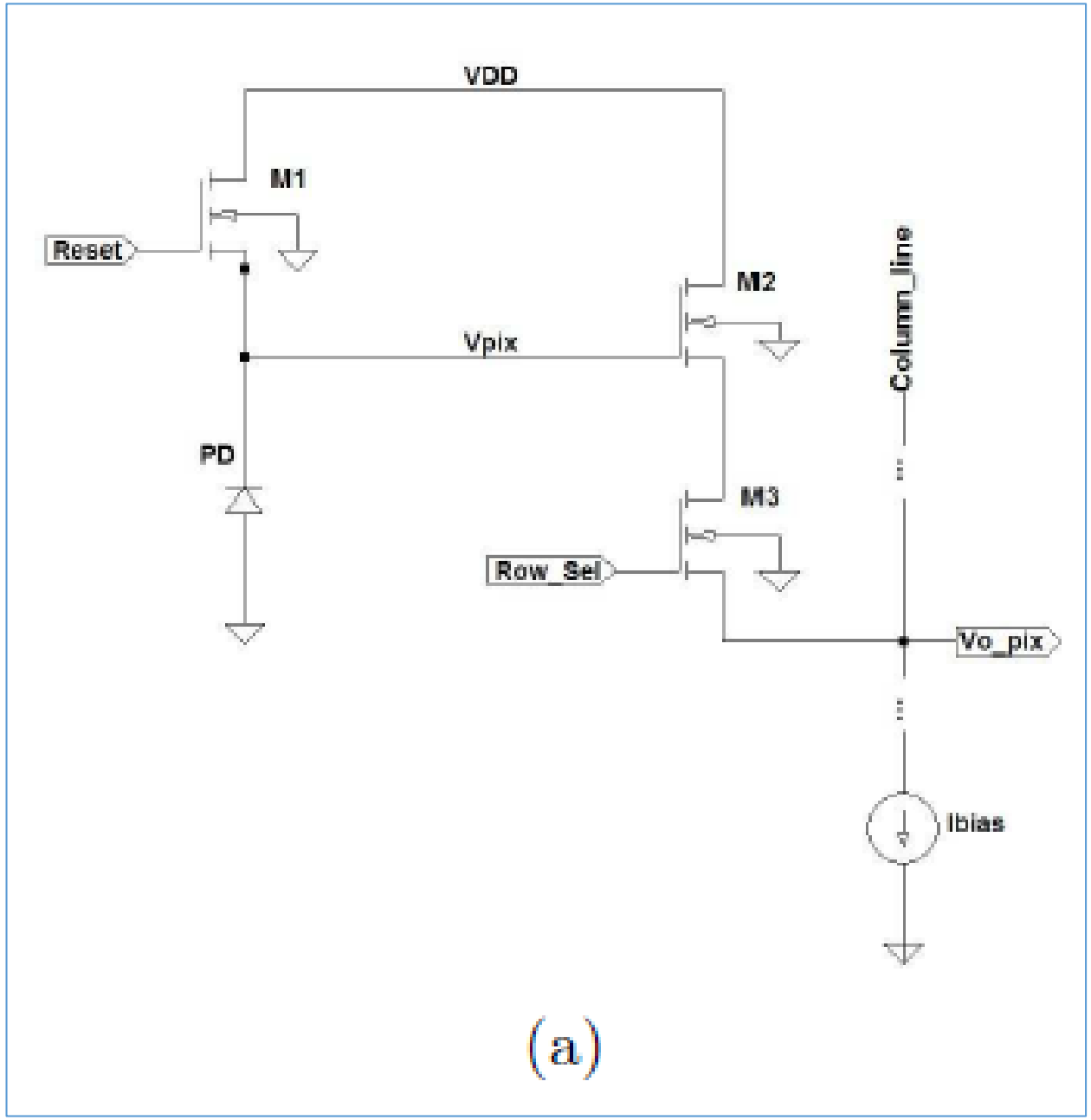
“Advanced Pixel Architectures for Scientific Image Sensors”, by R. Coath et al.,

Three Transistor Active Pixel Sensors (3T-APS)

-- Reset --> “reset noise”

-- Row Selection





Explanation of the 3T operation

3.3.1.1 3T-APS

The simplest APS configuration is the three transistor pixel (3T-APS), presented on figure 3.8, its operation is as follows:

1. The cycle starts when the row select transistor (M3) is turned on (selecting all of the pixels of a same row of the matrix). If implementing a noise reduction circuit, such as double sampling, it is required to access the pixel before reset, thus ROW_SEL is activated slightly before M1 is turned on in order to read the signal at the end of integration time.

2. The reset transistor (M1) is then turned on to take the photodiode to a known voltage in order to begin integration. For the configuration of figure 3.8a this reference voltage is $V_{DD} - V_{th}$, where V_{DD} is the supply voltage and V_{th} is the MOSFET threshold voltage. Advance reset techniques looking to reduce the image lag and reset noise have been developed, such as active reset [27] and flushed reset [28] among others. The reset and select transistors if possible should have minimum dimensions in order to maximize the pixel's fill-factor.

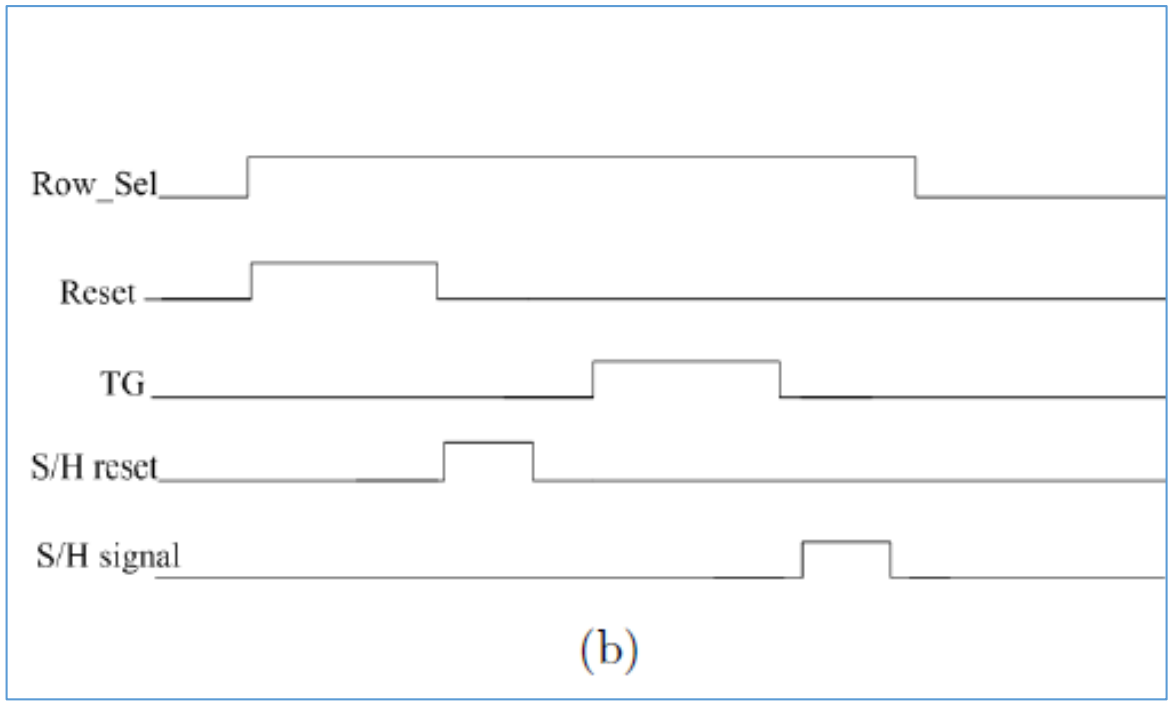
3. Integration starts when the reset transistor is turned off. During this integration time, the photogenerated charge discharges the sensing capacitor. The drop in the voltage at the sensing node (Vpix) of the photodiode is proportional to the incident light as described by equation 3.16.

4. When the row select signal is active, the source-follower (SF) transistor M2 buffers the photodiode voltage to the pixel's output $V_{0,pix}$. The source-follower requires a current sink, usually shared per column. Since the SF is inside the pixel, if possible its size is kept at a minimum .

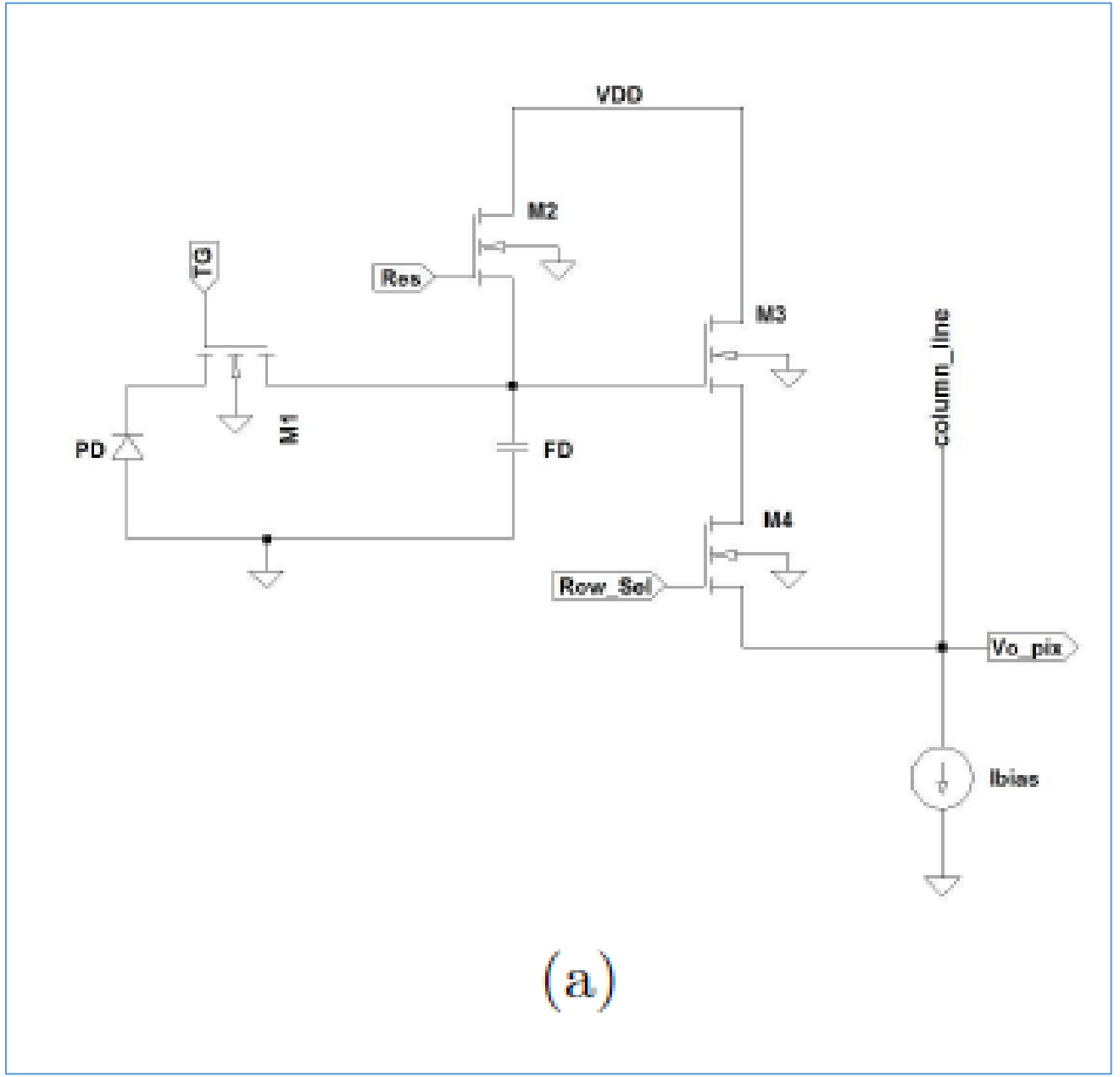
Four Transistor Active Pixel Sensors (4T-APS)

-- Enabling double sampling to cancel such as “reset noise”

-- Better S/N owing the smaller capacitance of FD



(b)



(a)

Explanation of the 4T operation

3.3.1.2 4T-APS

This configuration solves some of the issues with 3T-APS by separating the photodetection and photoconversion regions (figure 3.9). The accumulated charge is transferred to a separate node, known as floating diffusion (FD), where the carriers are converted to voltage. One extra transistor must be added to transfer the charge from the photodiode to the FD. Its operation is as follows:

1. Assuming initially no charge on the photodiode, slightly before the charge transfer the FD capacitance is reset through transistor M2.
2. The reset value is read and the select transistor (M4) activated.
3. After reset readout, the signal charge accumulated in the PD is transferred to the FD by turning on the TG signal on transistor M1, then this new signal is read.
4. This process is repeated periodically reading the signal charge and reset charge.

So that, how about the 2T ?

-- I do not accumulate the information yet

-- But it is clear that there is no “reset”

==> It would mean that the reference voltage is recovered by CR-RC circuit with a time-constant (therefore, it should be long)

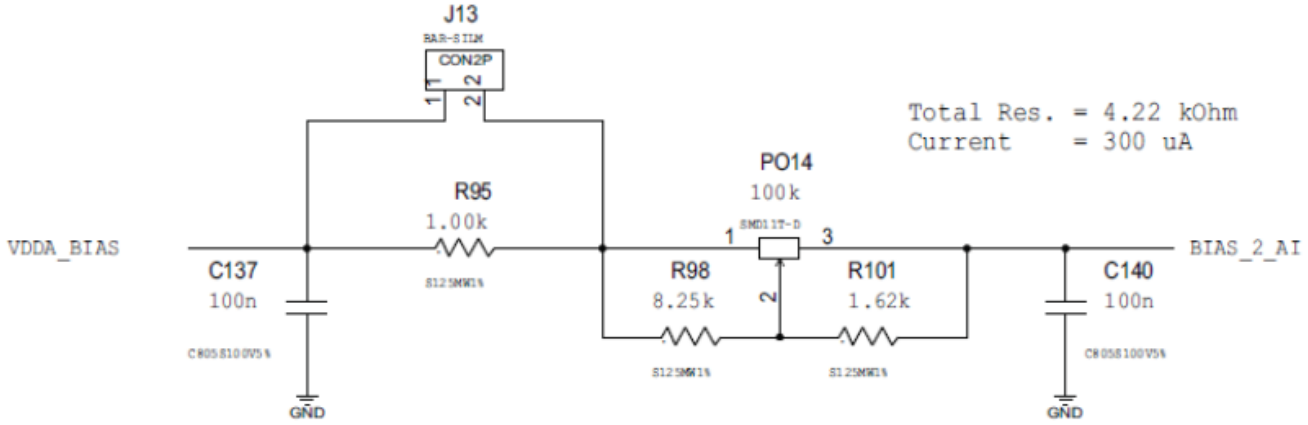
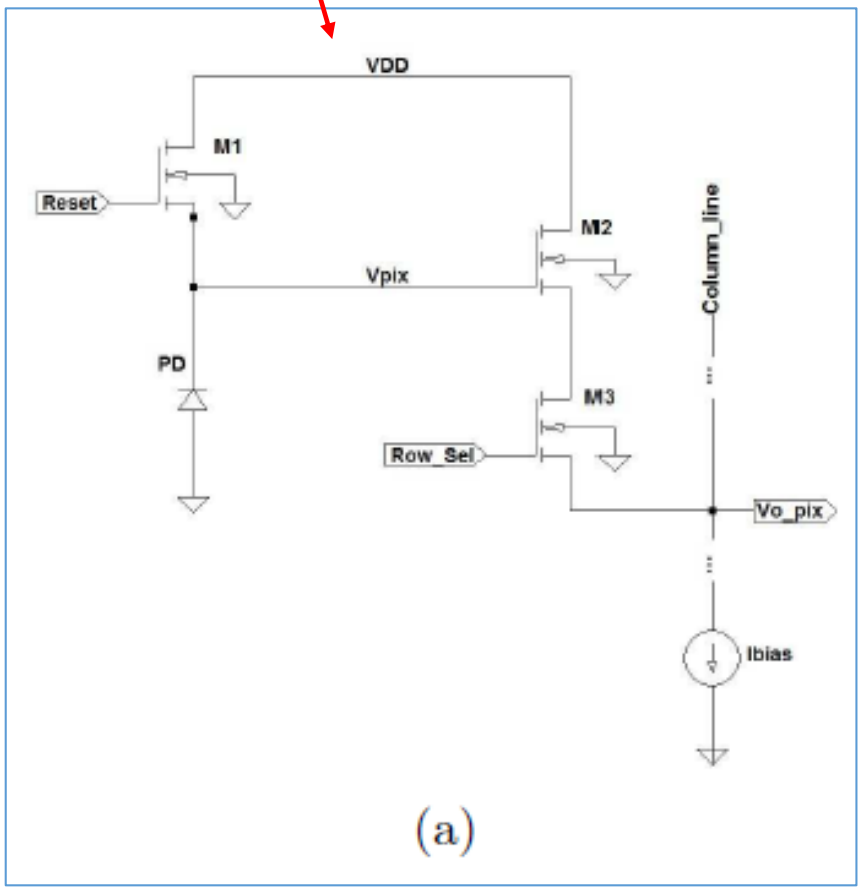


图 2. 参考电流偏置产生原理

Topic 2

Why there is PMOS transistor ?

Only for this circuit, 3 NMOS are enough . . .



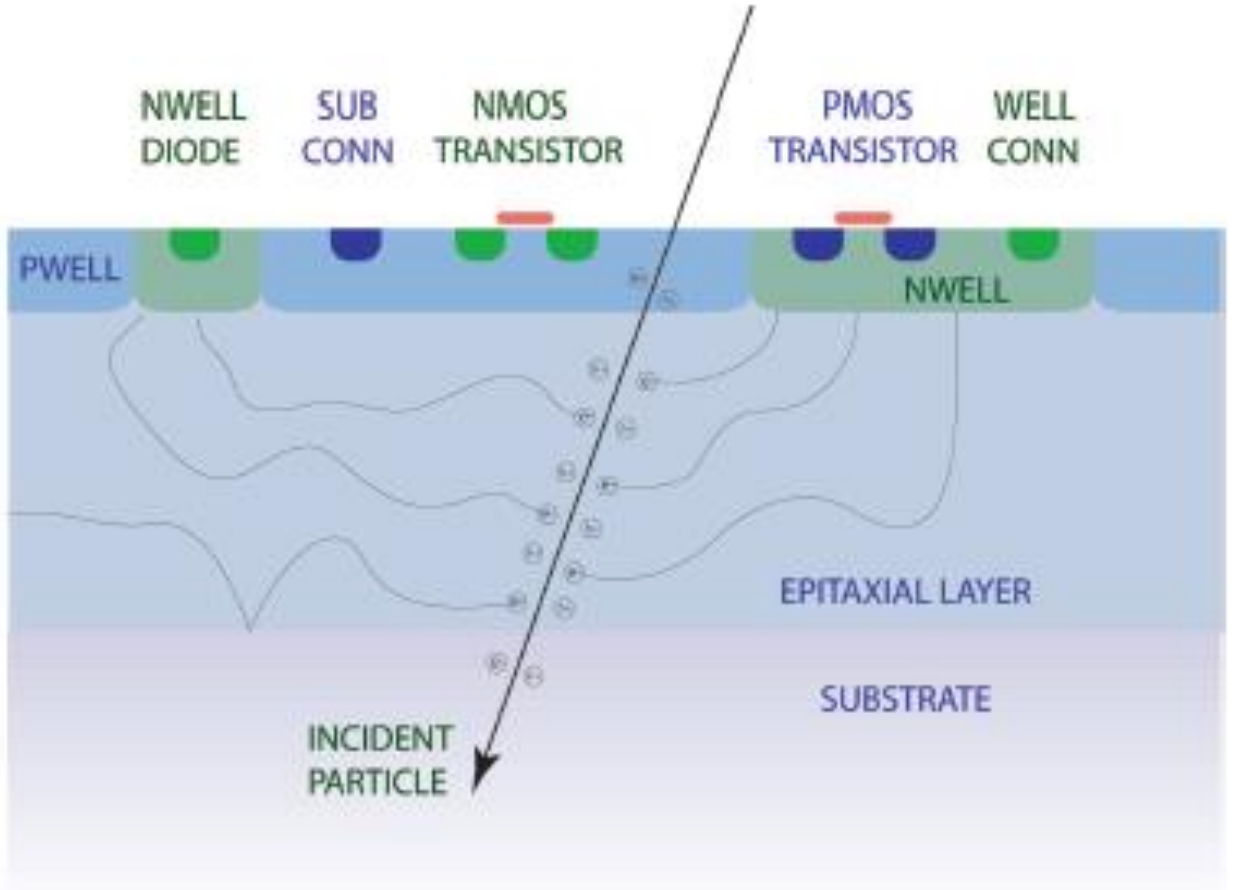


Figure 1: Cross-Section of a Typical CMOS Pixel

Example : Inverter Logic

-- Something we learn as an introduction of CMOS circuit

-- Many functions are realized with this complemental parts. However, I do not know how it function for current JadePix1 ..

Layout

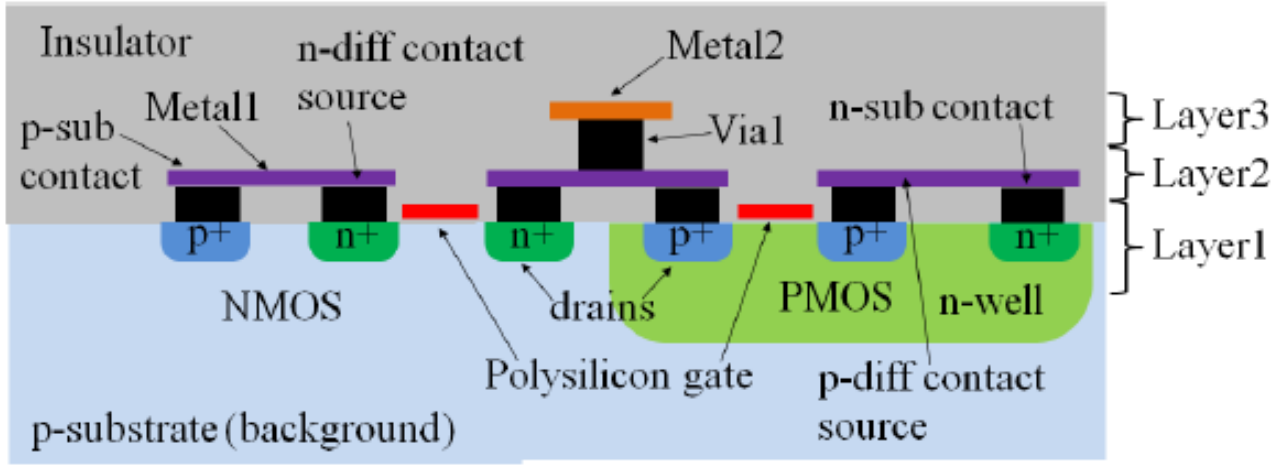


Figure 3.5: Cross-section view of a CMOS wafer.

Circuit

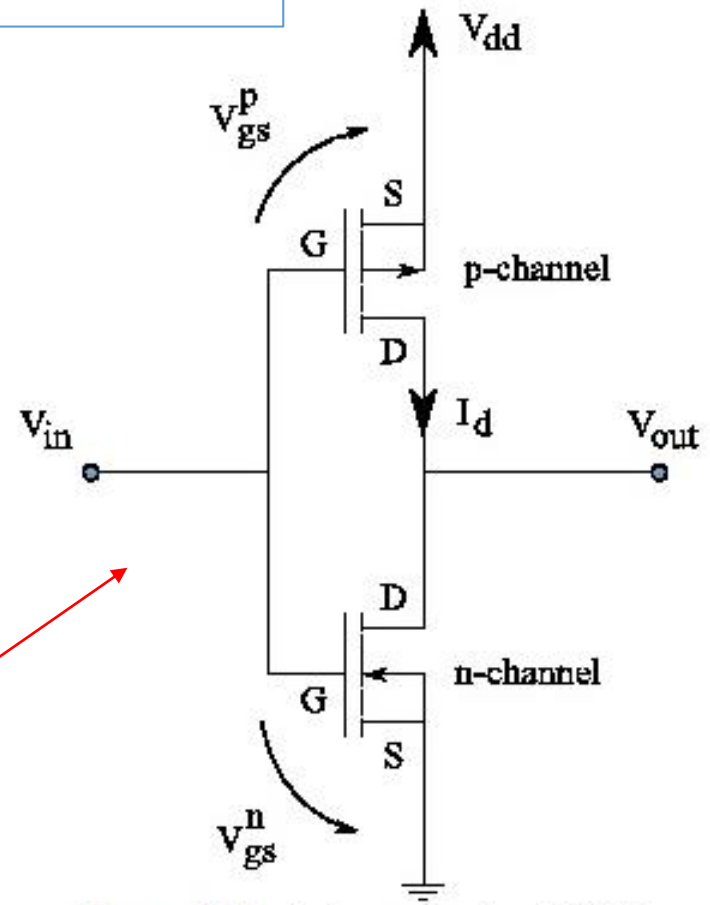


Figure 7.11: Schematic of a CMOS inverter circuit. In the stationary case the circuit does not consume any power when assuming perfect devices without leakage current. NBT stress is imposed on the p-channel device at $V_{in} = V_{low}$.

Topic 3

Pixel Size

For example, 0.25 μm process
==> size ~ 0.25*20 = 5μm ^{2}

Pixel Layout and Pixel Size

- Pixel size mostly determined by
  - Contact size
  - Poly-gate to contact spacing
  - Metal to metal spacing
- 20F for 4T cell
- 13-16F for 3T cell