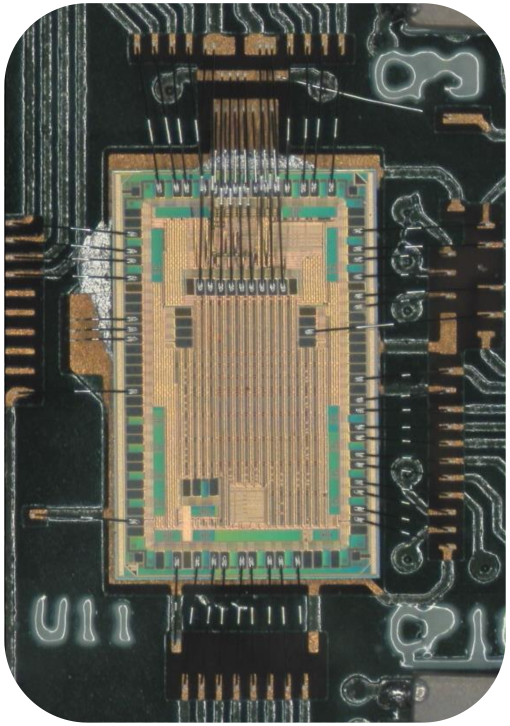
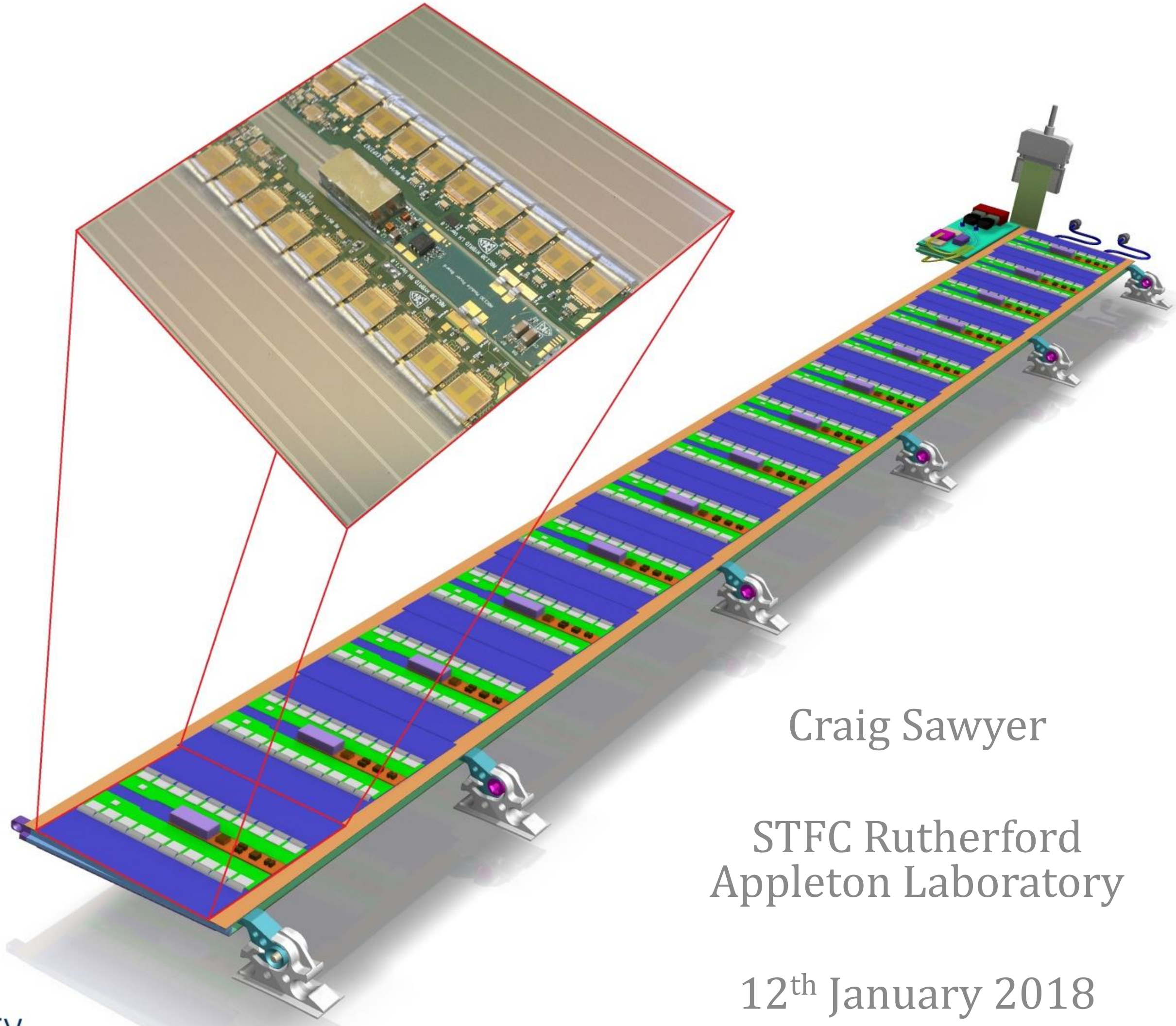
BUILDING THE NEXT GENERATION OF SILICON STRIP DETECTOR

MODULE, STAVE AND PETAL ASSEMBLY FOR THE ATLAS ITK STRIP DETECTOR





ATLAS EXPERIMENT

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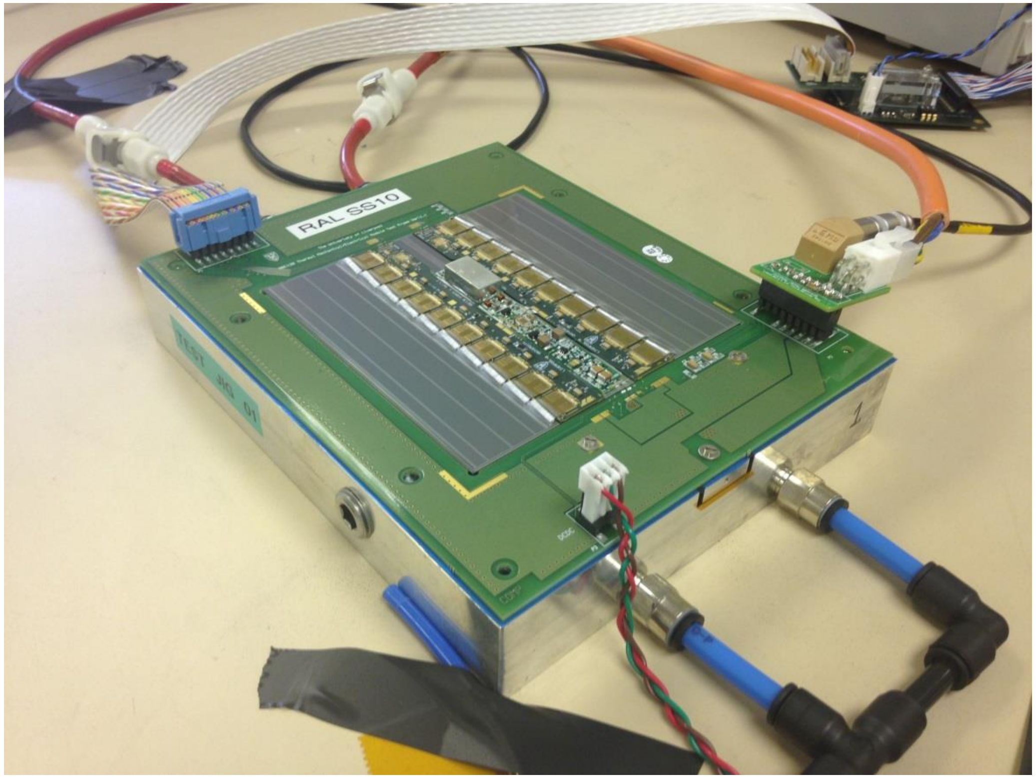
12th January 2018

Science & Technology Facilities Council
Rutherford Appleton Laboratory

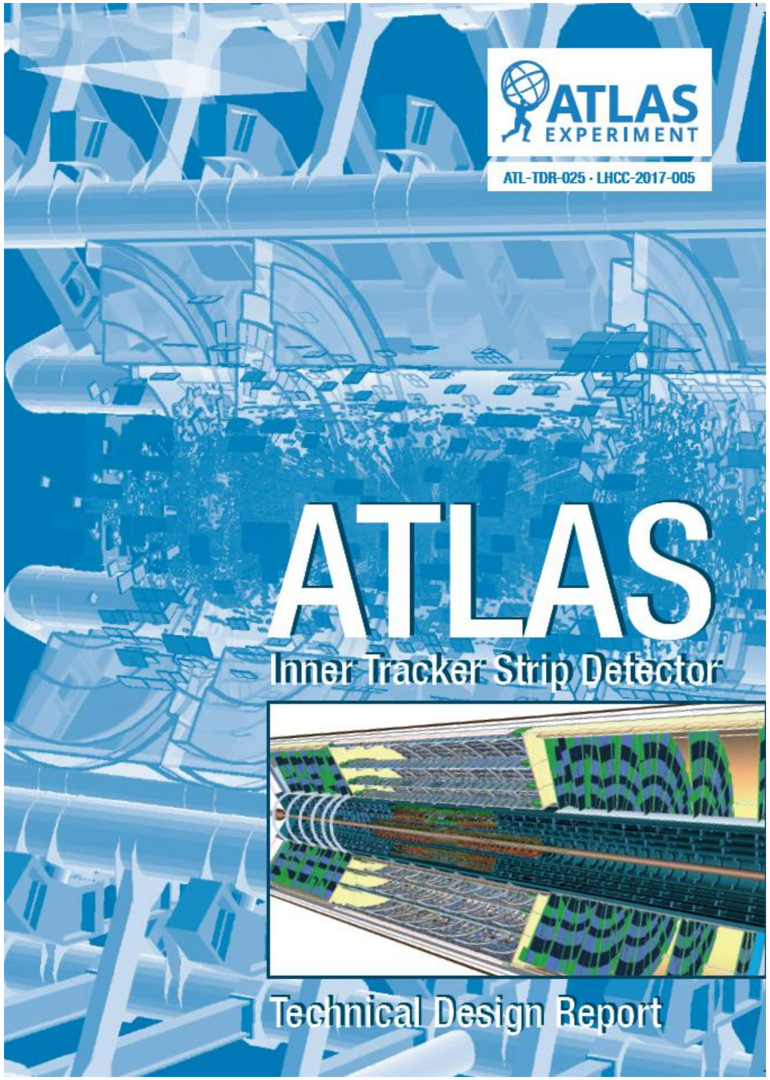
Outline

- Introduction
- LHC Roadmap
- Phase-II Motivation
- ATLAS
- ITk Upgrade
- Strip Detector
- Sensors
- ASICs
- Modules
- Irradiation & testbeam
- End-of-life & noise
- Local supports & systems tests
- Coming soon…

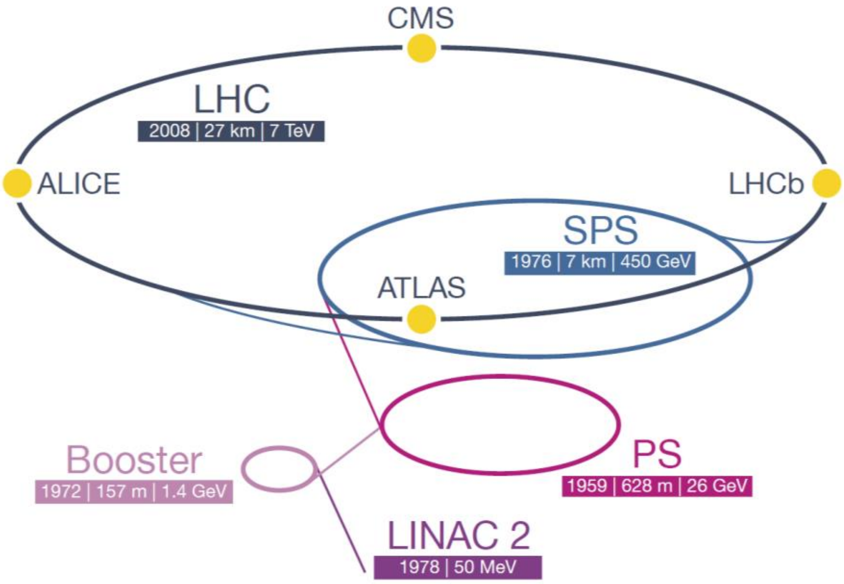


Introduction

- 2026 will see the start-up of an upgraded LHC (HL-LHC)
- In the preceding long shutdown (LS3) major experimental upgrades will be installed including a new all-silicon Inner Tracker (ITk) for ATLAS
- The Technical Design Report (TDR) of the strip part of this tracker was released in April 2017 [1]
- The pixel TDR has been submitted to LHCC review
- Today I will discuss where we are with the strip detector in terms of prototyping and also where we are (hopefully!) heading



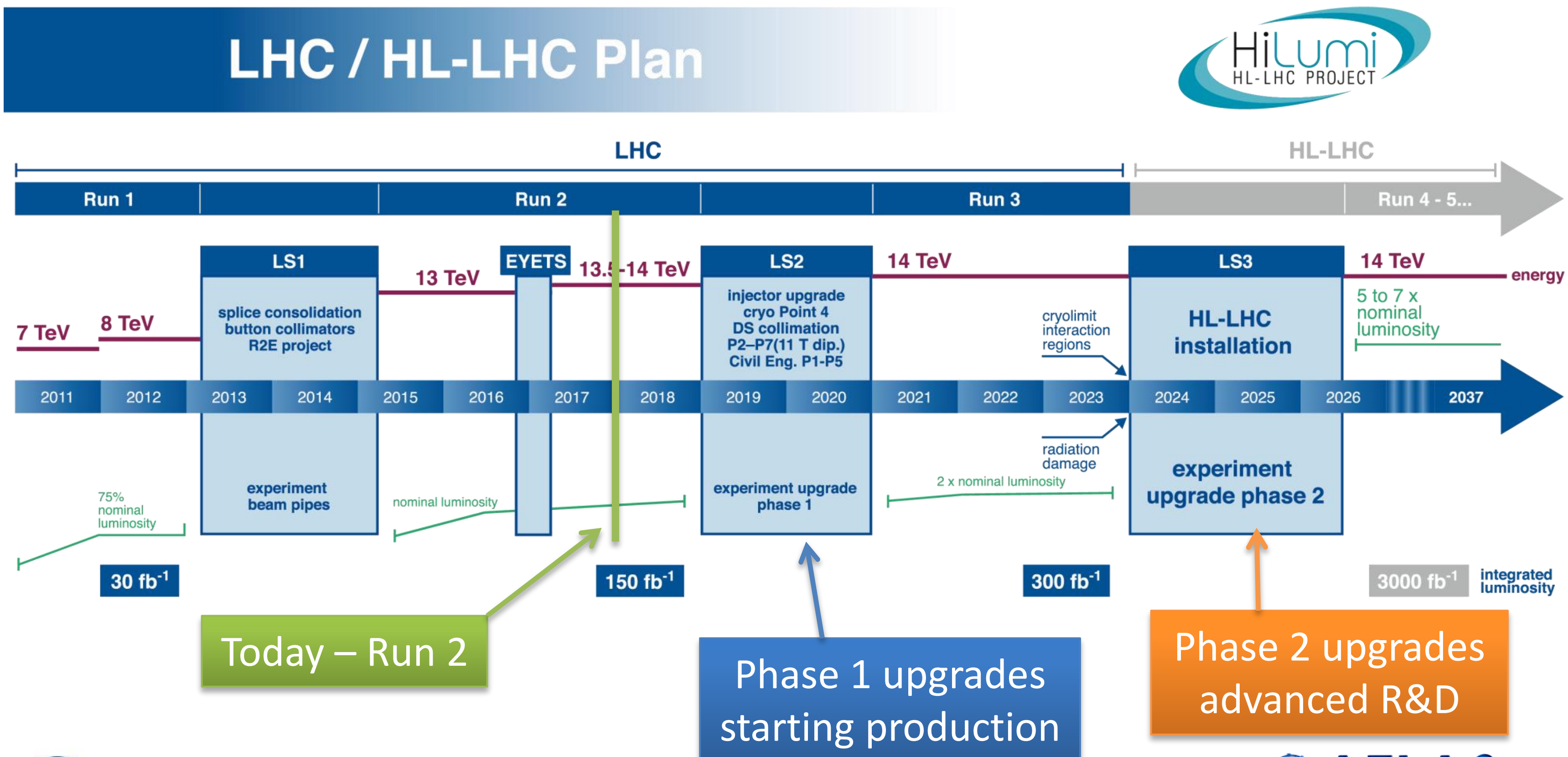
Large Hadron Collider (LHC)



- Worlds highest-energy particle collider
  - 27 km circumference
  - Max. $\sqrt{s}$ = 14 TeV
- Run 1:
  - $\sqrt{s}$ = 7 TeV in 2011
  - $\sqrt{s}$ = 8 TeV in 2012
- Run 2:
  - $\sqrt{s}$ = 13 TeV ongoing

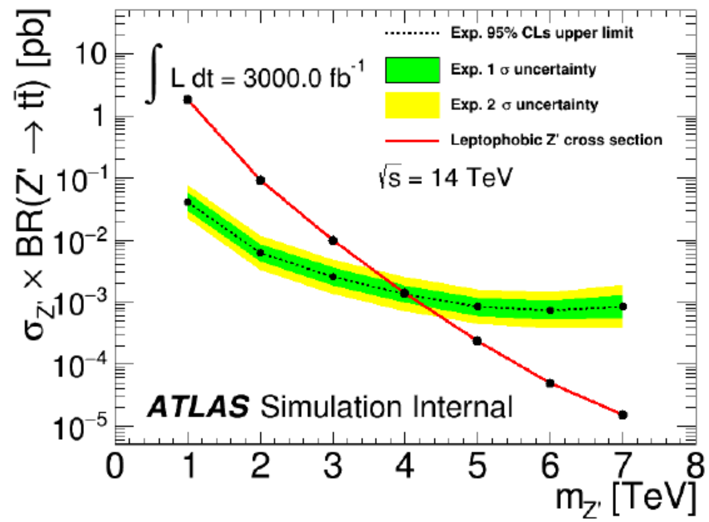
Future of the LHC

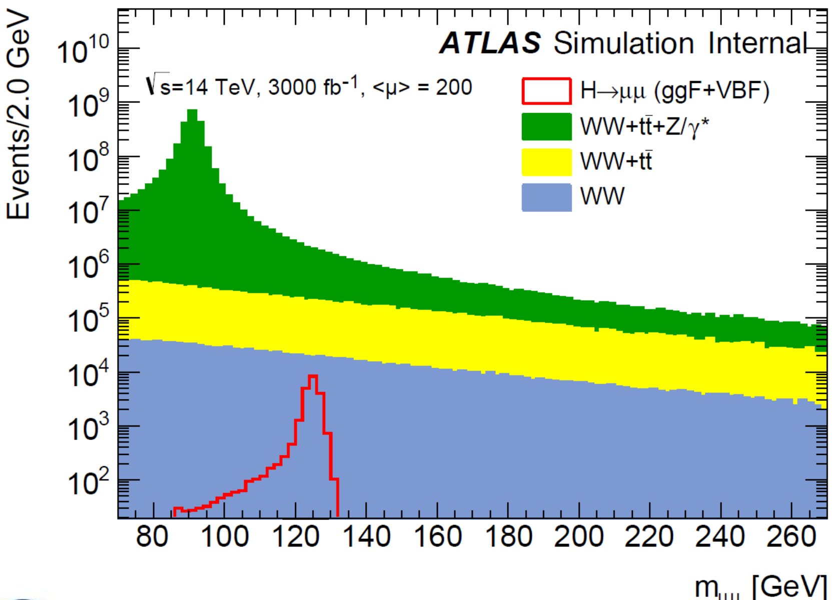
- Current LHC running continues until the end of 2023
- 2024-2026 sees High Luminosity LHC (HL-LHC) upgrade/installation
- At the same point experiments carry out “Phase 2” upgrades
- The rest of this talk will concentrate on the strip part of the new all-silicon tracker being installed by ATLAS in Phase 2

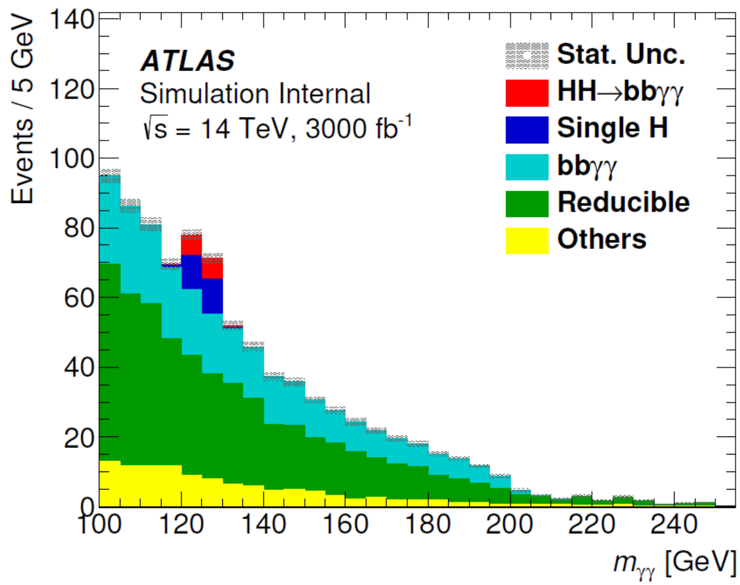


Phase 2 Motivation

- Physics motivations include:
  - Precision measurements
  - Searches for rare processes
  - Searches for additional Higgs bosons
  - Searches for exotic BSM particles

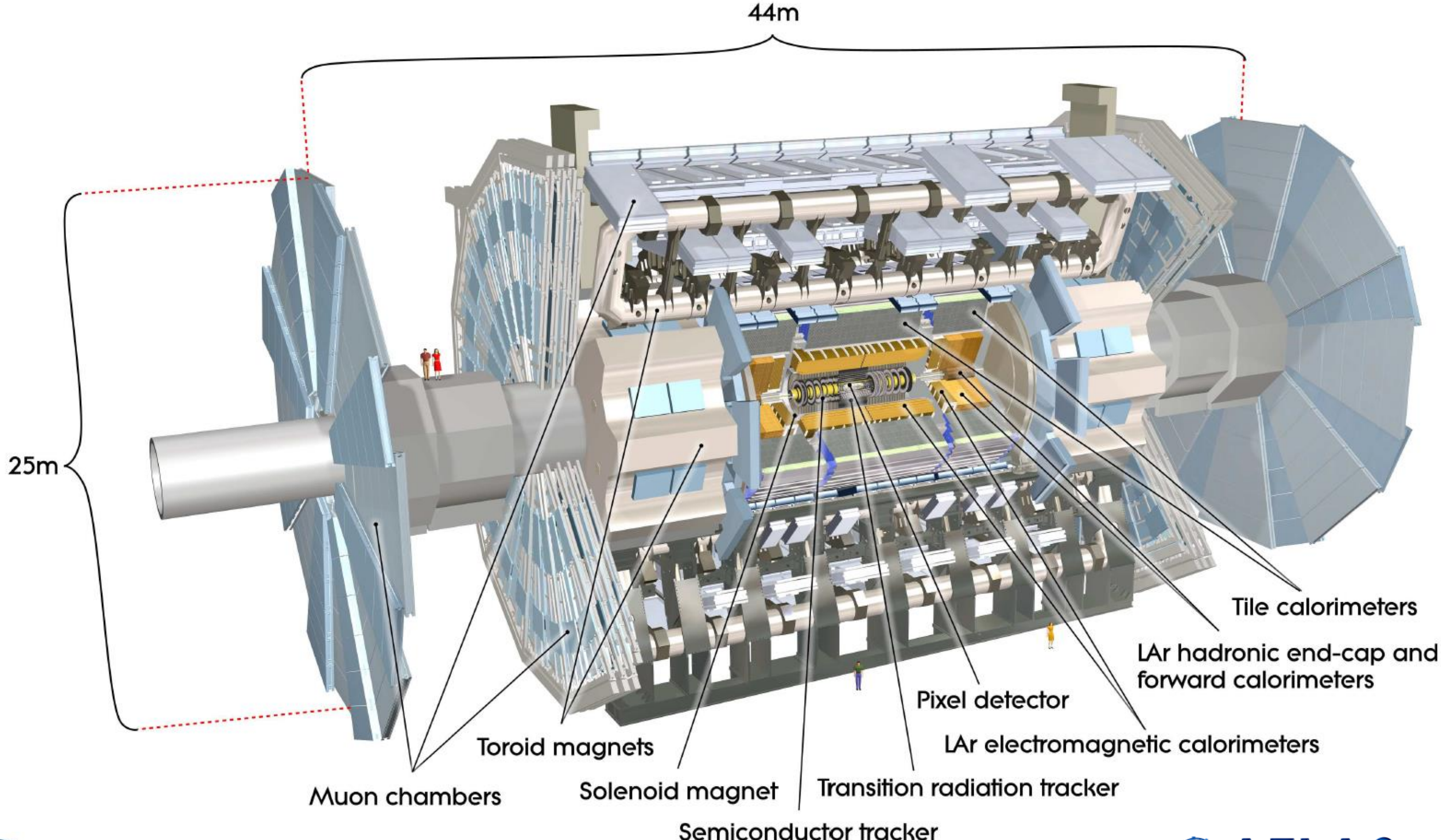






ATLAS Detector

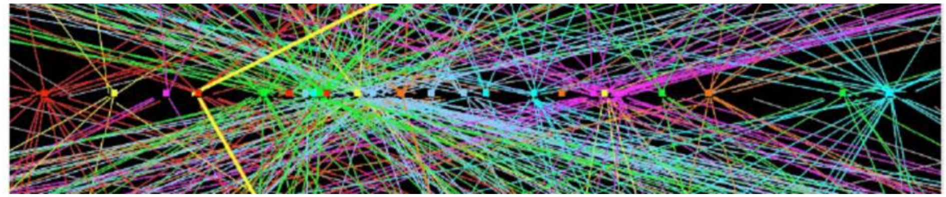
- 7000 ton general purpose detector
- 3000 physicists, 175 institutions, 38 countries



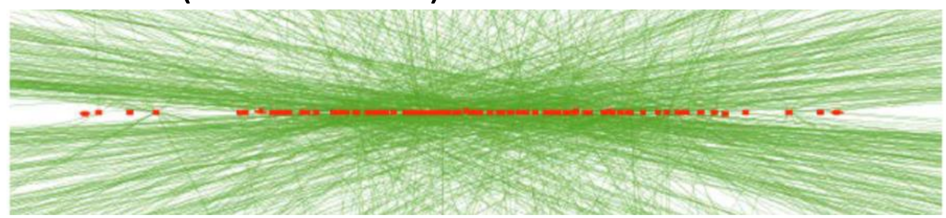
ATLAS ITk Upgrade

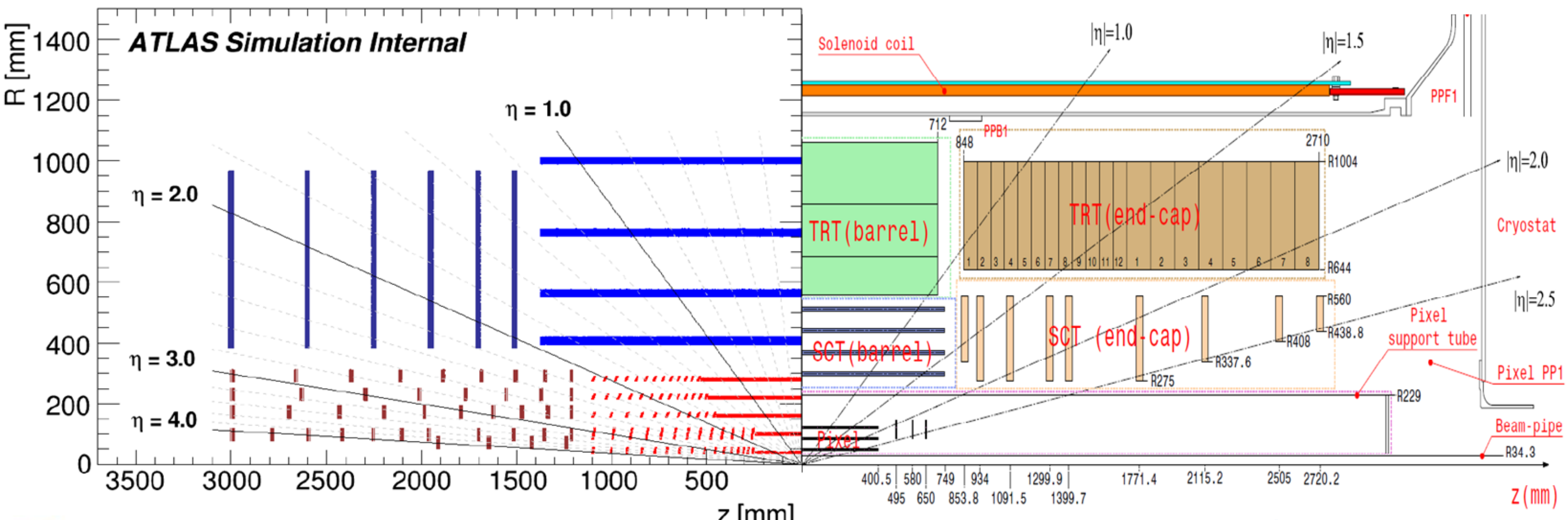
- Current ID [2] designed for:
  - 400 fb^{-1} (PIX), 700 fb^{-1} (SCT), 850 fb^{-1} (IBL)
  - $\mu = 50$ ($L = 2 \times 10^{34}\ cm^{-2}s^{-1}$)
- Phase 2 upgrade requires new inner detector
  - 3000-4000 fb^{-1} lifetime
  - $\mu = 200$ ($L = 5\text{-}7.5 \times 10^{34}\ cm^{-2}s^{-1}$)

LHC (25 vertices)



HL-LHC (200 vertices)

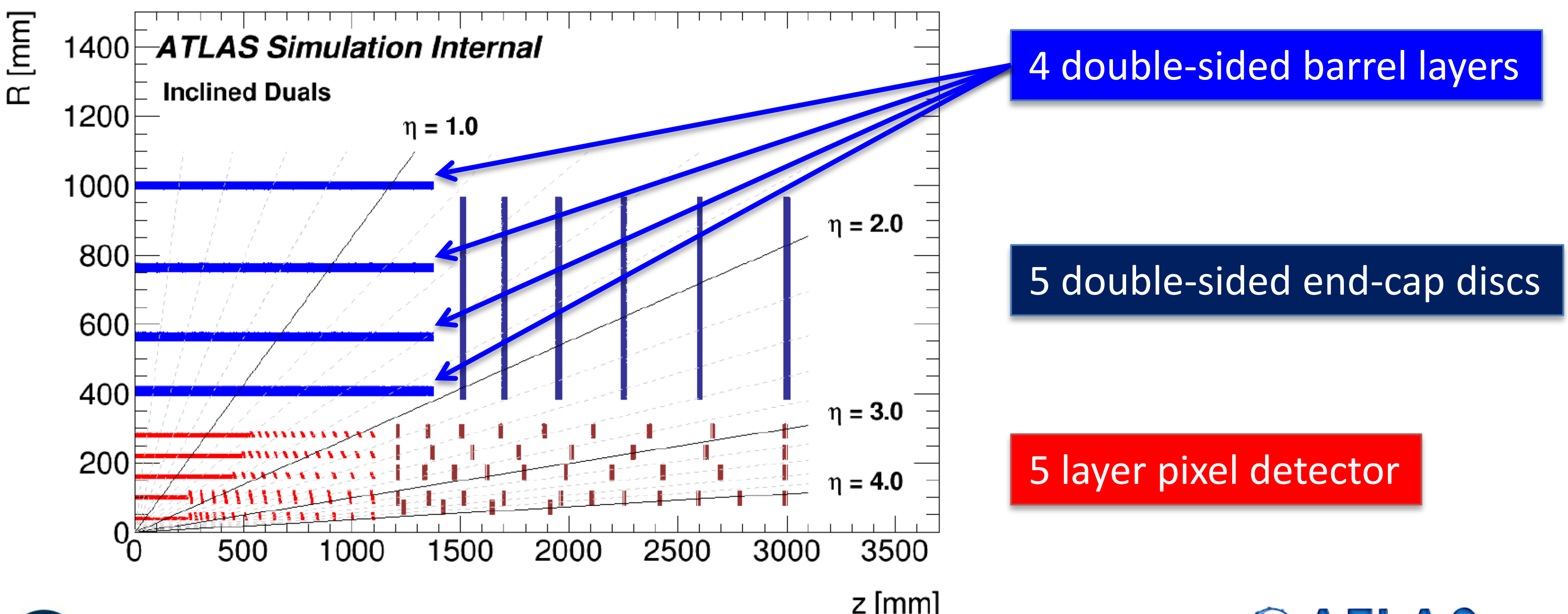




ITk Detector

- All silicon inner tracker to be installed in LS3
- Tracking coverage up to $|\eta|=4.0$
- Inner layers built from pixels
- Outer layers built from strips
  - Inner two barrel layers use short (2.4cm) strips
  - Outer two barrel layers use long (4.8cm) strips

Requirement	Pseudorapidity interval $|\eta| < 2.7$	$2.7 < |\eta| < 4.0$
Pixel+Strip clusters	≥ 9	≥ 9
Pixel clusters	≥ 1	≥ 1
Holes	< 3	< 3
Pixel holes	< 2	< 2
Strip holes	< 3	< 3
Double Strip holes	< 1	
p_T [MeV]	> 900	> 400
$|d_0|$	≤ 2 mm	≤ 10 mm
$|z_0|$	≤ 25 cm	≤ 25 cm



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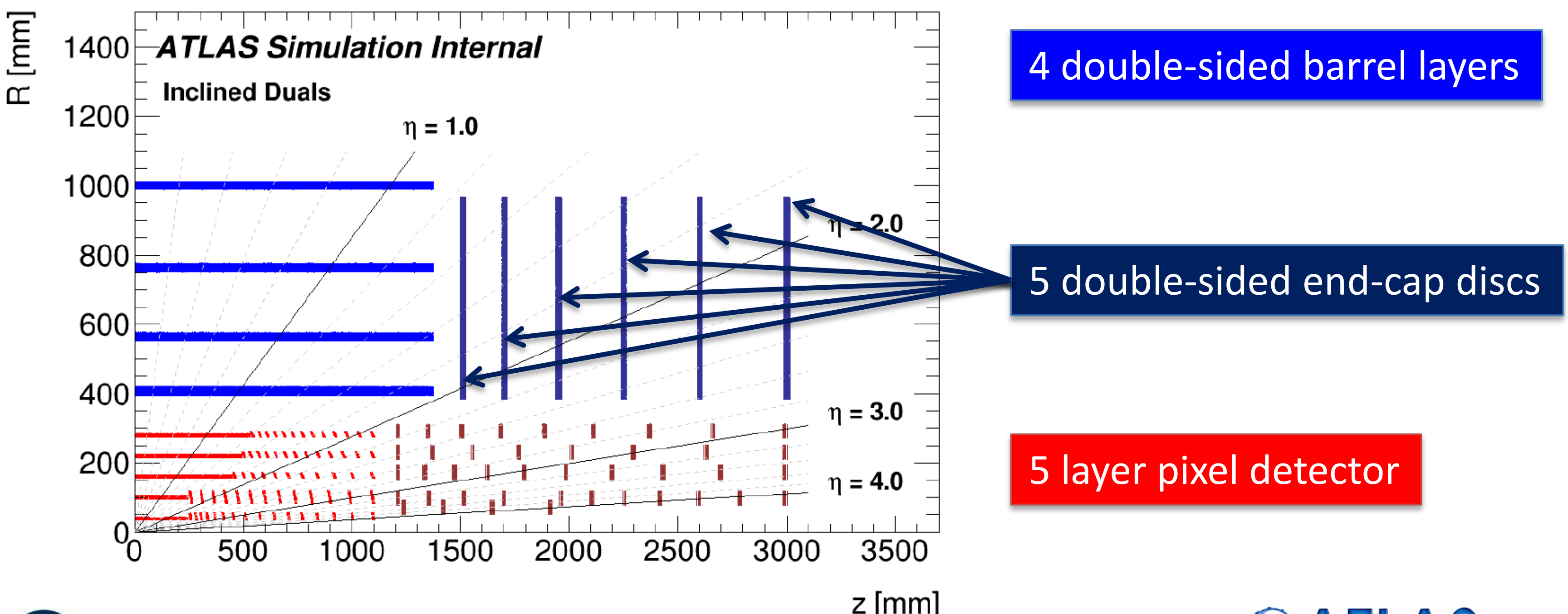

ITk Detector

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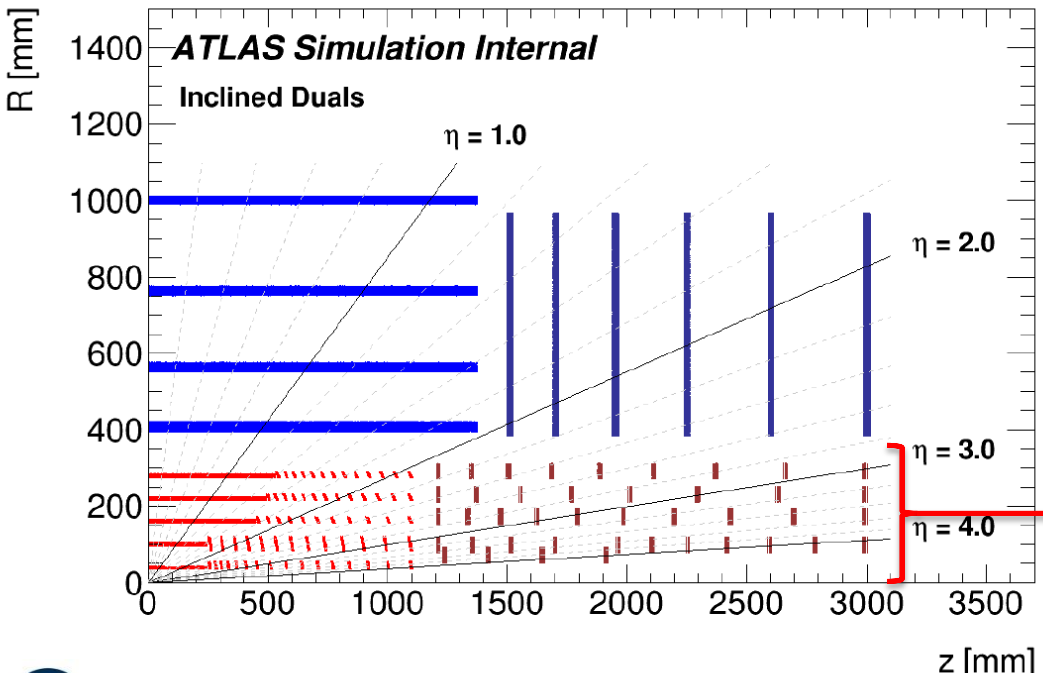
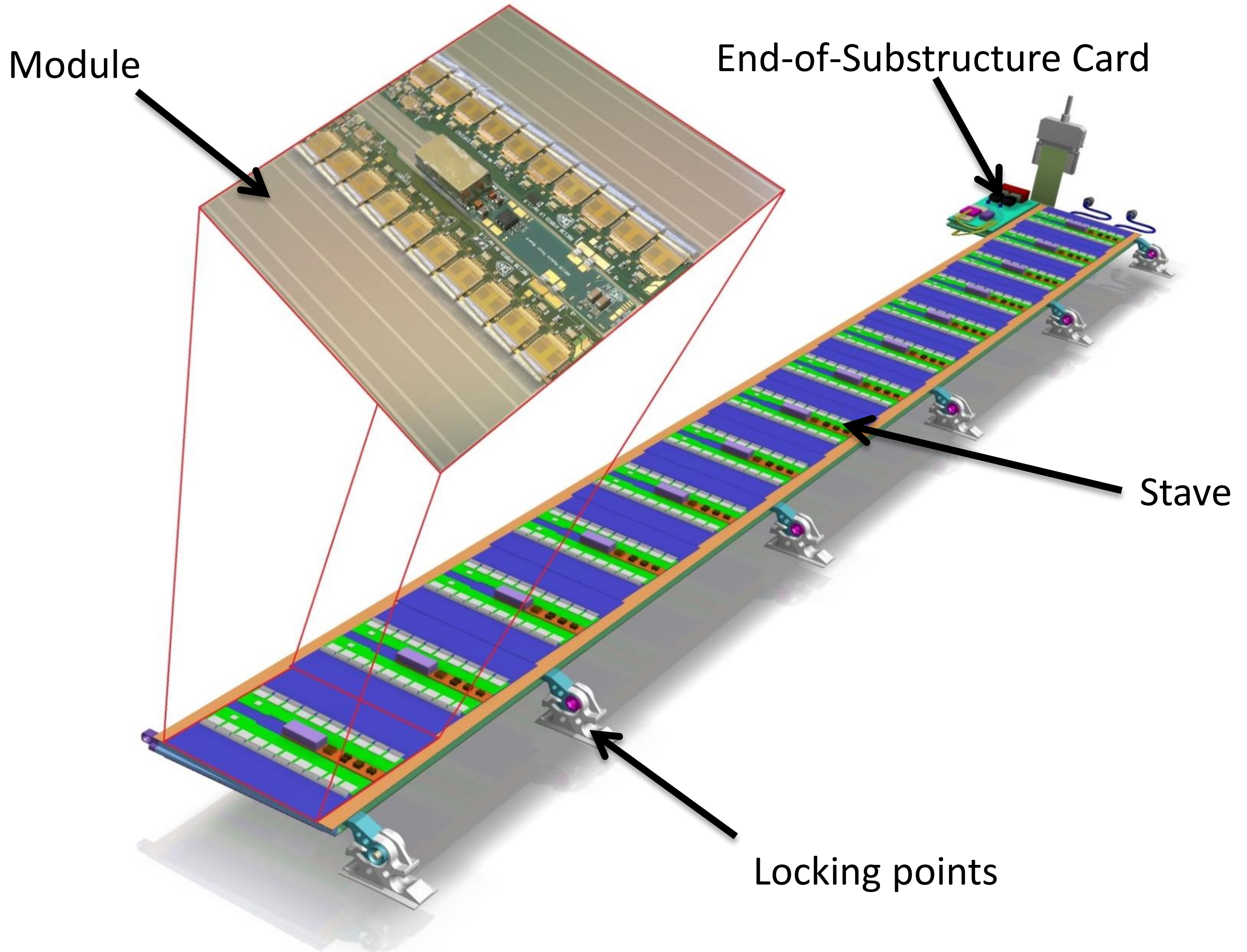


4 double-sided barrel layers

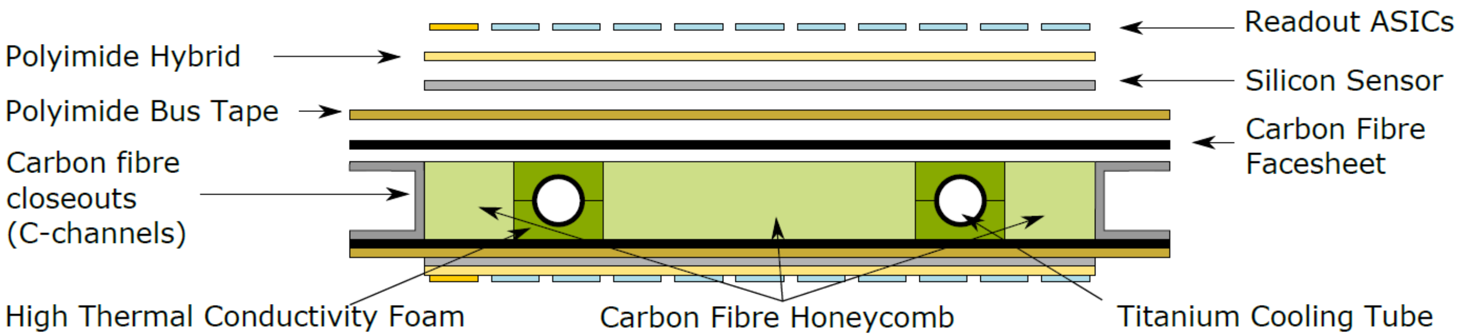
5 double-sided end-cap discs

5 layer pixel detector

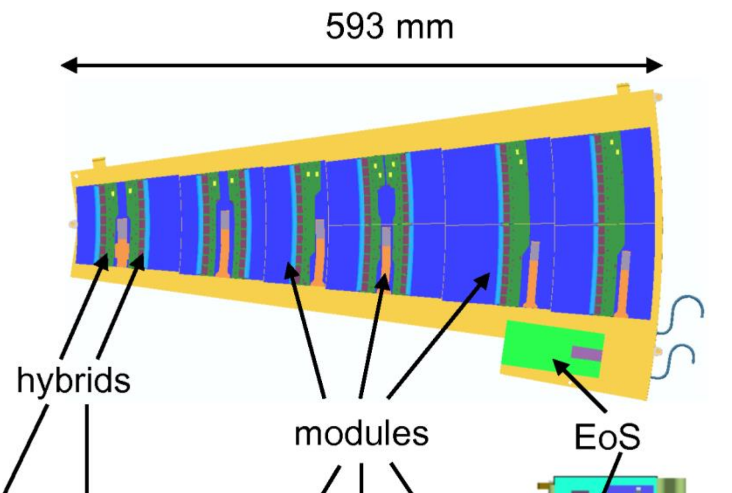
Strip Building Blocks

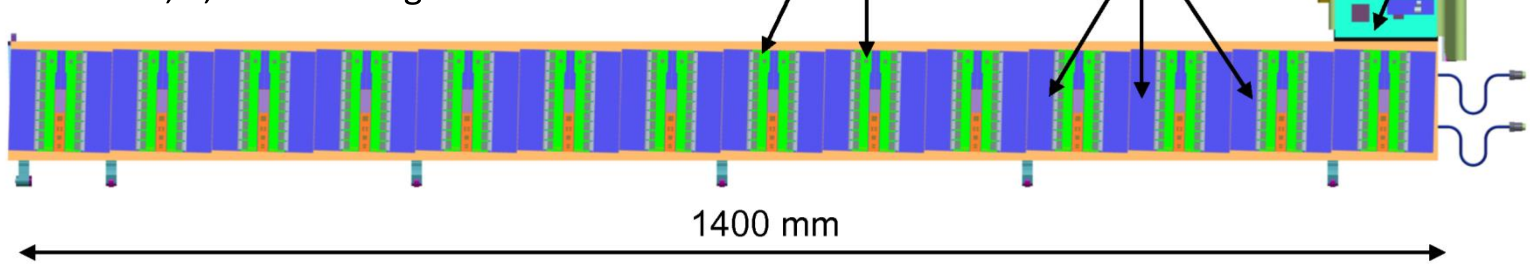


Strip Local Supports



- Staves and petals provide:
  - Mechanical support
  - Geometric location control
  - Cooling
  - LV power
  - HV power
  - Detector Control System signals
  - Timing, Trigger and Control signals
  - Data readout
  - T, V, I monitoring readout





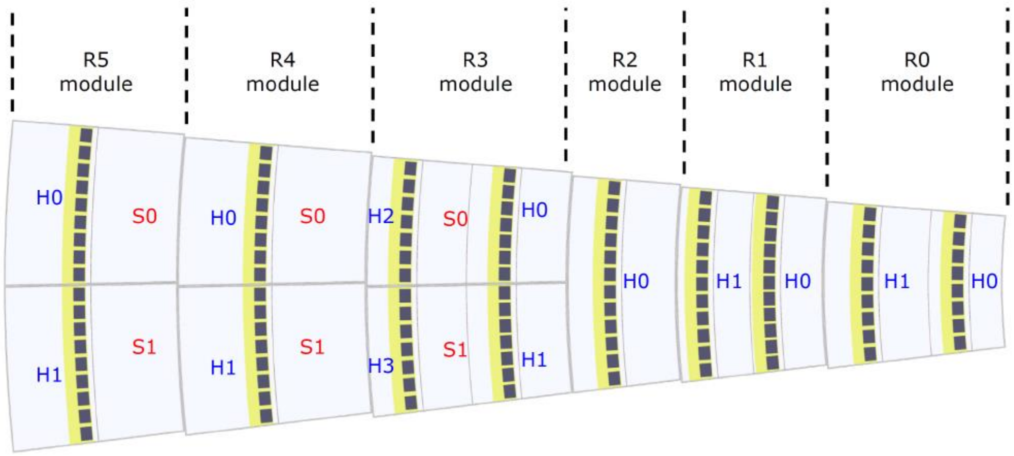
Numerology of ITk Strips

Barrel Layer:	Radius [mm]	# of staves	# of modules	# of hybrids	# of of ABCStar	# of channels	Area [m^2]
L0	405	28	784	1568	15680	4.01M	7.49
L1	562	40	1120	2240	22400	5.73M	10.7
L2	762	56	1568	1568	15680	4.01M	14.98
L3	1000	72	2016	2016	20160	5.16M	19.26
Total half barrel		196	5488	7392	73920	18.92M	52.43
Total barrel		392	10976	14784	147840	37.85M	104.86
End-cap Disk:	**z-pos. [mm]**	**# of petals**	**# of modules**	**# of hybrids**	**# of of ABCStar**	**# of channels**	**Area [m^2]**
D0	1512	32	576	832	6336	1.62M	5.03
D1	1702	32	576	832	6336	1.62M	5.03
D2	1952	32	576	832	6336	1.62M	5.03
D3	2252	32	576	832	6336	1.62M	5.03
D4	2602	32	576	832	6336	1.62M	5.03
D5	3000	32	576	832	6336	1.62M	5.03
Total one EC		192	3456	4992	43008	11.01M	30.2
Total ECs		384	6912	9984	86016	22.02M	60.4
Total		**776**	**17888**	**24768**	**233856**	**59.87M**	**165.25**

Strip Sensors

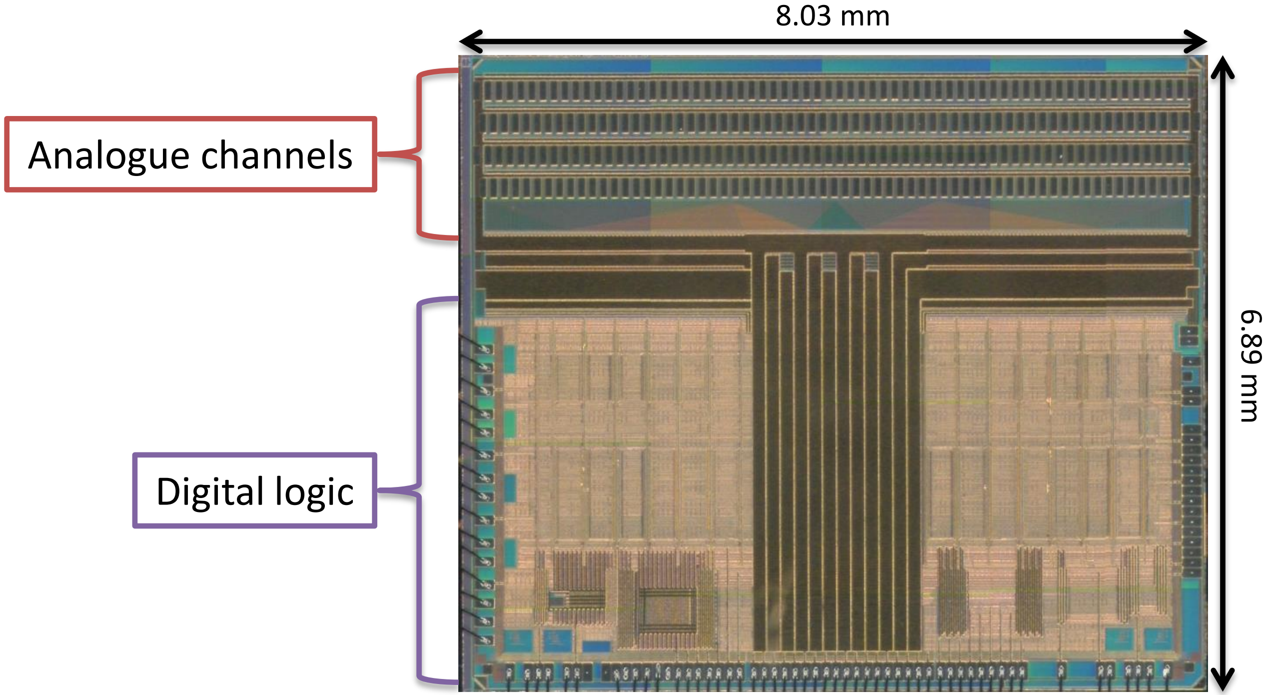
- *n*+-on-*p* silicon strip sensors
  - Collects electrons
  - Single sided processing
  - Good radiation tolerance
- 2 types of barrel sensors with 75.5 µm strip pitch, short-strip with 24.1 mm strips and long-strip with 48.1 mm strips
  - Stereo angle (±26 mrad) by placement of sensors on the stave
- 6 types of EC sensor with 69.9-80.7 µm strip pitch and 18.1-60.2 mm strips
  - Stereo angle (20 mrad) directly implemented in the sensor design

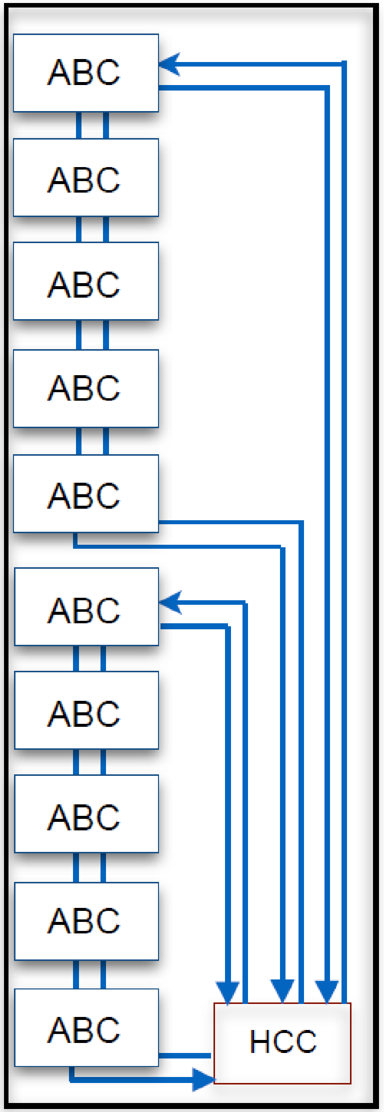
Ring/Row	Strip Length [mm]	Strip Pitch (inner) [µm]
Ring 0 Row 0	19.0	75.0
Ring 0 Row 1	24.0	79.2
Ring 0 Row 2	29.0	74.9
Ring 0 Row 3	32.0	80.2
Ring 1 Row 0	18.1	69.9
Ring 1 Row 1	27.1	72.9
Ring 1 Row 2	24.1	75.6
Ring 1 Row 3	15.1	78.6
Ring 2 Row 0	30.8	75.7
Ring 2 Row 1	30.8	79.8
Ring 3 Row 0	26.2	71.1
Ring 3 Row 1	32.2	74.3
Ring 3 Row 2	32.2	77.5
Ring 3 Row 3	26.2	80.7
Ring 4 Row 0	54.6	75.0
Ring 4 Row 1	54.6	80.3
Ring 5 Row 0	40.2	76.2
Ring 5 Row 1	60.2	80.5



Strip ASICs – ABC130/HCC130

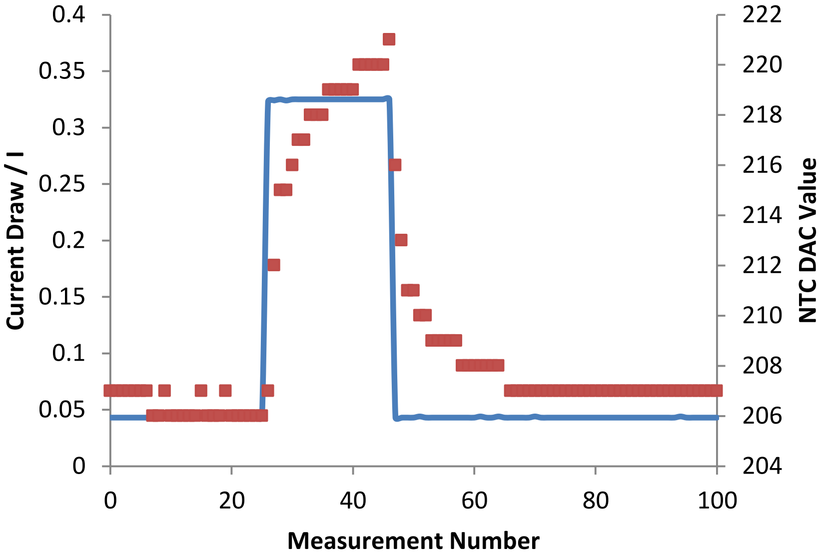
- Current generation of prototype chip
- 130nm ATLAS Binary Chip (ABC130) and Hybrid Controller Chip (HCC130) fabricated in GF CMOS 8RF process
- 256 analogue front ends per ABC130 including:
  - Charge integration
  - Pulse shaping
  - Adjustable pre-amplifier, feedback and comparator stages
  - On-chip calibration circuitry (60 fF capacitor)
- ABC130s read out in loops via daisy chained signal routing

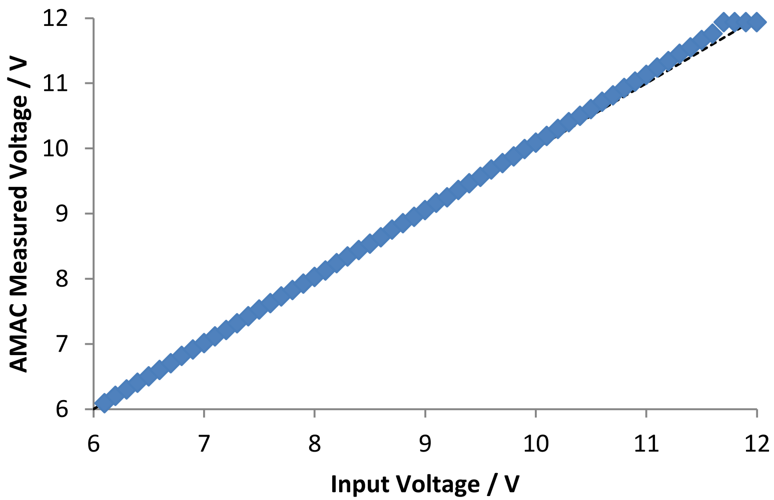


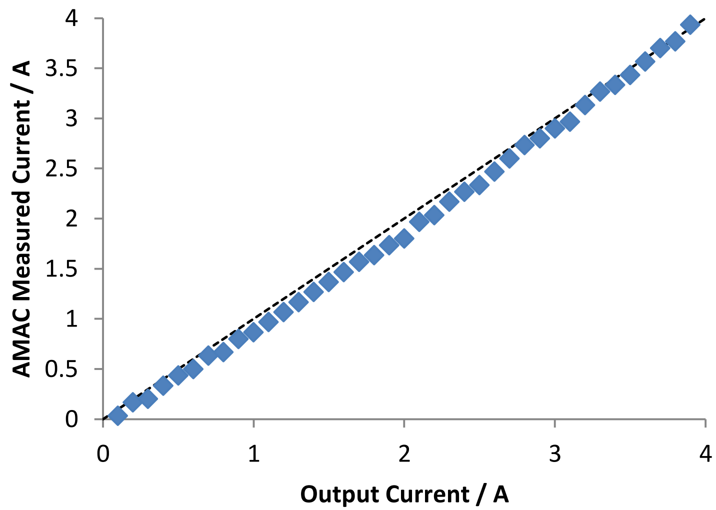


Strip ASICs – AMAC v1a

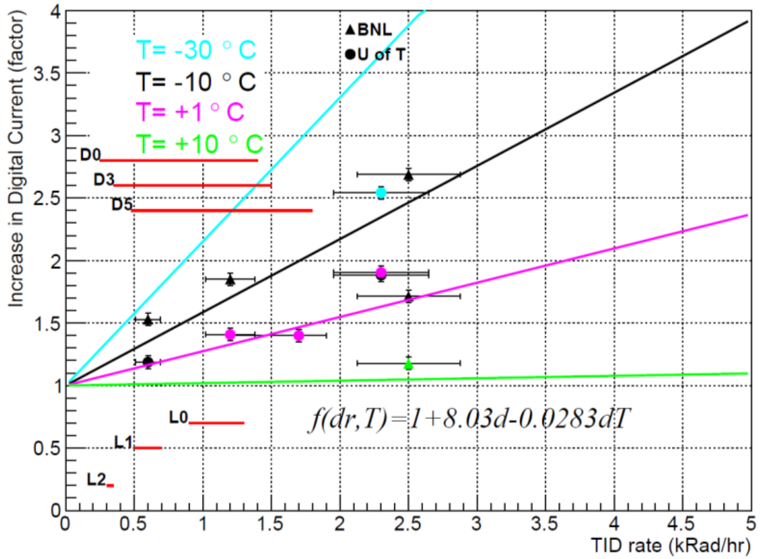
- Prototype version of Analogue Monitor and Control (AMAC) ASIC already in hand
- Monitors temperature, voltages and currents
- Controls on-module DCDC converter
- Controls on-module HV switch (GaNFET)
- Include autonomous interlocking capabilities



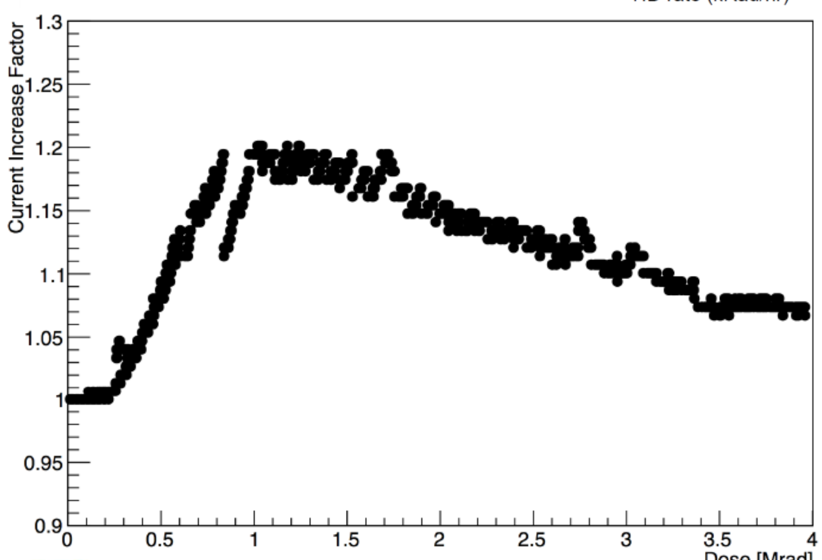


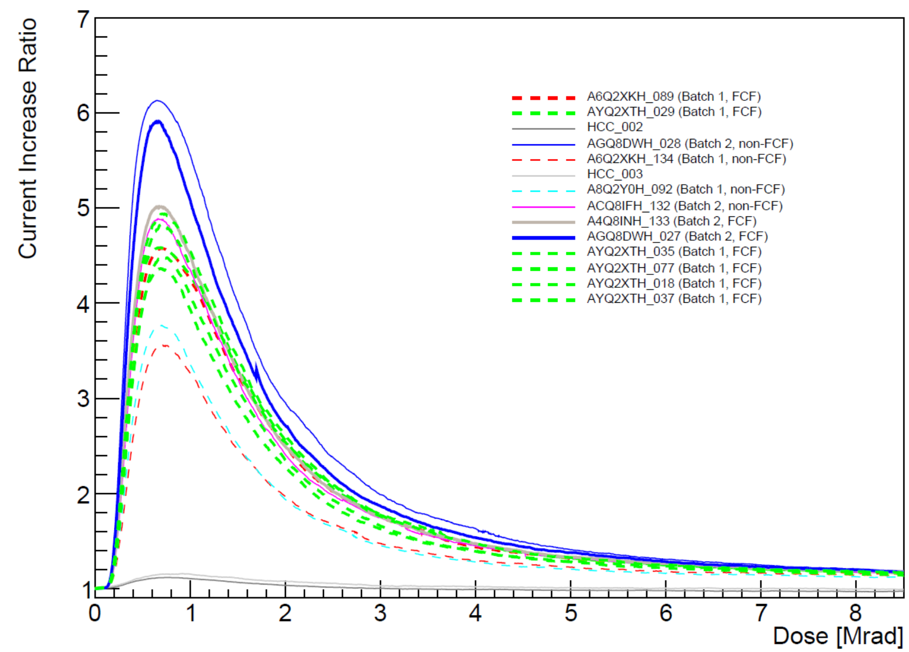


TID Effects – Digital Current



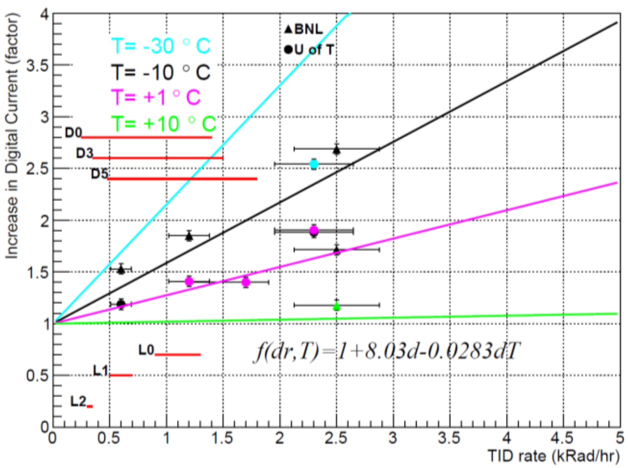
- GF 130 nm has a "feature" of increasing transistor leakage current with radiation
- Seen in current ATLAS IBL
- Similar effects seen on strip prototype chips
- Current efforts ongoing to understand:
  - Global fits to low temperature data
  - Chip-by-chip variation
  - Expected current draw of production chips

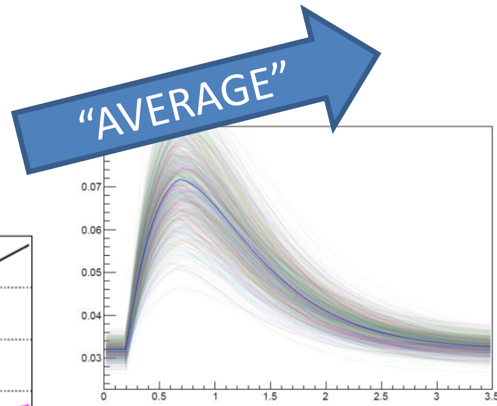


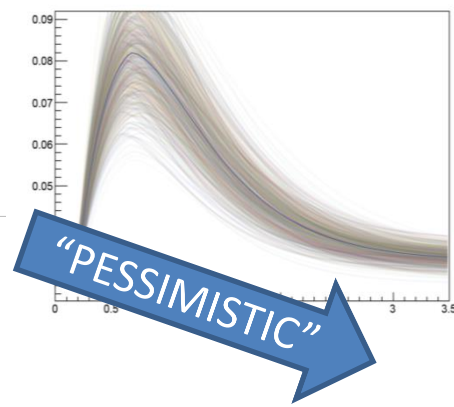


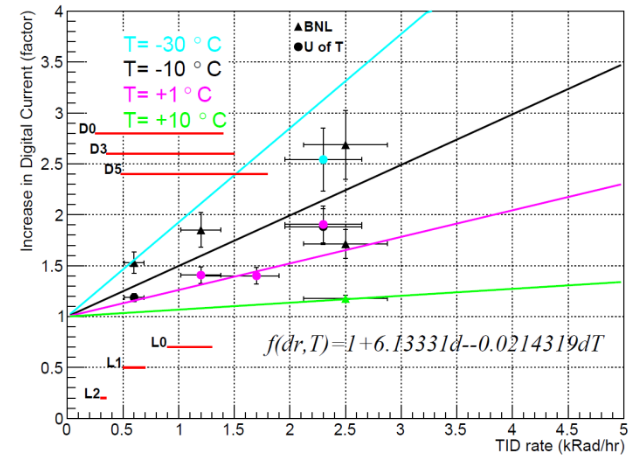
TID Effects – including batch variation

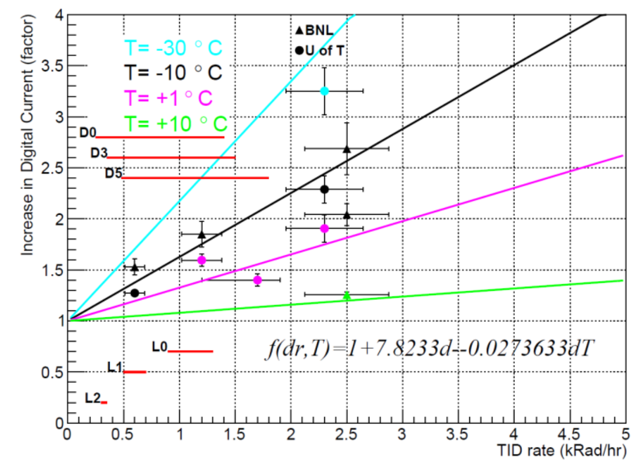
- Recent measurements suggest that from the two batches of chips that we have received, batch 2 sees a larger effect than batch 1
- Attempts ongoing to include this variation in global fits





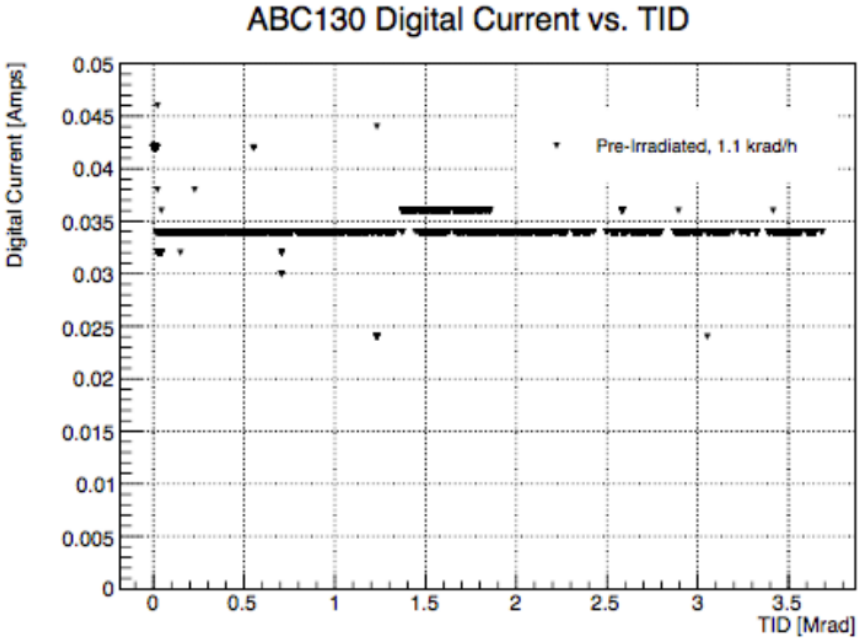


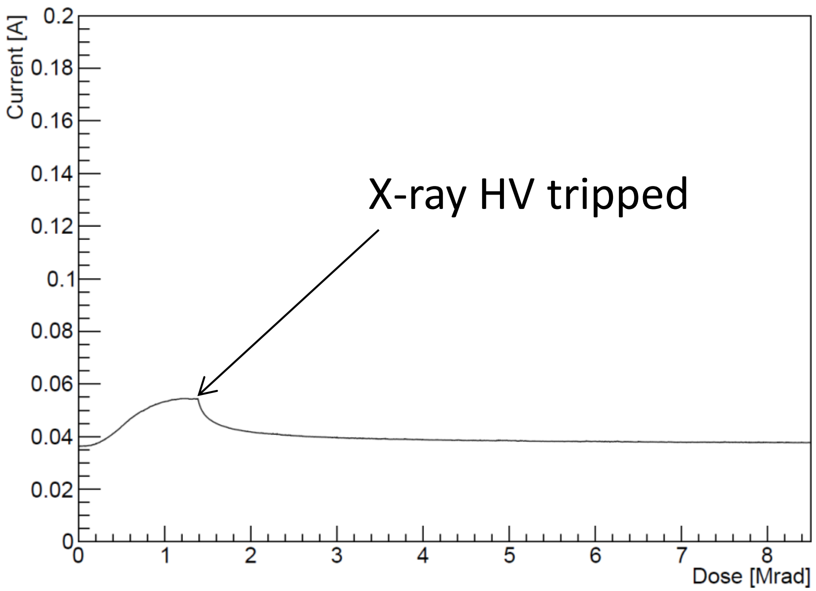




What about pre-irradiation?

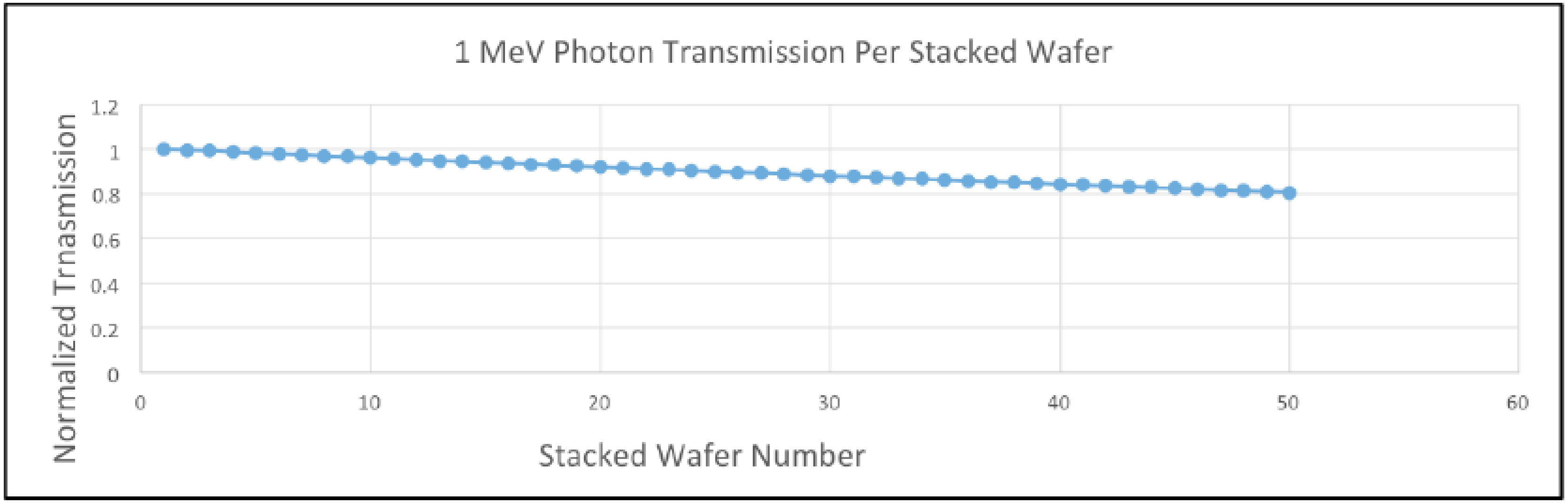
- Considering the possibility of pre-irradiating chips over the peak
- Have irradiated one chip unpowered to 8.5 Mrad @ 8.5 Mrad/hr
- Then irradiated to 3.5 Mrad @ 1.1 krad/hr
- 6 months later re-irradiated at 8.5 Mrad/hr
- Evidence of returning (smaller) peak in second re-irradiation





Pre-irradiation in production

- Can be done using ^{60}Co sources
- Stack of 50 wafers gives only 20% dose difference front to back (assuming 1 MeV photons)
- About to send 1-2 wafers to Taiwan to try with their "wall of sources" facility
- Will take 24 hr to reach around 8 Mrad



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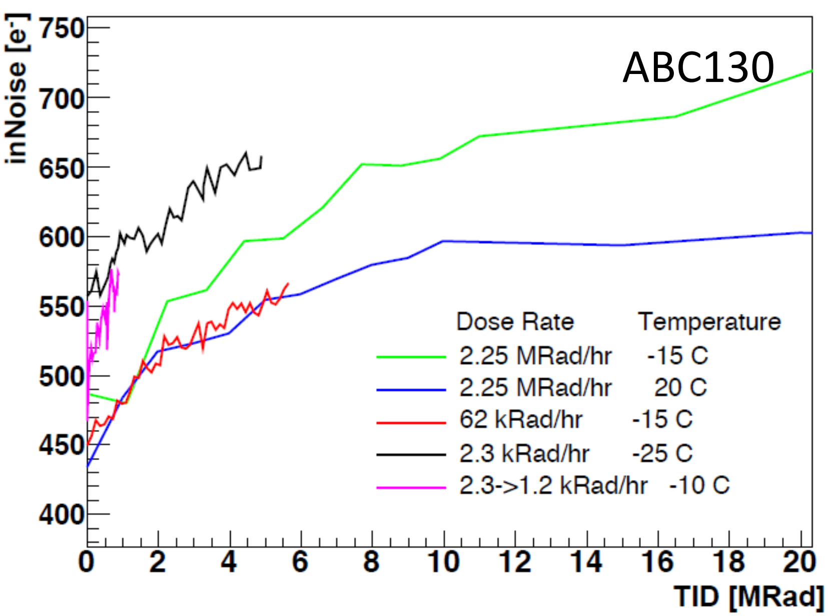
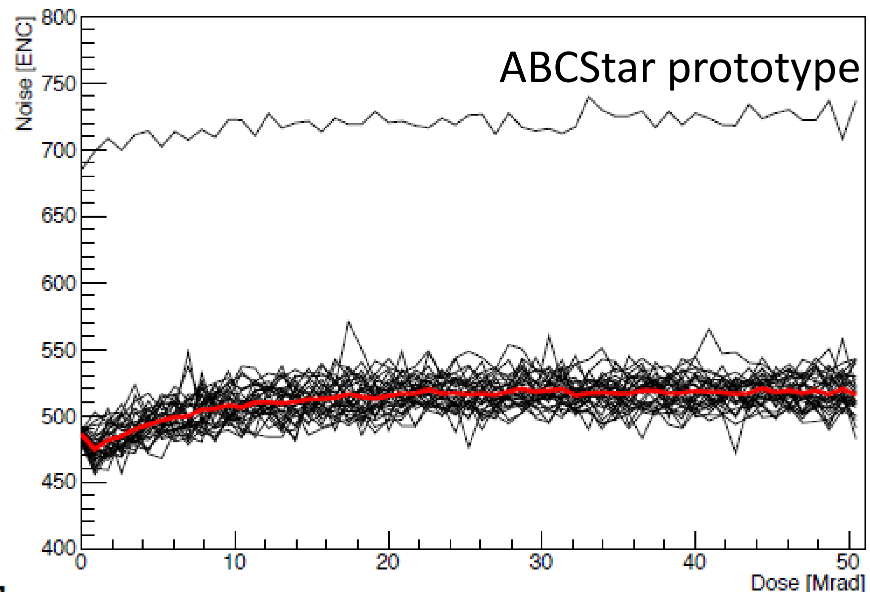
TID Effects – Noise

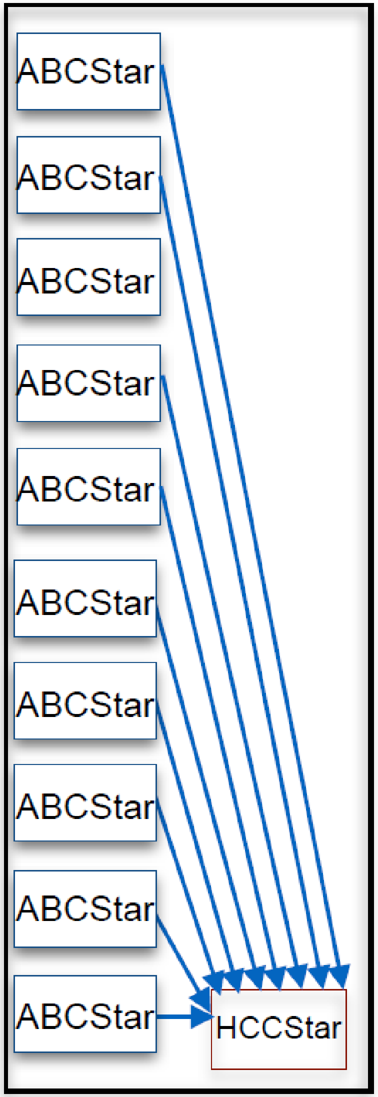
- Measurements of ABC130 found a larger than expected noise increase
- Increase expected to arise from $^{1}/_{f}$ noise
- Simulations suggest pre-rad effect is only be 3% but reports [3,4,5] of 130 nm technology suggest large increases for NMOS
- No increase observed for enclosed structures
- Such a change already prototyped using 32 channel prototype chip





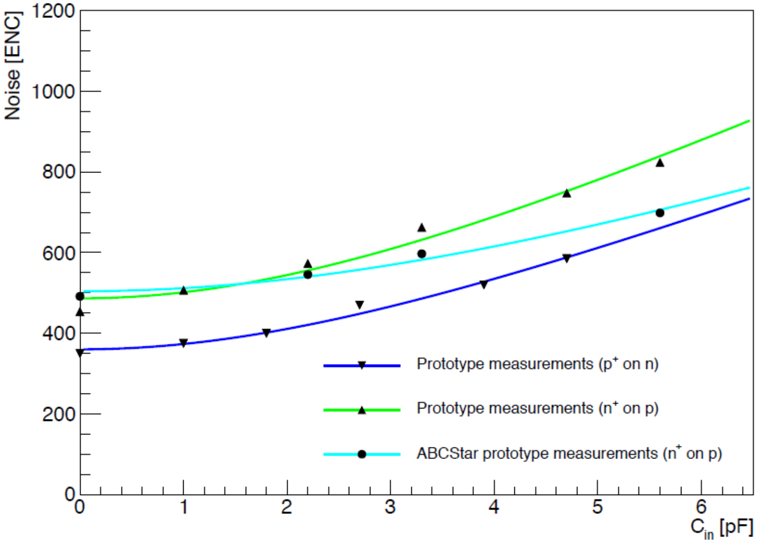
Production chipset

- Design of production chipset already well developed
  - AMACv2 already submitted in November
  - HCCStar and ABCStar will be submitted early in 2018 (PDRs next week)
- AMACv2 heavily based on AMACv1a but with increased monitoring/control channels and communication protocol
- Major change in readout architecture to meet changed rate requirements (L0/L1 changed from 500/200 kHz to 1 MHz/400 kHz)
  - Daisy chain no longer suitable
  - Changed to "star" architecture
- Two ABCStar FE changes in addition to the enclosed geometry change (see next slides)



Analogue Changes

- Already discussed the change to enclosed geometry to reduce the noise increase with TID
- In addition two other changes have been made:
  - Resistive feedback and differential booster stage to improve noise performance when operated with n^+-on-p sensors
    - Originally designed for p^+-on-n
  - Different ESD protection circuit
    - Improves level of protection
    - Reduces parasitic capacitance
- Enclosed geometry and n^+-on-p changes already demonstrated on prototypes
- ESD circuitry change under test as we speak



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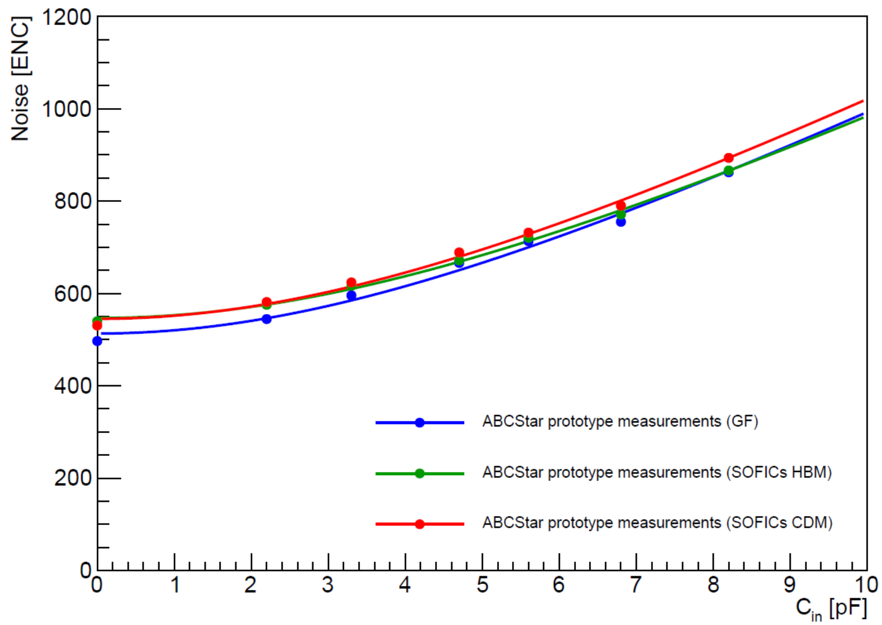
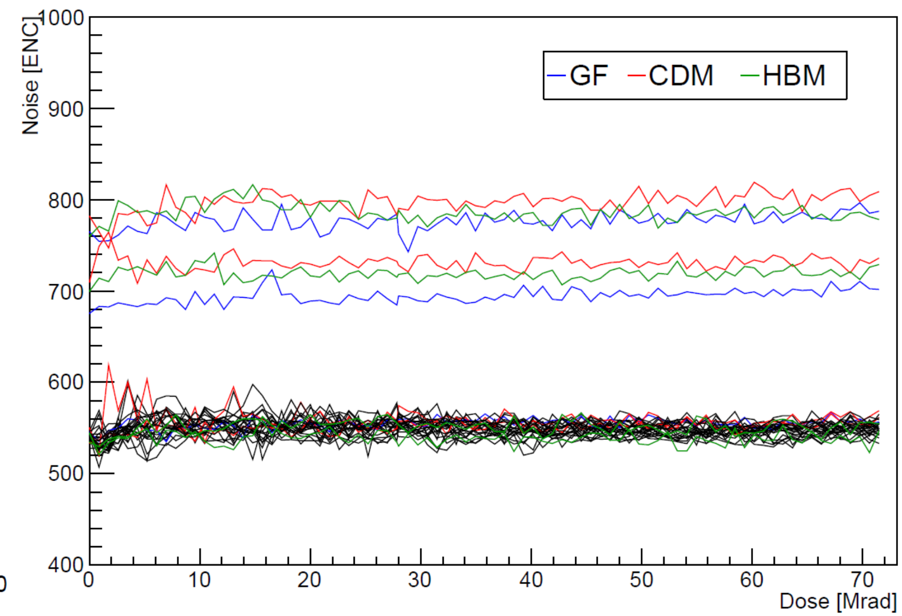
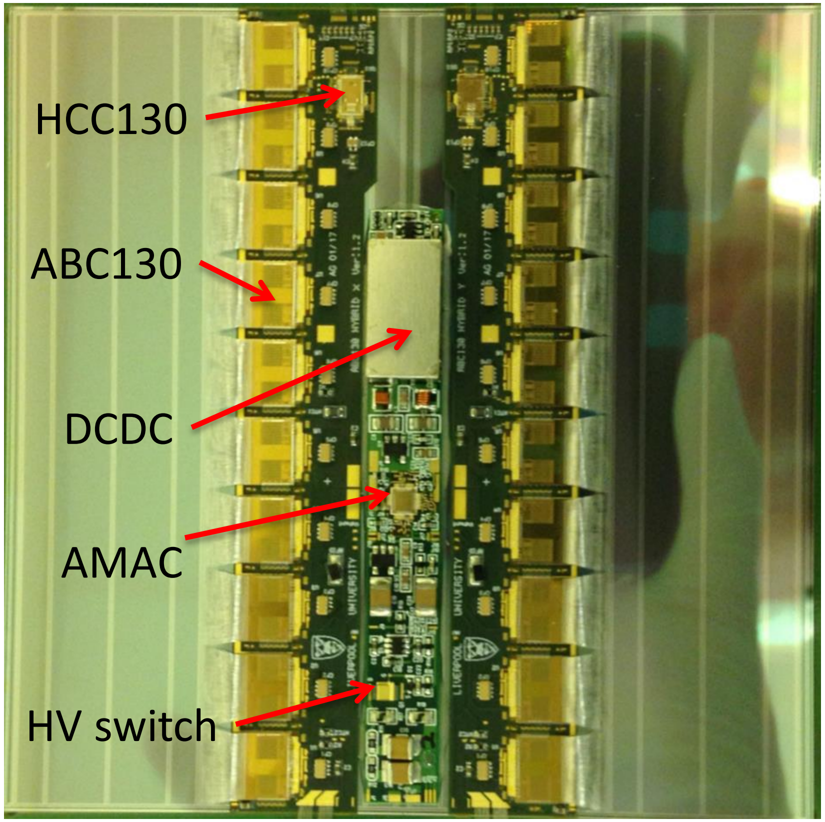
FE Protection Changes

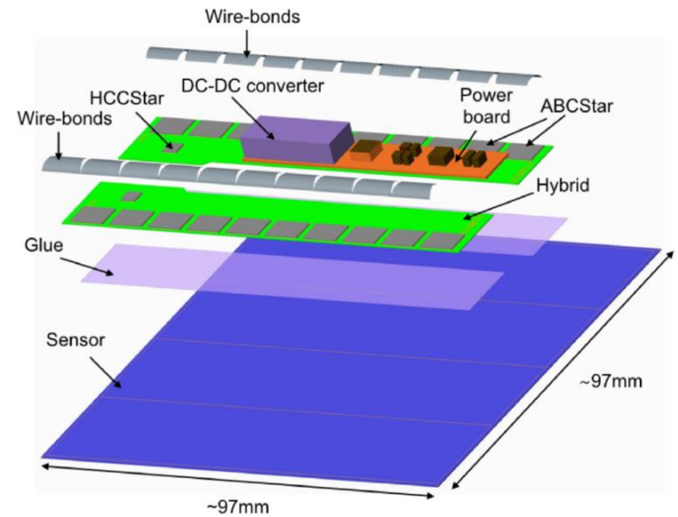
- Intending to change from GF standard protection to a protection circuit provided by SOFICs
  - Lower capacitance
  - Better protection
- See no worse performance of SOFICs protection compared to GF
- Proton irradiated chips to be tested soon

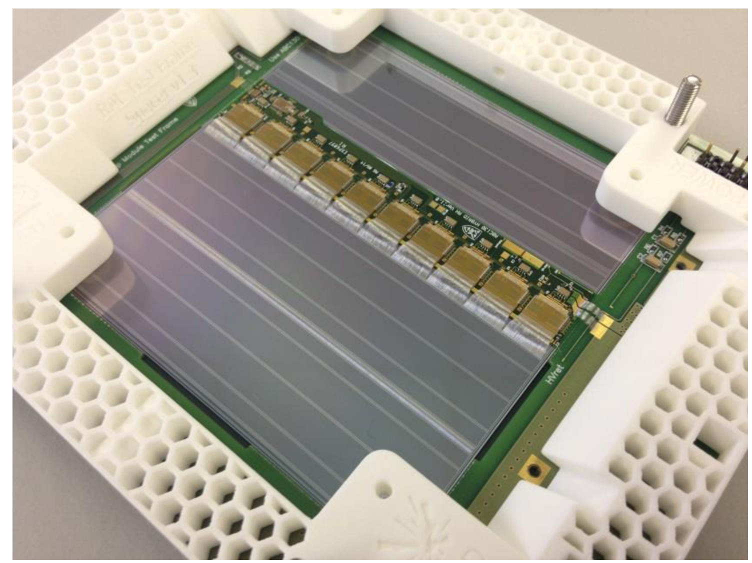




Strip Modules



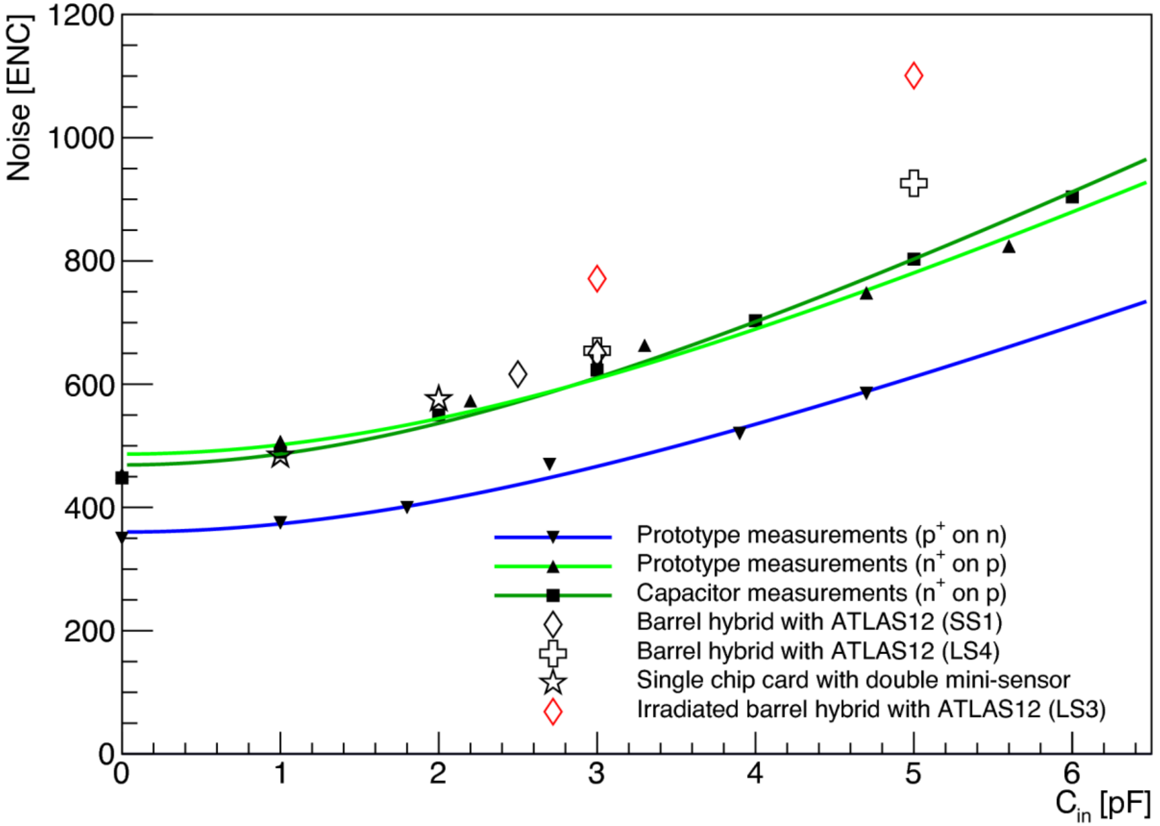




- Extensive program to demonstrate module functionality with prototype chipset
- Long-strip, short-strip and R0 modules have been successfully built

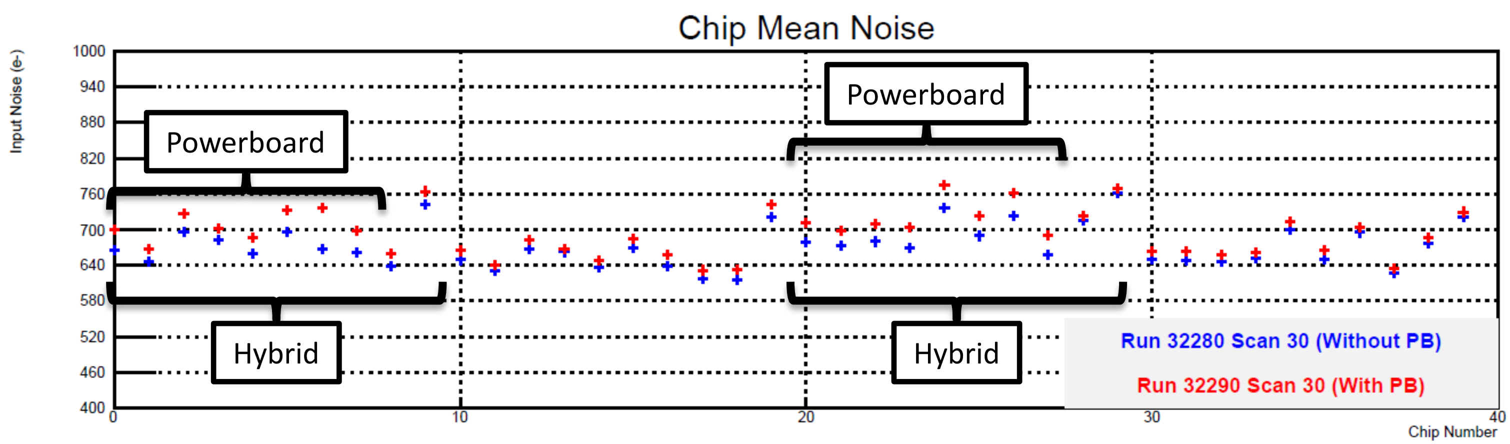
Noise

- Prototype FE chips, single ABC130s and barrel modules used to measure noise vs. capacitance
- Good agreement with simulation and expectation



Module Results

- Comparing results before and after powerboard placement can see a couple of effects:
  – Increased noise due to additional capacitance on strips running underneath hybrids
  – Further additional noise on those channels running underneath the powerboard
- Very little change between module performance before and after powerboard placement



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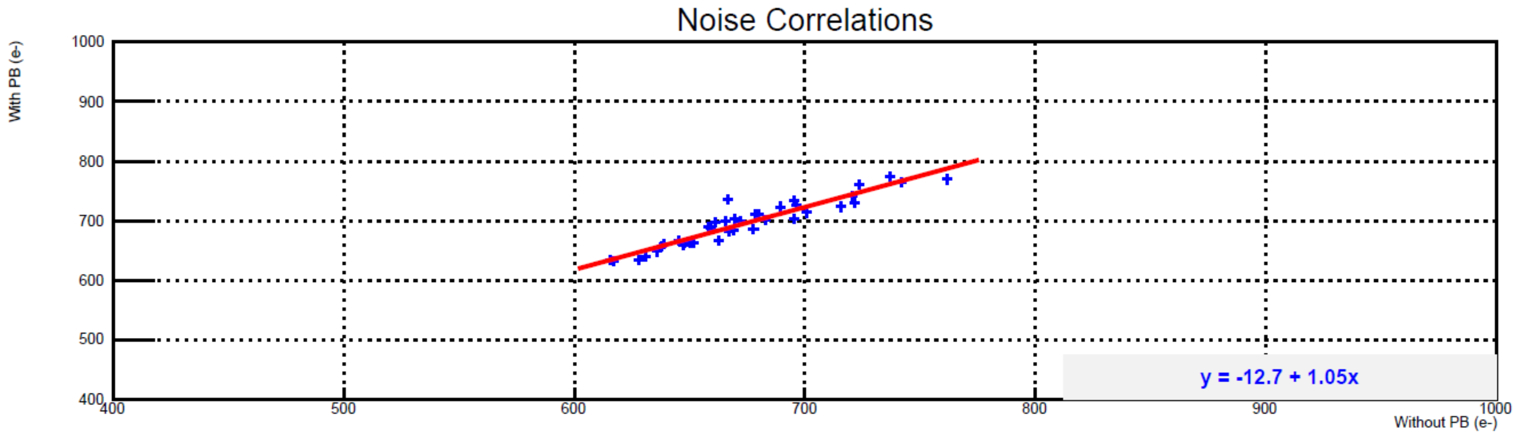
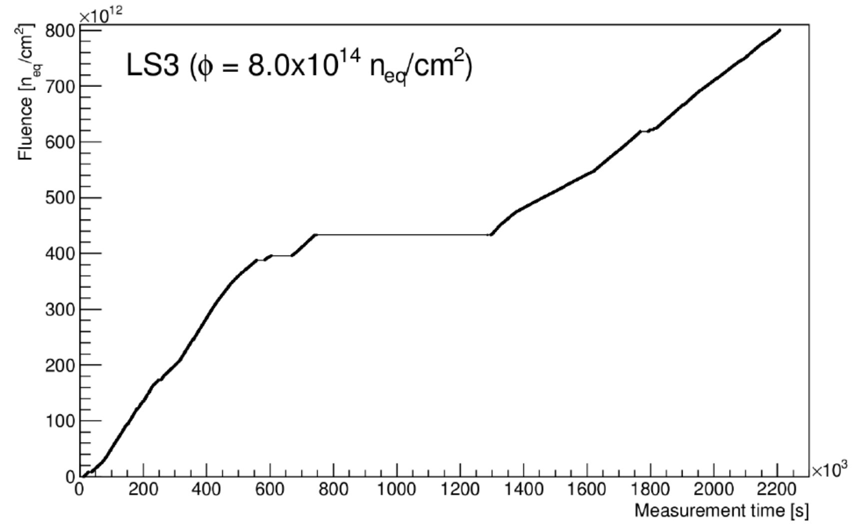
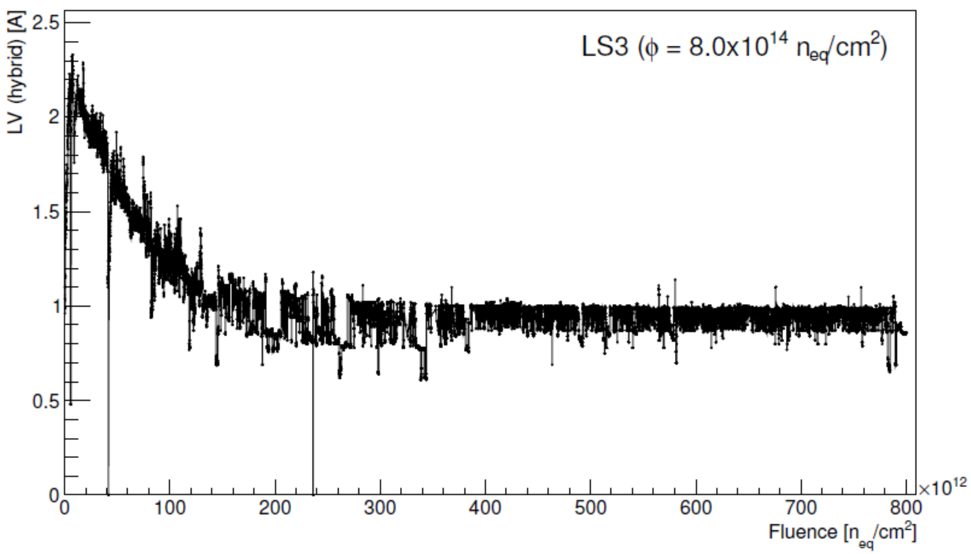
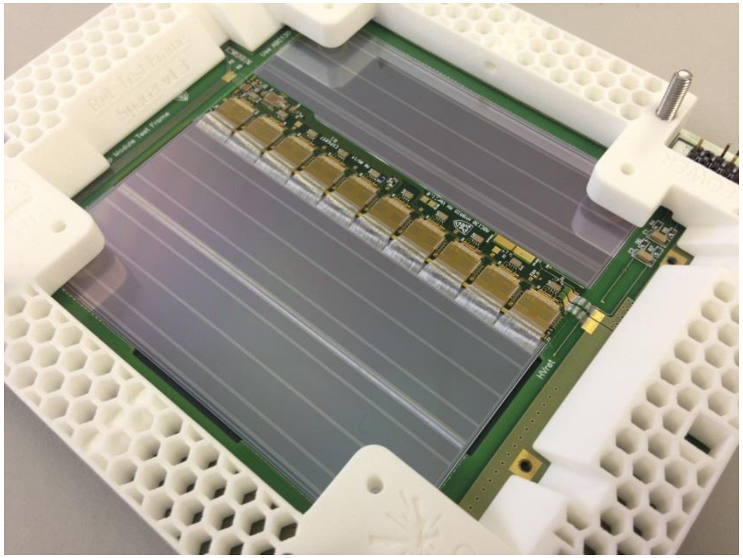


Module Irradiation

- Module with mixed long and short strips irradiated at CERN PS
- $8.0 \times 10^{14}\ n_{eq}/cm^2 = 37.1$ Mrad
- Highest fluence (without safety factor) expected at any point of strip detector

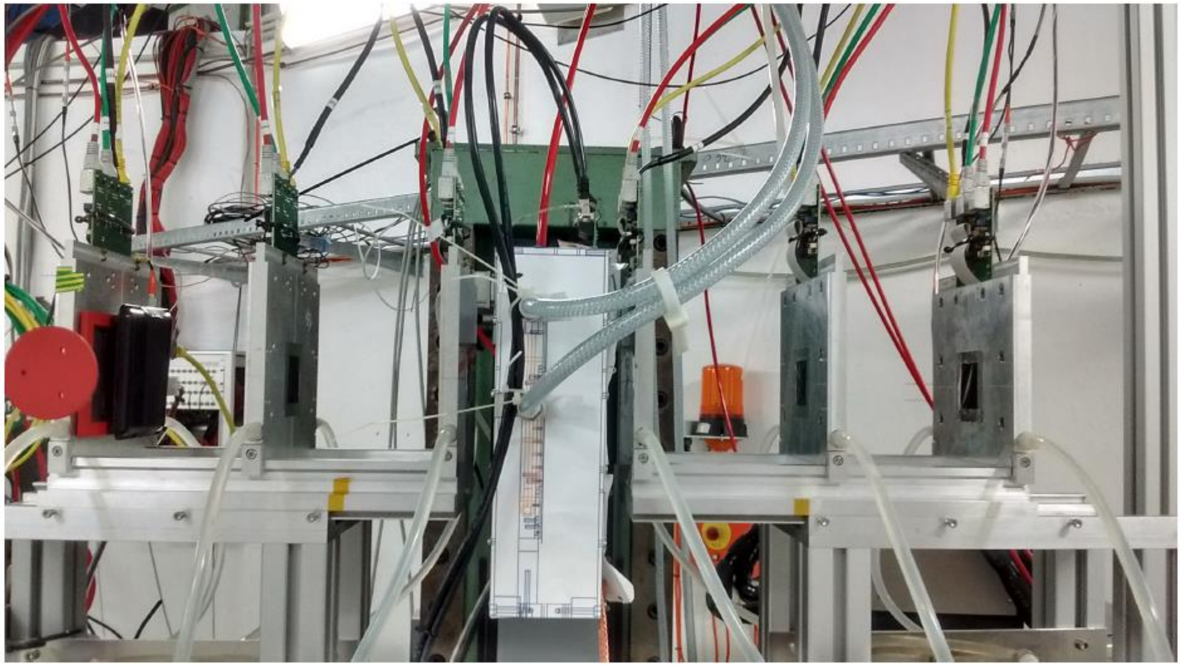






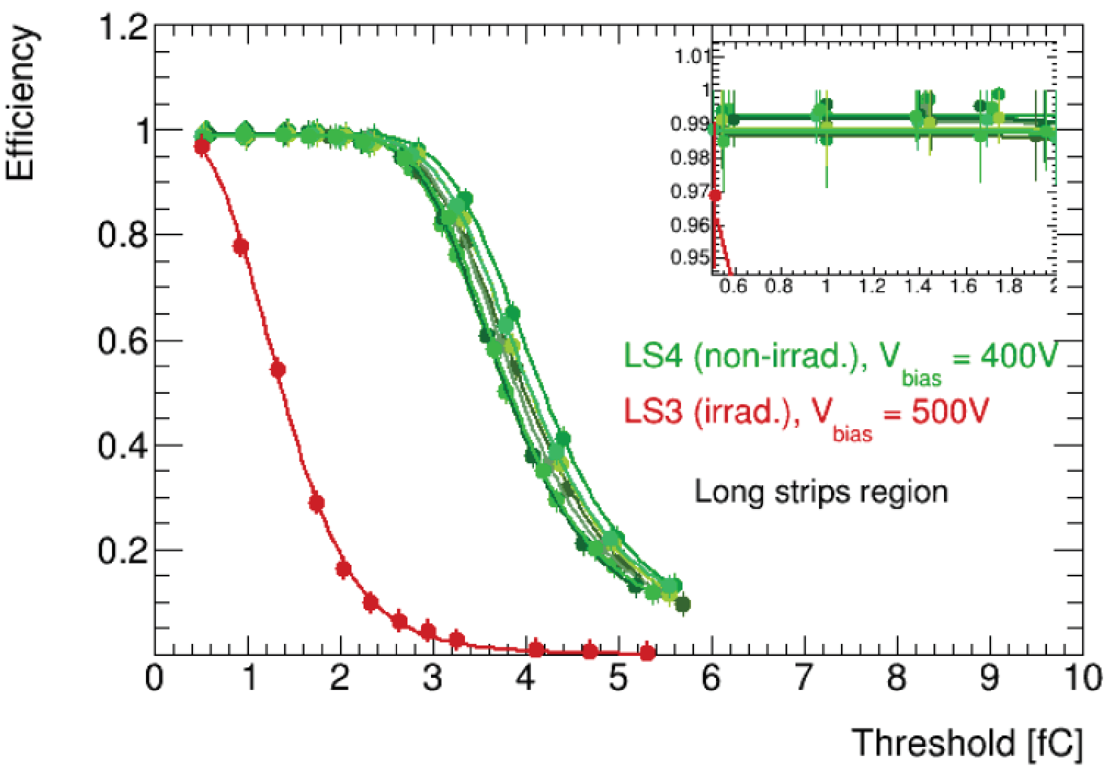
Testbeam

- "Ultimate" test of module functionality
- Have run unirradiated/irradiated sister modules at testbeams at CERN and DESY
- Similar telescopes at both facilities give 1.5-2.0 µm pointing resolution on device under test (DUT)
- Can compare these results to
  - Analogue readout measurements of sensors
  - Bench top module testing



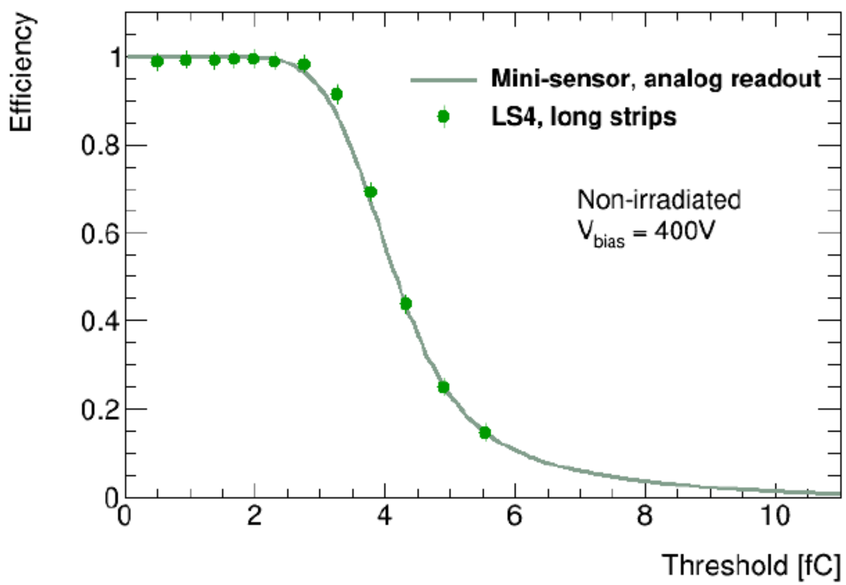
Efficiency curves before and after irradiation

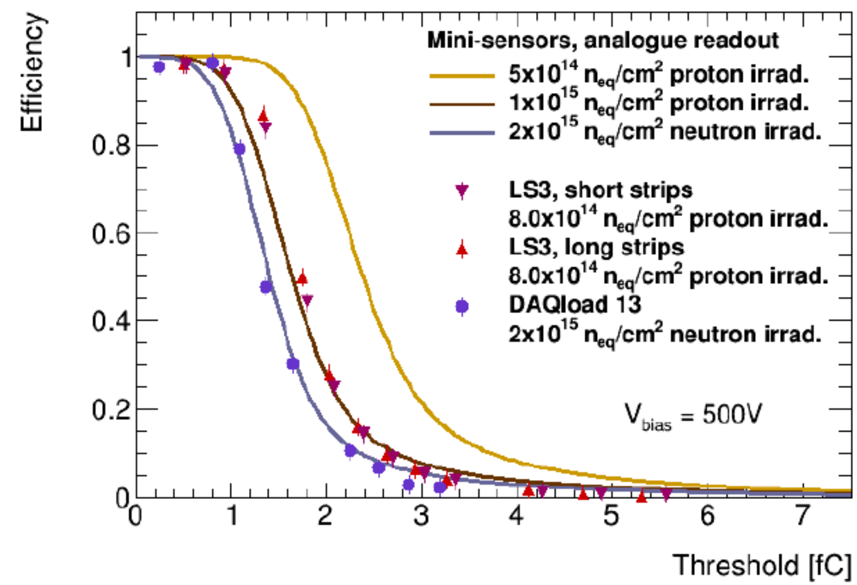
- Look at efficiency vs. threshold comparing irradiated module to unirradiated module
- See (expected) decrease in charge collection with irradiation
- Note that no annealing was done on the irradiated module



ABC130 vs. analogue readout

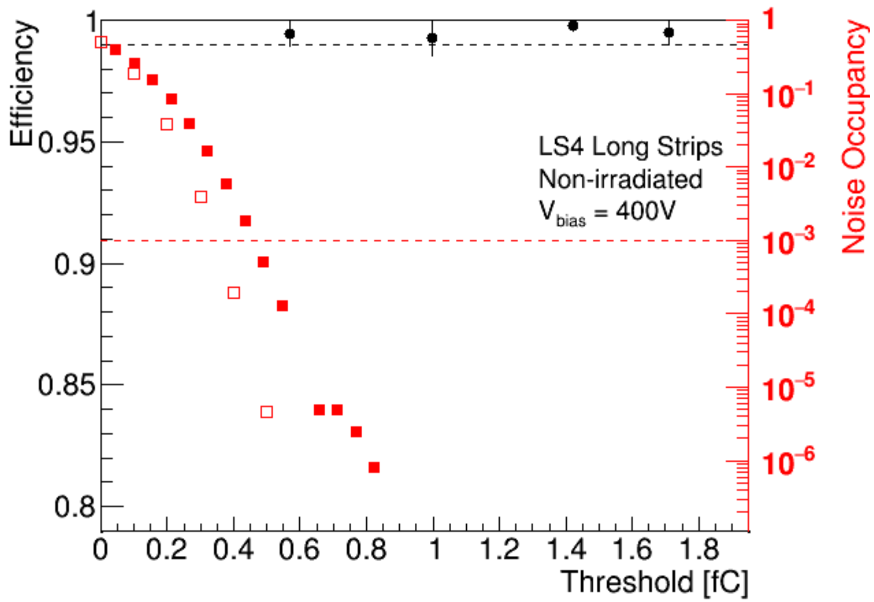
- Can compare testbeam results to analogue readout of sensors using ^{90}Sr source
- Very good agreement both before and after irradiation

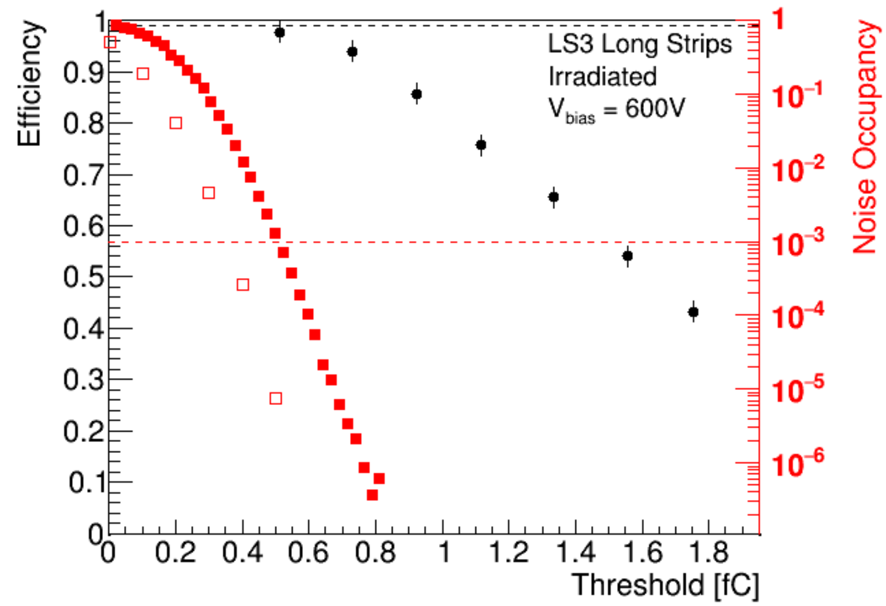




End-of-life performance

- Once of the most important results to come from testbeam is the expected end-of-life performance
- Modules are required to have
  1. 99 % detection efficiency
  2. Less than 10^{-3} noise occupancy
- Assuming threshold for (1) is lower than threshold for (2) we have demonstrated an operating window at end-of-life





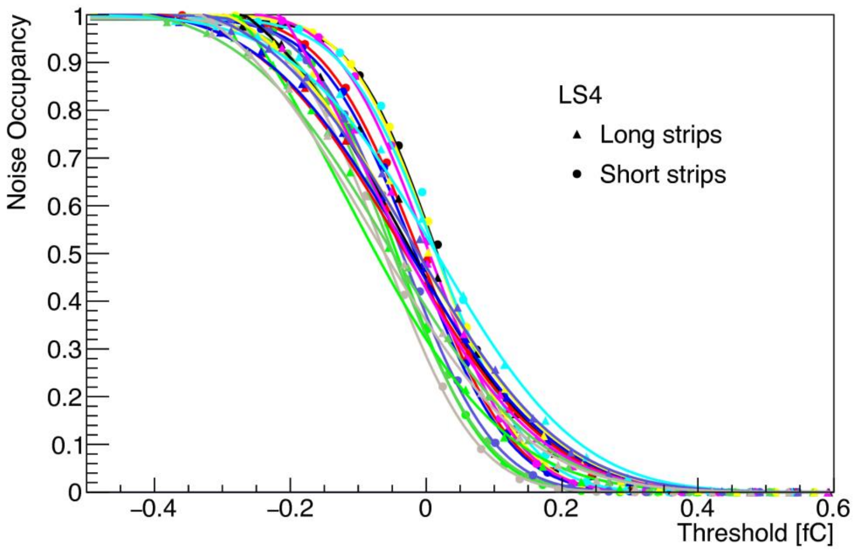
Projected end-of-life

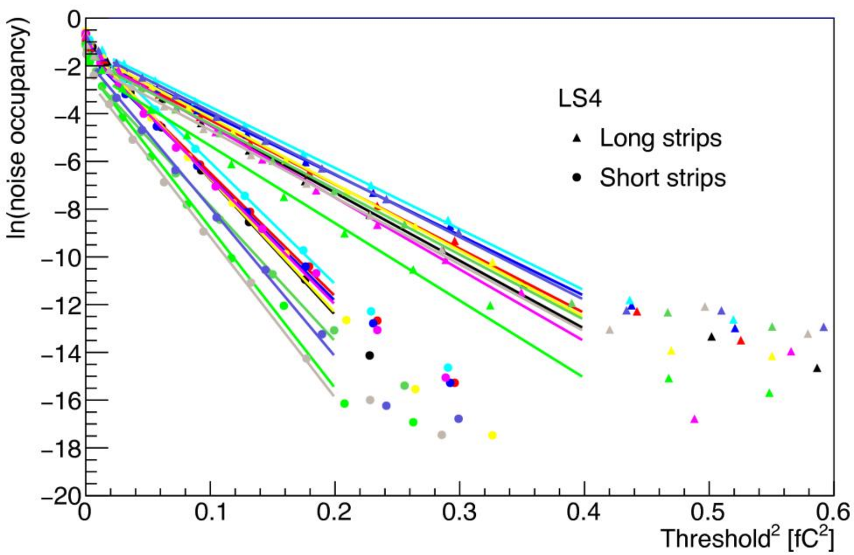
- Noise occupancy and efficiency requirements for an operating window map very well onto a S:N ratio of 10:1
- Extrapolating to new front end, production sensors and higher voltage gives S:N ratios of no worse than 18:1
- The detector should work!

Module Type	Fluence $10^{14} n_{eq} cm^{-2}$	Charge ke^- 500 V	Charge ke^- 700 V	Noise e^-	S/N 500 V	S/N 700 V
SS	8.1	13.7	16.1	630	21.8	25.6
LS	4.1	17.3	19.5	750	23.1	26.0
R0	12.3	11.5	14.0	650	17.7	21.5
R1	10.1	12.5	15.0	640	19.6	23.4
R2	8.7	13.3	15.7	660	20.3	23.9
R3	8.0	13.8	16.2	640	21.4	25.1
R4	6.8	14.6	17.0	800	18.4	21.3
R5	6.0	15.3	17.6	840	18.3	21.1

Noise Estimation Methods

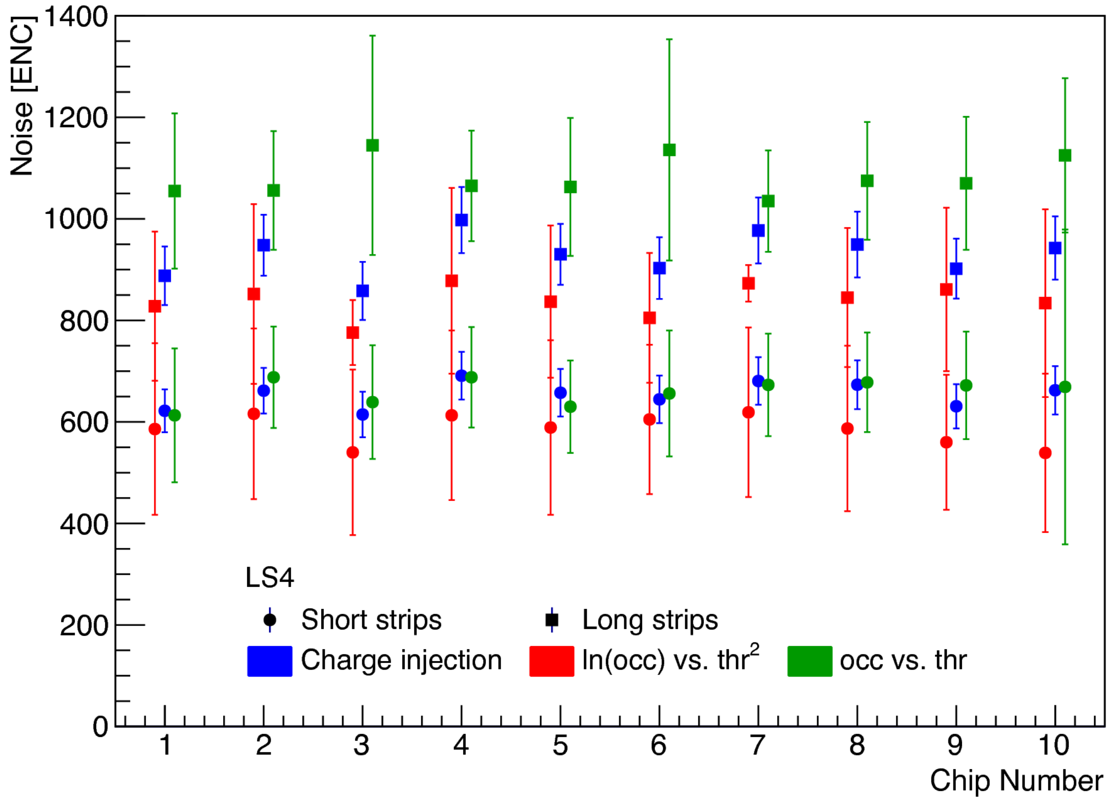
- Noise occupancy is extracted from performing S-curve measurements of efficiency vs. threshold with no charge injection
- Results can either be converted to ln(occ) vs. thr^2 and fitted linearly or fitted with an ERFC function
- The former fits the tail of the noise Gaussian whilst the latter is more dependent on the core
- Comparing the two results gives an idea of, amongst other things, the non-Gaussianity of the noise





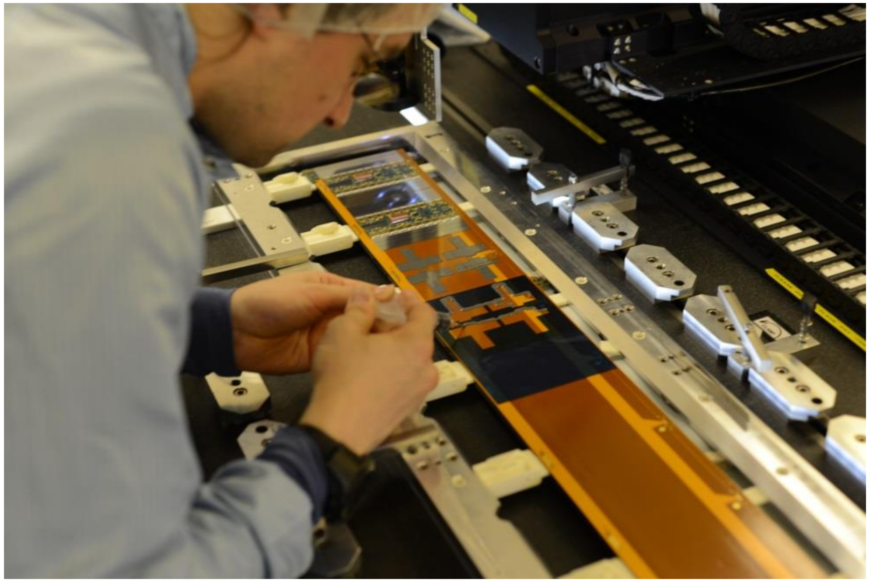
Noise Estimation Methods

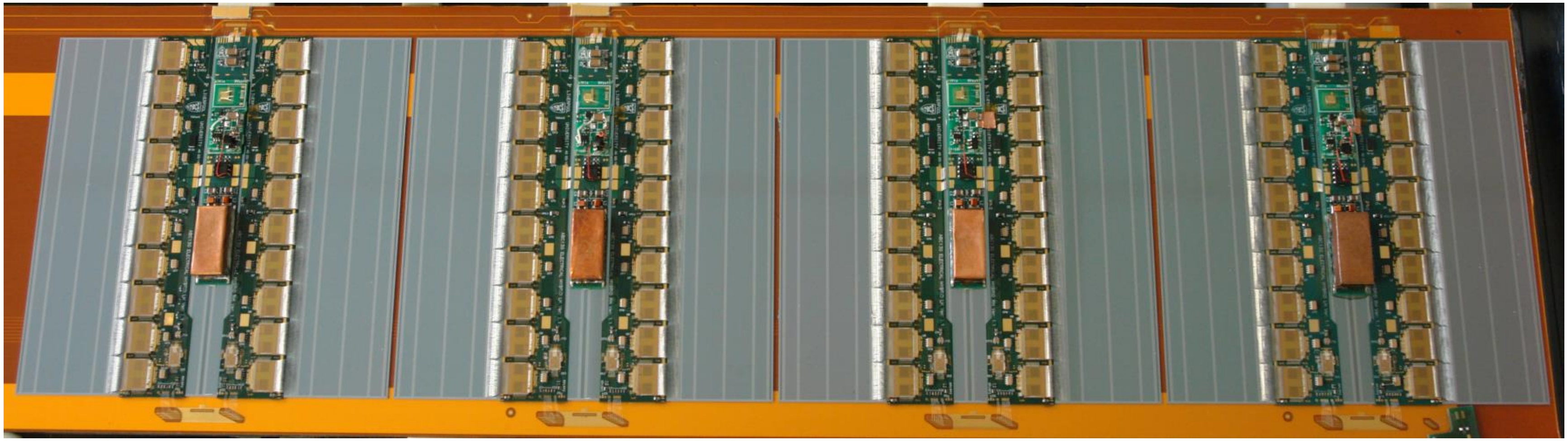
- Methods of noise estimation agree within 10-20%
- Additional set of points shown here includes the results of S-curve measurements with 1.5 fC of charge injection



Modules on Staves

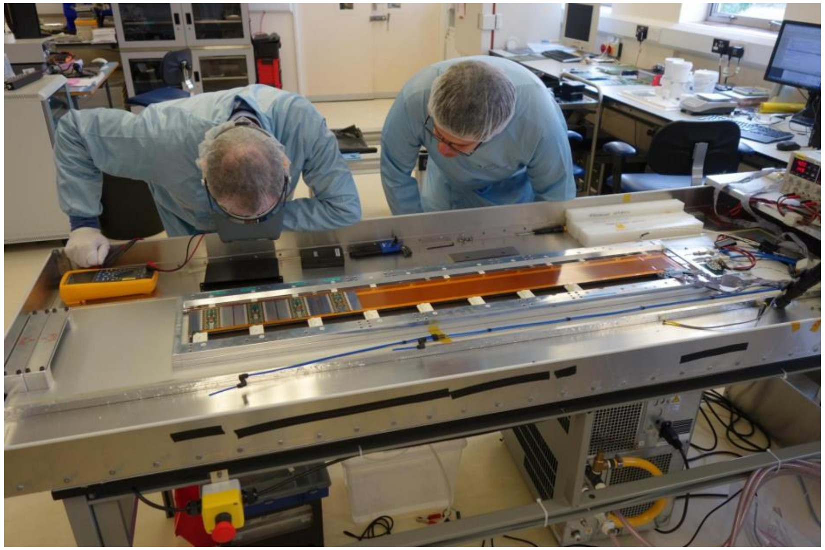
- Have mounted 8 modules on a double sided stave (4 per side)
- All modules on one side have HV-MUX, all modules on the other side do not
- Electrical end-of-stave card designed at DESY

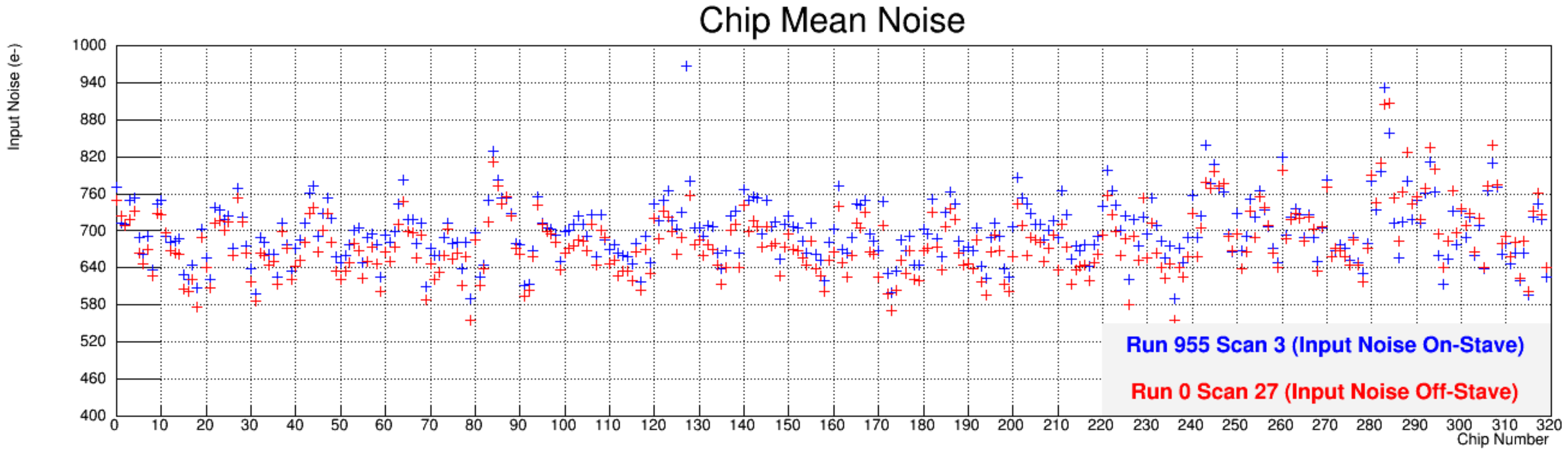




Results from Stavelet

- Stavelet successfully tested
- Noise on stave consistent with results before loading (within 15 ENC)
- Did take some playing to get this going!
- For example, long investigation showed that a filter had to be added to HV switch circuitry
- All results already fed back into the most recent powerboard design





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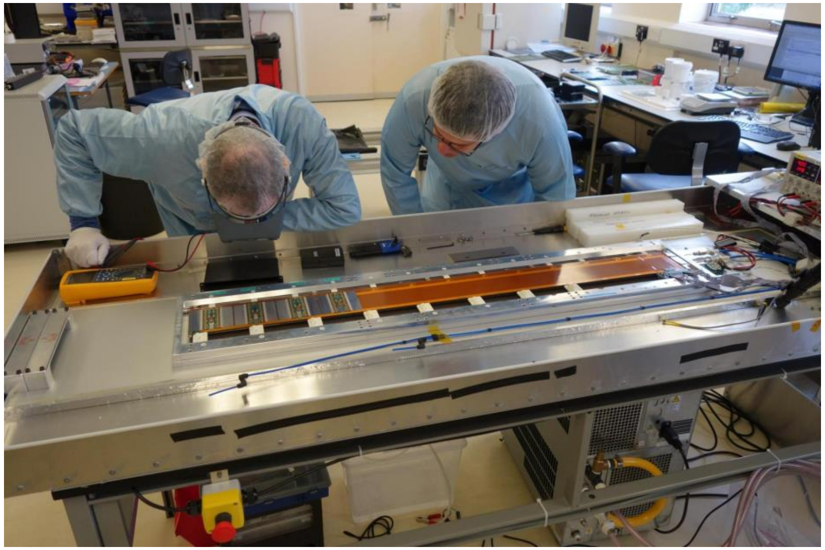
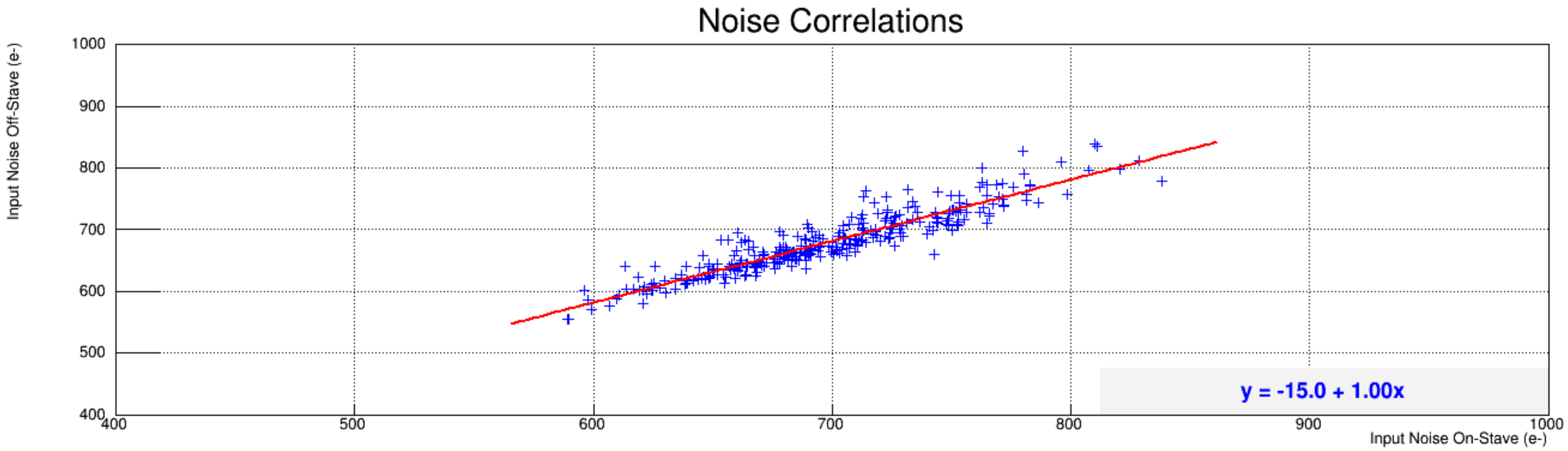
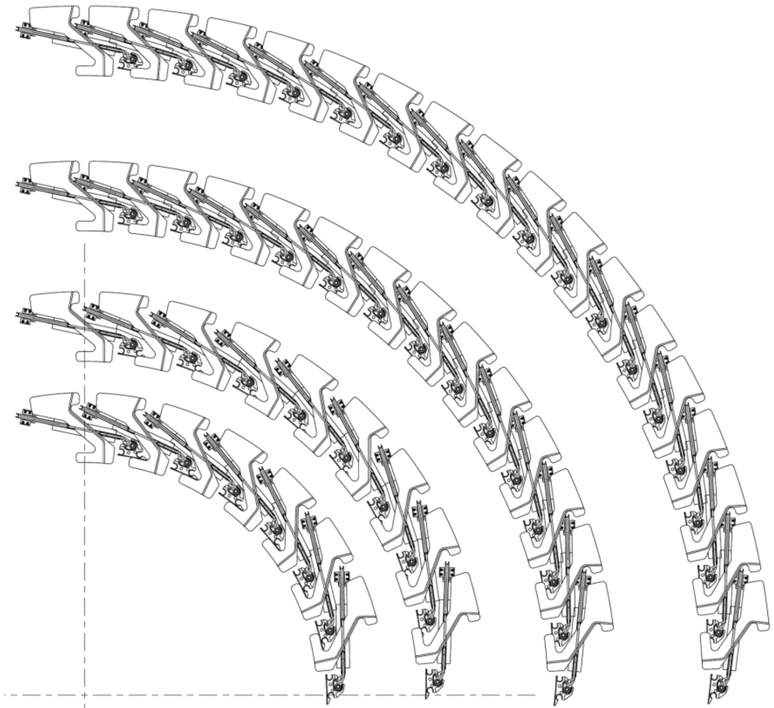
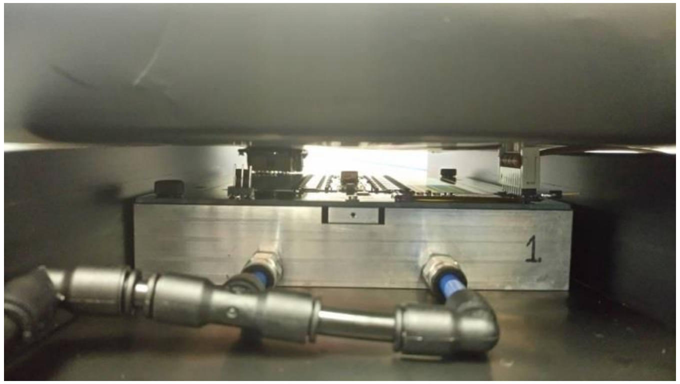




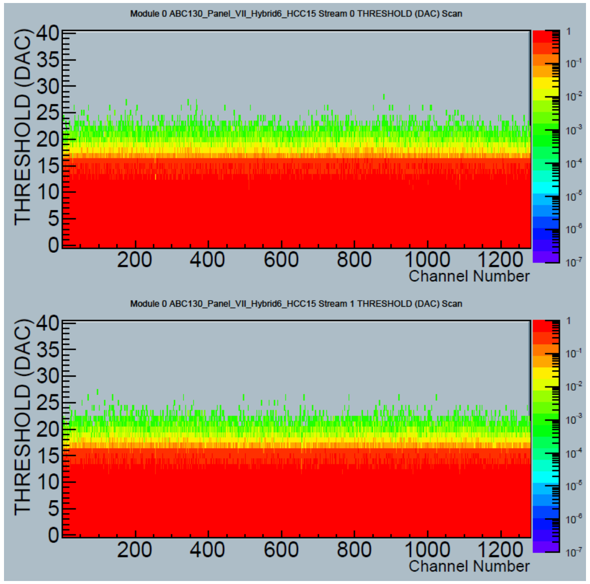
Towards system tests





- Eventually we want to have representative systems tests
- Including representative mechanical support, powering, cooling, cabling etc.

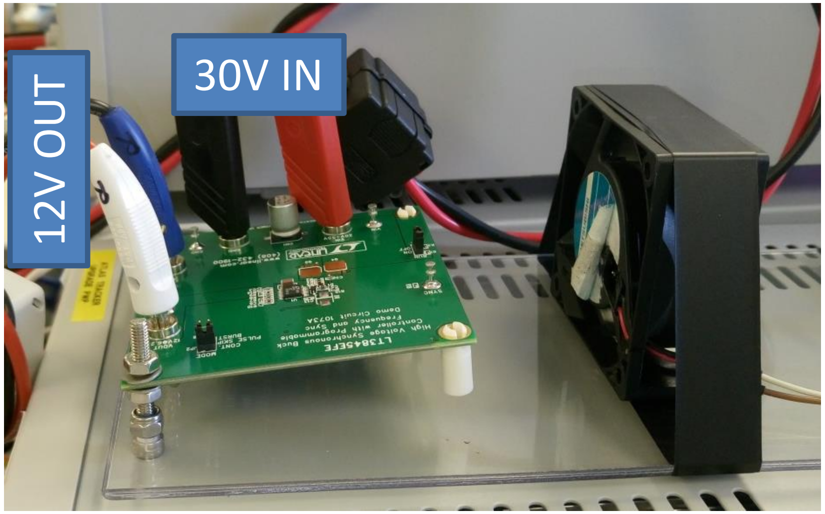
- Layout includes overlapping staves
  - Initial tests done using an aggressor module placed as close to the stave modules at possible
  - Modules in the end will be closer

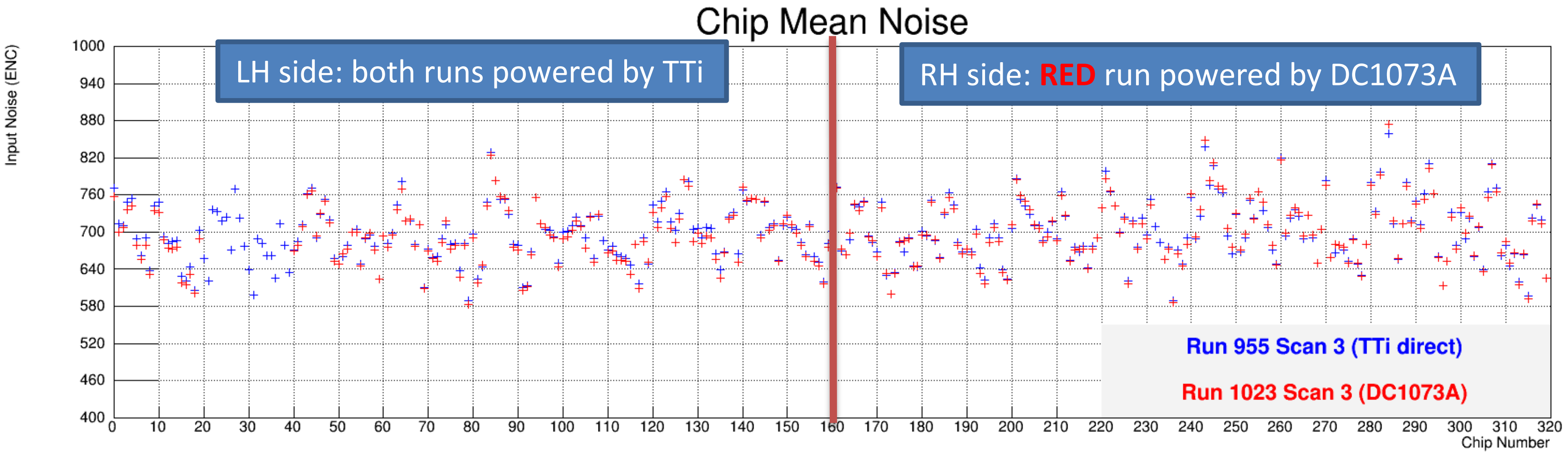


Towards system tests

- Eventually we want to have representative systems tests
- Including representative mechanical support, powering, cooling, cabling etc.

- Baseline powering includes a commercial 48-12 V DCDC at PP2 (inside the muon system)
  - Initial tests done powering one side of the stave with a commercial demonstrator board
  - Still not representative cable lengths and voltage drops





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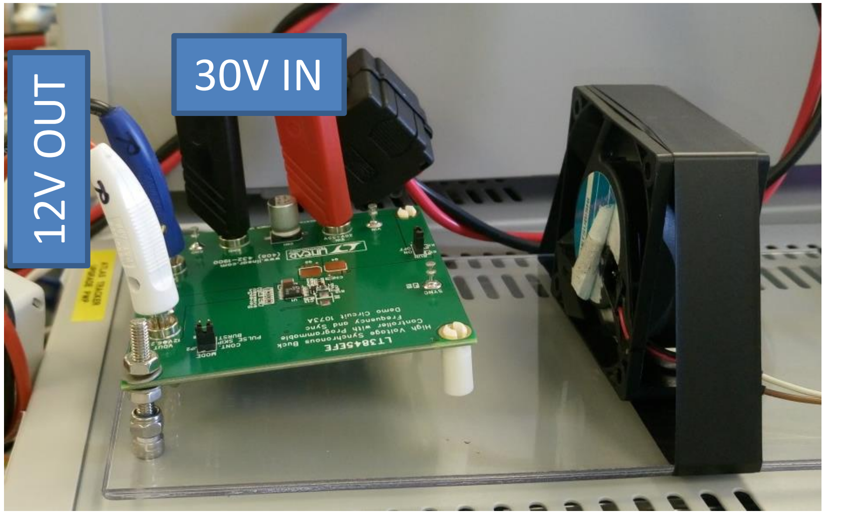

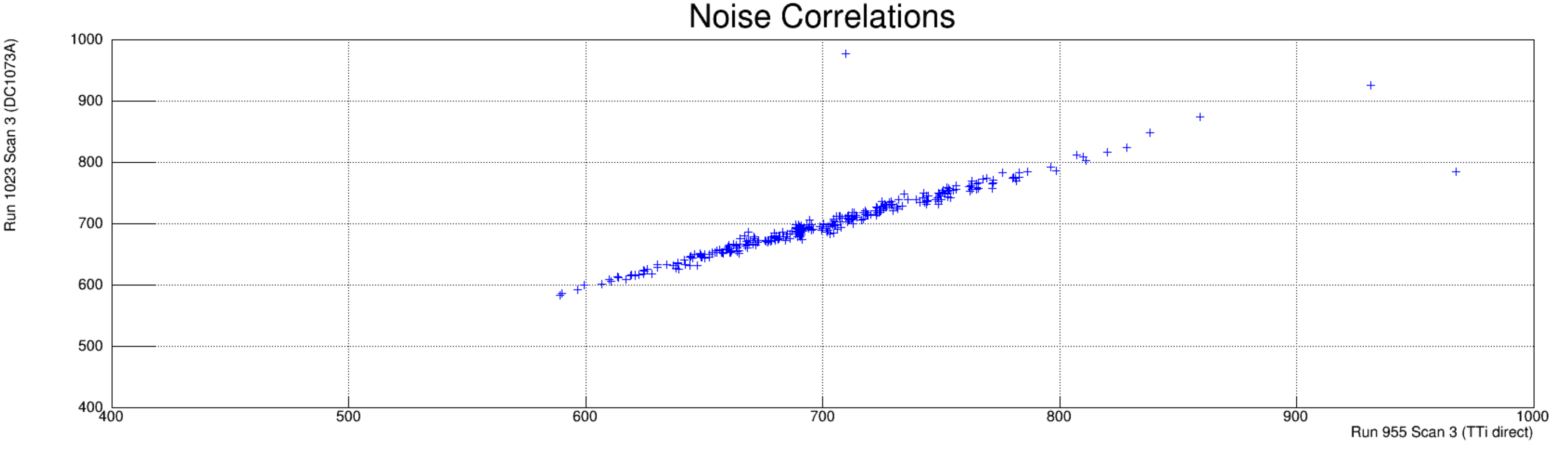

Coming Soon…

AMACv2 (submitted November 2017)
ABCStar/HCCStar to be submitted Q1 2018

Q1 2018 – full 13 module ABC130/HCC130 stave side (first with optical readout)
Q2 2018 – full 13 module ABC130/HCC130 double sided short strip stave (first full double sided)
Q2 2018 – electrical petal (first full petal)
Q3 2018 – full 14 module long strip stave (first full length and first long strip stave)
Q3 2018 – systems tests with 3 ABC130/HCC130 staves/petals (first test with proper overlap and representative powering chain)
Q3/Q4 2018 – first ABCStar/HCCStar modules
Q1 2019 – first Star staves (essentially final objects!)
Q3 2019 – preproduction (5%)
Q4 2019 – systems tests with 3 ABCStar/HCCStar staves/petals (first test with final objects)
Q2 2020 – systems tests with 8 ABCStar/HCCStar staves/petals (modularity of services)
Q3 2020 – production

Coming Soon…

AMACv2 (submitted November 2017)
ABCSta /HCCStar to be submitted 2018

Q1 2018 – ful ABC1 eadout)
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Q3 2020 – production

Disclaimer: not official, my own estimates

Conclusions

- Following the publication of the strip TDR in April 2017, development and prototyping has continued at a good pace
- We are on track to have submitted all of the final chips by early in 2018 and have first production module prototypes by the end of 2018
- Preproduction (2019) and production (2020) are feasible targets
- There is lots to do but the schedule suggests that we will be ready for HL-LHC in 2026

THANK YOU…

…QUESTIONS?

References

[1] ATLAS Collaboration, *Technical Design Report for the ATLAS Inner Tracker Strip Detector*, CERN-LHCC-2017-005 (2017).

[2] ATLAS Collaboration, *The ATLAS Experiment at the CERN Large Hadron Collider*, JINST **3** (2008) S08003.

[3] V. Re, M. Manghisoni, L. Ratti, V. Speziali, and G. Traversi, *Total ionizing dose effects on the noise performances of a 0.13 µm CMOS technology*, IEEE Transactions on Nuclear Science **53** (2006) 1599–1606.

[4] V. Re et al., *Review of radiation effects leading to noise performance degradation in 100 nm scale microelectronic technologies*, 2008 IEEE Nuclear Science Symposium Conference Record, 2008.

[5] X. J. Zhou, D. M. Fleetwood, R. D. Schrimpf, F. Faccio, and L. Gonella, *Radiation Effects on the 1/f Noise of Field-Oxide Field Effect Transistors*, IEEE Transactions on Nuclear Science **55** (2008) 2975–2980.