A Serializer ASIC at 5 Gbps for Detector Front-end Electronics Readout

1. Overview.
2. Test results of LOCs1, the 5 Gbps 16:1 serializer.
3. Test results of the LCPLL.
4. Test results of the CML driver.
5. Future work: LOCs6.

Jingbo Ye
On behalf of the ATLAS LAr Calorimeter Collaboration

Overview

1. Overview
2. LOCs1
3. LCPLL
4. The CML driver
5. LOCs6

- This R&D work for the upgrade of the readout of the Liquid Argon Calorimeter of ATLAS is funded by US-ATLAS and is carried out by the team of:

D. Gong, C. Liu, T. Liu, and A. Xiang

Department of Physics

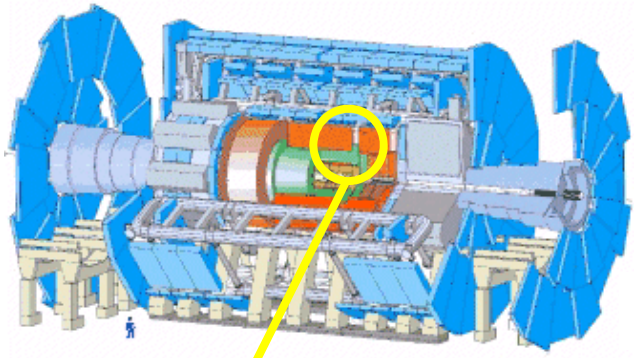
SMU

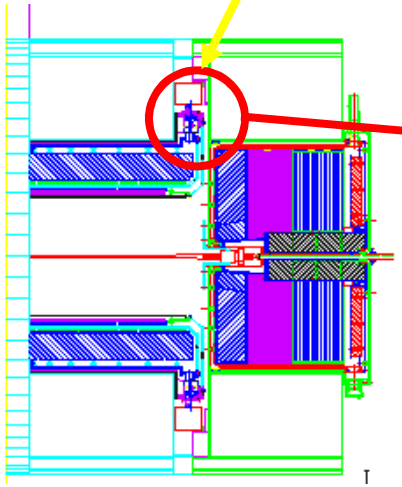
Dallas, Texas

Overview: the Present LAr Optical Link

1. Overview
2. LOCs1
3. LCPLL
4. The CML driver
5. LOCs6

The ATLAS detector



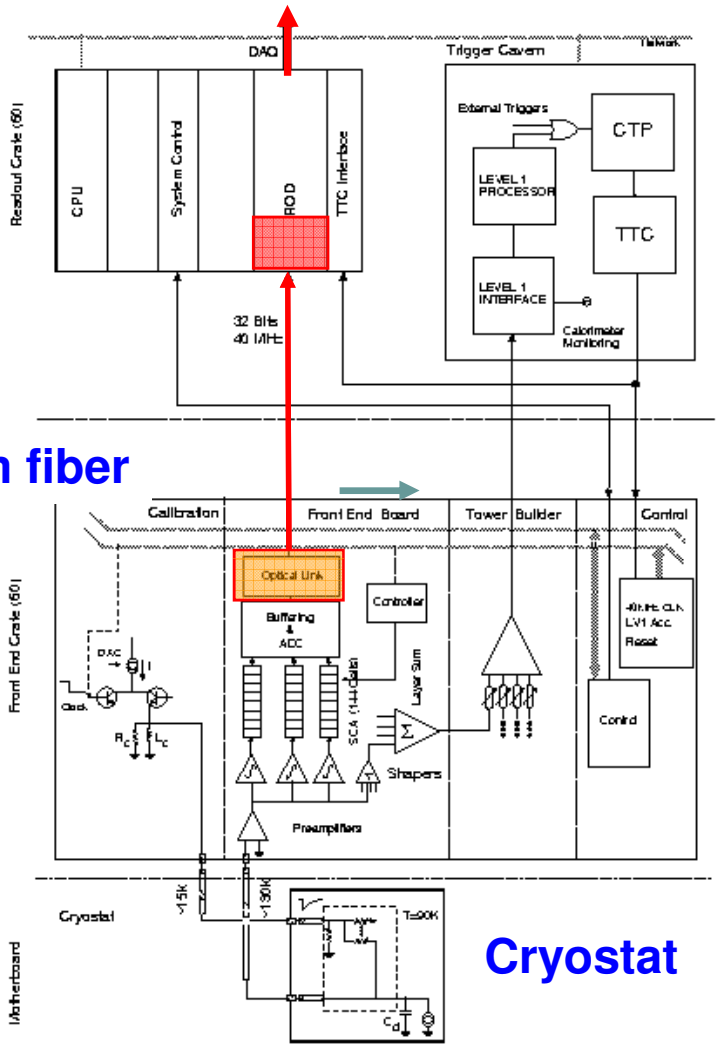


The LAr front end electronics box

Back End Crate

150 m fiber

Front End Crate



Cryostat

There are 128 chs/FEB, 1524 FEBs read out by the link. Total data rate is over 2Tbps for LArg.

Overview: the proposed upgrade

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2. LOCs1
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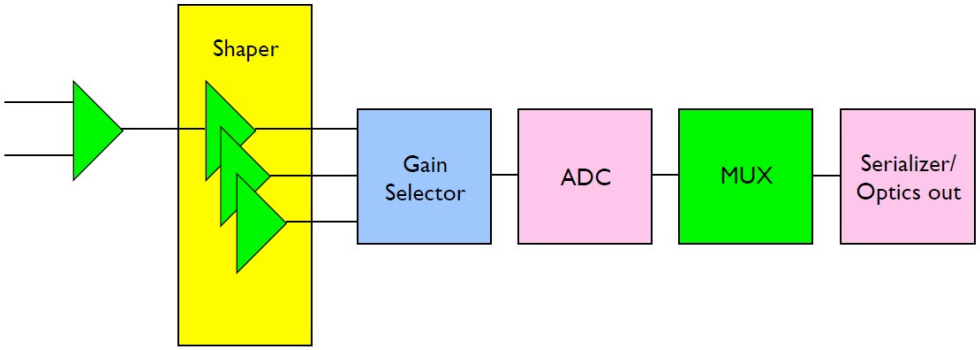
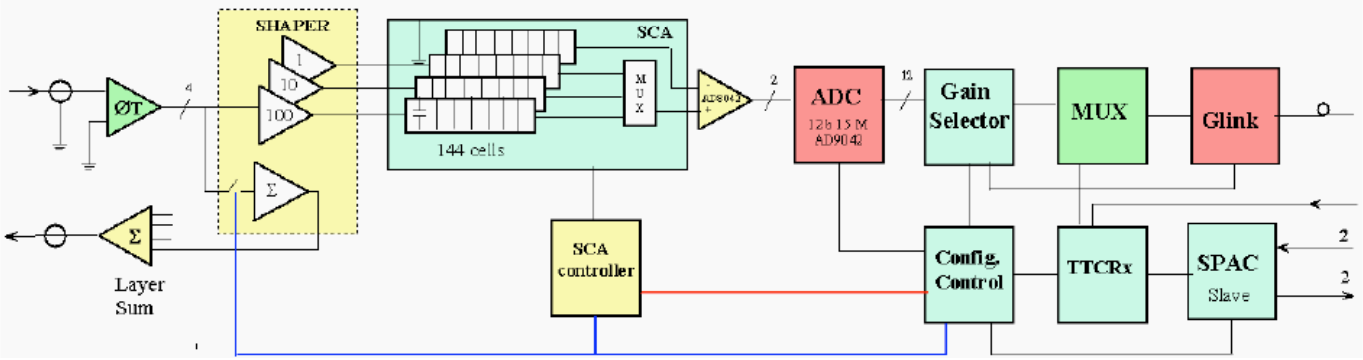
- The tentative FEB2 architecture:



L1 trigger off FEB:
1. Stream data at 100 Gbps.
2. Parallel fiber optics with redundant channels.
3. Fewer ASICs, simpler design.

- Compared with FEB1:



L1 trigger on FEB:
1. 1.6 Gbps over one fiber. No redundancy.
2. Analog pipeline with associated logic.
3. Total of 11 ASICs and rad-tol qualified COTS.

- Major requirements on the optical link:
  - 100 Gbps per FEB data bandwidth with 20% channel redundancy. A total bandwidth of about 150 Tbps.
  - Low power: 80 W/FEB. Design goal for the link: 20 W.
  - Radiation tolerant.

Overview: concept and ASICs

1. Overview
2. LOCs1
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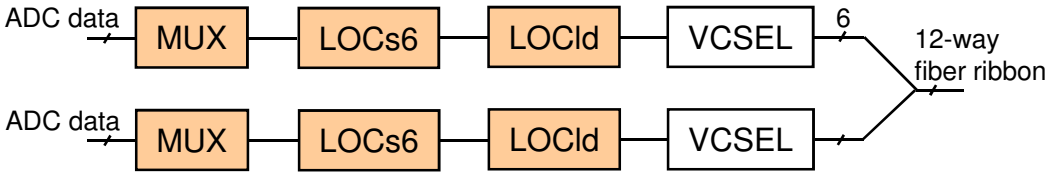
- The Link-on-Chip (LOC) is a concept we proposed for the upgrade of ATLAS LAr FEB optical link.
- The ASIC technology has been chosen to be a commercial 0.25 μm silicon-on-sapphire CMOS technology.
- Over time the concept of the transmitting side of the 100 Gbps link has been evolved to be:



  - MUX is the interface of the link to upstream electronics.
  - LOCs6 is a 6-lane serializer.
  - LOCld is a laser driver.
  - For the moment we choose the laser to be a VCSEL.
  - Packaging of these blocks has not been addressed.

- For the receiving side of the link we plan to use Serdes-embedded FPGAs. There we benefit from the developments in the Versatile Link common project.
- The most challenging part in this link is the serializer LOCs6. This is 6-lane serializer bank with redundancy switches. Each serializer needs to run at 8-10 Gbps. Details will be discussed later.

Overview: ASIC protopye

1. Overview
2. LOCs1
3. LCPLL
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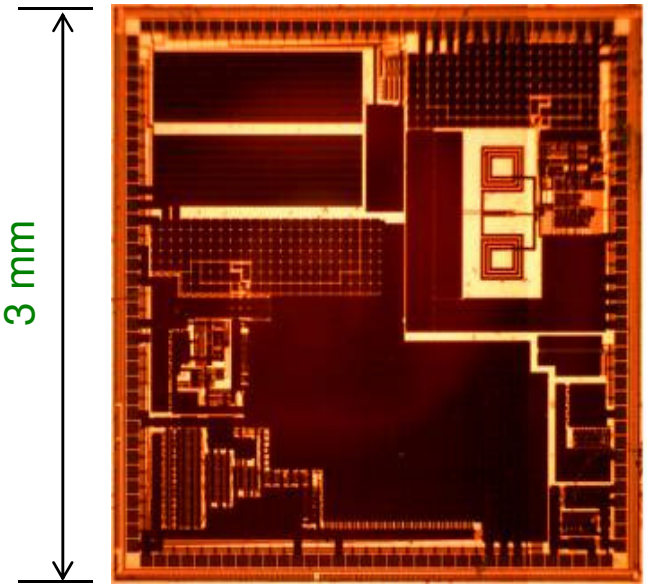
5. LOCs6

- To check the serializer design, and to probe the highest speed possible with this technology, we submitted a prototype chip which we call SMU_P1. In this 3 mm × 3 mm tile, we have the following designs:
  - LOCs1, a 5 Gbps 16:1 serializer.
  - The LCPLL, a 5 GHz LC VCO based phase locked loop.
  - The CML driver.
  - A divide-by-16 circuit.
  - A varactor, a voltage controlled capacitor.
  - An SRAM block, designed by INFN Milano.
- SMU_P1 was submitted for fabrication in Aug. 2009. The chips (143 of them) arrived at SMU in Nov. 2009. Test setup was prepared during that time window.
- Here we report the test results of LOCs1, the LCPLL and the CML driver.



SMU_P1

The 5 Gbps Serializer LOCs1

1. Overview
2. LOCs1
3. LCPLL
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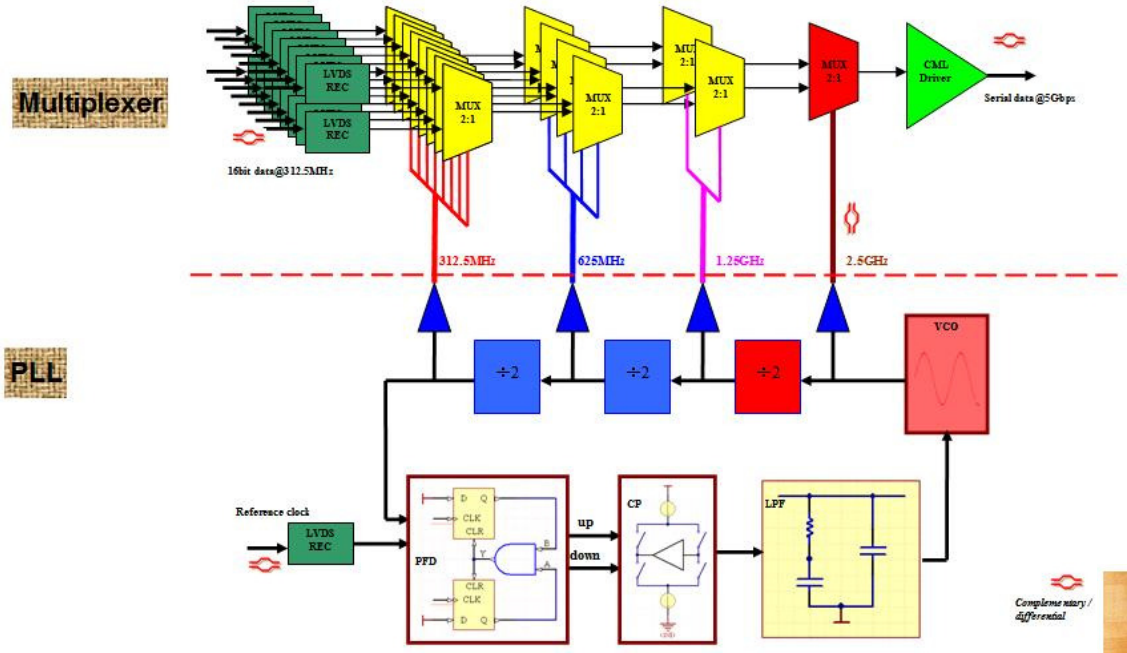
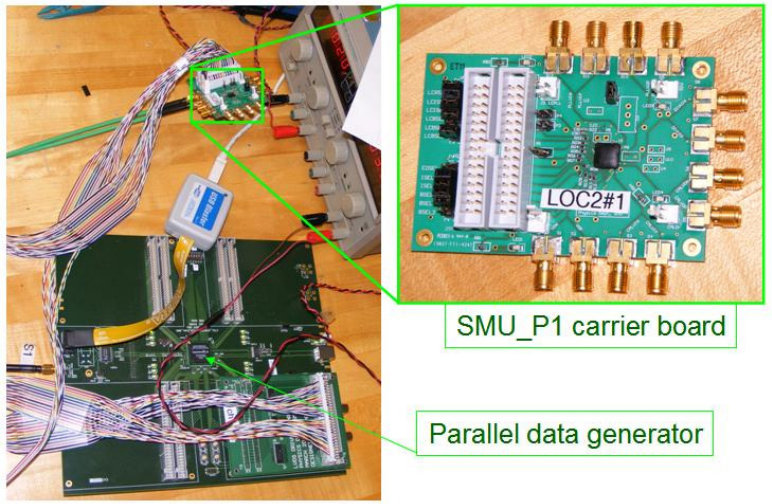
5. LOCs6

- LOCs1
  - A 16:1 serializer



- The design was carefully simulated and reviewed by a committee org.-ed by LAr.
- Test setup includes an FPGA based pattern generator, and a chip carrier board. A total of 12 carrier boards have been assembled.



The 5 Gbps Serializer LOCs1

1. Overview
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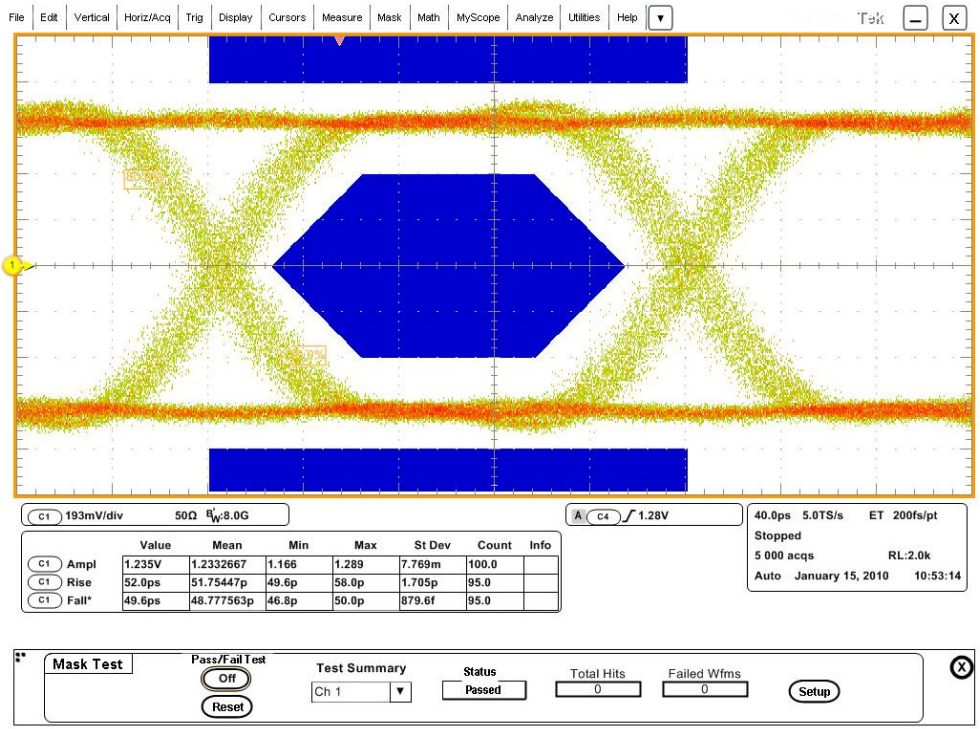
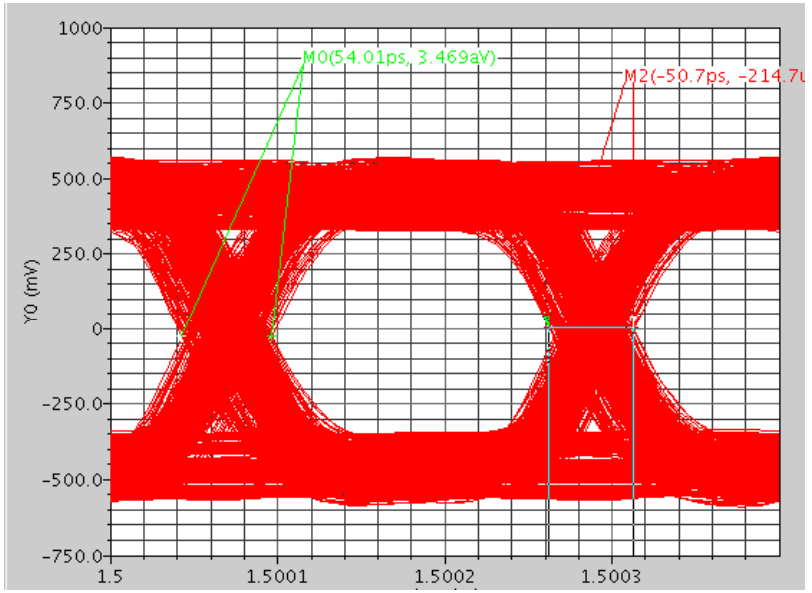
5. LOCs6

- Eye mask test



Eye mask at 5 Gbps. The mask is adapted from FC 4.25 Gbps and scaled up to 5 Gbps



Simulation result at 5 Gbps

The 5 Gbps Serializer LOCs1

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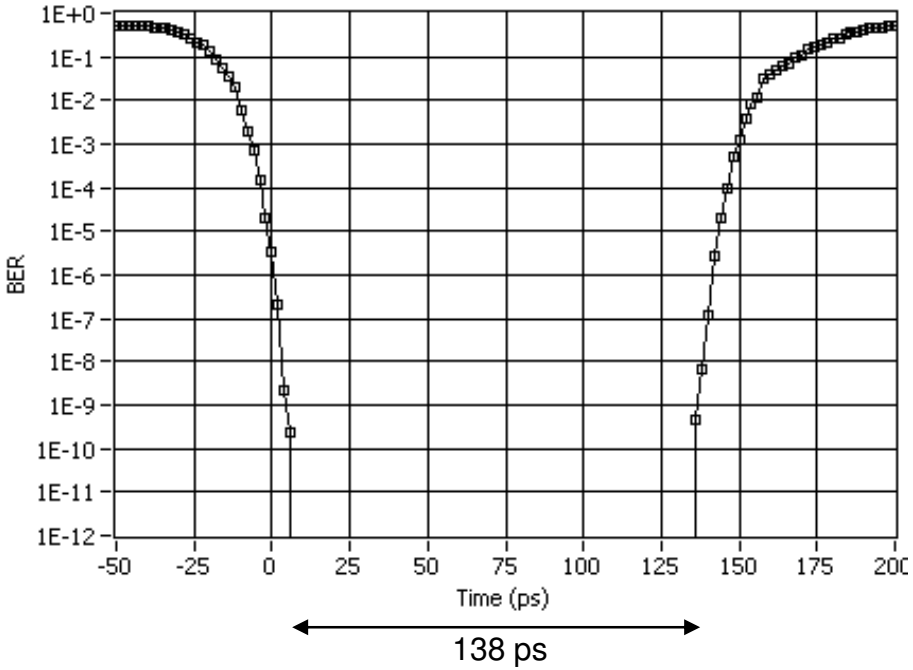
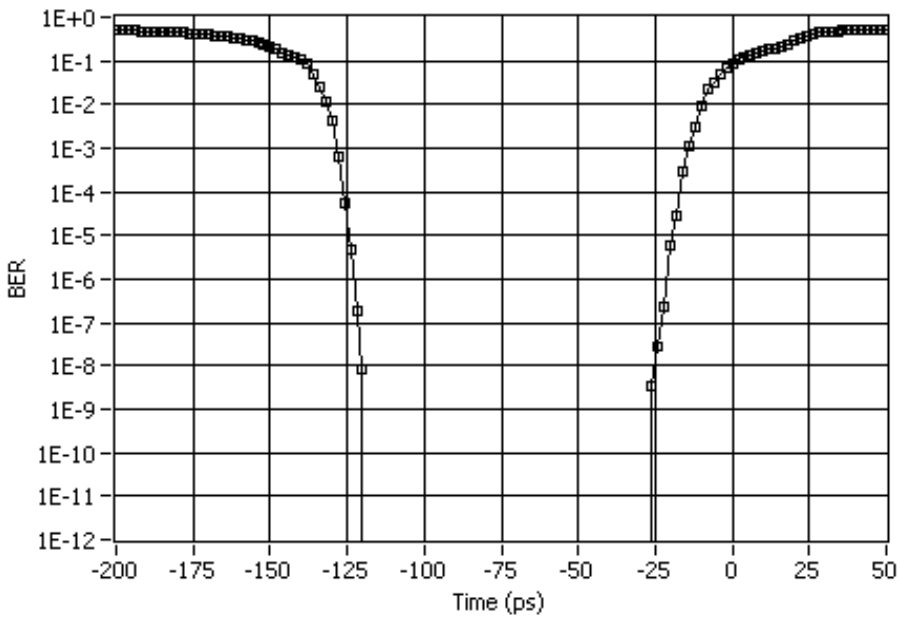
- BER tests



Bathtub scan at 5 Gbps.



Bathtub scan at 5.8 Gbps.

The 5 Gbps Serializer LOCs1

1. Overview
2. LOCs1
3. LCPLL
4. The CML driver
5. LOCs6

- Test results summary:
  - 12 chips wired bonded to PCBs for testing. Five boards have problems: 2 Vcc shorts, 2 Vcc open, 1 with a stuck bit. They are all traced to the place where the chip is encapsulate: chip problems? Wire bonding problems? Tests on more chips will tell.
  - For the 7 chips/PCBs that are working:
    - Range (Gbps): min: 3.8 – 4.0, max: 5.7 – 6.2.
    - Power (based on 1 chip): 507 mW at 5 Gbps.
    - Output signal at 5 Gbps:

amplitude (V)	1.16 ± 0.03
Rise time (ps)	52.0 ± 0.9
Fall time (ps)	51.9 ± 1.0
Random jitter (ps)	2.6 ± 0.6
Total deterministic jitter (ps)	33.4 ± 6.7
DJ: periodic (ps)	15.1 ± 3.4
DJ: data dependent (ps)	3.0 ± 2.3
DJ: duty cycle (ps)	15.2 ± 3.8
Total jitter at BER@1E-12 (ps)	61.6 ± 6.9
Eye opening at BER@1E-12	(69.3 ± 3.7)%
Bathtub curve opening at BER@1E-12 (ps)	122 ± 18 *

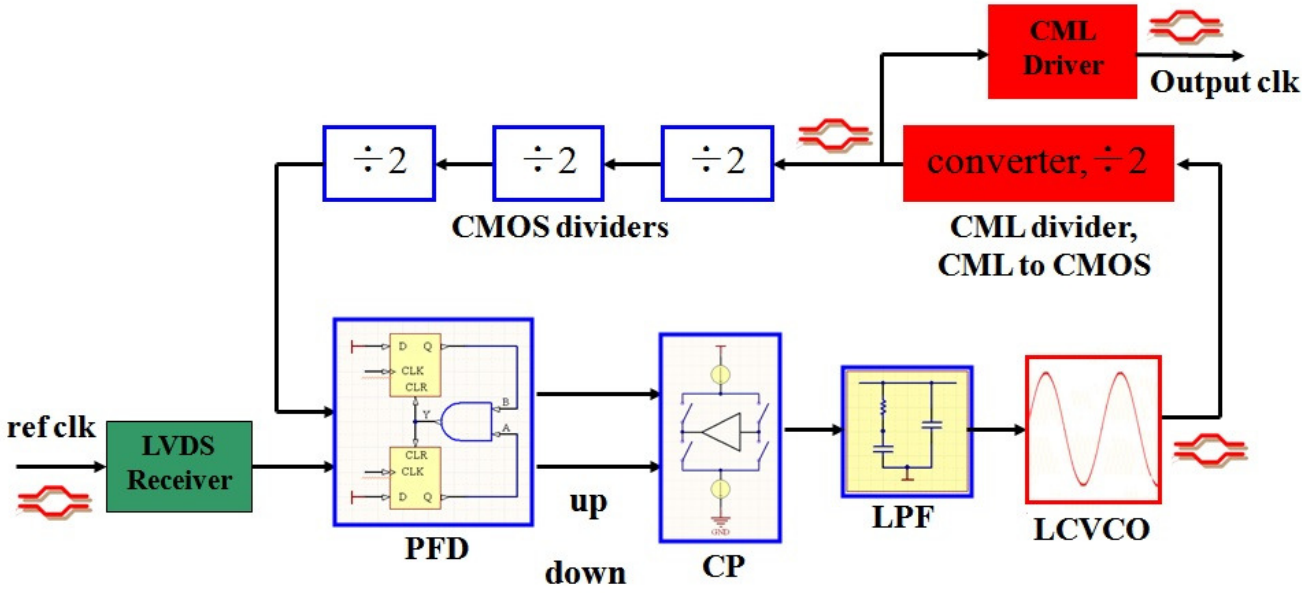
* Limited by instrument. Need to update equipment.

  - Preliminary: also successfully tested 1. at LN2 temperature; 2. with Vcc down to 2.0 V for high reliability and cryogenic applications.

The 5 GHz LCPLL

1. Overview
2. LOCs1
3. LCPLL
4. The CML driver
5. LOCs6

- LCPLL
  - Fast, low power, low jitter, compared with ring oscillator based PLL.
  - As of now no precise modeling of the C (varactor).
  - The design was not optimized due to manpower/time limitation, but reviewed by the committee organized by LAr.



The 5 GHz LCPLL

1. Overview
2. LOCs1
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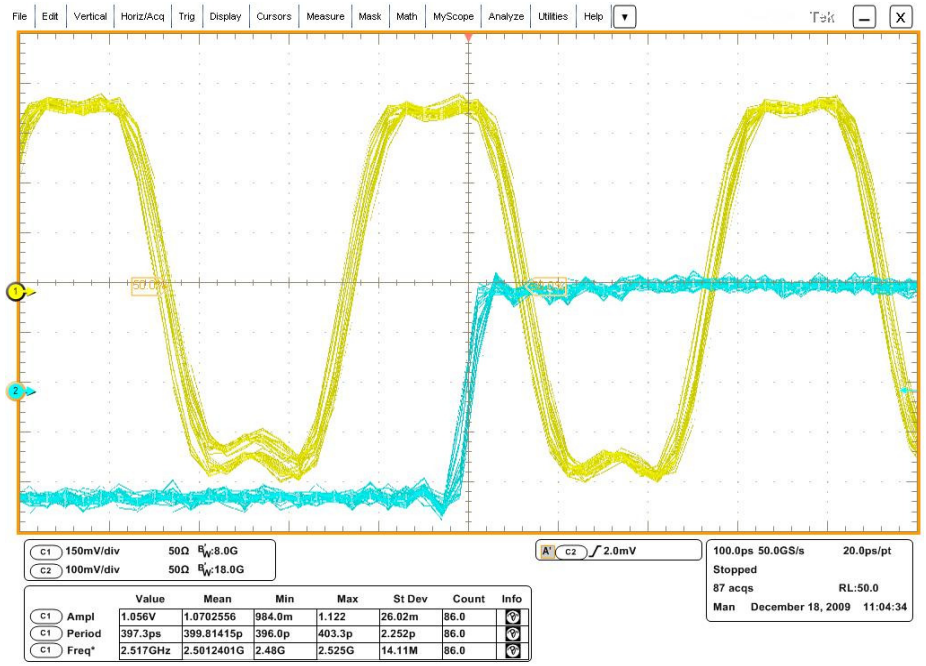
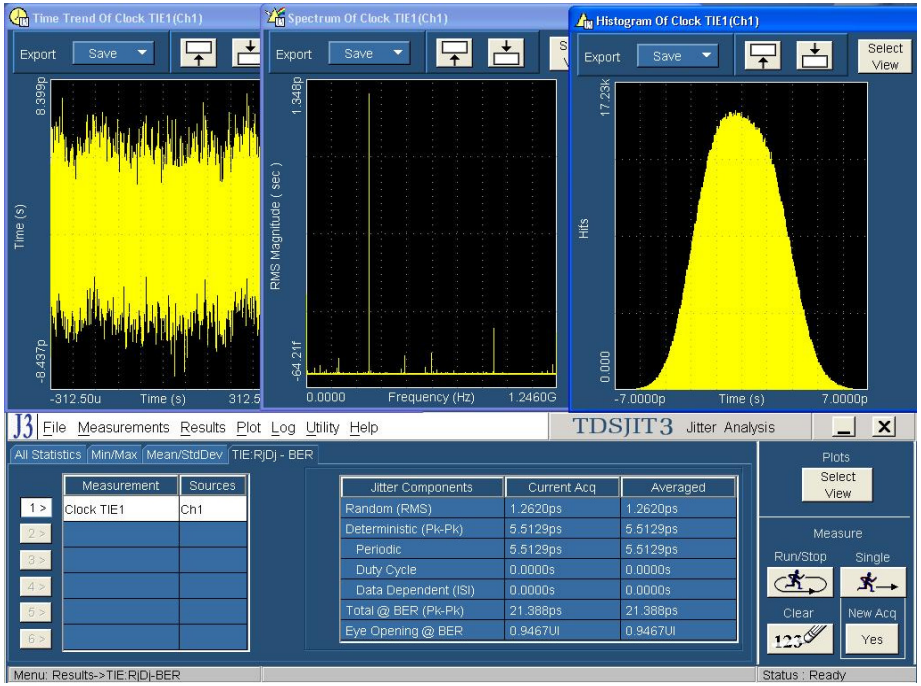
- Test results.



The output clock locks to the input clock.



The jitter analysis.

The 5 GHz LCPLL

1. Overview
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- Test results.

	lower limit				higher limit			
Board ID	1	2	3	4	1	2	3	4
VCO frequency (GHz)	4.752	4.616	4.480	4.744	4.984	5.008	4.968	4.992
input freq (MHz)	297.0	288.5	280.0	296.5	311.5	313.0	310.5	312.0
output freq (GHz)	2.38	2.29	2.24	2.37	2.50	2.51	2.484	2.50
Ampl (pos – neg) (V)	1.06	1.22	1.30	0.98	1.07	1.21	1.30	0.98
rise time (ps)		66.2	47.0	67.1		67.2	42.1	66.1
fall time (ps)		64.6	46.5	68.5		66.8	41.9	66.4
Random jitter RMS (ps)	1.28	2.49	2.05	1.81	1.26	1.06	1.08	1.83
Deterministic jitter (ps)	12.61	11.00	13.95	15.46	5.51	5.10	16.63	8.43

- Tuning range: 4.7 to 5.0 GHz. Simulation: 3.8 to 5.0 GHz. Possible cause: the first stage divider.
- Power consumption: 121 mW at 4.9 GHz. (compare: ring oscillator based PLL, 173 mW at 2.5 GHz)

The 5 GHz LCPLL

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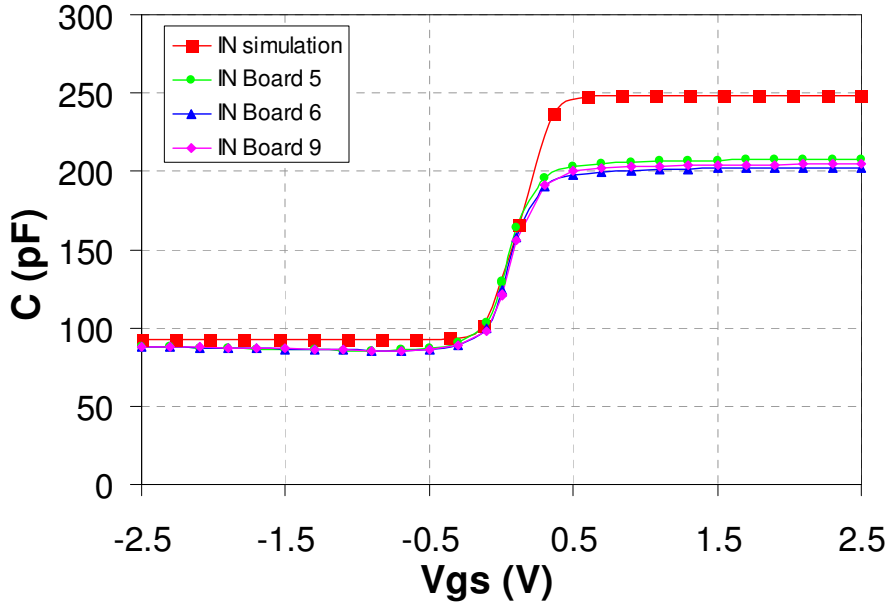
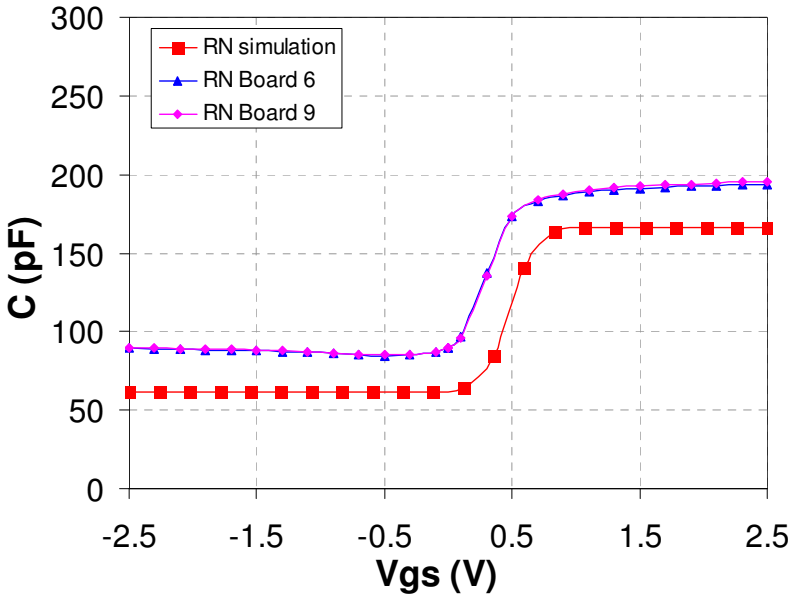
- Debug about the narrow tuning range, possible two causes: not a well behaved varactor, or the first stage divider.
  - Varactor measurements (thanks to F.Lanni, S.Rescia and H.Chen at BNL)





  - We use RN type varactors in the present design.
  - Varactors behave well although the absolute values deviate from what are simulated.

The 5 GHz LCPLL

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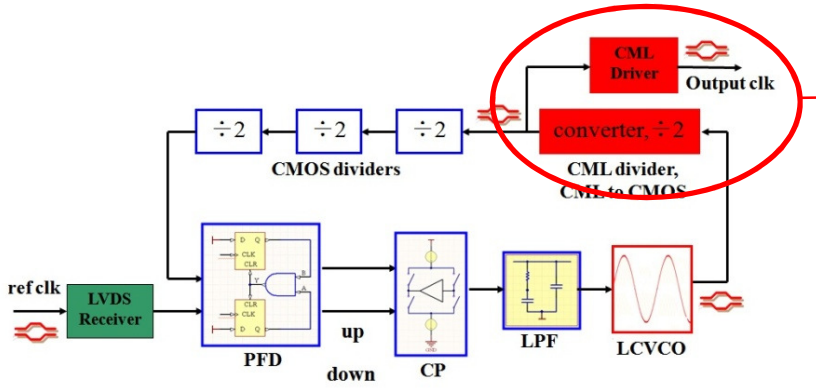
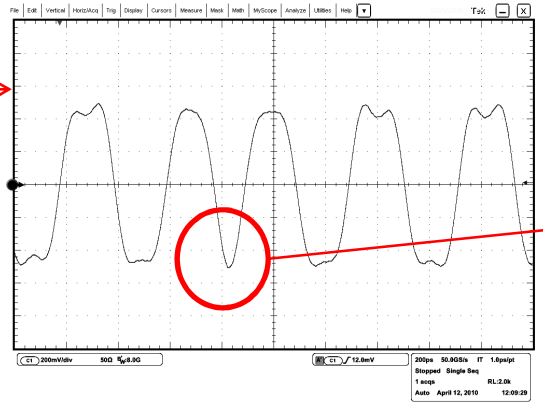
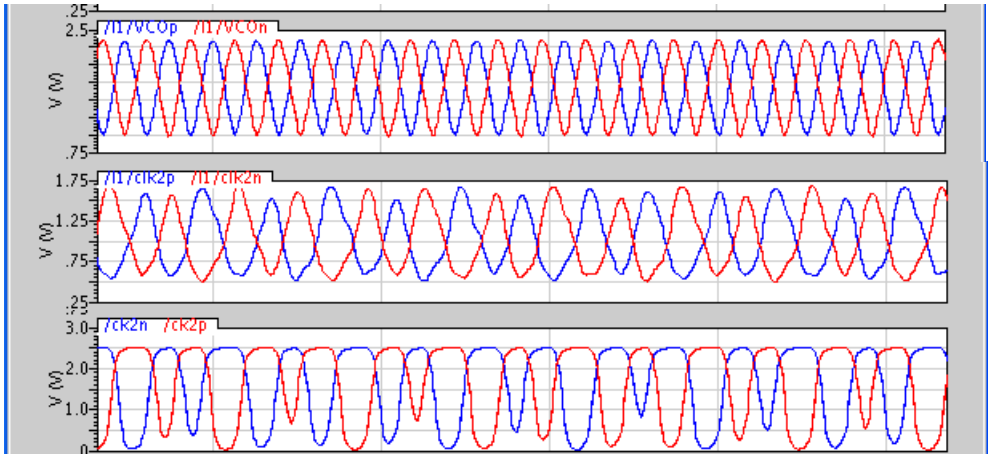
- The first stage divider, the measurement:





The output exhibits an abnormal cycle when the control voltage (Vctrl) to the LCVCO is at1.5 V.

- The simulation:



LCVCO output when Vctrl = 1.5 V.
The waveform is perfectly okay.

The output of the first ÷2 has distorted waveform.

The output of the CML to CMOS converter exhibits the same waveform as measured at the CML driver output.

- We think that's the cause. **It can and will be fixed in the next design.**

The CML driver

1. Overview
2. LOCs1
3. LCPLL
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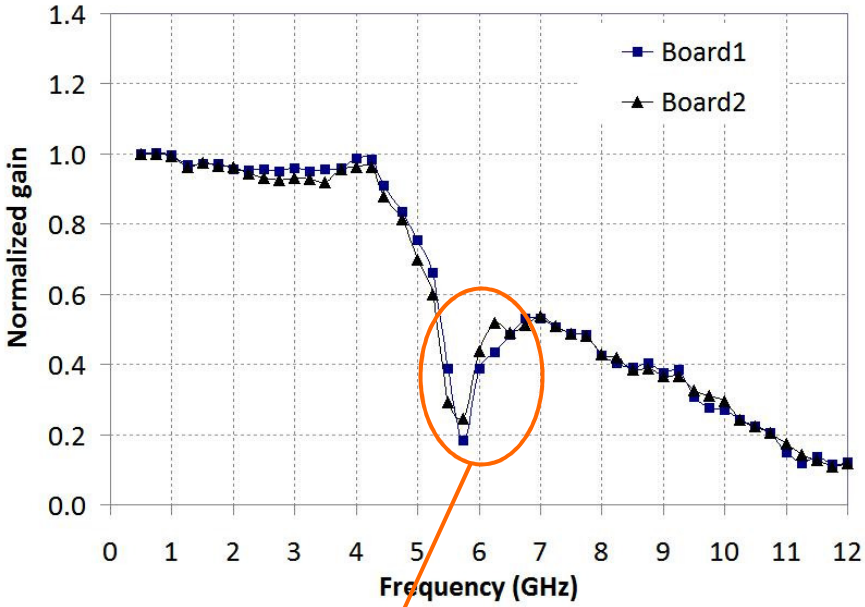
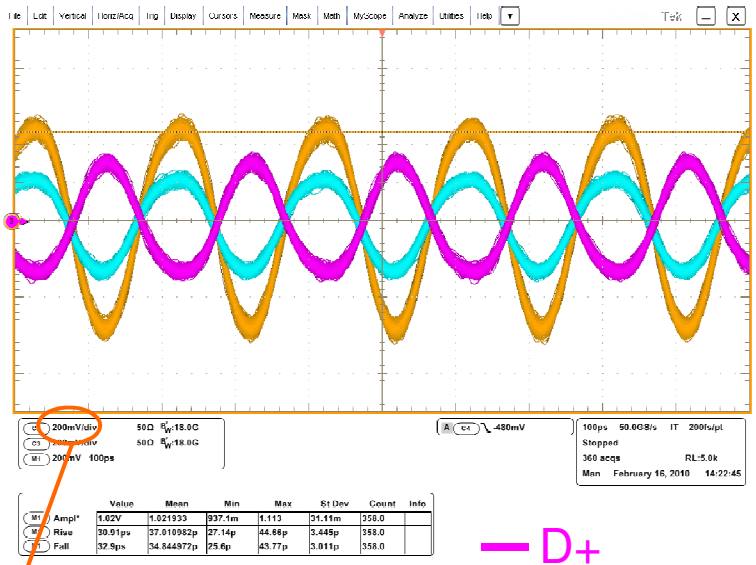
5. LOCs6

- The CML driver is a copy of the output driver used in LOCs1.
  - We single out this driver to study the possibility of a 10 Gbps link. But we did not have time to optimize the design, again due to limited manpower and time before the submission.
- Test results.



Under investigation

Output waveform, 5 GHz



200 mV/div.

D+
D–
D+ – D-

The CML driver

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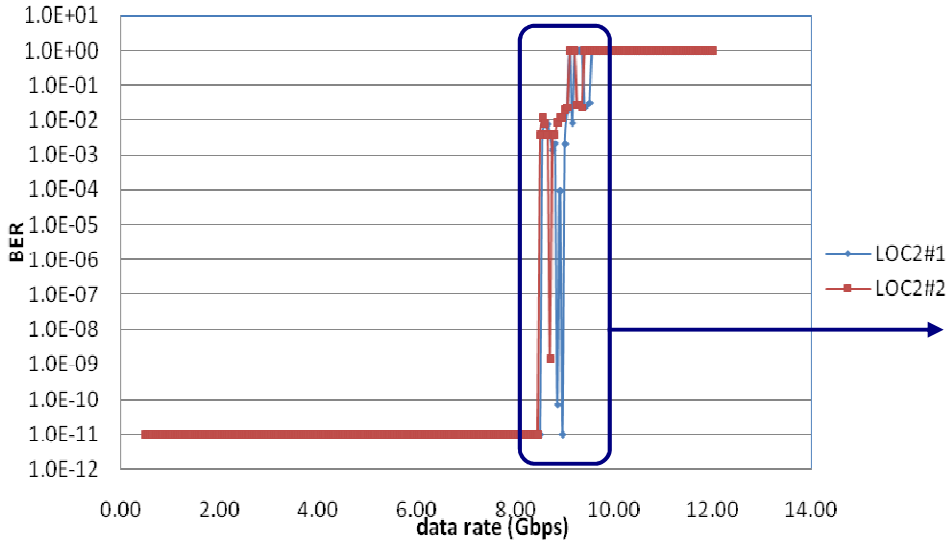
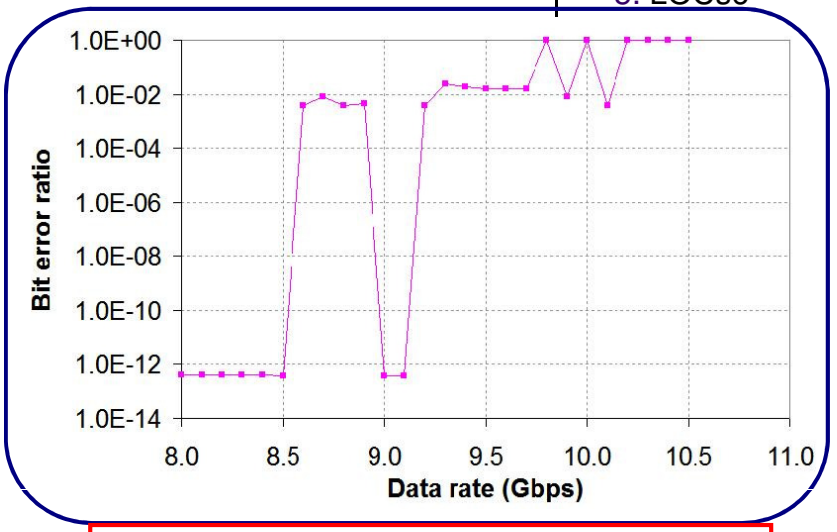
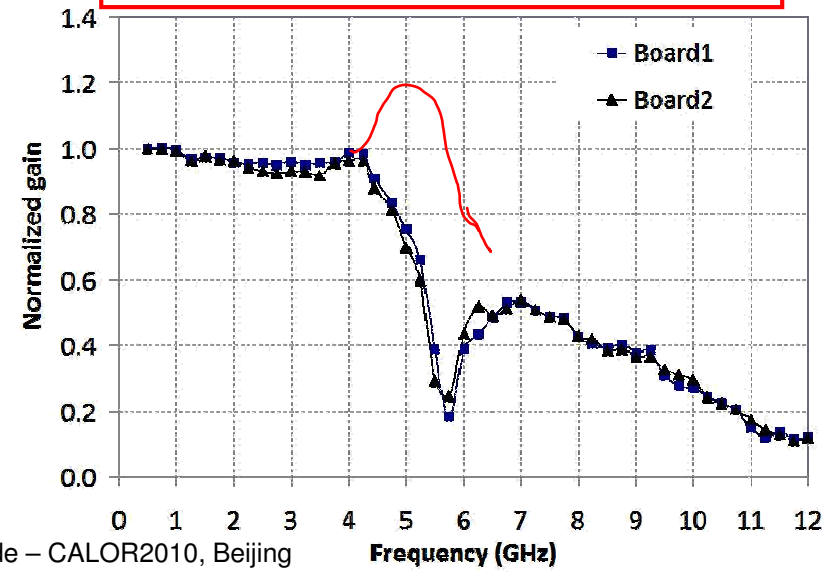
- Test results.
  - Without receiving side equalizer.





Good for 8 to 8.5 Gbps without signal equalization on the receiving side.

  - With receiving side equalizer (FPGA), we tested this driver up to 11 Gbps (limited by instrument).
- Future tests.
  - Understand the dip at ~6 GHz.
- Possible future improvements.
  - Boost frequency response (pre-emphasize) at ~5 GHz.



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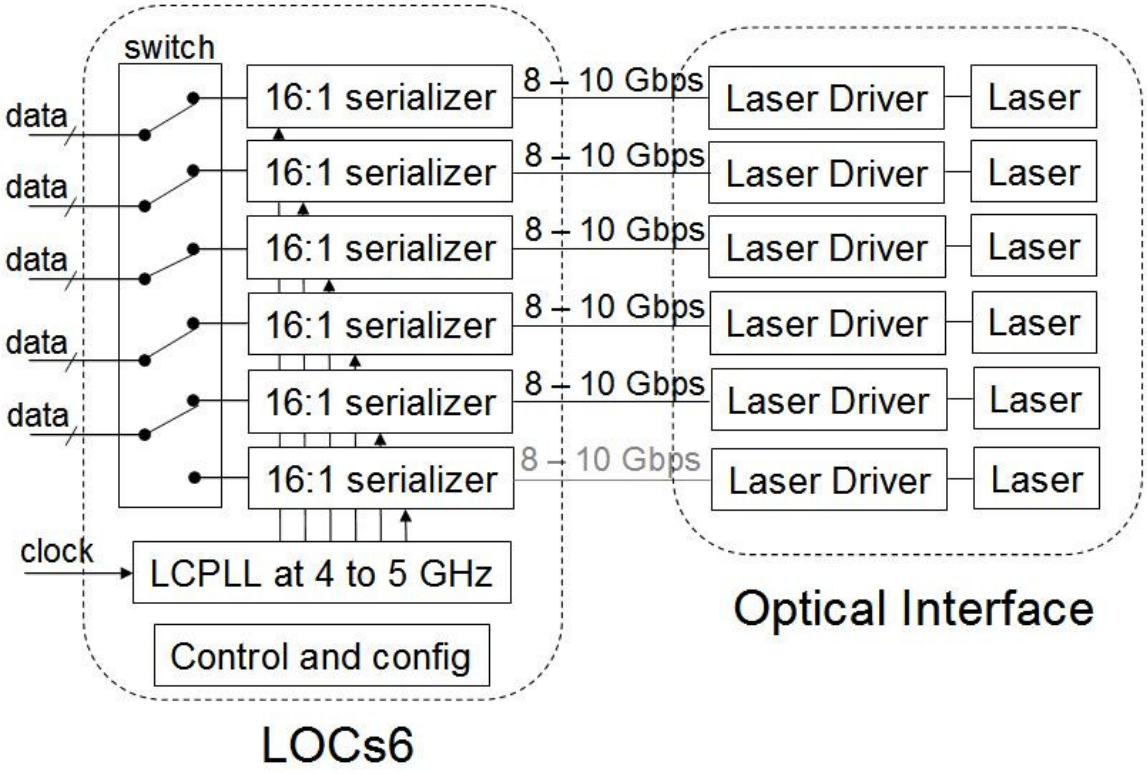
Future work: LOCs6

- To meet the challenges of a link of 100 Gbps per FEB, we propose:
  - Two serializer chips per FEB with a 12-way fiber ribbon.
  - The serializer LOCs6 block diagram is shown below.
  - This way a 20% redundancy can be implemented.
  - By sharing the clock unit, we hope to reduce the power.
- The plan: design LOCs6 in 2010 – 2011.



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Acknowledgements

- We thank US-ATLAS for providing the research funds. We hope that the funds will continue at a proper level to the work in the future.
- We are deeply grateful to Paulo Moreira for his kind help throughout the design of LOCs1. Without his support, we would not be possible to be here today to talk about this ASIC.
- We also would like to thank Fukun Tang, Mauro Citterio, Francesco Lanni and many other collaborators in our community for their kind help and support in this project.
- We would like to thank Suen and PK from IPAS for helping us in the test setup.