

# ATLAS LAr Calorimeter Readout Electronics Upgrade R&D for sLHC

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*On behalf of the ATLAS Liquid Argon Calorimeter Group*

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**BROOKHAVEN**  
NATIONAL LABORATORY

*a passion for discovery*



# Outline

## ■ Introduction

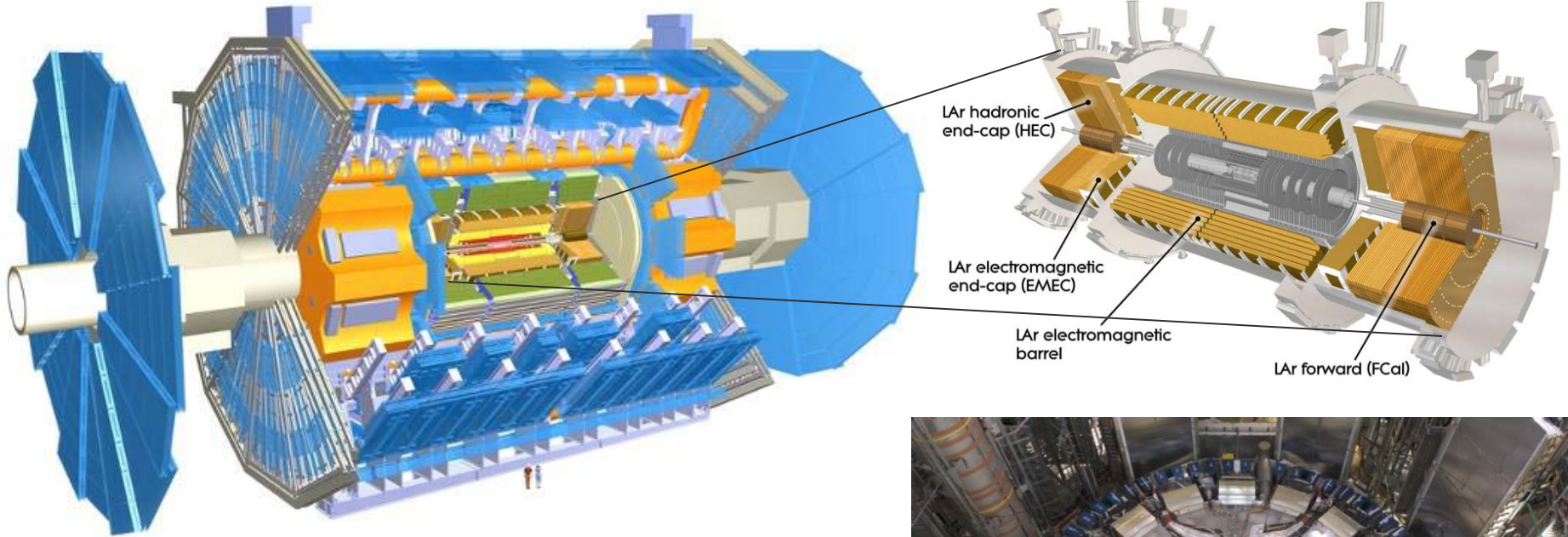
- ATLAS Liquid Argon Calorimeter
- Current LAr Readout Electronics
- LAr Electronics Upgrade Motivations

## ■ Readout Electronics Upgrade R&D Studies

- Front-end mixed-signal ASIC design
  - BNL, Columbia Univ., Univ. of Penn., INFN Milan, IN2P3
- Radiation tolerant optical link in Silicon-on-Sapphire
  - SMU
- High speed back-end processing unit based on FPGA
  - BNL, Univ. of Arizona, SUNY Stony Brook, IN2P3 LAPP, INFN Milan, Dresden, CERN
- Power supply distribution scheme
  - BNL, Yale, INFN Milan, Univ. of Milan

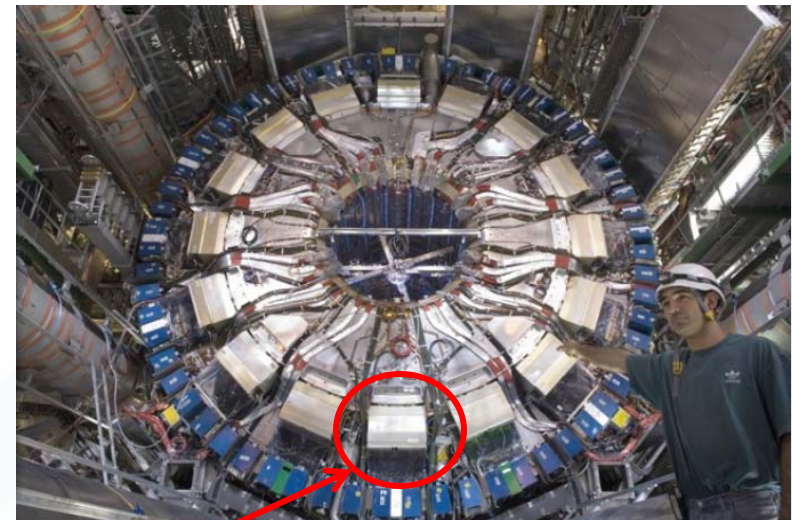
## ■ Summary

# ATLAS Liquid Argon Calorimeter (LAr)



## ■ Liquid Argon Calorimeter

- **Electromagnetic Barrel (EMB)**
  - $|\eta| < 1.475$  [Pb-LAr]
- **Electromagnetic End-cap (EMEC)**
  - $1.375 < |\eta| < 3.2$  [Pb-LAr]
- **Hadronic End-cap (HEC)**
  - $1.5 < |\eta| < 3.2$  [Cu-LAr]
- **Forward Calorimeter (FCAL)**
  - $3.1 < |\eta| < 4.9$  [Cu,W-LAr]



Front End  
Crate

Barrel calorimeters in  
detector hall, surrounded  
by barrel toroids

# Current LAr Readout Electronics

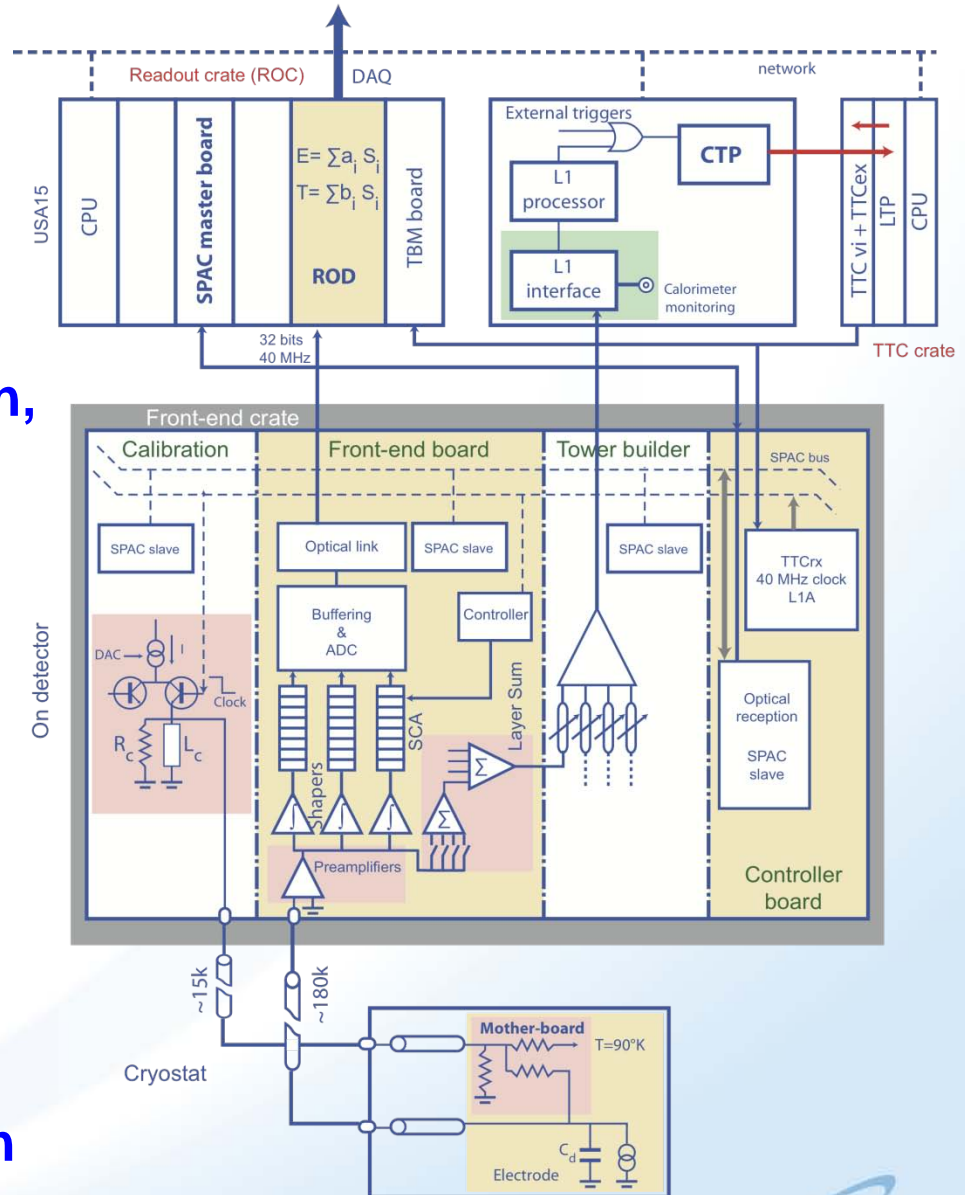
## 182,468 detector channels

## Front-end Electronics

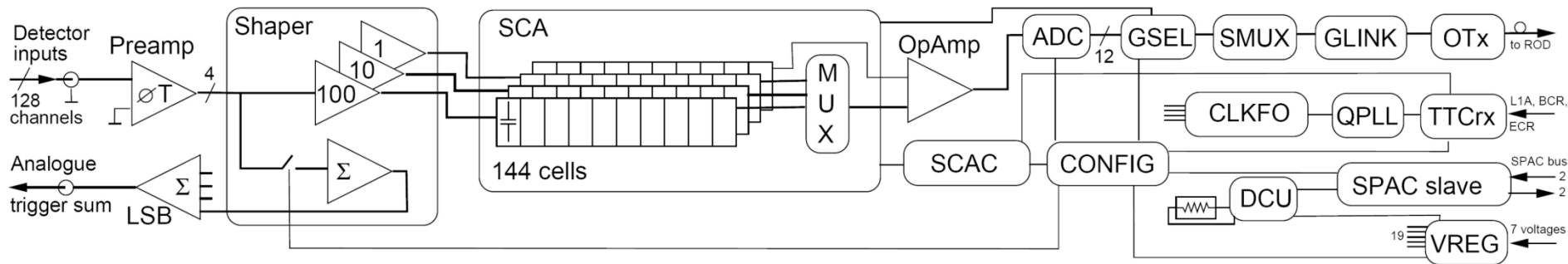
- 58 Front End Crates
- 1524 Front End Boards
- ~300 other boards (calibration, tower builder, controller, monitoring)
- 58 LV Power Supplies
- ~1600 fiber optic links between FE and BE

## Back-end Electronics

- 16 Back End Crates
- 192 Read Out Driver Boards
- 68 ROS PCs
- ~800 fiber optic links between ROD and ROS



# Current Front-end Architecture



## ■ FEB Complexity

- 11 ASICs
- Several technologies with obsolescence of some technologies (e.g. DMILL)
- 19 voltage regulators
- Analog pipelines (SCA)
- ~80W/board, water cooled

## ■ Radiation/lifetime issues

- Qualified for 10 years LHC operation
- Limited number of spares (~6%)

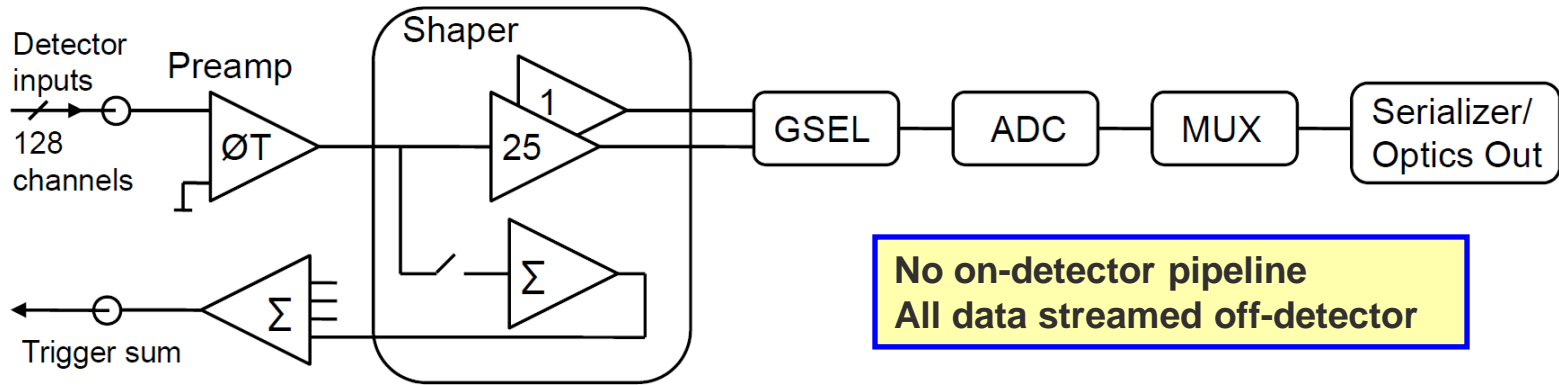
## ■ Other limitations

- L1 trigger rate  $\leq 100\text{kHz}$
- L1 trigger latency  $\leq 2.5\mu\text{s}$
- Consecutive L1 trigger spaced more than 125ns
- Fixed analog trigger sums

## ■ FEB Upgrade

- Component-level replacement impossible
- Full replacement based on current technologies
- No increase of power budget

# Proposed Front-end Architecture



## ■ Proposed FEB baseline architecture keeps many options open

- Shaping and gain settings
- Analog vs. digital pipeline
- On/off detector pipeline
- Analog vs. digital gain selector
- Possibly provide analog trigger sums to decouple potential trigger upgrade

## ■ FEB upgrade propagates to other boards

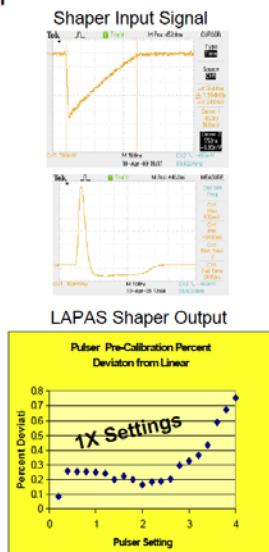
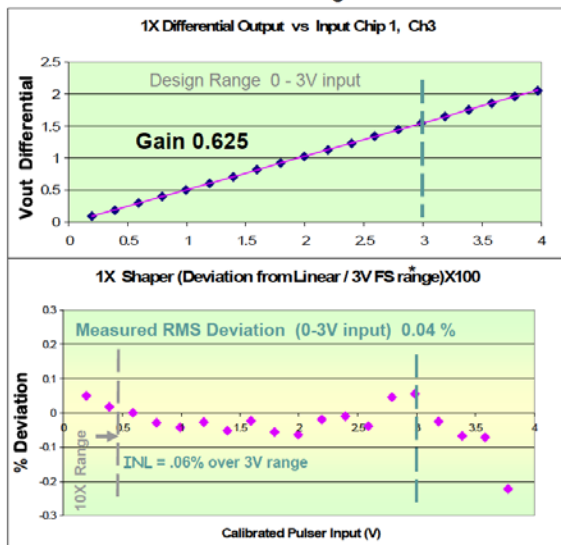
- Digitization at each bunching crossing, data rate is  $\sim 100\text{Gbps/board}$
- Higher speed, higher radiation resistance optical link
- LV power supplies
- Back-end electronics
- Possibly interface to L0Calo/L1Calo digitally



# Analog Front-end: Preamp & Shaper

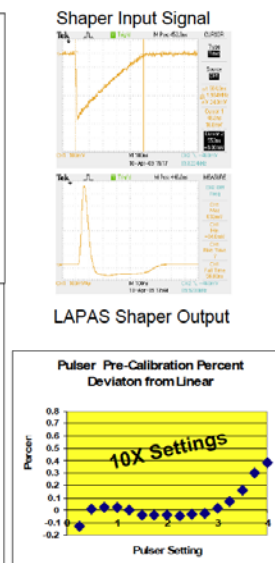
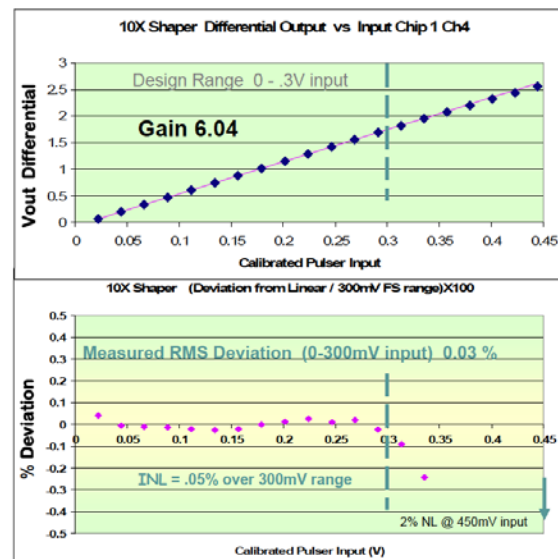
## LAPAS ASIC Automated Linearity Measurement

Using AFG3252 & MSO4401



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Using AFG3252 & MSO4401



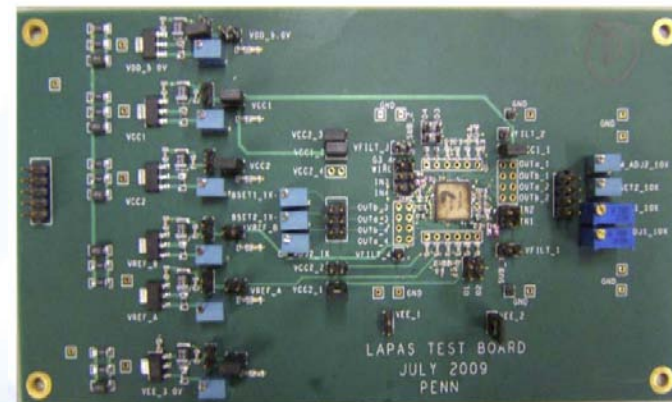
### LAPAS testing with hand wired prototype

- All measurements as expected
- DC results very close to simulations, shaper peaking time is 37ns as predicted
- Preamp and shaper transient response is good, no shaper control tuning required
- Common mode auto-tracking is excellent
- No significant concerns about first TID results

### New test PCB is available, full characterization is still in progress

- Future plan: explore other SiGe technologies (IHP, AMS) and feasibility of CMOS only design

### Test Printed-Circuit Board



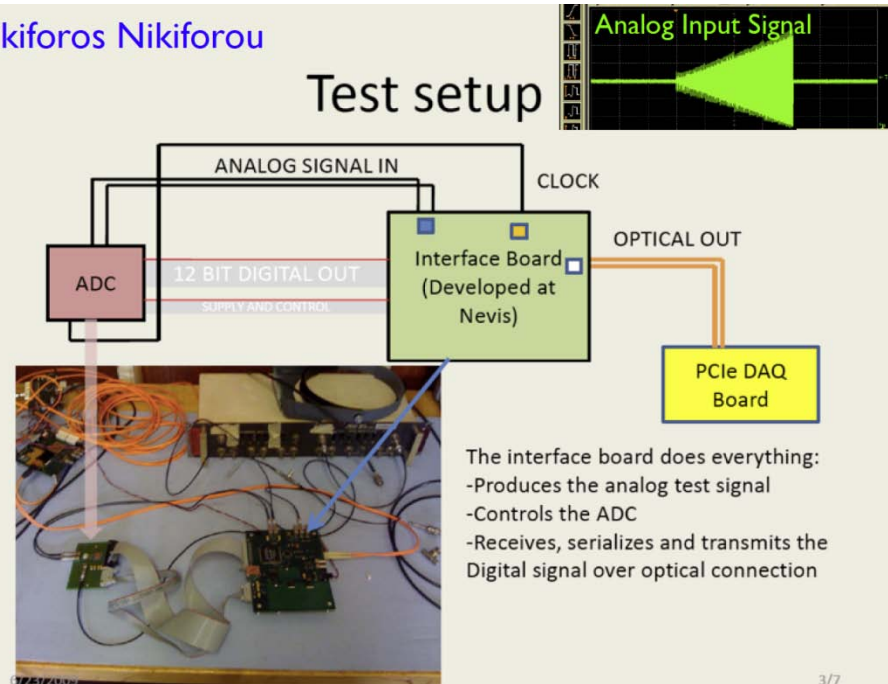


# COTS ADC Radiation Test

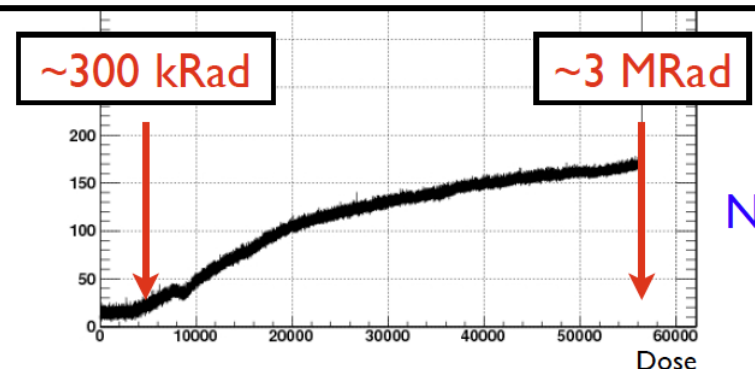
- **ADC is the most technologically challenging component in the new architecture**
- **COTS ADC radiation test**
  - Verify radiation tolerance of commercial ADC
  - Testing of few commercial devices: ADI-AD9259, ST-RHF1201, TI-ADC5821
  - Analysis on-going from data taken under live proton irradiation at Mass. General Hospital
  - Preliminary results
    - ST-RHF1201 suffers dynamic range reduction after ~300krad
    - ADI-AD9259 draws excess current
  - More radiation test is planned

Nikiforos Nikiforou

## Test setup



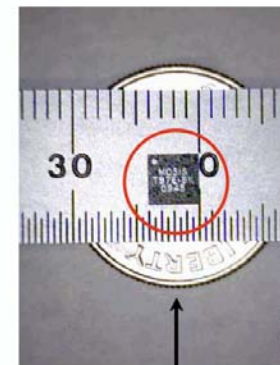
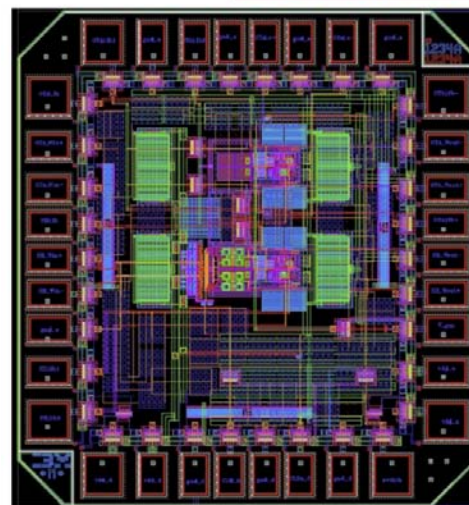
## Reduction in # of ADC values (max 3404)



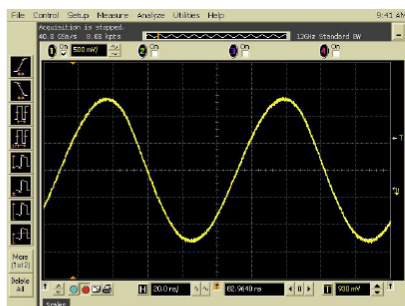
# Mixed-signal ASIC: ADC Development

## Nevis09 Chip

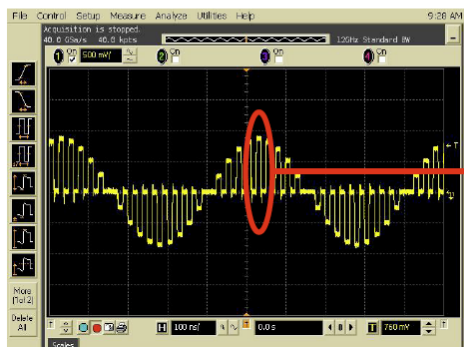
- **12-bit pipeline ADC design**
  - 1.5 bits/stage with digital error correction
  - Critical component: amplifier in every stage
- **Nevis09 chip**
  - 12-bit precision OTA in IBM 0.13 $\mu$ m CMOS 8RF
  - Implemented in chip: OTA + cascade of two T/H to achieve S/H effect for testing
- **Testing is still on-going, preliminary test results: 65dB**



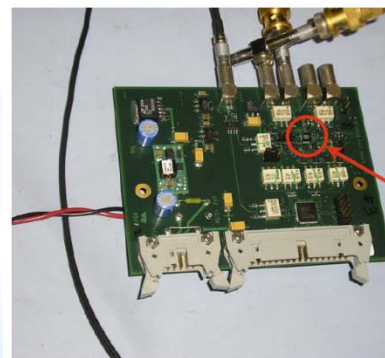
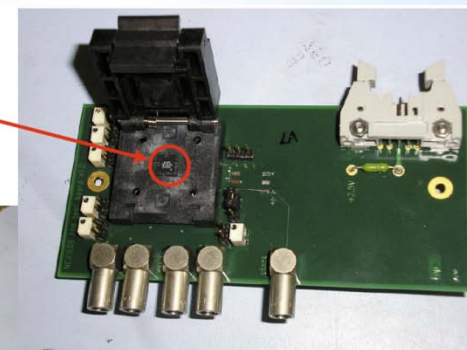
Dime  
~2 euro cents  
(in size)



← OTA out  
S/H out



Basic functionality  
+ irradiations



Performance testing

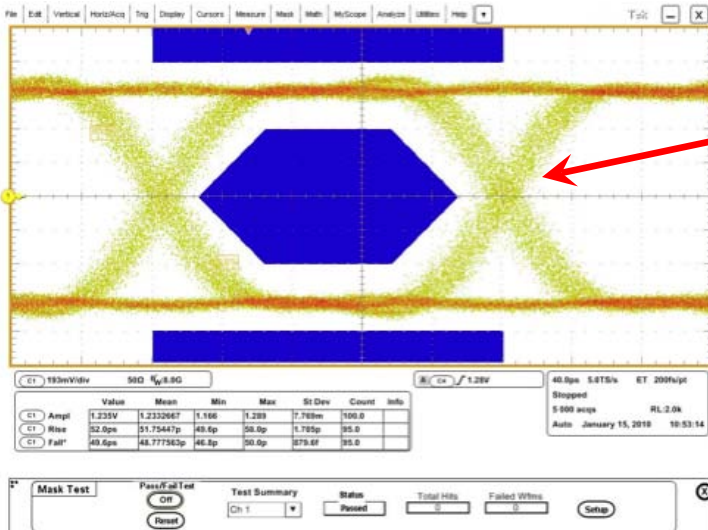
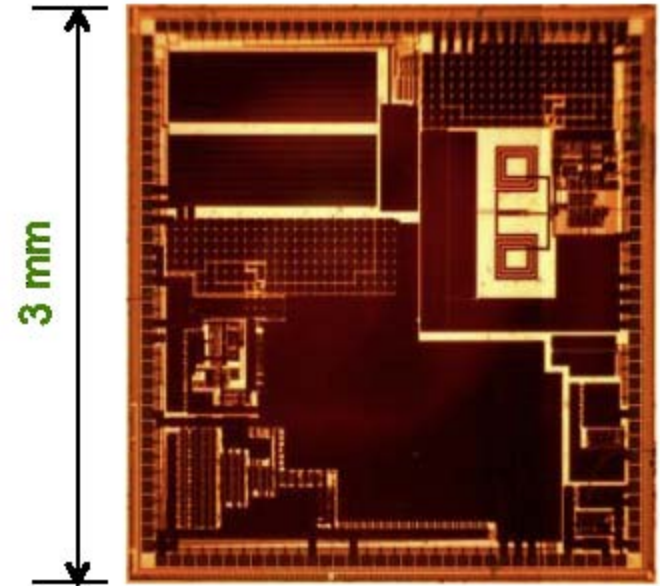
# Radiation Tolerant Optical Link

**SMU\_P1 in 0.25 $\mu$ m Silicon-on-Sapphire consists of the following function blocks**

- LOCs1, a 5Gbps 16:1 serializer
- The LCPLL, a 5GHz LC VCO based PLL
- The CML driver
- A divide-by-16 circuit
- A varactor, a voltage controller capacitor
- An SRAM block

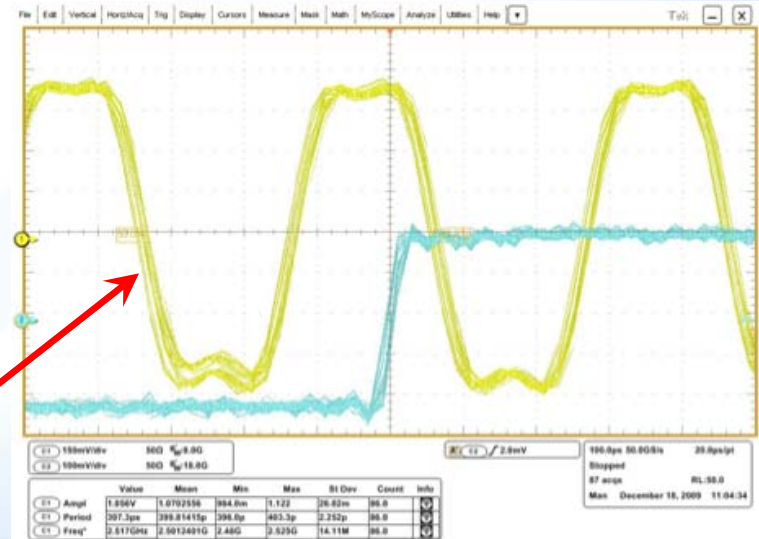
**Testing is still on-going, preliminary test results**

- **Serializer:** range 3.8 to 6.2Gbps, power 507mW,  $T_j \sim 62$ ps, eye opening  $\sim 69\%$  UI at  $1e-12$
- **LCPLL:** tuning range 4.7 to 5GHz, power 121mW at 4.9GHz,  $R_j < 2.5$ ps,  $D_j < 17$ ps



Eye diagram of serializer running at 5Gbps

The 5GHz LCPLL output clock locks to the input clock



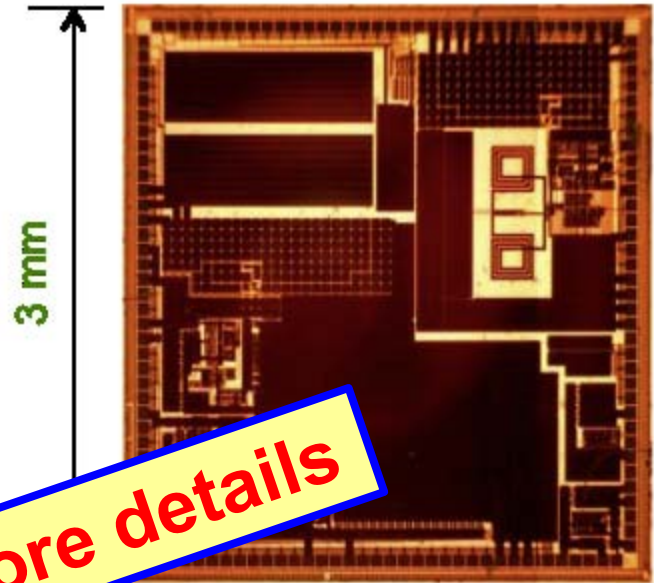
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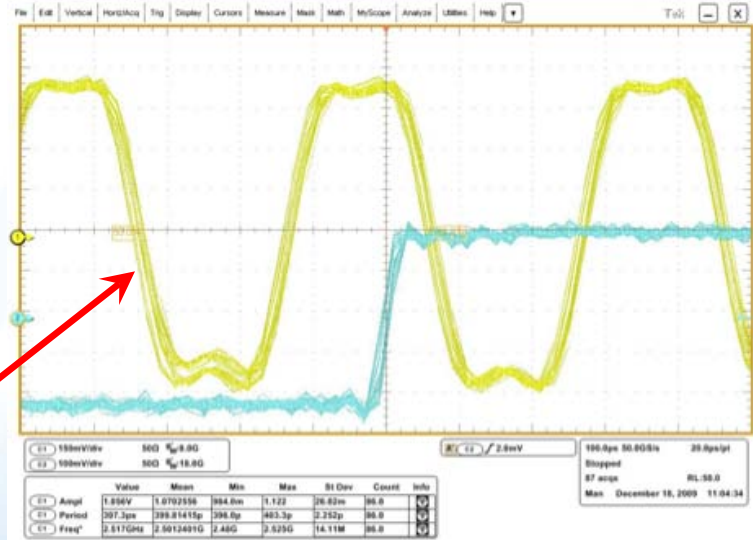
- Serializer: range 3.8 to 6.2Gbps, power 507mW,  $T_j \sim 62$ ps, eye opening  $\sim 69\%$  UI at  $1e-12$
- LCPLL: tuning range 4.7 to 5GHz, power 50mW,  $R_j < 2.5$ ps,  $D_j < 17$ ps



**See Jingbo's talk for more details**

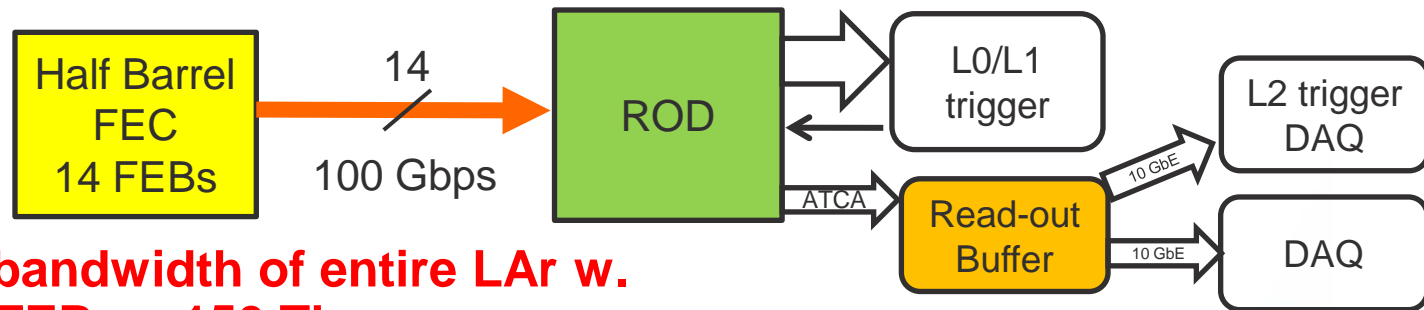


Eye diagram of serializer running at 5Gbps



The 5GHz LCPLL output clock locks to the input clock

# Readout Driver (ROD) Upgrade R&D

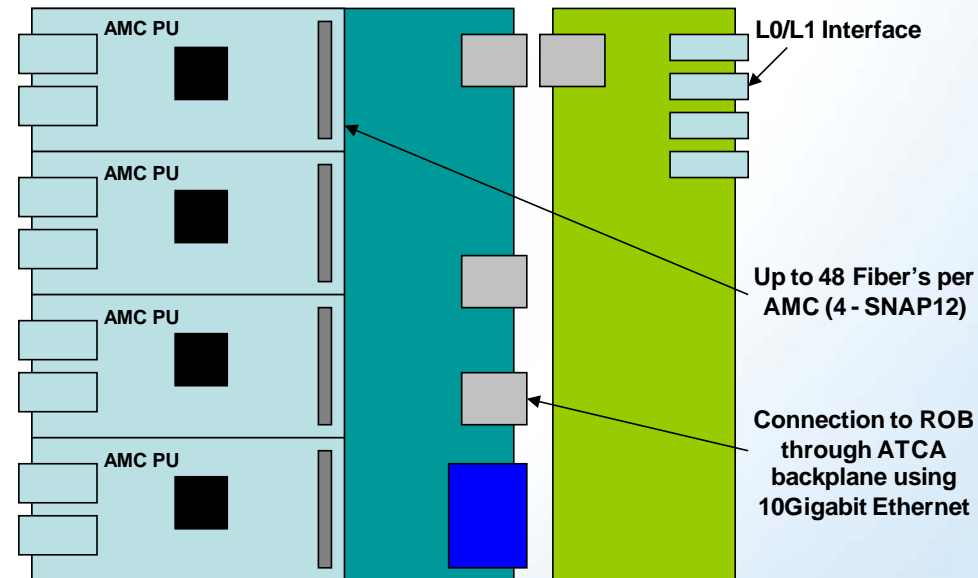


## Data bandwidth of entire LAr w. 1524 FEBs > 150 Tbps

- High speed parallel fiber optical transceiver (e.g. 12 fibers @ 10 Gbps)

## ROD R&D

- Address issues of bandwidth and achievable integration on the ROD
- ROD based on FPGA high speed SERDES and FPGA based DSP to take advantage of parallel data processing
- Perform L0/L1 trigger sum digitally after E-conversion with flexible and finer granularity within a realistic latency budget
- Follow up and explore technology evolution (e.g. FPGA, ATCA)



# Sub-ROD and Injector Development

## Sub-ROD and Injector in US

- ATCA form factor
- 75Gbps parallel fiber optic links
- FPGA SERDES: Xilinx Virtex 5 FX on Sub-ROD and Altera Statix II GX on Injector

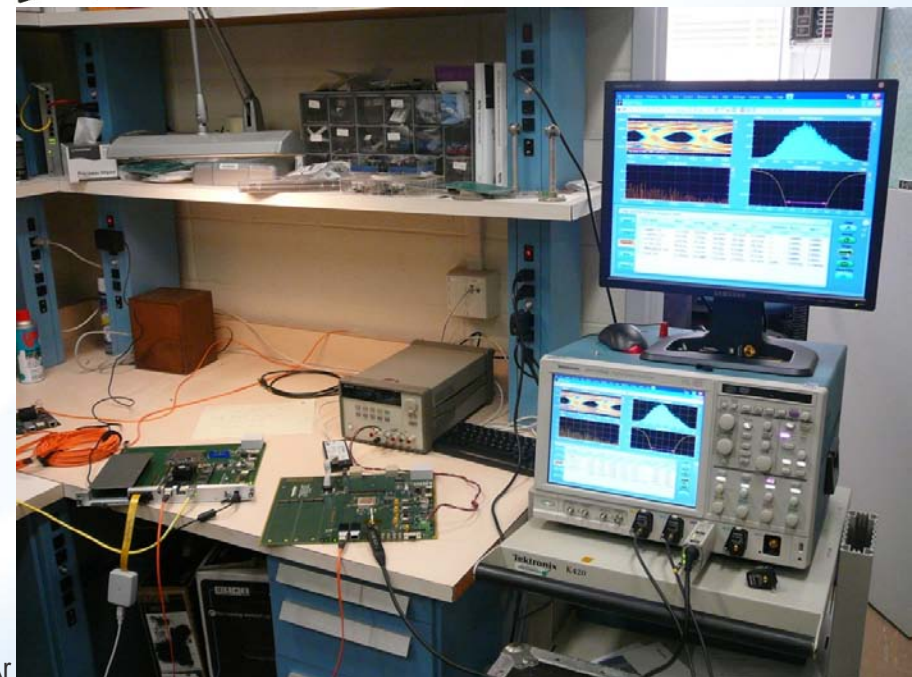
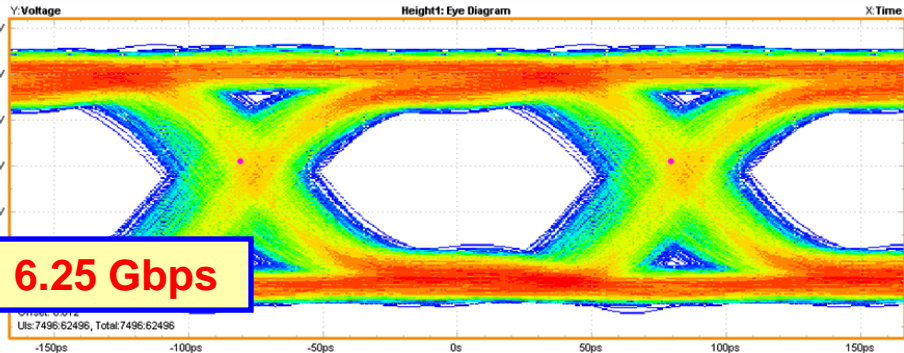
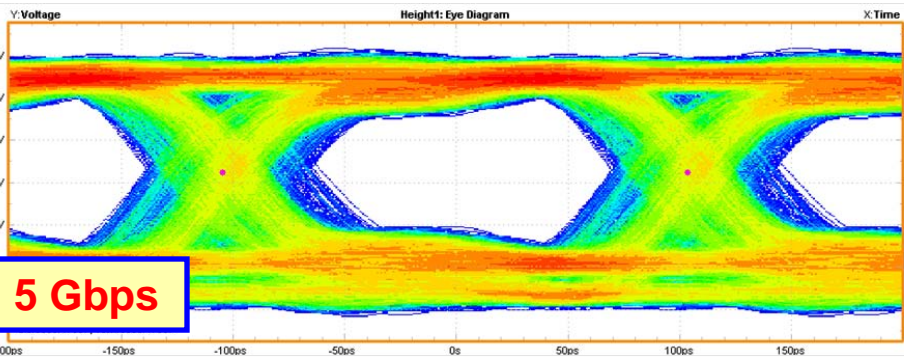
## Slice integration test

- SNAP-12 parallel optical transceiver from Emcore and Reflex Photonics
- BERT from 2.4 to 6.25Gbps per link
- Used as test stand for latency study

ATCA Sub-ROD



Sub-ROD Injector



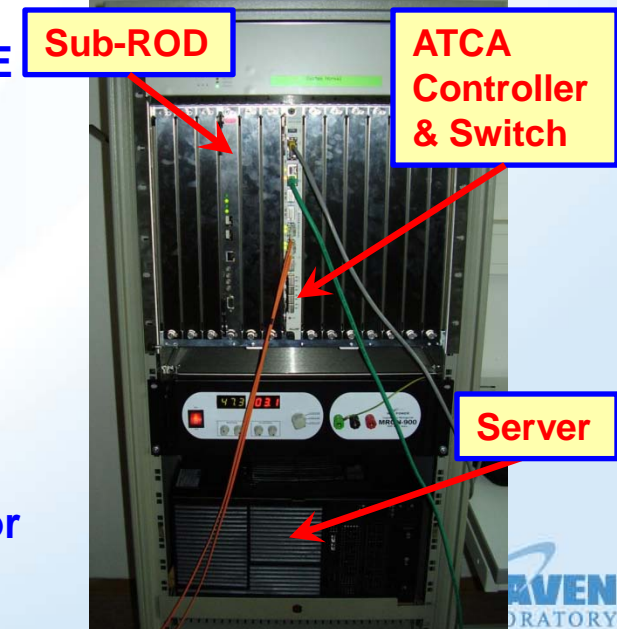
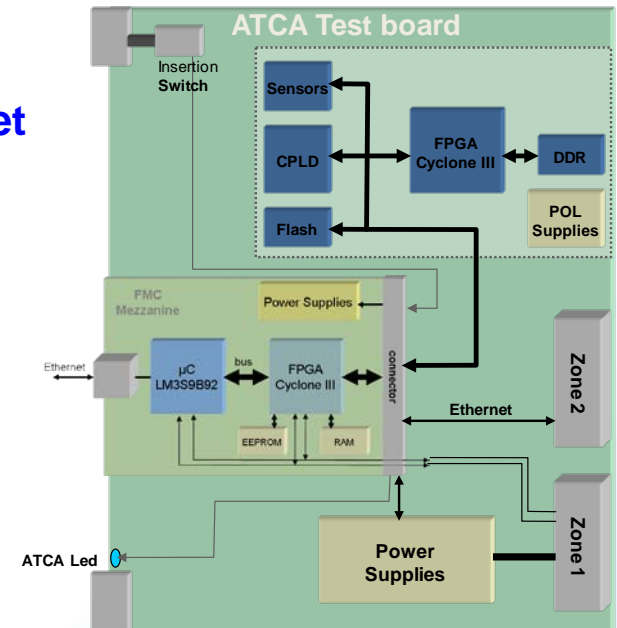
# ROD R&D in ATCA Platform

## ATCA test board development in LAPP, France

- ATCA controller tests: I/O, IPMI management, Ethernet communication
- ROD demonstrator tests: board configuration, ATCA compliant power supplies, FPGA design
- Software development based on Linux and GNU GCC
- IPMI (*Intelligent Platform Management Interface*) Controller for ATCA boards in FMC format provides ATCA ROD board management
- In development and will be available this summer

## ATCA ROD test bench in Dresden, Germany

- Radisys Promentum ATCA sys-6010 crate with 10GbE and dual star backplane
- 1 ATCA Sub-ROD from BNL
- 10GbE Switch with XFP transceiver with 10GbE connection to server PC
- Installation of ROS software to simulate real data transfer and DAQ system as in ATLAS
- Investigating 10GbE implementation
- Test integrated ROD/ROB functionality, also useful for normal ROD tasks and data integrity tests with PC







# Summary

- **Radiation levels and probably natural aging of the electronics will require an upgrade of the front-end electronics**
- **Opportunity to apply modern technology and revise architecture**
  - Continuous data streaming off-detector
  - Fully digital L0/L1 trigger information with flexible granularity, while interface to trigger system will be guided by physics and MC simulation
- **Major challenges**
  - Modern technology requires lower voltages, difficult to maintain the required large dynamic range and stringent noise performance
  - Critical radiation hard components (analog front-end, ADC, optical link and power supply)
  - Extremely large bandwidth off-detector readout
  - High performance data handling with very strict latency budget
- **R&D is progressing smoothly**
  - 3 different ASIC/chiplet available, more test results expected soon
  - Priority for the next 2-3 years to demonstrate the feasibility of the readout architecture in different scales

# Backup Slides

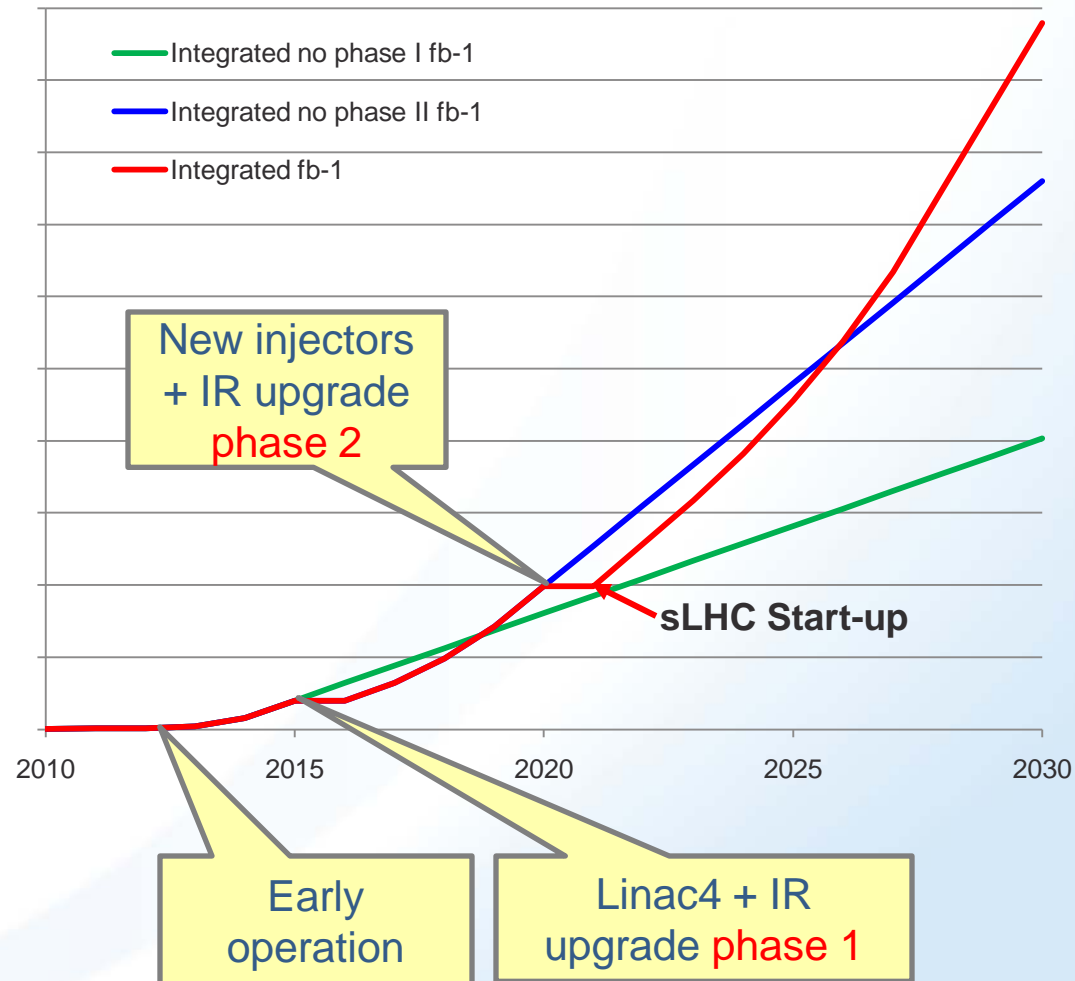
# LHC Upgrade Expectation

## LHC upgrade includes 2 phases

- sLHC (phase 2 upgrade) expected to start up ~2020
- ATLAS LAr calorimeter plans for LHC phase 2 upgrade

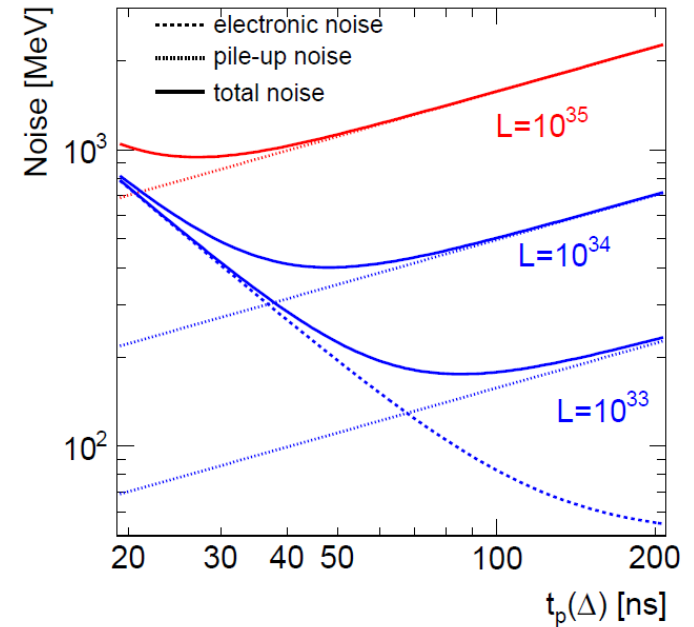
## New requirements to LAr calorimeter readout electronics

- Radiation environment assumed to scale x10
- Total power consumption kept same



# New Readout Challenges at sLHC

- **Radiation hardness: 10 times more radiation**
- **Dynamic Range**
  - EM: from 50 MeV to 3 TeV (10 mA): 16 bits
  - HEC: up to 1 TeV (0.3 mA)
- **Relative energy resolution:  $\sigma_E/E \sim 10\%/\sqrt{E} \oplus 0.7\%$**
- **Electronic calibration:  $< 0.25\%$**
- **Fast shaping to optimize signal/noise ratio**
  - Up to 20 times more pile-up events
  - Optimal hardware shaping time scales as  $L^{-1/4}$ ,  $t_p(D) \sim 28\text{ns} @ 10^{35}$
- **Digital filtering signal reconstruction: To adapt to changing LHC luminosity**
- **Minimal coherent pickup noise:  $< 5\%$  of incoherent noise**
- **Data to be used for both DAQ and L0/L1 trigger**
- **Same power consumption**



Radiation tolerance criteria of the LAr electronics at sLHC.

	ASICs	COTS		LVPS
		(multiple lots)	(single-lot)	
TID (kGy)	5.8	78	19	4.5
NIEL (n/cm <sup>2</sup> )	$1.7 \times 10^{14}$	$6.6 \times 10^{14}$	$1.7 \times 10^{14}$	$7.7 \times 10^{13}$
SEE (p/cm <sup>2</sup> )	$3.2 \times 10^{13}$	$1.3 \times 10^{14}$	$3.2 \times 10^{13}$	$2 \times 10^{13}$

