

MARTE

Multi-platform Real-Time Framework

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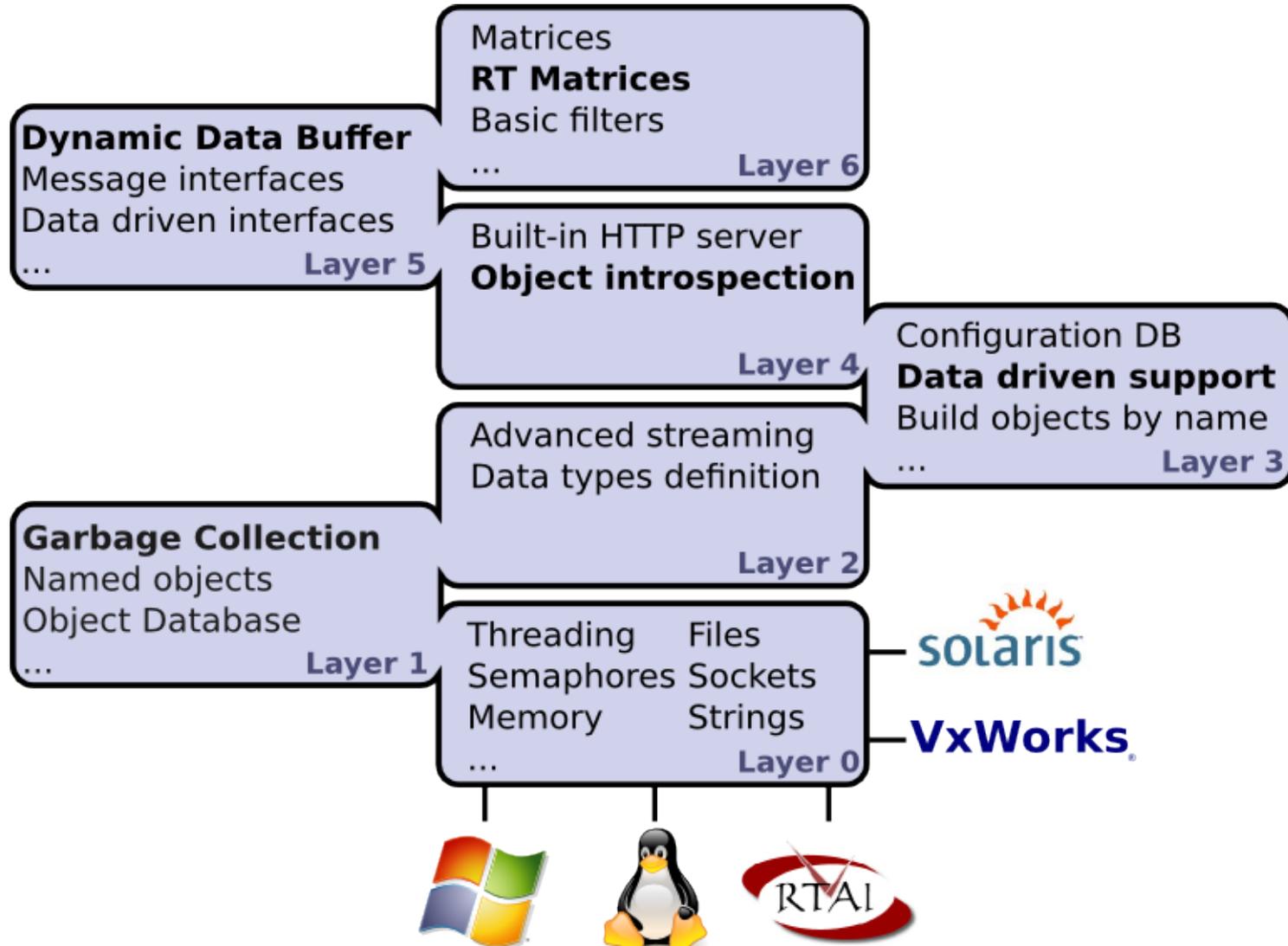


EFDA
JET

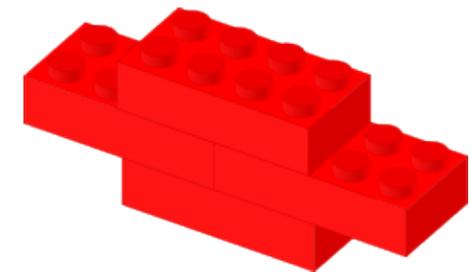
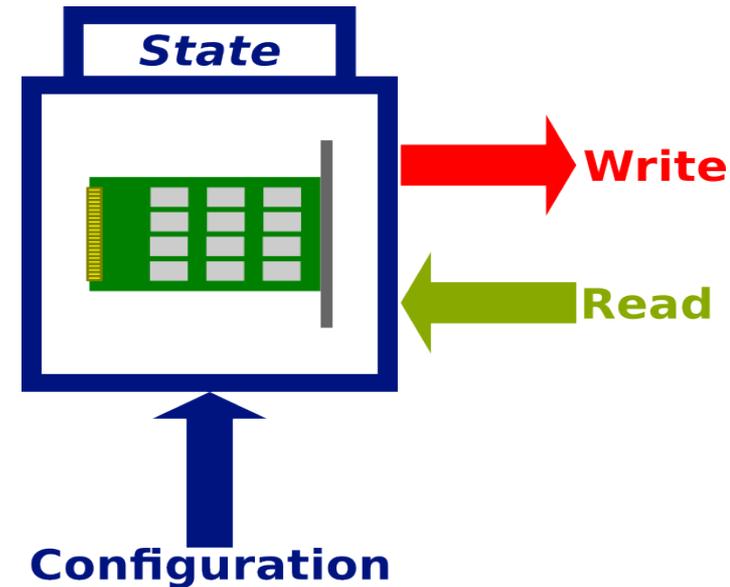
- What is MARTe?
- MARTe foundations - RT Library
- Components description
- Interfacing with MARTe
- Vertical Stabilisation – an example
- Future developments
- Conclusions

- **Multi-platform C++ real-time framework**
 - Modular
 - Clear boundary between algorithms, hardware interaction and system configuration
 - Reusability and maintainability
 - Simulation
 - Develop / debug in non real-time environments
 - Data driven
 - Provide live introspection tools
 - HTTP (+CINT), logging

BaseLib2 – support library



- Atomic block
 - Algorithms
 - Hardware interface
- Only piece of the system which may need to be developed
- Data driven configuration
- Can be inserted and removed *at anytime*
- Consume and produce data



Object Configuration

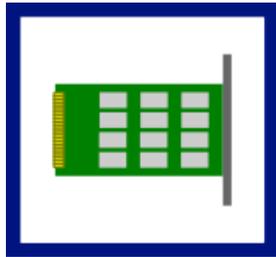


- Structured syntax
- Similar to XML
- Classes are automatically created
- Configuration is validated by the created object
- Asserting and parsing functions available

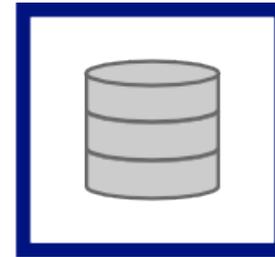
```
+HttpServer = {  
    Class = HttpService  
    Port = 8084  
}  
  
...  
  
+Control = {  
    Class = ControlGAM  
    Controller = {  
        NoPlasmaVelocityGain = 0.0  
        NoPlasmaCurrentGain = 40.0  
        IPWaveform = {  
            Times      = {0 120}  
            Amplitudes = {0.5 0.5}  
            Rounding   = 50  
        }  
    }  
    ...  
}
```

- Large part of the code expected to be executed during configuration phase
 - Trap errors as soon as possible
- Special kind of GAMs provide interface with hardware
 - Unique high level interface to any kind of hardware
 - Clear boundary between algorithms and hardware
- Simulation
 - GAMs to simulate the inputs (replacing the hardware)
 - Predict the output of the system using models
 - Live swap of GAMs when required
 - Debug and error tracking

Common GAMs



Hardware I/O



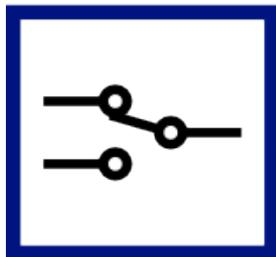
Persistence



Algorithms



Debug

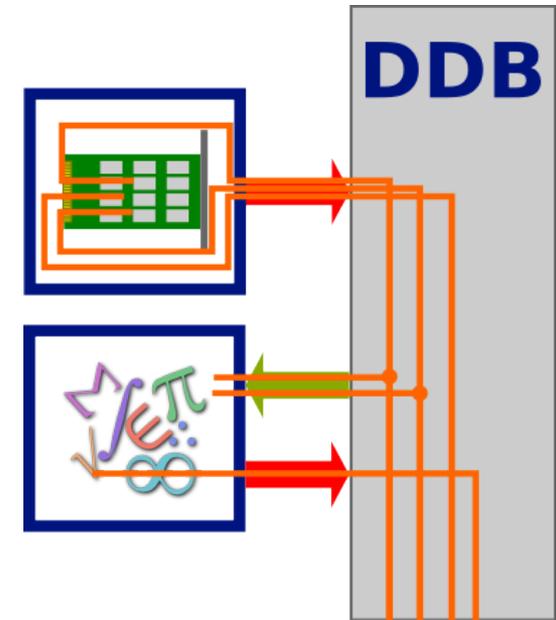


Decision taking



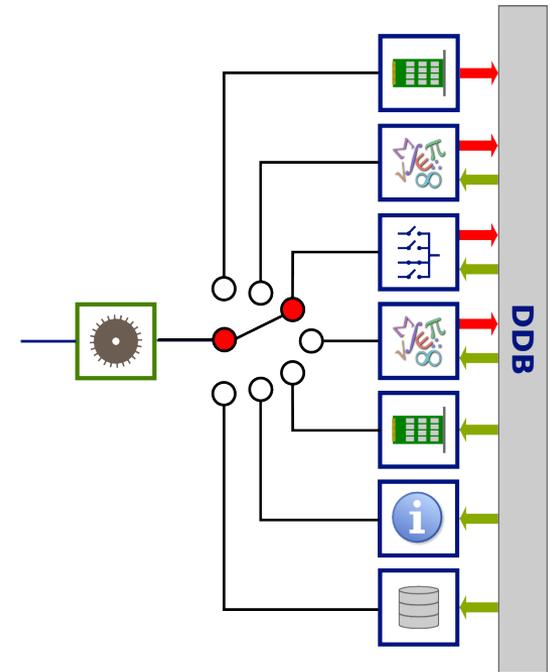
Information

- GAMs shared data through a memory bus
- MARTe guarantees coherency between requested and produced signals
- Set of GAMs allow to stream data to different MARTe systems

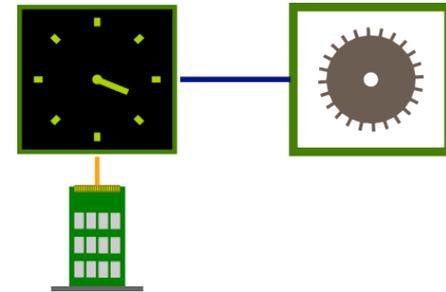




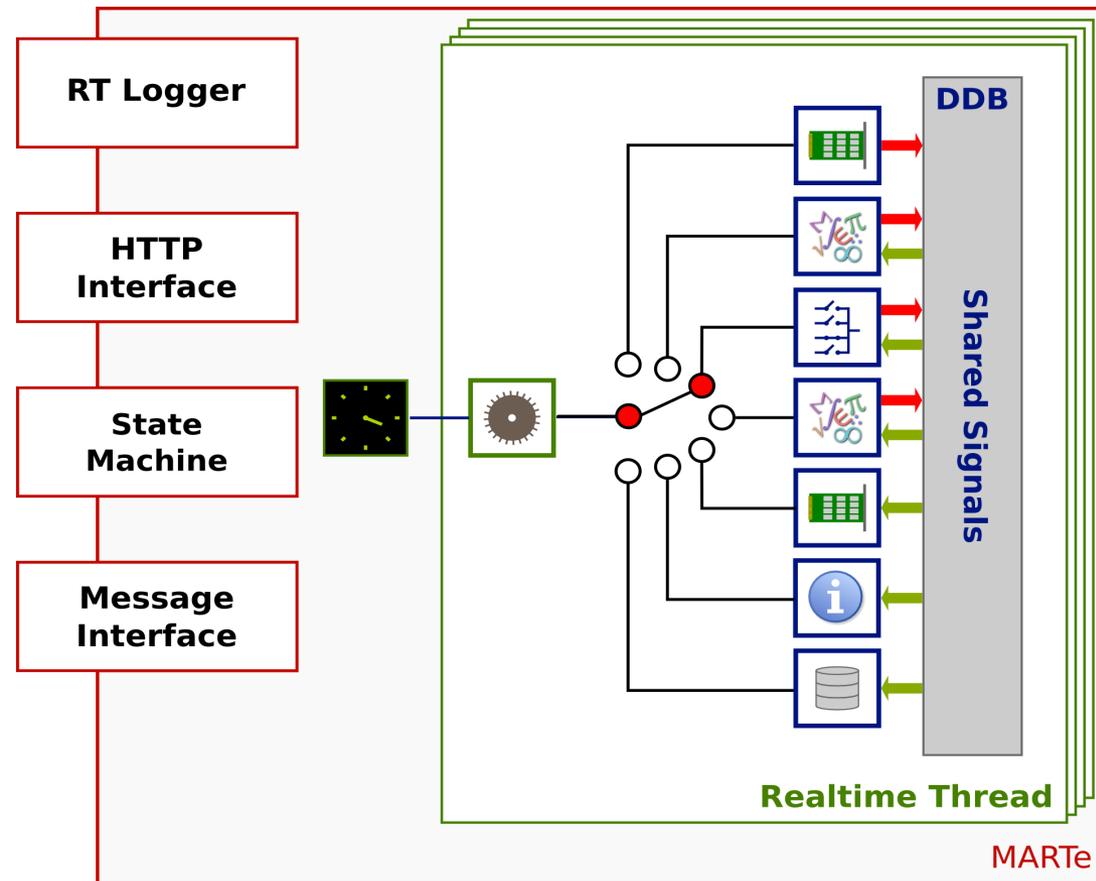
- Sequentially executes GAMs
 - Works as micro-scheduler
 - Can be allocated to specific CPUs
- Keeps accurate information about execution times
- Requires an external time and triggering mechanism



- Timing for the real-time thread(s)
- Usually provided by an external hardware
- Cycle time can be specified
 - Defines when a new cycle should start
- MARTe supports polling and interrupt based sources



- At least one RT-Thread
- RT-Threads can execute in parallel
- Several utility components available
 - Logger
 - HTTP server
 - ...



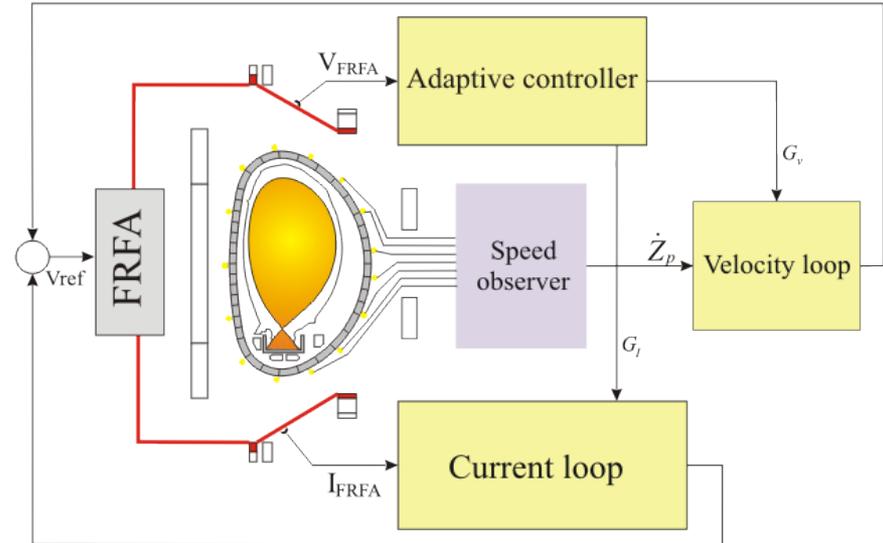


- The preferred way is through a *Message Interface*
 - High level protocol
 - Implemented in BaseLib2
- HTTP interaction is widely used for retrieving information
 - Can also be used to change values
 - GAMs configuration
 - State machine
 - ...

Vertical Stabilisation



- Elongated tokamak plasmas are susceptible to a vertical axisymmetric instability
- **Dedicated Vertical Stabilisation System required**
- **Essential system for operation**
- **Growth rate of 1000s^{-1}**
- **Loss of control can produce forces in the order of the 100's of tonnes**

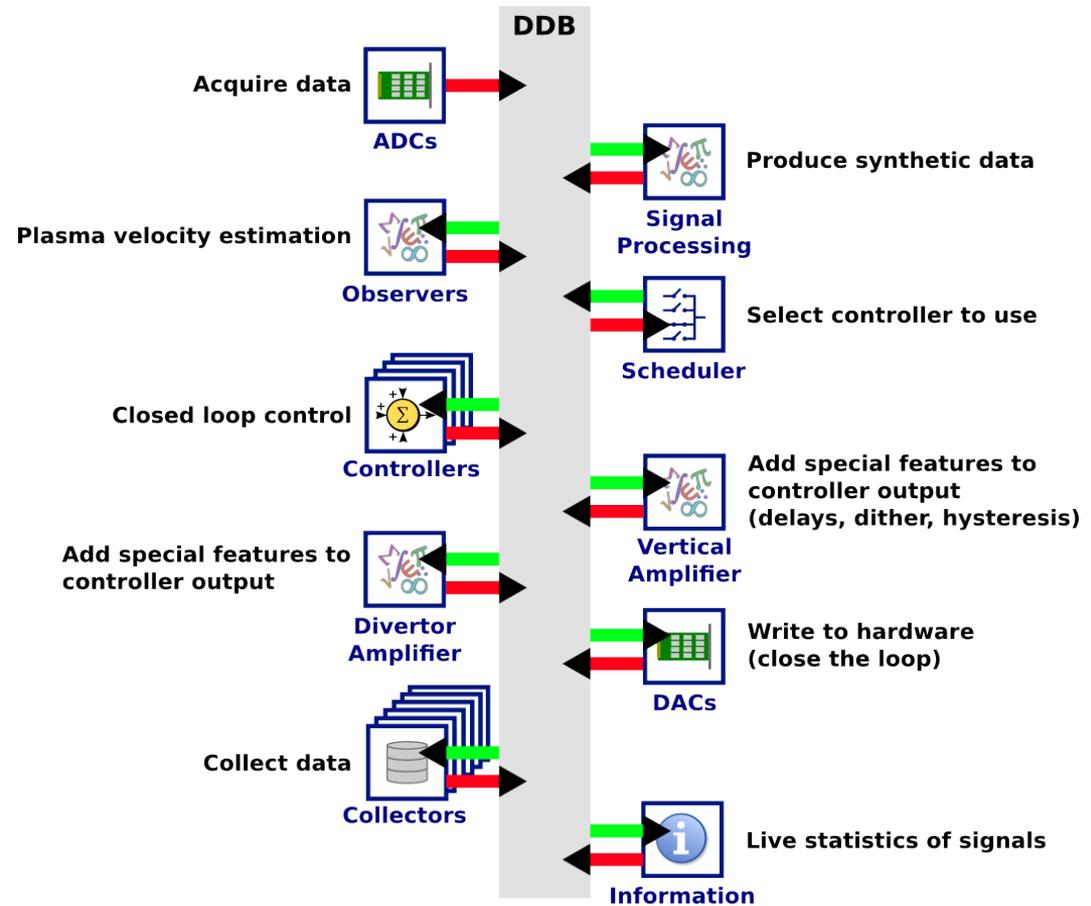
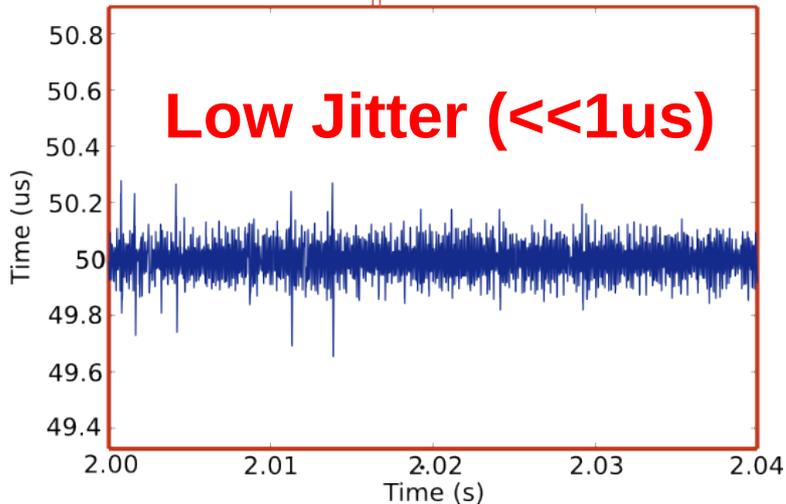
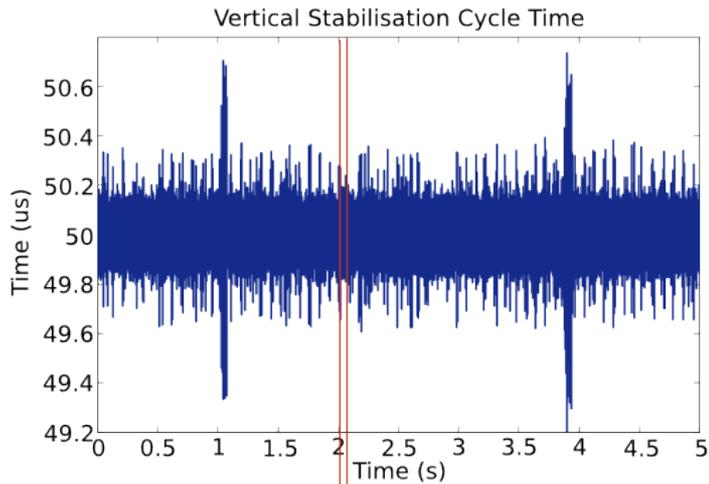


VS - An example



- Closed loop
 - $50 \pm 1 \mu\text{s}$ (with max. jitter of **$2.5 \mu\text{s}$**)
- 18 GAM instances
 - Altogether execute in less than $40 \mu\text{s}$
 - Synchronization always achieved within $0.8 \mu\text{s}$
- 192 signals acquired by ADCs and transferred at each loop
- Always in real-time (**24 hours per day**)
 - **1.728×10^9 $50 \mu\text{s}$ cycles per day**

VS Execution



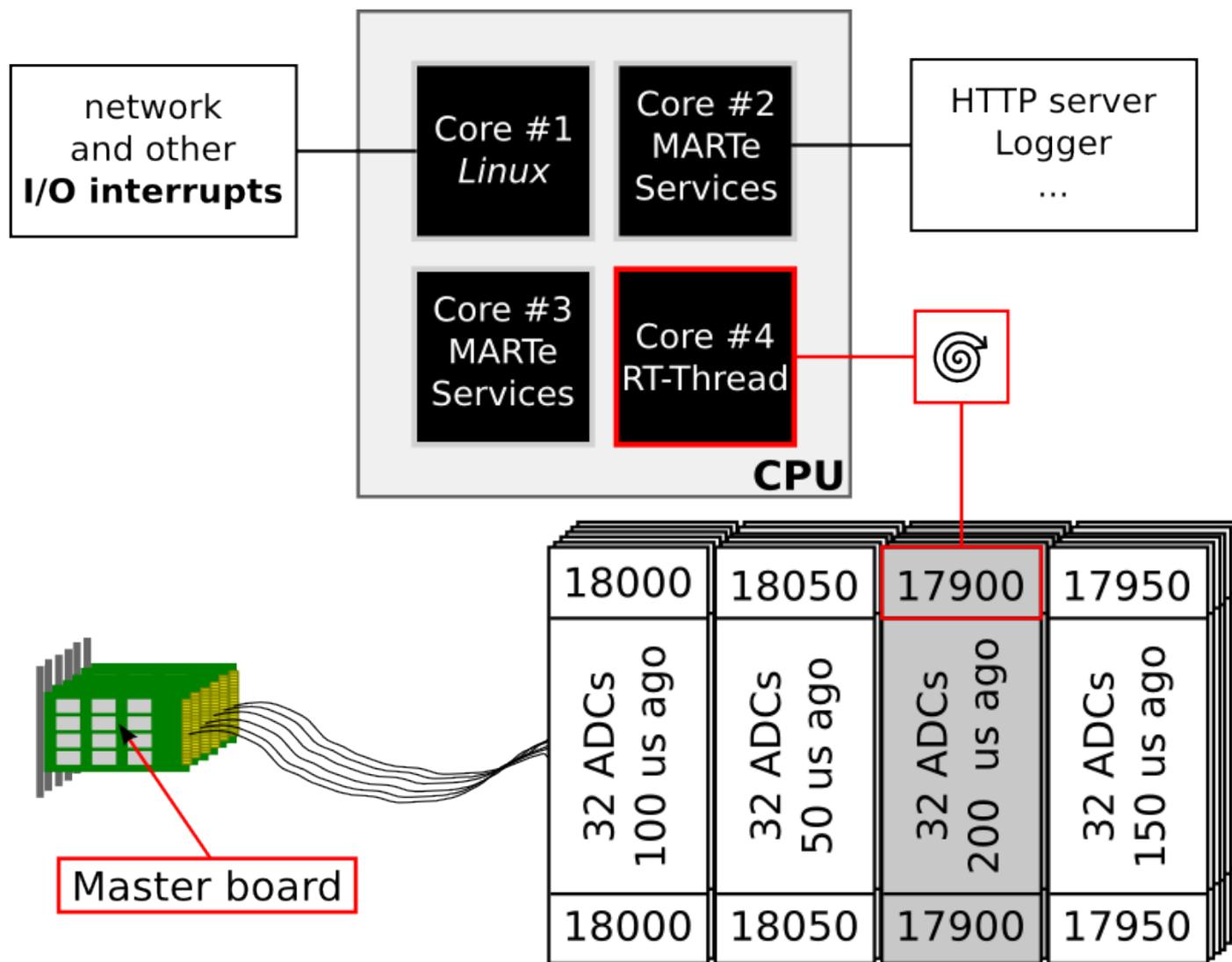
- System is always RT
 - JET is a pulsed based machine
 - ITER will have very long pulses
- First tests with continuous data streaming
 - **Without compromising RT**
 - Bandwidths of ~ 70 MBytes/s
 - To be published
- Testing remote driving of systems

- Modular C++ framework
 - Based on multi-platform RT library
 - Built over data driven modules
 - Clear boundary between hardware and algorithms
 - Interface and behaviour fully configurable
- Drives the VS system
 - Essential system, faults are not acceptable
 - **50 μ s loop cycle with a jitter inferior to 1 μ s**
 - Average jitter in the order of 200ns

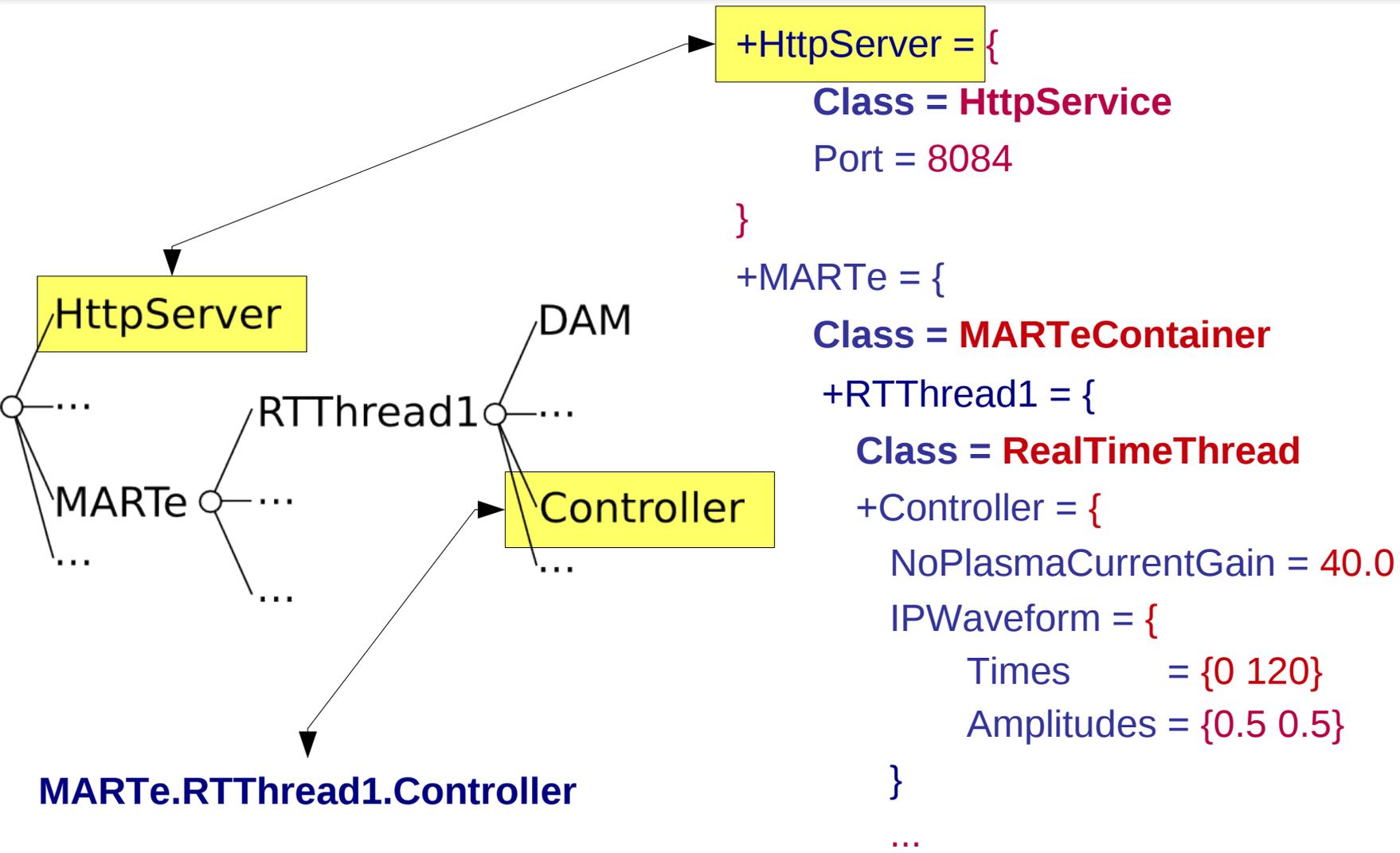
Support slides



Hardware Synchronization



Configuration DB

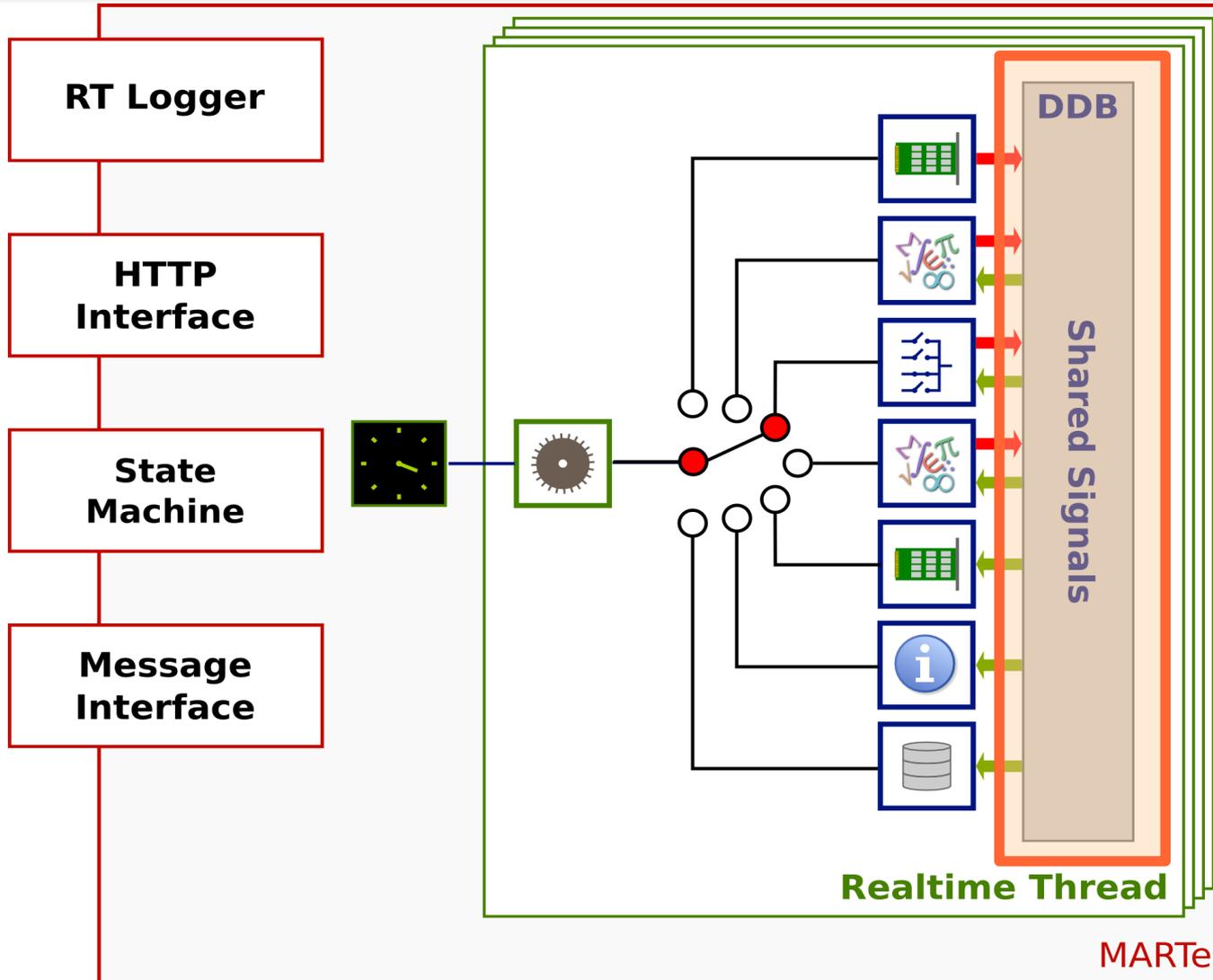


MARTe.RTThread1.Controller

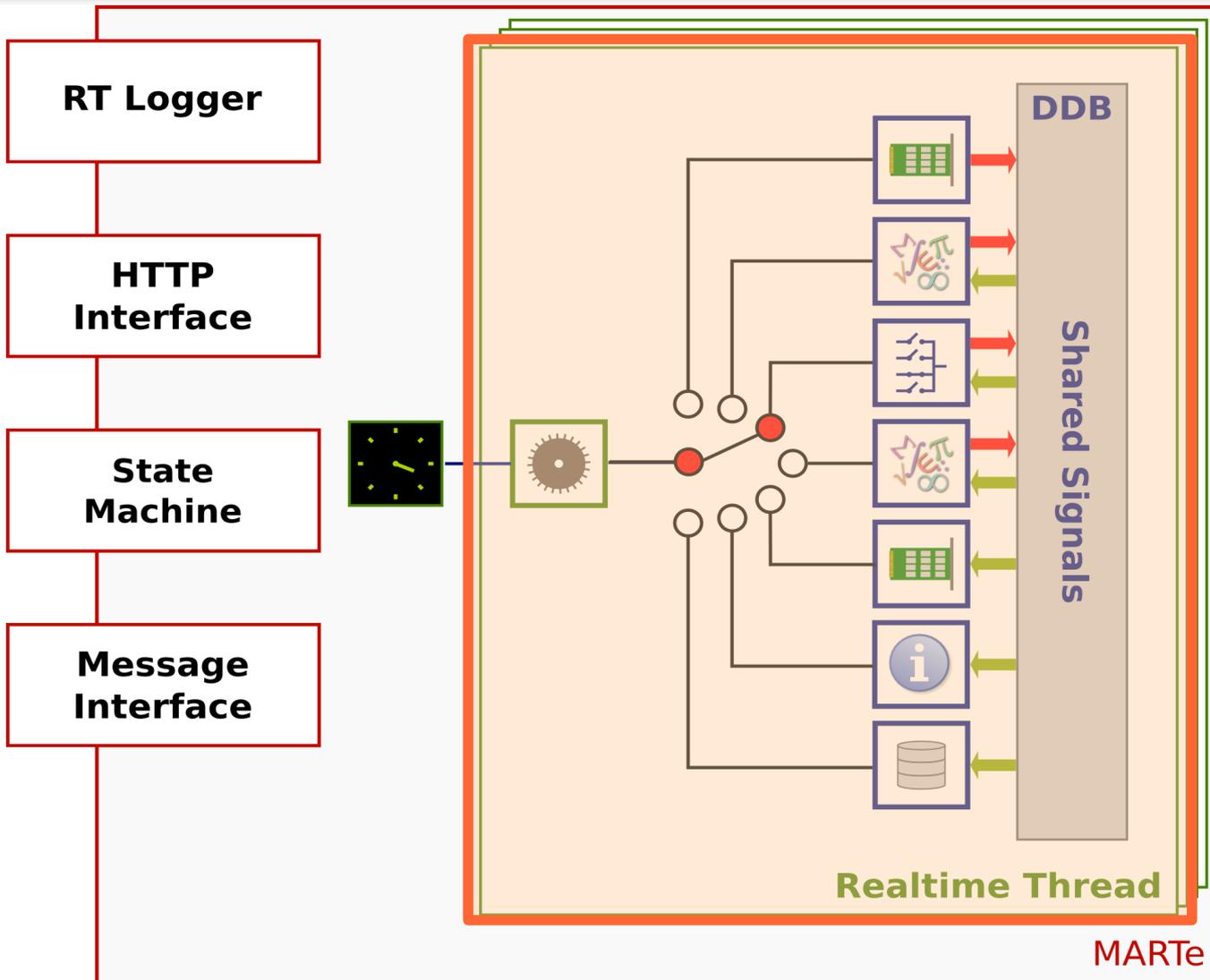
- Objects that implement the **Message Interface** are able to send and receive synchronous and asynchronous messages
- Messages allow to interface by protocol
- Messages can contain object configurations
- Can be sent through the network
- Important mechanism in the design of MARTe

- **Closed loop**
- Only possible because RT processes aren't disturbed
- Full access to the computer without compromising RT
- **50 μ s loop cycle with a jitter inferior to 1 μ s**

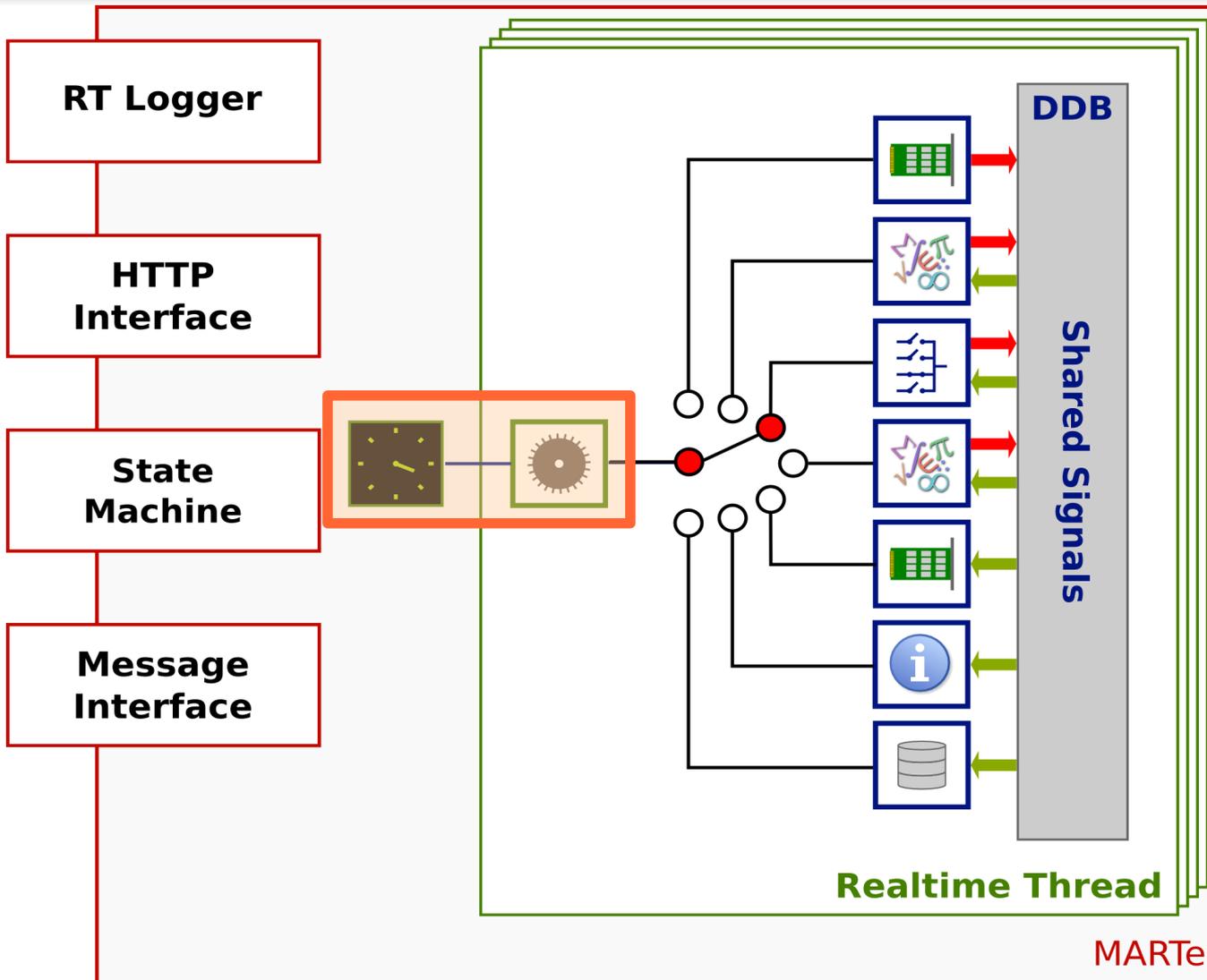
Dynamic Data Buffer



Real-time thread



Synchronisation



BACK
REFRESH

- (MARTeContainer) MARTe > w
 - + (MenuContainer) MARTe > w
 - + (GCReferenceContainer) DriverPool
 - + (GCReferenceContainer) Messages
 - + (DataPollingDrivenTTS) ExternalTimeTriggeringService
 - (RealTimeThread) Thread_1 w
 - (DDB) DDB
 - + (TimeInputGAM) CAAdc > w
 - + (SignalProcessingGAM) SPGAM > w
 - + (VSObserverGAM) VSObserver
 - + (SchedulerGAM) Scheduler > w
 - + (ControlGAM) Control > w
 - + (DummyControllerGAM) Dum1
 - + (DummyControllerGAM) Dum2
 - + (DummyControllerGAM) Dum3
 - + (VAMGAM) VAM > w
 - + (DAMGAM) DAM > w
 - + (OutputGAM) ATCADac
 - + (DataCollectionGAM) Collection > w
 - + (DataCollectionGAM) ControllerSignals > w
 - + (DataCollectionGAM) DebugSignals > w
 - + (DataCollectionGAM) Performance > w
 - + (EventCollectionGAM) AsyncSignals
 - + (DataCollectionGAM) WaveformCollection

3.300e+001	0.000000
3.500e+001	5000.000000
1.000e+002	5000.000000
1.330e+002	0.000000

Saturations

VS1 current adaptation parameters

Saturation	Value (abs)
Max current gain	30.000000
Min current gain	0.000000

PCU1 current adaptation parameters

Parameter	Value
Voltage delta threshold	50000.000000
High gain	-10000.000000
Low gain	-5000.000000
Keep low gain for	12000 usescs

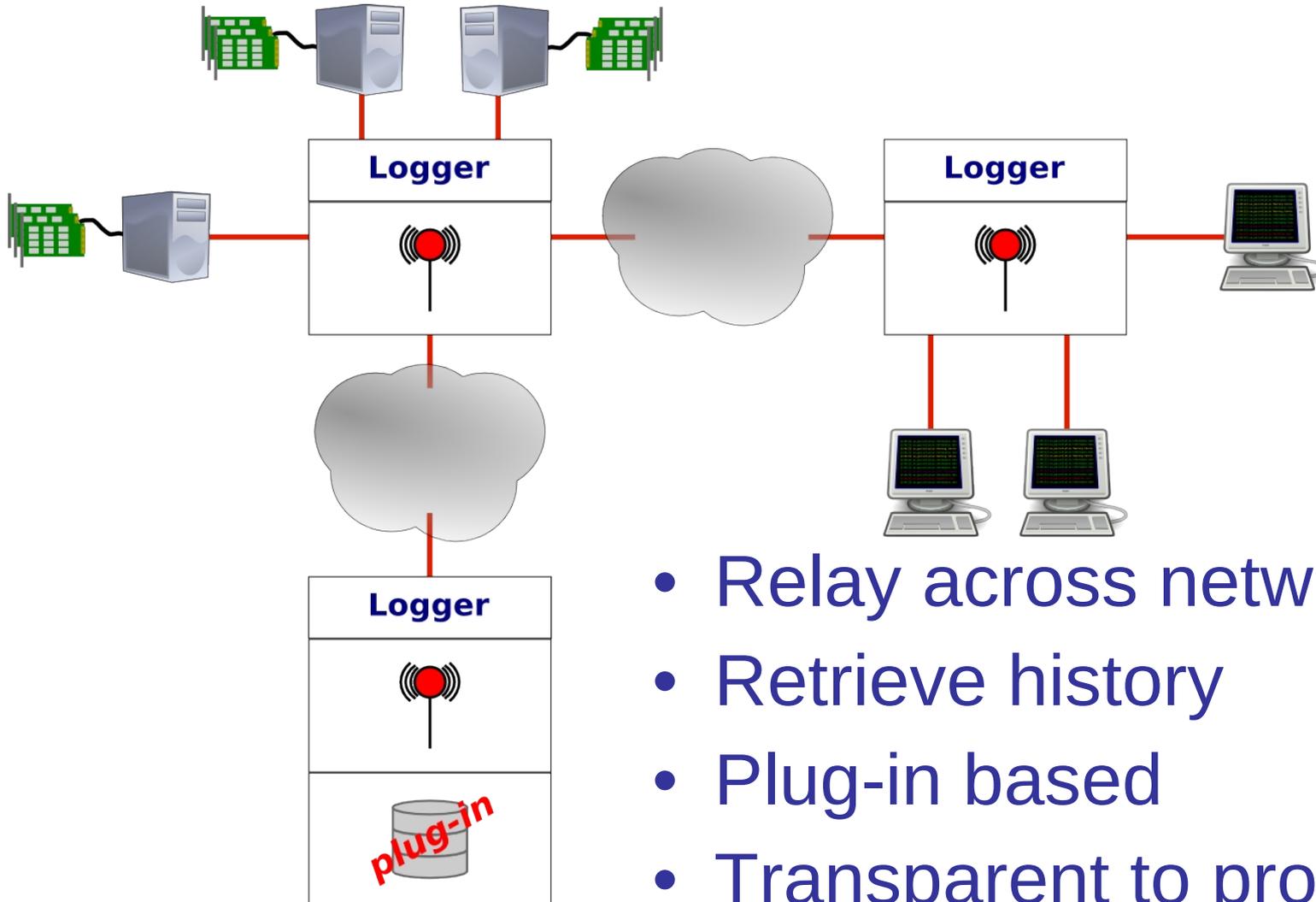
PCU2 current adaptation parameters

Parameter	Value
Amplifier current saturation index threshold	2500.000000
High gain	-15000.000000
Low gain	-5000.000000
Alpha	0.500000
Beta	0.800000

Automatically built

Done

MARTE tools - logger

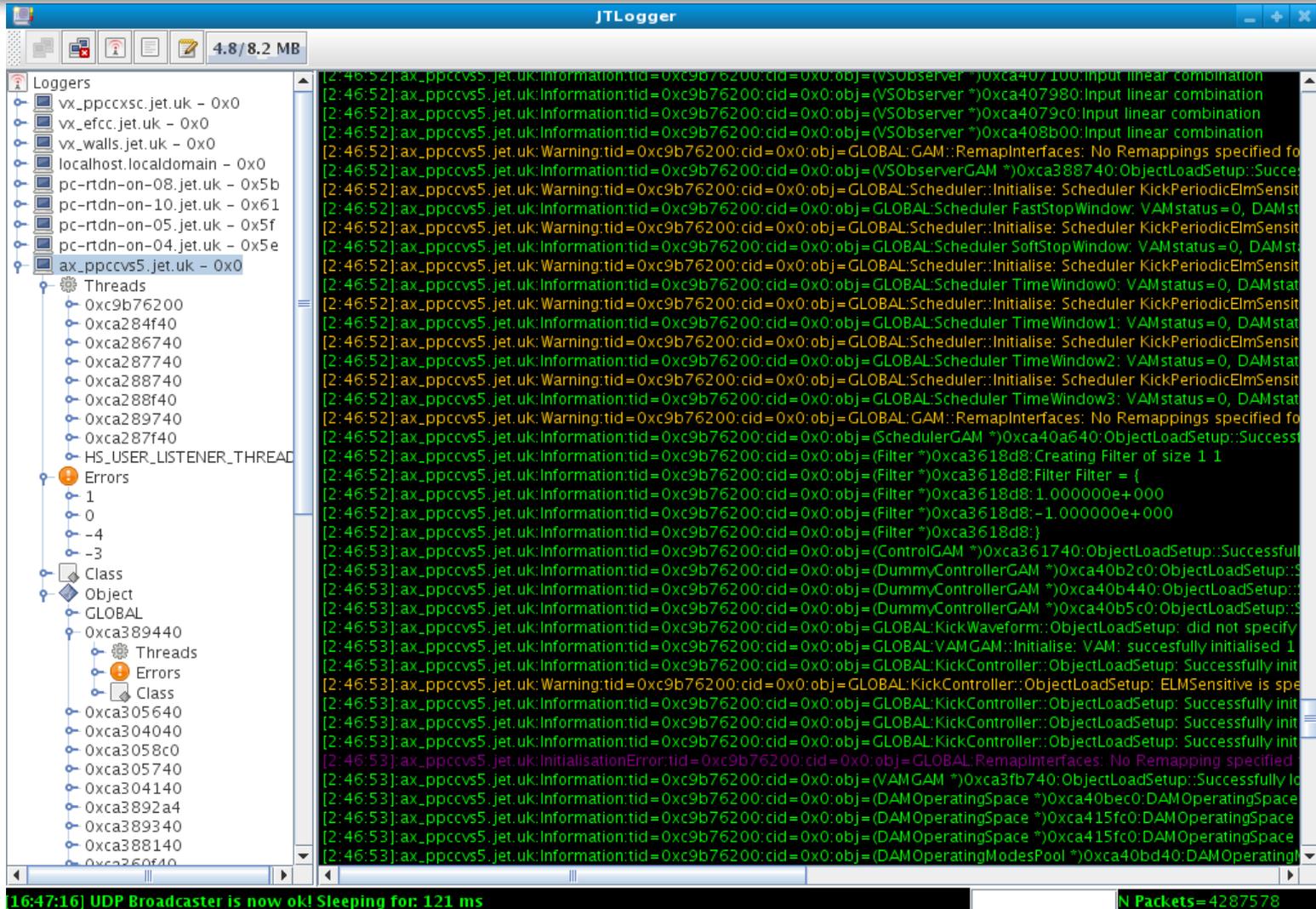


- Relay across networks
- Retrieve history
- Plug-in based
- Transparent to producers

- 6 ATCA Data Acquisition Boards
- 2MSPS - 18 bit ADCs
- PCIe interface
- Intel Core 2 Quad
- Digital I/O
 - Connection to new amplifier



• See *FESPP-25* in the Poster Area



The screenshot displays the JTLogger application window. The title bar reads "JTLogger" and the status bar shows "4.8 / 8.2 MB". The interface is divided into three main sections:

- Loggers:** A tree view on the left showing various loggers such as "vx_ppccv5c.jet.uk - 0x0", "vx_efcc.jet.uk - 0x0", "vx_walls.jet.uk - 0x0", "localhost.localdomain - 0x0", "pc-rtdn-on-08.jet.uk - 0x5b", "pc-rtdn-on-10.jet.uk - 0x61", "pc-rtdn-on-05.jet.uk - 0x5f", "pc-rtdn-on-04.jet.uk - 0x5e", and "ax_ppccv5.jet.uk - 0x0".
- Threads:** A tree view under the selected logger "ax_ppccv5.jet.uk - 0x0" showing threads like "0xc9b76200", "0xca284f40", "0xca286740", "0xca287740", "0xca288740", "0xca288f40", "0xca289740", "0xca289f40", and "HS_USER_LISTENER_THREAD".
- Errors:** A tree view showing error counts for "1", "0", "-4", and "-3".
- Class:** A tree view showing the class hierarchy, including "GLOBAL" and "0xca389440".

The main log area on the right displays a stream of log messages, including information, warnings, and errors, with timestamps and thread IDs. The status bar at the bottom indicates "16:47:16] UDP Broadcaster is now ok! Sleeping for: 121 ms" and "N Packets=4287578".

The Goal



- Use MARTe to run the JET Vertical Stabilisation

Essential system for operation

Closed loop control cycle time:

Target:

$50 \pm 1 \mu\text{s}$

(with max. jitter of $2.5 \mu\text{s}$)

Achieved:

$50 \pm 0.10 \mu\text{s}$

(max jitter of $0.80 \mu\text{s}$)

