FRONT-END READOUT & DAQ for SI TRACKERS at LINEAR COLLIDER

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International Linear Collider Workshop 2010
Friendship Hotel, Beijing, China, 26-30 March 2010
R&D on Front End Electronics

The FEE is closely related to the fact 1) that microstrips are currently the baseline for LC sensors and 2) to the cycle of the ILC machine.

- **Long shaping time** (relatively slow cycle machine)
- **Power cycling** (possible)
- **Digitization and pre-processing**: Take advantage of the time between inter-bunch trains for highly processed, controlled, fault tolerant and flexible readout (fully programmable).
PURSUING OUR R&D LINE ON THE ELECTRONICS
Goal: Integrate 2048 channels in 90nm (65nm?) CMOS: but by elementary blocks of 256 channels: multiplexing factor 256:1

- Amplifiers: 20 mV/MIP over 10 MIP range
- Shapers: 500ns–2μs (now optimizing at 500 ns)
- Sparsifier: Threshold the sum of 3-5 adjacent channels
- Samplers: 8 samples at sampling clock period (80ns)
  Event buffer 8 depth
- Noise baseline: O (375 + 10.5 e-/pF @ 1 μs shaping, 200μW power)
- ADC: 8 bit-ADC
- Power dissipation/channel for the overall FE chain: 1-1.5 mWatt
- Buffering, digital pre-processing
- Calibration
- Power switching (could save a factor of about 70)
- Total number of readout channels: 10⁷ channels
Main features of the new circuit (new= currently under design)

128 channels: Preamplifier, shaper, sparsifier, analogue pipeline (8x8 cells), 8-bit ADC, plus structure de tests/block

2D memory structure: 8x8/channels

Fully digital control:
- Bias voltage (10-bit) and current (8-bit)
- Power cycling (in optional)
- Shaping time programmable
- Sampling frequency programmable
- Internal calibration
- Sparsifier threshold programmable per channel
- Event tag and time tag generation

2 Trigger modes: Internal (integrated sparsification)
External (LVTTL) for beam test
Developing a mix-mode FE readout with pulse-height reconstruction, zero suppression, full digital control (highly fault tolerant, flexible/robust) power cycling, in DSM CMOS technology

Channel #i

- Préamplification + CR-RC Shaper
- Calibration
- Sparsificateur
- Bias generator: Bias voltage (10bits), bias current (8bits), reference voltage (10bits)
- Main control: pipeline, time stamp, event stamp, calibration, A/D conversion

Input interface, Initial Setup

Registre ADC,
Gray Counter
MULTIPLE XER
OUTPUT interface

3/27/2010

FEE-RO, DAQ for Strips at LC, A. Savoy-Navarro, LCWS2010
BUT: Major changes

- Now 130nm IBM technology (previously UMC-130)
- Total revisit and optimization of the analogue main blocks (preampli+shaper; sparsifier+2D pipeline; ADC; DACs & controls)
- Revisit the targeted values of the main parameters to more modest values as the technology is much more sensitive.
- Modeling (VERILOGA) of the analogue part that follows the new design of each blocks in order to prepare the digital part while the analogue part is still in progress.
- Develop a mix mode simulation
- Define a modular architecture of the 128 channel chip by blocks of 32 (corresponding to the elementary multiplexing: 1 ADC / 32 channels)

Goals: Submit each of the major blocks by mid May 2010 and, while they are in foundry, proceed to the full 128 channel chip design.
NEW SiTR_IBM130-128

New modular architecture

2 Bloc of 2x32 channels
FEE-chip: the basic blocks

- Preamplifier - Shaper block

Crucial piece!!

Modified parameters:

- Preamp: 20 mV/MIP over 10 MIP
- Shaper: Peaking time at 0.5 μs

Work in progress
FEE-chip: sparsifier+pipeline block

Zero suppression synopsis

Adder-Inverter

Work in progress

3/27/2010

FEE-RO, DAQ for Strips at LC, A. Savoy-Navarro, LCWS2010
FEE – ADC block

Two important elements of The Wilkinson ADC: The Comparator and Ramp Generator.
Now: 8bit-ADC

Work in progress: Block submitted to foundry
May 2010
Based on the expertise of the LPSC Team we will explore several DAC Designs for the later version of the Chip (SiTR_128) 

Low area implementation for R2RDAC

C2C versus Segmented Mode DAC: speed; dynamic range; high value for Cu

Presently: block with the previous DAC version translated in IBM-130 for May
MODELING the FEE-RO chip

**Verilog-A modeling:**

Why Verilog-A modeling?

- Model analog channel
- Develop in parallel analog and digital
- Test and validate digital code concepts
- Verify interactions between the two sides
- Setup mixed signal environment while analog is not available
- Faster simulations => faster debugging loops
MODELING the FEE-RO chip

- Verilog-A modeling: Work process
  - Code all non-generic components
  - Use Cadence Model Writer
  - Compile source codes to Virtuoso
  - Generate symbols
  - Draw schematics with models instances
  - Simulate to validate model
Verilog-A modeling:

Example of Validation tests

Detector signal simulation

Preamp-shaper simulation

Full chain simulated including multichannel simulation: now refining modeling

FEE-RO, DAQ for Strips at LC, A. Savoy-Navarro, LCWS2010
DAQ issues

• Processing of the data on detector at the various stages
• Synchronization
• Linking to the global DAQ
• Cabling

Work in progress, indeed mostly just starting...
DAQ step 1: data processing on the module

Some challenging aspects/consequences of the elementary module microcosm:

✓ **High processing level on chip**: taking advantage of the machine cycle & the potential DSM CMOS tech., the chip includes a fair amount of data processing.

✓ **The readout pitch vs sensor size & channel number/module**

An elementary module in the designed architecture of the detector, will include a relatively large number of channels (Order 2000) because of the small **readout pitch (50 µm)** and of the **large size of the sensor (10x10cm²)**. For a basic multiplexing 256/1 at the ADC level, this means 8 FEE chips.

✓ **Connection of the chips onto the sensor**: How to output the data is strongly related to the way the chips are connected on the sensor. Also various ways to gather them are under study (superchip or?)

∇ Choose to work as much as possible in parallel mode (vs daisy chaining)
∇ Concentrate the data output at the module level => 1st concentration step: Buffering plus some data output processing plus data synchronization
Explored solutions at the module level

- 8 SiTR_256 on kapton TAB linked to a buffer
  1st concentrator level/unit
- 8 SiTR_256 Gathered on a Superchip
  Including the 1st concentrator unit

- Data are sent from each chip to the concentrator unit on module
- Synchronization via the bunch trains:
  - bunch addressing is performed at chip level by the internal chip clock
  - module & train synchronization from global DAQ via the concentrator unit
DAQ step 2: gathering in parallel mode several modules into supermodules
Not taken into account:
- FTD data
- Zero suppression

Just starting to work on this item: lot to be done!!

3 “floors”:

F1: chip on sensor, full readout chain in a single chip (A/D, zero suppression, multiplex ...)

F2: on detector sides, daisy chains chips, data buffering, preprocessing ...

F3: processing, azimuthal sector, track reconstruction

Total number of modules:
- 500 (SIT) + 2500 (SET) + 2000 (ETDs)
- 5000 modules of 1792 channels

Total number of channels:
- $10^6$ (SIT) + $5 \times 10^6$ (SET) + $4 \times 10^6$ (2 ETDs)
- $10 \times 10^6$ channels
- $\sim 5.12$ Gbytes
Reading out the DAQ sub-elements

- On the “module”:
  Chaining of 8 SiTR_130-256

- “Super Module”:
  Chaining the adjacent ladders toward a level 1 concentrator

- Half cylinder (“Detector Element”):
  Level 1 concentrator (toward level 2?)

- Toward the global Silicon DAQ system by Optical fibers

- Send to Global DAQ system

Depending on the final requirements

Just starting to think about the topology design & how to build the DAQ chain:

*Just getting our nose out of the FEE chip....LOT to DO: setting of a task force*
CLIC & ILC: different e+ e- machines (technology, Ecm range) ⇒Thus their cycles are different ⇒so the environmental conditions imposed to the detectors & their associated electronics ⇒So also the Physics (going to higher Energy)
Adapting strip VFE (preampli+shaper) to CLIC has started.

We also have some idea based on our LHC previous experience how to achieve a fast pulse reconstruction and get a time-stamping with $O(25\text{ns})$ resolution.

Questions:
- Time Stamping $O(100\text{ps})$? If needed where? One dedicated layer?
- Pulse shaping at 20ms is feasible (?) 10ns requested anyway
- Power dissipation? could be kept reasonable?

<table>
<thead>
<tr>
<th>VFE Parameters (For CLIC case)</th>
<th>Circuit realised</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bruit du préamplificateur + shaper (à Cdet = 10pF)</td>
<td>$\sim 1000 \ e^-$</td>
</tr>
<tr>
<td>Gain en charge en sortie du shaper</td>
<td>30 mV/MIP</td>
</tr>
<tr>
<td>Consommation du préamplificateur</td>
<td>$&lt; 250 \mu W$</td>
</tr>
<tr>
<td>Consommation du shaper</td>
<td>$&lt; 100 \mu W$</td>
</tr>
<tr>
<td>Linéarité à 10 MIP</td>
<td>1%</td>
</tr>
<tr>
<td>Linéarité à 20 MIP</td>
<td>2%</td>
</tr>
<tr>
<td>Temps de montée en sortie du shaper</td>
<td>10 - 25ns</td>
</tr>
<tr>
<td>Temps de descente en sortie du préamplificateur</td>
<td>$&lt; 250$ns</td>
</tr>
<tr>
<td>Temps de descente en sortie du shaper</td>
<td>$&lt; 200$ns</td>
</tr>
</tbody>
</table>
Test prototypes in realistic lab test bench or beam tests

SiTR 130-4 + HPK modules

CERN SPS

S/N=23.4

DAQ test beam developments allow developing/exploring future DAQ strategy & Architecture => important!

FEE-RO, DAQ for Strips at LC, A. Savoy-Navarro, LCWS2010

3/27/2010
Go to 256 channels
Go to deeper DSM when mature (90 or 65 nm)
Thinning (50 µm)
Direct connection chip onto sensor
Design/strategy of the DAQ architecture on detector:
  => synchronization
  => data processing, compacting & buffering
  => cabling
Linking with general DAQ
Adapting FE to CLIC cycle
Bunch tagging at CLIC
Pursue developing TOT alternative

As for all the Silicon Tracking R&D topics: have a short term baseline and
Keep on developing longer term, beyond the baseline solutions.
Each step in the development is submitted to the evaluation in realistic
test beam conditions: important!