Introduction of SOI
Pixel Development

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http://rd.kek.jp/project/soi/
• Introduction of SOI Technology
• SOI Pixel Detector Development
• On-Going R&D’s
• Summary
SOI Wafer Production (Smart Cut by SOITEC)

1. Initial silicon
2. Oxidation
3. Implantation
4. Cleaning and bonding
5. Splitting
6. Annealing and CMP touch polishing
7. Donor wafer becomes new wafer A

CMOS (Low R)
Sensor (High R)
Bulk CMOS vs. SOI CMOS

In SOI, Each Device is completely isolated by Oxide.
Industry move: Bulk CMOS to PD-/FD- SOI CMOS

Faces many barriers to further miniaturization

Bulk Transistor

PD-SOI Transistor

Body is Partially Depleted and ‘floats’ independent from Bulk substrate

FD-SOI Transistor

Ultra-Thin Body (undoped)

Ultra-Thin Body is Fully Depleted

Box can optionally be ultra-thin, too

Addresses scalability issues

No History Effect
No kink effect

Tsi ~ 5-10nm (e/o process)
Tbox ~ 145nm / Tultbox ~ 10-30nm

(from "Fully DepletedSOI", Xavior Cauchy, SOI Industry Consortium)
Steep Sub Threshold Slope

Gate voltage is not wasted to deplete the bulk.

Lower Threshold (Leakage Current) is possible without increasing Leakage Current (Vth).
SOI Performance: Smaller Junction Capacitance

Cj is 1/10 of Bulk technology. Gate Capacitance is 30-40% Lower.

High Speed / Low Power
Radiation Tolerance

SOI is Immune to Single Event Effect

Gate Oxide

Depletion Layer

But not necessary strong to Total Ionization Dose due to thick BOX layer

This must be remedy for the application under high radiation environment.
Operation at Cryogenic Temperature

Bulk MOS

SOI MOS (worked in 1.4K)

KINK

Hysteresis

4.2K

4.2K
SOI Pixel Detector (SOIPIX)

Monolithic Detector having fine resolution of silicon and data processing power of CMOS LSI by using Silicon-On-Insulator (SOI) Technology.
Feature of SOI Pixel Detector

- No mechanical bonding. Fabricated with semiconductor process only, so high reliability, low cost are expected.
- Fully depleted thick sensing region with Low sense node capacitance.
- On Pixel processing with CMOS transistors.
- Can be operated in wide temperature (4K-570K) range, and has low single event cross section.
- Based on Industry Standard Technology.
# Lapis (*) Semiconductor 0.2 μm FD-SOI Pixel Process

| Process | 0.2μm Low-Leakage Fully-Depleted SOI CMOS  
1 Poly, 5 Metal layers.  
MIM Capacitor (1.5 fF/um²), DMOS  
Core (I/O) Voltage = 1.8 (3.3) V |
|---|---|
| SOI wafer | Diameter: 200 mmϕ, 720 μm thick  
Top Si : Cz, ~18 Ω-cm, p-type, ~40 nm thick  
Buried Oxide: 200 nm thick  
Handle wafer: Cz (n) ~700 Ω-cm,  
FZ(n) >1 k Ω-cm, FZ(p) >1 k Ω-cm |
| Backside process | Mechanical Grind, Chemical Etching, Back side Implant, Laser Annealing and Al plating |

(*) Former OKI Semiconductor Co. Ltd.
Regular Multi-Project Wafer (MPW) run. (~twice/year)

U. of Hawaii
Fermi Nat'l Accl. Lab.
Lawrence Berkeley Nat'l Lab.
INP Krakow
U. Heidelberg
Louvain-la-Neuve Univ.

JAXA
RIKEN
AIST
Osaka U.
KEK
Kyoto U.
Tohoku U.
Tsukuba U.

IHEP/IMECAS/SARI China

SOIPIX MPW run Wafer
Submission from Chinese Coleague

- 2013.1 MX1594
  IHEP (Lu Yunpeng) 6x6 mm$^2$ + 2.9x2.9 mm$^2$
  SARI (Ning, Wang, Li Tian) 2.9x2.9 mm$^2$

- 2012.7 MX1542
  IMECAS (Zhao Kai) 12.2x12.2 mm$^2$ + 2.9x2.9mm$^2$

- 2011.10 MX1501
  IHEP (Liu Gang, Lei Fan) 2.9x2.9 mm$^2$
  IHEP (Lu Yunpeng) 2.9x2.9mm$^2$

- 2011.1 MX1442
  IHEP (Liu Gang) 2.4x2.4mm$^2$

- 2010.8 MX1413
  IHEP (Zheng Wang, Lei Fan) 2.4x2.4 mm$^2$ x2
Transistor Type

Core Transistor (1.8V): Normal Vth & Low Vth
I/O Transistor (3.3V): Normal Vth & High Vth

Body Floating
Source-Tie (Type 1)
Source-Tie (Type 2)
Structure of Top Si

1 Poly + 5 Metal MIM Capacitor on 3M
Sensor Structure

- **PS & NS --- High Doping Density Layer (Top Si is removed)**
- **BPW, BP2, BP3 & BNW --- Low Doping Density Layer (Top Si is not removed)**
Trace Fuse (option)

You can chase the chip location where it come from if you include this fuse in your design.

Number of Fuse (total 16 lines)
* Lot No. : 4 lines (1~15)
* Wafer No. : 5 lines (1~31)
* Chip Location in wafer : 7 lines (1~127)
I/O Cell Libraries

We prepared several I/O frames for your convenience.

Chip Frame for Pixel

I/O Buffers
+ Vdet ring
+ Vbias ring
+ BPW

6 mm Frame

2.9 mm Frame
We get minimum number of I/O cells from Lapis. Then we have created many more for users.

Please provide us your I/O cells if you develop new one.

<table>
<thead>
<tr>
<th>Lapis Library</th>
<th>KEK IOLIB5M3</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>S02_IT4N_2_5M</td>
<td>ioIT4N_5M2</td>
<td>Digital Input Buffer</td>
</tr>
<tr>
<td>S02_OT4A_2_5M</td>
<td>ioOT4A_5M2</td>
<td>Digital Output Buffer</td>
</tr>
<tr>
<td>S02_VDD33_5M</td>
<td>ioVDD33_5M3</td>
<td>3.3 V Power</td>
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<tr>
<td>S02_VDD18_5M</td>
<td>ioVDD18_5M3</td>
<td>1.8V Power</td>
</tr>
<tr>
<td>S02_VSS_5M</td>
<td>ioVSS_5M3</td>
<td>Ground</td>
</tr>
<tr>
<td>S02_CORNER_VER2_5M</td>
<td>ioCORNER_5M2</td>
<td>Corner Cell</td>
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<td></td>
<td>iodr_5M2</td>
<td>Analog pad with protection diodes and resistor</td>
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<tr>
<td></td>
<td>iod_5M2, iod_5M3</td>
<td>Analog pad with protection diodes</td>
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<td></td>
<td>iothr_5M2</td>
<td>Direct analog pad</td>
</tr>
<tr>
<td></td>
<td>iobuf_5M2</td>
<td>Digital bidirectional Input/Output Buffer</td>
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<td></td>
<td>ioring29_5M3</td>
<td>IO ring for 2.9mm chip</td>
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<td>ioring29L2_5M3</td>
<td>IO ring for 2.9mm chip with 200um bias spacing for pixel (new)</td>
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<tr>
<td></td>
<td>ioring60_5M3</td>
<td>IO ring for 6.0 mm chip</td>
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<td>IO ring for 6.0 mm chip with 200um bias spacing for pixel</td>
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<tr>
<td></td>
<td>LVDSDRV_00</td>
<td>LVDS Driver</td>
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<tr>
<td></td>
<td>LVDSRCV_00R</td>
<td>LVDS Receiver with 100 Ohm terminator</td>
</tr>
<tr>
<td></td>
<td>LVDSRCV_01</td>
<td>LVDS Receiver without terminator</td>
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<tr>
<td></td>
<td>LVDSBIAS_00</td>
<td>LVDS Bias Circuit</td>
</tr>
<tr>
<td></td>
<td>io lvds</td>
<td>LVDS cells layout example</td>
</tr>
<tr>
<td></td>
<td>io_AOBUF33EN_5M3</td>
<td>Analog output buffer</td>
</tr>
<tr>
<td></td>
<td>ioBIAS33_5M3</td>
<td>Analog buffer bias circuit</td>
</tr>
<tr>
<td></td>
<td>io_aobuf</td>
<td>Analog buffer layout example</td>
</tr>
</tbody>
</table>
• We are using relatively large mask to enable many designs and large sensors
• Low cost per area.
• Smallest chip area: 2.9 x 2.9 mm²
Stitching Exposure

Mask Layout

Exposed Layout

If you want much larger detector …
Riken SOPHIAS detector

- Width of the Buffer Region can be less than 10um.
- Accuracy of Overwrap is better than 0.025um.
It was difficult to process 8” FZ-SOI wafer in CMOS process.

<table>
<thead>
<tr>
<th>Before Oxidation</th>
<th>Conventional SOI Process</th>
<th>Improved SOI Process</th>
</tr>
</thead>
</table>

We optimized the process parameters, and succeeded to perform the process without creating many slips.
High Resistive wafers

- CZ(n) 0.7 kΩcm 260 µm
  - Mechanical Grind

- FZ(n) 7 kΩcm 500 µm
- FZ(p) 40 kΩcm 500 µm
  - Chemical Etch
  - Over Deplete
  - INTPIX3e
Data Acquisition Board

- Soi Evaluation Board with SITcp (SEABAS)
- A FPGA controls the SOI Pixel chip
- Directly transferred to Ethernet
On-Going SOI Projects in Japan

- INTPIX: Genera Purpose Integration Type
- CNTPIX: General Purpose Counting Type
- SOPHIAS: Large Dynamic Range for XFEL
- PIXOR: Belle II Vertex Detector
- XRPIX: X-ray Astronomy in Satellite
- MALPIX: TOF Imaging Mass Spectrometer
- TDIPIX: Contamination Inspection
- LHDPIX: Nuclear Fusion Plasma X-ray
- ...

© Rey. Hori
Integration Type Pixel (INTPIX)

\[ V_{\text{sense}} = \frac{Q}{C} \approx \frac{0.6 fC}{8 fF} = 70 mV \]

Size: 14 \( \mu \)m x 14 \( \mu \)m with CDS circuit
INTPIX6 Pixel
2 Gain
12 x 12 um²
INTPIX4
Pixel Size: 17 um x 17 um
No. of Pixel: 512 x 832 (= 425,984)
Chip Size: 10.3 mm x 15.5 mm
V_{sensor}=200V, 250us Int. x 500
X-ray Tube: Mo, 20kV, 5mA

Fine resolution & High Contrast

X-ray Image of a small dried sardine taken by a INTPIX4 sensor (3 images are combined). (A. Takeda)
Cu Kα and Kβ is separated
Noise ~ 23e⁻ @ -50°C

188 eV (FWHM)

Al-Kα (1.49 keV)

(Energy (keV))

Counts

(FWHM=280eV
Readout Noise=23 electrons rms
Fano Noise=15 electrons rms

Si Escape?

Mo-Kα 17.44 keV

Cu-Kβ 8.90 keV

Cu-Kα 8.04 keV

Entries 399115
Mean 0.3669
RMS 2.137
χ² / ndf 0.4078 / 2
Constant 116.8 ± 8.3
Mean 33.41 ± 0.03
Sigma 0.5014 ± 0.0305

(Kyoto Univ.)
Compton Electrons from High-Energy X-rays
Issues in SOI Pixel

Sensor and Electronics are located very near. This cause ..

We need additional back-plane to suppress these effects.

We need additional back-plane to suppress these effects.
Buried p-Well (BPW)

**Substrate Implantation**

- Cut Top Si and BOX
- High Dose

**SOI Si**

**BPW Implantation**

- Keep Top Si not affected
- Low Dose

- Suppress the **Back Gate Effect**.
- Shrink pixel size without losing sensitive area.
- Increase break down voltage with low dose region.
- Less electric field in the BOX which improve radiation hardness.
$I_{d}-V_{g}$ and BPW

**NMOS**

**w/o BPW**

**with BPW=0V**

Back gate effect is suppressed by the BPW.
Nested Well Structure

- Signal is collected with the deep Buried P-well.
- Back gate and Cross Talk are shielded with the Buried N-well.
Impurity Concentration

Peaks of BNW and BPW are separated ~0.7 µm to reduce capacitance.
Double SOI Wafer

- Shield transistors from bottom electric field
- Compensate electric field generated by the trapped hole in the BOX.
- Reduce crosstalk between sensors and circuits.
Cross Talk Simulation

**Signal On the Sensor**

Cross Talk from the circuit to the sensor can be reduced 1/10, and signal shape will be bipolar. \(\rightarrow\) disappear in charge amp.

**Induced Signal at the Sensor**
- Standard SOI (690e-)
- Double SOI (63e-)

Voltage vs. time graph showing the response of the sensor to different signals.
Negative View

Gate

Top-SOI

BOX2

BOX1

Sub

Middle-SOI

0.3um
Suppression of Back-Gate Effect with Middle-Si layer

a) Middle-Si Floating

b) Middle-Si = GND

Back-Gate Effect is fully suppressed with the Middle Si Layer of fixed voltage.

Nch Core Normal-Vt
L / W = 0.2 / 5.0um
Vd=0.1V
Trapped Charge Compensation (Threshold Control) with Middle-Si Layer

Threshold voltage of a transistor is controlled with the bias voltage of the Middle-Si layer. This indicates effects of the trapped charge in the BOX can be compensated with the bias voltage.

Nch Core Normal-Vt
L / W = 0.2 / 5.0 um
Vd=0.1V, Vback: floating
Double SOI Irradiation Test

We could observe restoration of the threshold shift with applying negative voltage to the SOI2 layer.
Summary

• SOI technology has many good features; low power, low variability, large operating temperature range, no latch up..., and Industries are moving to extremely thin SOI.

• SOIPIX is monolithic detector, and many kinds of detectors are already working.

• We have ~twice/year regular MPW runs with increasing no. of users.

• The process technology is still progressing; Higher resistivity wafer, Nested well structure, Larger mask size, Stitching, and Double SOI, etc. …

• We welcome new collaborators to the SOI pixel development!