Development of SOI Electronics

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Outline

1. SOI Technology in Microelectronics
2. SOI in System Integrated Chip
3. SOI in Harsh-Environment Application
4. Relative Works of our Research Group
5. Summary
SOI Technology in Microelectronics

Bulk Planar

Extremely Thin SOI

Ultra Thin Body & Box

CMOS: SOI vs. Bulk

High-Speed (Low Capacitor), Low-Power (Low Leakage), No Latch-up, Better SER etc.
Advantages of FDSOI CMOS technology:

- No Kink effects, No body-contact area;
- More speed, Less RC, Lower Power;
- Easy design transfer from Bulk;
- First choice for Sub-10nm node.
SOI in System Integrated Chip

- High Performance CMOS Circuits
- Excellent Analog/RF Circuits
- Complex MEMS/Sensor/Actuator
- Dedicated Optical-devices
- SOI, to fabricate complex SOC.

Flow sensor

SOI Pixel Detector

Spring

Bolometer

SOI thickness (µm)

[O. Lacoste et al., *IEEE Sensors* 2004]

[M. El Ghorba et al., *Transducers* 2007]

[S. Sobieski et al., *Sensors Letters*, 2009]
SOI in Harsh-Environment Application

- Less susceptibility to soft errors
  - SER reduced by 5~7X
  - Low power high reliability
  - No single-event latch-up
  - FDSOI has better SER than PDSOI

High-Temp: Guaranteed Operation To 225°C For Five Years Pressure!
SOI in Harsh-Environment Application

Total Dose radiation — cumulative radiation from trapped protons, electrons, solar energetic particles. These can cause permanent damage to most unhardened electronics. Especially for SOI Circuits!

Gate-Oxide, Buried-Oxide, Field-Oxide, Island-Edge and Substrate Engineering.

Research on TID Hardening offers more chances for harsh environments application!
Relative Works of our Research Group

- **SOI CMOS Device Physics**

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**Physical Theories; SOI CMOS Device Models.**
Relative Works of our Research Group

- Large Scale SOI CMOS Circuits

SRAM & Structured ASIC Circuits
Relative Works of our Research Group

- **SOI CMOS Reliability and Electro-Magnetic Compatibility**

Temperature, voltage and radiation.

Reliability; Electro-Magnetic Compatibility; Radiation Hardening.
Relative Works of our Research Group

- Radiation Hardening by Technology and Circuit Design

![Graphs and Diagrams]

\[ I(t) = f(LET) \cdot (e^{-\alpha t} - e^{-\beta t}) \]

Reliability; Electro-Magnetic Compatibility; Radiation Hardening.
Summary

- **Advanced SOI Electronics**
  - First choice beyond 10nm node CMOS Tech.
  - Possibility to fabricate complex SOC.
  - Ability for harsh environment application.

- **Relative Works of our group**
  - SOI CMOS Device Physics.
  - Large Scale SOI CMOS Circuits.
  - SOI CMOS Reliability and EMC.
  - Radiation Hardening by Tech. and Design.

- **Farther efforts to improve chip ability**
  - Find and solve related scientific problems.
  - To get better chips with excellent performance.
THANKS!