Status report of Vertex detector

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Outline:

- Introduction
- R&D activities
- Progress since April meeting
- Summary and outlook
Introduction
CEPC and its beam timing

Circular $e^+e^-$ Higgs (Z) factory  two detectors, 1M ZH events in 10yrs
$E_{cm} \approx 240$GeV, luminosity $\sim 2 \times 10^{34}$ cm$^{-2}$s$^{-1}$, can also run at the Z-pole

Pretzel Scheme

- Baseline design in pre-CDR
- 48 bunches / beam
- Colliding every 3.6μs, continuously
  →Power pulsing not applicable

Partial Double-ring Scheme

- Crab-waist collision to reduce beam and AC power
- Avoiding pretzel scheme to increase the flexibility and luminosity
- 196ns bunch spacing
- 48 bunches / train
- Duty cycle: 9.4μs/181μs

Reference: CEPC/SppC with ILC (FCC), J. Gao, LCWS 2015, Nov. 2-6, 2015, Whistler, Canada
Detector requirements

- Efficient tagging of heavy quarks (b/c) and τ leptons

\[ \sigma_{r\phi} = a + \frac{b}{p(GeV) \sin^{3/2} \theta} (\mu m) \]

- \(a\) depends on single point resolution \(\sigma_{s.p.}\) & on the lever arm
- \(b\) depends on the distance between the innermost layer to IP and on the material budget

- to achieve \(a=5\) and \(b=10\) (B=3.5T):
  - \(\sigma_{sp}\) near the IP: \(\leq 3 \mu m\) → Fine pixel
  - material budget: \(\leq 0.15\%X_0/layer\) → Low power consumption
  - first layer located at a radius: \(~1.6\ cm\)
  - pixel occupancy: \(\leq 1\ %\) → Fast readout

**Target:** fine pitch, low power, fast pixel sensor + light structure
Various sources of backgrounds studied with Monte Carlo simulation:
- Beamstrahlung
- Lost Particles
- Synchrotron Radiation
- Hit density $\sim 1 \text{ hit cm}^{-2} \text{ BX}^{-1}$ (Preliminary)
Considerable due to 280K BX/s:

- TID $1\text{Mrad/\text{year}}$
- NIEL $1 \times 10^{12} n_{\text{eq}} / (\text{cm}^2 \text{ year})$
- A safety factor of 5 applied

Radiation levels

![Graph showing total ionizing dose and 1 MeV neutron equivalent flux](image)
Detector Layout

Vertex detector:
• 3 layers of double-sided pixels
• $\sigma_{SP}=2.8\mu m$, inner most layer
• readout time <20$\mu$s

VXD Geometry

| Layer | R (mm) | |z| (mm) | $|\cos \theta|$ | $\sigma_{SP}$ ($\mu$m) | Readout time ($\mu$s) |
|-------|--------|---------|---------|-----------------|------------------|-------------------|
| Layer 1 | 16 | 62.5 | 0.97 | 2.8 | 20 |
| Layer 2 | 18 | 62.5 | 0.96 | 2.8 | 20 |
| Layer 3 | 37 | 125.0 | 0.96 | 4 | 20 |
| Layer 4 | 39 | 125.0 | 0.95 | 4 | 20 |
| Layer 5 | 58 | 125.0 | 0.91 | 4 | 20 |
| Layer 6 | 60 | 125.0 | 0.90 | 4 | 20 |
R&D activities

- CMOS pixel sensor-funded by IHEP and State key laboratory
- SOI pixel sensor- funded by NSFC
Technology options

Many technologies from ILC/CLIC could be referred. BUT, unlike the ILD, the CEPC detector will operate in continuous mode. → without power-pulsing

**Pixel sensor:** power consumption < 50mW/cm², if air cooling used

- **HR-CMOS** sensor with a novel readout structure
  - relatively mature technology
  - <50mW/cm² expected
  - Capable of readout every ~4μs
- **SOI** sensor with similar readout structure
  - Fully depleted HR substrate, potential of 16μm pixel size design
  - Full CMOS circuit
- **DEPFET:** possible application for inner most vertex layer
  - small material budget, low power consumption in sensitive area
- **3D-IC:** ultimate detector, but not mature enough
Pixel sensor R&D activities

Initial sensor R&D targeting on
  – *Pixel pitch* ~16μm
  – *Power consumption at the current level* <100mW/cm²
  – *Integration time* 10-100μs

• **HR-CMOS sensor**
  – *Towards complete CMOS & thick, fully depleted substrate*
  – *more in-pixel functional circuitry → faster read-out & less power, radiation tolerant*
  – *TowerJazz CiS 0.18μm process*

• **SOI sensor**
  – *Fully depleted substrate: 50 μm thick, larger signal charge*
  – *Develop in-pixel circuit for minimum layout area*
  – *LAPIS 0.2μm process*

*Detailed information: Y. Lu, CEPC-SppC study group meeting, 2016 April*
CPS - Charge collection simulation

Motivation:
- Guide the diode geometry optimization and study radiation damage with different types of epitaxial layer

Simulation with different parameters
- Hit position
- Diode geometry
- Thickness and resistivity of the epitaxial layer
- Radiation damage

Y. Zhang, et al, NIMA 831(2016)99-104

Pixel cluster with four different epitaxial layers

Charge collection with non-ionizing damage
Goals: sensor optimization and in-pixel pre-amplifier study

Floorplan overview:
- Two independent matrices: Matrix-1 with $33 \times 33 \, \mu m^2$ pixels (except one sector SFA20 with $16 \times 16 \, \mu m^2$ pixels), Matrix-2 with $16 \times 16 \, \mu m^2$ pixels.
- Matrix-1 includes 3 blocks with in-pixel pre-amplifier
- SFA20 in Matrix-1 contains pixel with AC-coupled pixels

Tower Jazz CIS 0.18 μm, November 2015 submission

Two types of wafer:
- 18 μm HRES epi wafer
- 700Ω Czochralski wafer
First CPS prototype design - pixel structures

- DC-coupled SF pixels: 2T/3T structure
  - different diode geometries
    → to verify the TCAD simulation results
  - two biasing modes (2T/3T)
  - two transistor types (nmos/pmos SF)

Y. Zhang (IHEP)

- AC-coupled pixel
  - sensing node AC-coupled with circuit
  - diode bias voltage could be higher than power supply, i.e. up to 10V
    → larger depletion region & lower $C_d$
    → higher SNR

Y. Zhou (IHEP)
First SOI pixel prototype – design and test

- Compact Pixel for Vertex (CPV1)
  - 16*16 μm with in-pixel-discrimination
  - Pixel array: 64*32 (digital) + 64*32 (analog)
  - Double-SOI process for shielding and radiation Enhancement
  - Submitted June, 2015

- Test (preliminary)
  - Threshold scan
  - Temporal noise ~ 17e-
  - Radiative source response

CPV1 digital pixel layout

Y. Lu, J. Dong (IHEP)
Progress since April meeting
CMOS pixel sensor study

New funding from MOST (2016-2021)

R&D targeting on
- *Position resolution* 3-5μm
- *Power consumption* <100mW/cm²
- *Integration time* 10-100μs

CMOS pixel sensor
- *Small pixel size*
- *In-pixel functional circuitry*
- *Novel readout scheme → faster & less power*
- *Full functional chip*
- *~2 MPW and 1 engineering run*
• Purpose: small-size digital pixel design verification

• Proposed floor plan:
  – 4 sub-matrices with different pixel structures, each matrix with 32 columns by 64 rows pixels
  – Pixel size: less than $22 \times 22 \, \mu m^2$
  – Each pixel contains a sensing diode, a pre-amplifier and a discriminator
Small pixel size DMAPS in-pixel design

Y. Yang (IHEP)

**Design goal:** contradictory with each others, carefully tradeoff required

- **Sensing + Amplification + Digitalization in** each single **pixel:**
  - Complex in-pixel electronics
- **Highly compact pixel size:** \( \approx 20 \times 20 \ \mu m^2 \)
  - \( >40\% \) pixel size to shrink compare with similar design
- **Low noise:** 20 - 30 e\(^{-}\)
  - In-pixel noise reduction required
- **Fast readout speed:** several tens \( \mu s / \text{frame} \); around 100 ns/row with rolling shutter readout strategy
  - Elaborate operation timing

**Technical proposal:**

- **High voltage biasing** to the sensing diode (**up to 10 V**), fully depleted Epi. layer.
  - Higher seed pixel signal; less diode equivalent capacitance
- **In pixel CDS** (Correlated Double sampling): pixel offset reduction
- **High precision comparator** with **simple architecture**
Proposed architectures

Version 1: differential amplifier + latch
- DMAPS sensor + discriminator based on one stage differential amplifier
- With offset-compensated technique

- Similar transistor numbers
- Version 1 has lower amplification factor while suffer less from LATCH ‘kickback noise’

Version 2: 2 stage CS amplifiers + latch
- DMAPS sensor + discriminator based on the two stages of single-end amplifier
- Simpler structure than the version-1
Design goal:

- **Low-power** front-end with digital output pixel
- Pixel size: $22 \times 22 \, \mu m^2$
- Power consumption: $\sim 40 \, nW/pixel$
- Pixel ENC: $\sim 20 \, e^-$

Closed-loop front-end based on CSA
Critical design points

- A direct cascode amplifier for the CSA
  - Simple structure with high gain → for a compact layout
- A very low feedback capacitance $C_f$ (0.2 fF) with low mismatch → for a high charge-to-voltage conversion gain, low noise and low mismatch between pixels
- A single-end current comparator → for a compact layout
Goals:
- pixel size: 26*26 um$^2$
- Signal duration time: < 3 us
- Readout speed: 25 ns/hit
- power consumption: < 80 mW/cm$^2$

Solution:
- Fast front-end (discriminator) + zero suppression readout

Status:
- Front-end: peaking time 800 ns, duration time 3us
- Zero suppression readout: A XYZ solution has been designed, but the area needs to be optimized
- Other blocks are still under design
1.6mm: 64 row
3.2 mm: 128 col

- Chip area: about 8 mm²
- Pixel array 64 row*128 col
- Front-end using current comparator
- Last row add additional analog readout controlled by a small scan logic
- 10 bits R-2R voltage DAC used for bias
- Additional PAD used for negative voltage up to -8 V

Matrix readout using XYZ solution
- 8*8 pixels as a super pixel using 16 address lines XY
- every super pixel using the same 16 address lines
- add Z to identify different super pixel

Power, Analog Pads, Digital Pads
Voltage DACs, analog readout chain
Scan logic (Analog readout for test)
Periphery Readout Logic
Last row also used for analog readout
Clock for readout
Address line
8*8 pix	8*8 pix
1.6 mm
64 row
0.15 mm
0.5 mm
0.25 mm
Second SOI pixel prototype design

Y. Lu, Y. Yang (IHEP)

CPV2
- In-pixel CDS stage inserted
- To improve RTC and FPN noise
- To replace the charge injection threshold
- Submitted June, 2016

Pixel Layout: $16 \times 16 \, \mu m^2$
Common efforts on CMOS pixel sensor R&D

Collaboration for future electron-positron colliders:
IPHC Strasbourg (France)
IHEP, Shandong Univ. Central China Normal Univ. (China)

Target: 10 hits/cm²/µs, read-out speed ~1 µs, $\sigma_{s.p.}$ ~3 µm
- In-pixel Front-end: preamplifier + discriminator
- High speed sparse read-out at column level
- Second data compression logic by pattern recognition
- High speed data transmission
Common efforts on SOI pixel sensor R&D

Collaboration for future electron-positron colliders:

KEK (Japan)
IHEP (China)

• Sensor design
  – Optimization of diode structure
  – Guard ring and slim edge
• Circuit design
  – In-pixel discrimination
  – High speed data link
• Process
  – Thinning and back-side processing
• Time stamp scheme

SOIPIX workshop 14-15th July 2016 IHEP, Beijing
Summary and outlook

• R&D started along the baseline design specifications
• Pixel sensors design submitted
  – CPS diode optimization
  – SOI sensors with small pixel size
• 2\textsuperscript{nd} CPS prototype design in progress
  – More in-pixel electronics
  – New asynchronous readout architecture

• Test system in preparation and sensor characterization will start soon
• Overall sensor architecture in consideration
• Optimization study of vertex system needed
• Double-sided and light supporting structure, cooling,...
• Possible change of sensor design
  – Beam related background level
  – Impact of partial-double ring scheme, with time-stamp of microsecond
  – Impact of Z-pole running
Thanks for your attention!