A counting type SOI chip and synchrotron beam test results

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Outline

• Introduction
  – Challenges in SOI pixel technology

• A description of the chip (CPIXTEG3b)
  – Shielding enhancement
  – Chip architecture

• Electrical characterization
  – Measurement of shielding
  – Threshold dispersion and noise

• Synchrotron beam test
  – X-ray response
  – Micro-beam scan
  – Threshold scan

• Summary and outlook
Mutual interference between sensor and electronics

- **SOI offers outstanding benefits** (my personal view):
  - Quick turnaround
  - Extremely high density connections
  - Further thinning down to tens of um.

- **However, stronger interference between sensor and electronics**
  - Back-gate effect
  - Charge injection ← the focus of this talk

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The concept of charge injection

• Signal charge collection and amplification
  – Inverse-biased diode, Cd
  – Pixel amplifier, providing voltage gain or V/Q conversion

• The capacitive feedback path from transistors to collection electrode
  – Cp determined by Area/Tbox
  – Vout node is critical, but the feedback path exists everywhere.
Voltage amplifier case

For a source follower, $0 < A < 1$
- Lower gain

For a composite amplifier with $A >> 1$
- $V_{out} = -\frac{Q}{C_p}$
- $C_p$ dominates the gain

Denominator $= 0$, $V_{out}$ may be stuck at $V_{dd}$ or oscillate

Electrical model

\[
V_{out} = \frac{Q}{C_d} \times A
\]

\[
V_{out} = \frac{Q}{C_d + (1-A) \times C_p} \times A
\]
Charge-sensitive amplifier case

Without Cp

\[ V_{out} = \frac{Q}{C_f} \times A_2 \]

With Cp

\[ V_{out} = \frac{Q}{C_d + (1+A_1)C_f + (1-A_1A_2)\times C_p} \times A_1A_2 \]

\[ \approx \frac{Q}{C_f - A_2 \times C_p} \times A_2 \]

- C-S amplifiers are widely used in counting-type pixel
- For \( C_f \sim A_2 \times C_p \), \( V_{out} \) may oscillate.
Self-sustained oscillation of counting-type pixel

- Observed on a test structure that has no protection against charge injection at all.
  - Charge injection is a major issue for counting type SOI pixel!
Countermeasure: Double-SOI process

- Double-SOI is a critical ingredient for the success of counting-type pixel.
  - A new conductive layer SOI2 serves as a shielding layer
  - High sheet resistance, ~33kΩ/□
  - Increase Cd, 0.23 fF/um²
  - How to use it properly?
Critical design choices to enhance shielding

- Based on the experience and knowledge from study of Nested-wells*.

Simple guidelines in the CPIXTEG3b design (Double-SOI prototype)

- Kept the collection electrode clear of counter/discri., which leaded to
  - A small collection electrode of 16 um
  - A small counter of 6-bit

- Improved the shield grounding
  - Placed SOI2 contacts as many as possible
  - Used local bypass capacitor on SOI2 ground

- P-stop ring isolating pixels

*Detailed study on SOI shielding was reported at International Workshop on SOI Pixel Detector (SOIPIX 2015)
CPIXTEG3b chip

- **Signal processing chain in-pixel**
  - N-in-P sensor, 310um thick
  - Charge sensitive amplifier with electrical calibration capability
  - Discriminator with a local DAC to tune the threshold
  - 6-bit ripple counter & 6-bit shift register
  - Hundreds of transistors

- **Pixel array organization**
  - Data chain organized in column
  - Counting mode or shift-readout mode
  - Bidirectional data bus shared by all columns
  - 64*64 pixel array at a pitch of 50um
  - Chip area 6*6mm²
Setup for electrical characterizing

- Bare chip mounted in ceramic packages
- Hooked up with SEABAS* test system
- 4-channel oscilloscope synchronized with electrical test pulses
  - Measurement time-correlated with stimulus
- Chips from Double-SOI wafer and Single-SOI wafer
  - A unique chance for comparison

*A DAQ system developed by KEK, mainly for pixel chip readout
Front-end waveform inspection

- Double-SOI chips worked
  - Waveforms largely agree with simulation data;
  - Slower leading edge is due to capacitive load of cable;
- In the contrary, Single-SOI chips showed self-sustained oscillation
  - Managed to stop it by decreasing gain of shaper

Self-sustained oscillation observed on single-SOI chips
Pickup of digital switching

- Counter driven by external clock as a source
- 5mV @ shaper output for Double-SOI chip
  - 74 e\(^{-}\) referred to input charge
  - Submerged in noise floor (ENC ~ 113e\(^{-}\))
- 95mV for Single-SOI chip
  - ~3770e\(^{-}\) referred to input charge

![Graph showing signal levels and waveforms with annotations for Double and Single SOI chips.](image-url)
Threshold dispersion and noise

- Threshold dispersion without tuning
  - RMS $97e^{-} \cdot 1760e^{-}$
- ENC noise
  - Average $106e^{-}$
- Expected S/N $\sim 15$ @ 6 keV X-ray

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Synchrotron beam test

- KEK PF BL-14A
  - Beam spot 0.8mm in diameter
  - optional pin hole collimator, 10um beam spot

16 keV X-ray signal (shaper)

Beam profile measured by CPIXTEG3b

- 65419 photons, 16 × 19 pixels
- 153938 photons, 21 × 22 pixels

(16keV, threshold~1600e-) (6keV, threshold~900e-)

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Micro-beam scan@ 16 keV

- Beam spot ~ 10um, step size = 10um
  - Sensor bias = -70 V, fully depleted
  - Threshold ~ 2200e⁻

- Homogeneity needs further study
  - Threshold not tuned yet
  - CCE and charge sharing

- Point spread function
  - Full width < 50um @ 1% maximum height
Threshold scan

- Counting rate vs threshold
  - Monotonically as expected
  - Inclined plateau possibly due to energy spread of beam and charge sharing
  - Threshold touched noise floor @ 850e⁻
  - Consistent with electrical calibration (blue line)

16 keV 10×10 μm² beam

6 keV 800×800 μm² beam
Summary and outlook

- CPIXTEG3b was designed with an emphasis on the shielding of charge injection.
- Methods to mitigate the impact of sheet resistance of SOI2 verified:
  - Keep collection electrode clear of digital parts
  - Place SOI2 contacts as many as possible
  - Use local bypass capacitor on SOI2 ground
- Exciting measurement results achieved:
  - Charge injection well controlled
  - Sufficient S/N to detect 6 keV X-ray
  - Point spread full width < 50um @ 1% maximum height
  - Beam test S-curve consistent with electrical calibration
- Design of CNPIX1 finished recently, collaborative efforts between IHEP and KEK.
  - Much more powerful design: charge sharing arbitration, compact hexagonal layout, 18-bit counter, lower noise
  - Expecting the chips back around the end of this year.
Thank you for your time!
Backup slides
The challenges in SOI pixel technology(1)

• KEK SOI process
  – Deep sub-micron CMOS process, excellent for front-end electronics
  – Fully-depleted HR substrate, excellent for sensor
  – Thin dioxide insulation (BOX) between front-end and sensor, good for connections
  – A problem of mutual interference to solve, however

• Back-gate effect
  – Lateral potential increase alters the threshold of MOS transistors
  – A Buried-P-Well (BPW) layer implanted to form a “blanket” of uniform potential
  – Success of BPW has brought about the prosperity of integrating type SOI pixel
The challenges in SOI pixel technology(2)

- Counting type SOI pixel has to tackle another direction of interference
  - Voltage transition in front-end induces charge in sensor
  - Charge injection, \( Q = C \times \Delta V \)
  - A fundamental issue recognized since 1990’s
  - Different shielding schemes investigated

\[ \text{Charge injection from front-end to sensor} \]

\[ \text{N}^+\text{-P-N}^- \text{ structure} \text{ of shield and well used by CERN RD19, a failure in high temp. annealing process} \]

\[ \text{Nested-wells}, \text{ a modern version of N}^+\text{-P-N}^- \text{ developed in 2010’s, limited success due to high sheet resistance of shield (\sim 10k} \Omega/\square \text{)} \]