MicroTCA.4 /4.1 Hardware Standards & Software Guidelines Progress Overview

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for the xTCA for Physics Collaboration

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Standard Platforms for Physics

• Major Goals: Interoperable HW-SW components
  – 1. Interoperable HW-SW platform essentials, software diagnostics, interfaces
  – Lab users & Industry Collaboration to share, save on development costs
  – Speed “time to market”, lower costs by commercial availability, avoid 1-supplier traps (incl. custom lab sol’n)
  – Avoid dependence on vendor proprietary solution
  – Adaptable to new technology needs for >/= 2 decades
Physics Standards History

• Standards driven by new innovations for economic, performance advantages

• Lab-Developed Standards Timeline
  – 50 Years ago, ~1965, NIM, Nuclear Instrument Module
  – 40 Years ago, ~1975, CAMAC Data bus modules
  – 30 Years ago, ~1985, FASTBUS 10X BW bidirectional
  – 12+ Years ago, ~2004, ATCA, MTCA announced
    • Multi-GHz serial technology backplane
    • Redundancy for 0.99999 Availability at Shelf (Crate) level
    • Intelligent Platform Management Interface (IPMI)
  – 7+ Years ago- 2009 MTCA.4 HW, SW WG’s begin
# Physics Standards History

<table>
<thead>
<tr>
<th>Yrs. Ago</th>
<th>NAME</th>
<th>Features &amp; Technology Trigger</th>
<th>Status</th>
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</thead>
<tbody>
<tr>
<td>50 ('65)</td>
<td>NIM</td>
<td>Fast digital logic modules, ADCs, no data bus initially, triggered by discrete 0.7V Si switches plus new labs including SLAC</td>
<td>Still small commercial Instruments</td>
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<tr>
<td>40 ('75)</td>
<td>CAMAC</td>
<td>First data bus backplane, 24 bit unidirectional, 1 MHz transfers, analog-digital modules, triggered by new dense ICs</td>
<td>Small after-market activity exists</td>
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<tr>
<td>30 ('85)</td>
<td>FAST-BUS</td>
<td>10MHz 32bit bidirectional data bus, match bus of mainframe computers, board area 2X, spurred by µP’s, FPGAs, SLD at SLAC</td>
<td>Defunct</td>
</tr>
<tr>
<td>8 ('09)</td>
<td>MTCA</td>
<td>Serial backplane channels up to 12 GHz, spurred by Telecom industry. Triggered by Tx-Rx GHz chip industry, serial backplanes, redundant architecture, Intelligent Platform Management Interface (IPMI) for A=0.99999; ILC &amp; XFEL Projects</td>
<td>Physics adaptations launched at IHEP Real Time 2009</td>
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FASTBUS-SLD Story

• FASTBUS vs. Custom Chips
  – First pressed pin multilayer backplane developed at SLAC for use in SLD colliding beam detector
  – At same time first custom analog sampling arrays plus special logic chips developed at SLAC-Stanford made possible many front end boards inside of detectors
  – All Drift chamber, Calorimeter and Cherenkov front end electronics ended up inside the detector.
  – FASTBUS served very well on the detector platform with our first use of analog fiber-optic channels through rear transition modules to FASTBUS pre-processing cards.
PICMG xTCA for Physics 2002-16

- 2002 ATCA Announced by PICMG for Telecom industry
- 2004-06 ATCA with μTCA announced
- 2004-11 NSS-MIC paper advocating ATCA for ILC Controls
- 2005-07 Snowmass Physics controls papers DESY, SLAC
- 2005-11 Gromitz controls presentations DESY, SLAC
- 2007-06 First xTCA workshop FNAL
- 2009-06 xTCA for Physics WG’s Announced IHEP IEEE Real Time
- 2011-07 MTCA.4 with RTM Approved
- 2016-11 MTCA.4.1 Approved; Hot Plug, SHAPI Guidelines submitted
- 2017 –Q1 Hot Plug, SHAPI Approved; SPM, SDM submitted
## MicroTCA Glossary

<table>
<thead>
<tr>
<th>Abbr.</th>
<th>Definition</th>
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<tbody>
<tr>
<td>PICMG</td>
<td>PCI Industrial Computer Manufacturers Group</td>
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<tr>
<td>ATCA</td>
<td>Advanced Telecommunications Computing Architecture</td>
</tr>
<tr>
<td>MTCA.0</td>
<td>PICMG baseline Mezzanine Card for ATCA carrier card system</td>
</tr>
<tr>
<td>MTCA.4</td>
<td>1&lt;sup&gt;st&lt;/sup&gt; Physics version w/ Rear Transition Module</td>
</tr>
<tr>
<td>µRTM</td>
<td>Rear Transition Module</td>
</tr>
<tr>
<td>MCH</td>
<td>Microcontroller Hub</td>
</tr>
<tr>
<td>MTCA.4.1</td>
<td>Auxiliary Backplane Extension</td>
</tr>
<tr>
<td>µRTM</td>
<td>Rear Transition Module – no connection to Auxiliary Backplane</td>
</tr>
<tr>
<td>eRTM</td>
<td>Extended RTM mates to Auxiliary Backplane</td>
</tr>
<tr>
<td>eMCH</td>
<td>Extended MCH services Auxiliary Backplane</td>
</tr>
<tr>
<td>RPM</td>
<td>External Rear Power Module services Auxiliary Backplane</td>
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ATCA – MTCA Relationship

• ATCA
  – Large card & crate format, typ. 12 cards per crate
  – Dual redundant backplane architecture standard
  – Two Hub controllers split crate backplane in halves
  – Hot plug procedure + redundancy = 0.99999 Availability at crate level (5 minutes downtime per year)

• MTCA
  – Mezzanine card for ATCA carrier, 4 per carrier
  – Packaged in crate of any size, shape became MTCA.0
  – Similar dual redundant backplane developed by industry
MTCA.4 for Physics (or other)

• Rear Transition Module (RTM)
  – Key feature of ATCA to get all CABLES to rear, make hot-swap easy without disturbing cables, always a risk
  – MTCA had no RTM interface designed so standards team had to design, also doubling board space per slot

• Special Backplane Additions
  – Designated precision timing and trigger lines, card-to-card lines for vector summing, interlocking
  – Designated rear interface for HS serial lines for analog, digital and mixed uses (Classes to be followed by labs and vendors for interoperability); power MTCA-RTM card
MTCA.4 Backplane Architecture

[Diagram showing the backplane architecture with various sections and connections labeled.]

Courtesy K. Rehlich, DESY

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MTCA.4 12-slot Shelf

Open Spaces

Most cables from rear

Space for....

AMC Dual Star Backplane

Redundant:
- Power
- Fan
- Filter

Courtesy K. Rehlich & Elma

See similar units from Schroff, VadaTech

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12
MTCA.4 released July 2011

- MTCA.0 Extensions => MTCA.4 for Physics*

New Extension Features:
- AMC-RTM connector standardized with E-Keying, JTAG, IPMI Management & Power from AMC to RTM
- Low-jitter clock lines, point-to-point connections for vector, interlock summing
- RTM hot-swap feature same as AMC
- Linux based PCIe

*Not restricted to physics use!
MTCA.4 Summary

• Hardware
  – Successful development crate and infrastructure with close collaboration of labs, industry
  – DESY XFEL application modules developed in partnership with partner labs, industry
  – Multiple suppliers now offer crates form 2-12 modules per crate
  – Lab application developments ongoing, industry growing

• Software
  – Continued work on four documents: Standard Device, Process, Hardware API and Hot Plug Guidelines
Phase II HW: Auxiliary Backplane

• Proposal from DESY Partners: Low Level RF
  – Auxiliary backplane offers huge advantages in eliminating discrete coaxial cables
  – Decided to standardize but not dictating RF section
  – User can adapt basic form factor to other uses, or can have vendor add features

• Basic Features
  – Provision for Rear Power Modules, controllable +/- analog power, RTMs with ability to drive multiple crates, etc.
Enhancements MTCA.4 => MTCA.4.1

• New Extensions Added for MTCA.4.1
  – 1. Auxiliary RTM Backplane with RF performance
  – 2. Rear Power Modules (RPMs)
  – 3. MCH-RTM (Rear Transition Module)
  – 4. Boards & Protective Covers
  – 5. Applications Classes of RTMs

• Motivation
  – Routing RF signals on Aux BP eliminates coax cable jungle, improves system reliability
  – For RF solutions reduces rack 3X or more
  – Uses flexible (RF application not part of standard)
RTM Backplane mating to AMC BP
RTM Backplane Connector Zones

Zone 1 Area not standardized, user optional
Shield protects analog circuits from digital noise from front AMC backplane
Classes of Zone 3 RTM Zones

• Analog, Digital, Mixed
  – Increase interoperability with selection of lines for optimum transmission:
    • Analog differential
    • Digital
    • Clock
    • Mixed signal
    • User defined

• Classes Defined
  – A1.1, A2.1; D1.0, 1.1, 1..2, 1.3.
Greatly increased Analog via rear ±V power options, total AMC+RPM power, extension of control to additional crates
Cascading Shelves via MCH-RTM

Cascade of MTCA-4 crates (example PCIeExpress) to extend AMC slots

Future Upgrade Paths
- Bandwidth of AMC backplane 10 to 40GHz
- Wider Fat Pipe with extended MCH-RTM
- Computing power on MCH RTM
- Link through MCH-RTM to other shelves
MTCA.4.1 Final Hardware

- **MTCA.4.1 Enhancements**
- **Name** suggested by PICMG
- **Approved**, adopted, printed November 2016
- 160 pages
Software Guidelines Goals

• Goal:
  – Maximize Interoperability of basic software in common use for all applications
  – Hard copies available from PICMG
  – Repository accessible to all users (Github at DESY)
  – Guidelines, not rigid standards
  – However gaining maximum advantages will require some points of standard usage if users care about portability to other lab’s applications
Software Guidelines

• Prior standards
  – Very limited standardization of system SW
  – Real interoperability of lab, commercial products lost

• ATCA/MTCA Standards
  – MTCA.4 Linux PCIe platform based
  – ATCA/MTCA Intelligent Platform Management IPMI standard led by Intel, support by 200 companies
  – Out of band diagnostics & control down to board, device level; key to 0.99999 system Availability requirement
  – But true vendor interoperability including SW still lacking at board, applications level
Design Guide Definitions/Relations

- Standard Hot Plug Procedure (SHPP)
  - Eliminates interruption of service to replace faulty module or RTM

- Standard Process Model (SPM)
  - Platform agnostic access to thread scheduling, thread interlocks/synchronization, inter-thread communication, and timing services

- Standard Device Model (SDM)
  - Platform agnostic access to external devices
  - Integrated framework, API for stream-oriented, addressable devices

- Standard Hardware API (SHAPI)
  - Common (register-oriented) API for configuration/control/data readout on addressable devices
Device Removal Procedure
Standard Process Model Design Guide

- Standard operating model and Application Programming Interface (API)
- Code development to facilitate module re-use and portability
- Recommended for usage with MTCA.4 or MATCA.4.1 systems

Process Model Hierarchy

- Standard operating model and Application Programming Interface (API)
- Code development to facilitate module re-use and portability
- Recommended for usage with MTCA.4 or MATCA.4.1 systems
Standard Device Model Design Guide

MicroTCA™

PICMG® MTCA.4 Software Guideline

Standard Device Model Design Guide

Guidelines for designing I/O access software for MTCA.4 systems

May 4, 2017

Device Model Nomenclature
Standard Hardware API Design Guide

Guidelines for designing hardware access APIs for xTCA-based physics systems

PICMG® xTCA for Physics
Revision 1.0

Open Modular Computing Specifications

May 22-26 2017
TIPP’17 Beijing R. Larsen

Hardware API Model Nomenclature
2015-17 SW Progress Summary

• MTCA.4.1 Enhancements to MTCA.4
  – Full PICMG adoption November 2016

• Software Guidelines
  – Standard Hot Plug Procedure, Standard Hardware API
  – Full PICMG adoption November 2016
  – Standard Device Model, Standard Process Model
  – Submitted for PICMG adoption May 2017

• Proposed
  – SW Guideline for EPICS use cases for SDM, SPM, SHAPI: New volunteer user design team needed
PICMG xTCA for Physics Organization

PICMG
PCI Industrial Computer Manufacturers Group

PICMG xTCA for Physics Coordinating Committee

Hardware Working Group
PICMG Technical Committee

Founding Executive Members
IHEP, SLAC, FNAL, Cypress Systems

Software Architecture Working Group
PICMG Technical Committee
Summary Comment on Lab Standards

- Early lab standards were driven mostly by needs of *Detectors*, not accelerator controls
- MTCA.4, 4.1 designed for both
- ATCA finding some use in new LHC upgrades; choice depends on collaborators agreement
- MTCA finding use at several new labs/upgrades for controls, e.g. ESS, PLS
- Collaboration on detector applications, sharing solutions being encouraged at a number of labs including CERN, DESY
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- ITER
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- ESSB Portugal
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Companies
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