Electronics, trigger and data acquisition systems for the INO ICAL experiment

Satyanarayana Bheesette
For and on behalf of the INO/ICAL Electronics team

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ICAL, e-ICAL and m-ICAL

\[ \nu_\mu + n \to \mu^- + p^+ \]
\[ \bar{\nu}_\mu + p \to \mu^+ + n \]

Magnet coils

RPC handling trolleys

Total weight: 50Ktons

Satyanarayana Bheesette, TIFR, Mumbai          TIPP2017, Beijing, China          May 22-26, 2017
<table>
<thead>
<tr>
<th>Parameter</th>
<th>ICAL</th>
<th>e-ICAL</th>
<th>m-ICAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>No. of modules</td>
<td>3</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Module dimensions</td>
<td>16.2m×16m×14.5m</td>
<td>8m×8m×2m (90:1)</td>
<td>4m×4m×1m (720:1)</td>
</tr>
<tr>
<td>Detector dimensions</td>
<td>49m×16m×14.5m</td>
<td>8m×8m×2m</td>
<td>4m×4m×1m</td>
</tr>
<tr>
<td>No. of layers</td>
<td>150</td>
<td>20</td>
<td>10</td>
</tr>
<tr>
<td>Iron plate thickness</td>
<td>56mm</td>
<td>56mm</td>
<td>56mm</td>
</tr>
<tr>
<td>Gap for RPC trays</td>
<td>40mm</td>
<td>40mm</td>
<td>45mm</td>
</tr>
<tr>
<td>Magnetic field</td>
<td>1.3Tesla</td>
<td>1.3Tesla</td>
<td>1.3Tesla</td>
</tr>
<tr>
<td>RPC dimensions</td>
<td>1,950mm×1,910mm×24mm</td>
<td>1,950mm×1,910mm×24mm</td>
<td>1,950mm×1,910mm×24mm</td>
</tr>
<tr>
<td>Readout strip pitch</td>
<td>30mm</td>
<td>30mm</td>
<td>30mm</td>
</tr>
<tr>
<td>No. of RPCs/Road/Layer</td>
<td>8</td>
<td>4</td>
<td>2</td>
</tr>
<tr>
<td>No. of Roads/Layer/Module</td>
<td>8</td>
<td>4</td>
<td>1</td>
</tr>
<tr>
<td>No. of RPC units/Layer</td>
<td>192</td>
<td>16</td>
<td>2</td>
</tr>
<tr>
<td>No. of RPC units</td>
<td>28,800 (107,266m²)</td>
<td>320 (1,192m²) (90:1)</td>
<td>20 (74.5m²) (1440:1)</td>
</tr>
<tr>
<td>No. of readout strips</td>
<td>3,686,400</td>
<td>40,960 (90:1)</td>
<td>2,560 (1440:1)</td>
</tr>
</tbody>
</table>
Functions of ICAL electronics

- Signal pickup and analog front-end
- Strip hit latch
- Pulse shapers, timing units
- Background noise rate monitor
- Digital front-end and calibration
- Data network architecture
- Multilevel trigger system
- Backend data concentrators
- Event building, data storage systems
- On-line data quality monitors
- Slow control and monitoring
  - Gas system, magnet, power supplies
  - Ambient parameters
  - Safety and interlocks
- Remote access to detector and data

Particles produced in the neutrino interactions pass through alternating layers of iron plates and RPCs, leaving tracks in the latter. Tracks bend as per the charge of the produced particles, due to the ICAL’s magnetic field.
Sub-systems of ICAL electronics

- Analog Front-ends
- TDC ASIC
- Digital Front-Ends
- Trigger System
- Global services, calibration and synchronisation units
- Data network and backend hardware
- Backend DAQ software
- Low voltage system
- High Voltage module
- Electronics integration
Outline of an RPC detector

Detector size: 1,950mm × 1,910mm × 24mm
Pickup strips: 128 (64 each of X- & Y-planes)
Analog Front-End boards with Anusparsh ASICs

ASICs designed using 0.35µm SiGe BiCMOS process and packaged in QFN-48.

Combined mask set for Amp and Disc ASICs. 15 wafers in production for 16,600 amp and 8,300 disc ASICs.
Analog Front-End boards with NINO ASICs

Accepts inputs from 8 pickup strips of an SRPC.
8 differential drivers of unity gain.
One NINO chip with threshold control and other accessory circuits.
ICAL’s TDC ASIC

**Principle**
- Two fine TDCs to measure start/stop distance to clock edge (T1, T2)
- Coarse TDC to count the number of clocks between start and stop (T3)
- TDC output = T3+T1-T2

**Features and specifications**
- UMC 130nm technology, QFN64 package, 3.2mm×3.2mm in size
- Input clock: 10MHz (250MHz to DLL internally generated by PLL)
- 16 hit channels, 1 trigger and 1 calibration channel
- Four paired time stamps: leading edge 65.5µs (125ps), pulse width 64ns (250ps)
- Readout buffers: 91 locations
- 32-bit/hit, data on 4-and 11-line SPI bus.
- Self test features
DFE module – the workhorse

- Unshaped, digitized, LVDS RPC signals from 128 strips (64x + 64y)
- 16 analog RPC signals, each signal is a summed or multiplexed output of 8 RPC amplified signals.
- Global trigger
- TDC calibration signals
- TCP/IP connection to backend for command and data transfer.
Soft-core processor

FPGA (EP4CE115F780)

- Event data acquisition
- Monitoring data acquisition
- Command interface
- Remote system upgradation
- HV control and Monitoring
- Read/Write Hardware register access
- Flash memory Access
- TDC JTAG Access
- Wiznet Network Interface
DFE module

- Altera Cyclone 4
- HPTDC
- Wiznet 5300

Three boards
DFE with optical data interface

Xilinx Kintex-7 FPGA (XC7K160T-2FFG676I) and Aurora 64B66B IP core SFP module (AFBR-709SMZ), 10Gb Ethernet, 850 nm, 10GBASE-SR/SW
Test jig for DFE production QC
Calibration module
Performance of calibration module

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ICAL trigger scheme

- *In situ* trigger generation. Autonomous; shares data bus with readout system
- For ICAL, trigger system is based only on topology of the event; no other measurement data is used
- Huge bank of combinatorial circuits; Programmability is the game, FPGAs, ASICs are the players

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**Domino architecture**

- **RPC**
  - Level 0 Signals $T_{0L}$
  - Level 1 Signals $T_{1L}$
- **Segment**
  - Level 1 Signals $T_{1S_{1}}$-$T_{1S_{M}}$
  - Level 2 Signals $T_{2S_{MxN/P}}$
  - Level 3 Signal $T_{3S}$
- **Module**
  - Global Trigger Signal
Trigger criteria

Layer (N)

Multiplicity (M)

Group (P)

MxN/P

<table>
<thead>
<tr>
<th>Non-overlapped</th>
<th>Overlapped</th>
</tr>
</thead>
<tbody>
<tr>
<td>RPC Strip Rate</td>
<td>Chance Rate for Full Trigger</td>
</tr>
<tr>
<td>250 Hz</td>
<td>71 Hz</td>
</tr>
<tr>
<td>50 Hz</td>
<td>0.023 Hz</td>
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</table>
Trigger system for e-ICAL

Global Trigger System - GTS

1. SIGNAL ROUTER BOARDs - SRB, 10 no's
2. TRIGGER LOGIC BOARD - 1F
3. TRIGGER LOGIC BOARD - 2F
4. TRIGGER LOGIC BOARD - 3F
5. TRIGGER LOGIC BOARD - 4F

Note:
- FT – Fold Trigger
- ST – Segment Trigger
- GT – Global Trigger

120 RPCs

Cam Board

Ethernet

Console

GCLK

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Signal Router Board (SRB)
Trigger Logic Board (TLB)
Global Trigger Logic Board (GTLB)
Control and Monitoring Board (CAM)
Overview of ICAL data LAN

ICAL RPCs constitute a massive LAN with 30K nodes!

All cumulative traffic in high performance region

<table>
<thead>
<tr>
<th>Basic Data Size per RPC (Front end)</th>
<th>Data Rate at backend</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>Event data (ICAL)</td>
<td></td>
</tr>
<tr>
<td>Without pulse profile</td>
<td>4384 bits</td>
</tr>
<tr>
<td>With pulse profile</td>
<td>29984 bits</td>
</tr>
<tr>
<td>Without Pulse Profile</td>
<td>42.8Kbps (assming 10Hz event rate)</td>
</tr>
<tr>
<td>With Pulse Profile</td>
<td>292.8Kbps</td>
</tr>
<tr>
<td>Event data (ICAL-EM)</td>
<td>4384 bits</td>
</tr>
<tr>
<td></td>
<td>---------</td>
</tr>
<tr>
<td></td>
<td>1600Mbps (assming 10KHz event rate)</td>
</tr>
<tr>
<td>Monitor data (10s)</td>
<td>688 bits</td>
</tr>
<tr>
<td></td>
<td>3200688 bits</td>
</tr>
<tr>
<td></td>
<td>69 bps</td>
</tr>
<tr>
<td></td>
<td>312.6Kbps</td>
</tr>
</tbody>
</table>
Back-end data concentrator hardware

- Linux+Boost libs, Multi-threaded, lock-free
- No floating point operations, no disk i/o
- Estimate: 5 of DataConc servers each with 12 CPU cores will suffice one ICAL module
Back-end DAQ software

- Receives raw event (RPC) data that is pushed to it by the Data Concentrator.
- Combines raw data from various RPC’s into a single chunk of “event data” based on Event Number.
- Writes into ROOT format files into short term high speed RAID based storage.

Data recording, DQMs, Visualization and Control
Design scheme is complete. Prototyping is in progress.

<table>
<thead>
<tr>
<th>LVPS: Low Voltage Power Supply</th>
<th>RPC: Resistive Plate Chamber</th>
</tr>
</thead>
<tbody>
<tr>
<td>LVD: Low Voltage Distributor</td>
<td>AFE: Analog Front-End</td>
</tr>
<tr>
<td>DP: Distribution Panel</td>
<td>DFE: Digital Front-End</td>
</tr>
<tr>
<td></td>
<td>HV: High Voltage</td>
</tr>
</tbody>
</table>

Cables:- Each Cable will deliver power to four RPCs.
Cable Specification:-
DFE: 2 wires, +V and ground.
AFE: 12 wires; +V, -V and ground.
HV: 2 wires; +V and ground.
High voltage power supply

- Output voltage adjustable in the range ± 0-6KV (to generate 0-12KV) with output current up to 2µA.
- HV load regulation: better than 0.1% F.S
- Output ripple/noise voltage: within 200 mV (p-p).
- Adjustable HV Ramp rate 10-1000 Volts/sec, HV on/off control, HV output read back facility.
- HV load current read back facility with a resolution of 5 nA.
- Required LV Input supply: 12V @200mA
- Ambient fringe magnetic field: 500 gauss
Integration of electronics in RPC
Side views of the RPC tray
ICAL Prototype detectors

1m × 1m RPC stack in TIFR

2m × 2m RPC test stand in TIFR

2m × 2m RPC stack in Madurai

1m × 1m RPC stack in VECC

Operating 24×7 for many years
Some results from prototypes

\[ I_\theta = I_0 \cos^n \theta \]

\[ n = 2.15 \pm 0.01 \]

\[ I_0 = (6.217 \pm 0.005) \times 10^{-3} \text{ cm}^2 \text{ s}^{-1} \text{ str}^{-1} \]
Status and future outlook

- Design of baseline ICAL detector electronics completed, reviewed.
- Prototypes and limited quantities of various components and modules were produced, technologies and vendors identified.
- They are all tested, and are being used to read many ICAL prototype detectors, including the m-ICAL which is currently under construction.
- The project (ICAL) and the e-ICAL are delayed, hence large scale production of its electronics is put on hold.
- Meanwhile, revisions and upgrades – or even new architectures, of various components are being worked out.