Operational Experience with the ATLAS Pixel Detector

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Outline

• Introduction
  – Run 1 detector
  – Run 2 detector

• Operation and performance during Run 2
  – LHC operation in Run 2
  – Detector performance in Run 2

• Readout upgrades and radiation effects

• Conclusions and Future
The ATLAS Pixel Detector During Run 1

- **Sensor:**
  - n-on-n implants.
  - 1.64 cm x 6.08 cm x 250 μm.
  - 328 columns (50 μm pitch).
  - 144 rows (400 μm pitch).

- **Front-end chips:**
  - DSM 0.25 μm CMOS.
  - 16 front-end per sensor.
  - Analog block: Amplification and discrimination.
  - Digital: Readout, ToT computation.

- 3 cylindrical layers closed by two end-caps having three disks each.
- Layers at 50.5, 88.5 and 122.5 mm.
- Disks at ± 495, ± 580 and ± 650 mm.
- Layer names, from beam axis: B-Layer, Layer 1 and Layer 2.
- 80 millions channels, 1.7 m² of silicon.
- 1744 modules with 46080 readout channels each.
Pixel Upgrade at LHC First Long Shutdown (LS1 2013-2014)

- Increase of pile-up in Run 2: Need for more redundancy to reduce fake tracks for best tracking and b-tagging.
- Concern about module failures: Need to compensate failures and B-Layer degradation because of radiation damage and higher luminosity.
- Improve performance: Benefit from new technologies and go closer to the beam, allowing better resolution on impact parameters.
  
  **Insert a new innermost pixel layer (IBL)**

- Observed mortality of VCSEL in the backend (humidity) rose concern about the inaccessible VCSEL of the internal services: Displace the optoboards outside the tracker endplates, to make them accessible.
- Anticipating the increase of the bandwidth of Layer 1: Doubling the number of data fibers of Layer 1.
- 88 dead modules and 60 dead frontends at the end of Run 1 (5.3 %): Repare disconnections where possible.
  
  **Build and install new Service Panels (nSQP)**
3D Sensors
- p bulk
- $20.5 \times 18.8 \text{ mm}^2$, 1 FE-I4 chip
- 230 µm thick
- 50 µm × 250 µm pixels

Slim Edge Planar Sensor
- n-in-n, p-spray
- $41.3 \times 18.54 \text{ mm}^2$, 2 FE-I4 chips
- 200 µm thick
- 50 µm × 250 µm pixels

The IBL in a Nutshell

Stave cross section
- Carbon foam surrounded by carbon laminate
- Titanium cooling pipe ($CO_2$ evaporative cooling)
- Polyimide-Al-Cu flex for services
IBL Insertion and nSQP Integration
LHC and ATLAS Operation in Run 2

- LHC delivered more than 40 $fb^{-1}$ during 2015 and 2016, at a total energy of 13 TeV.

- The 4-layer Pixel Detector operated with a high “good-for-physics” fraction of 98.9 % in 2016.
Luminosity and Pile-up in Run 2

- During 2016, LHC routinely exceeded its forseen nominal performance ($10^{34} \text{cm}^{-2}\text{s}^{-1}$ and an average pile-up of 23).
- First level trigger (LVL1) and data acquisition maximum rate went to 85 kHz and 1 kHz respectively. Target for LVL1 is 100 kHz in 2017.
Reconstruction of an ATLAS Event With 17 Individual Collisions
The IBL Resolution

- IBL resolution measured by using the measurement difference between two IBL sensors in their phi-overlap region.
- In agreement with test beam measurements.
Efficiency of the B-Layer

- B-Layer efficiency for muons measured by the ratio $\frac{N_{\text{hits}}}{N_{\text{expected hits}}}$ and its slight degradation with absorbed fluence:
dE/dx Measurement in Run 2

• Resolution on dE/dx improved with IBL:
IBL Distorsions

- IBL stave distortion issue discovered during commissioning with cosmic rays in February 2015.
- It was found to be temperature dependent (10 µm/K).
- It was traced back to a CTE mismatch between the service flex and the stave structure, which bends the stave at operation temperature.
- Alignment performed for each run, to mitigate the effects on tracking, thanks to the achieved temperature stability (0.2 K rms).
Upgrades to Face Increasing Pile-up

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<tr>
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<th>Module Link Occupancy at 100kHz L1</th>
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<tbody>
<tr>
<td></td>
<td>μ</td>
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<tr>
<td>Maximum in 2016</td>
<td>40</td>
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<tr>
<td>Maximum in Run 2</td>
<td>60</td>
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<td>Maximum in Run 3</td>
<td>80</td>
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* Before upgrade

- **Layer 2**: IBL-like backend electronics installed and bandwidth doubled during 2015/2016 LHC stop.
- **Layer 1**: IBL-like backend electronics installed and bandwidth doubled during 2016/2017 LHC stop.
- **B-Layer and Disks**: IBL-like backend electronics to be installed in 2017/2018 LHC stop. For 2017, threshold increase for Disks is anticipated.
Radiation Effect on the Pixel Leakage Current

- Leakage current increases with absorbed fluence.
- Annealing periods are clearly visible.
Example: The Lorentz angle variation between commissioning with cosmic rays before Run 1 and before Run 2.

The low electric field region inside the bulk grows with absorbed fluence, leading to an increase of the Lorentz angle.

Fluence decreases with radius: The Lorentz angle of the B-Layer is higher in Run 2 than in Run 1, while the Lorentz angle of the two other layers is still compatible with it.

A simulation model is under construction and will provide soon a better data/MC agreement.
Conclusions and Future

• The 4-layer ATLAS Pixel Detector operates successfully during the LHC Run 2.
• IBL was subject to a few issues, all solved, without noticeable impact on the data quality nor on the ATLAS integrated luminosity.
• Readout upgrades to help in facing over-performance of LHC.

• A strategy is being discussed for the end of Run 2 (2017-2018) and Run 3 (2021-2023), to face luminosities of 2 and $3 \times 10^{34} \text{ } cm^{-2} s^{-1}$ respectively. Luminosity leveling is also considered with LHC and other experiments.
• Radiation effects are being watched and modelised, to be able to exploit the ultimate potential of the detector.

• The whole ATLAS tracker will be replaced by the new ITK tracker in 2024-2025, for data acquisition at the High Luminosity LHC, starting in 2026.