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Design of the Pixel Analog

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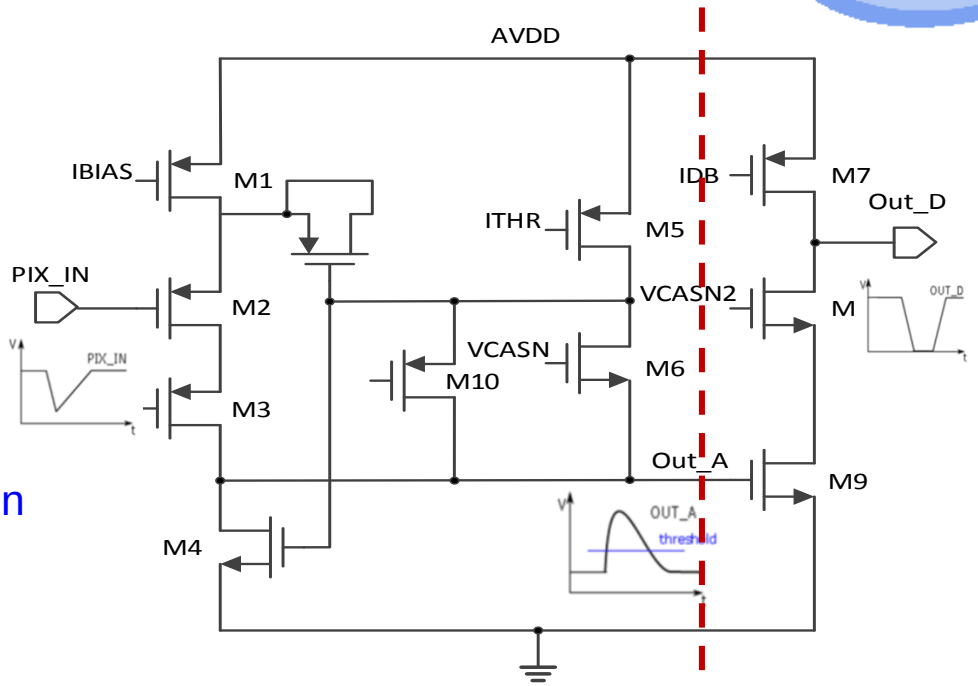
30 April 2019, Chip design review on CEPC Vertex Detector of MOST2 project

Schematic of Front-end

- **Operating principle derived from ALPIDE front end**

  D. Kim et al. DOI 10.1088/1748-0221/11/02/C02042

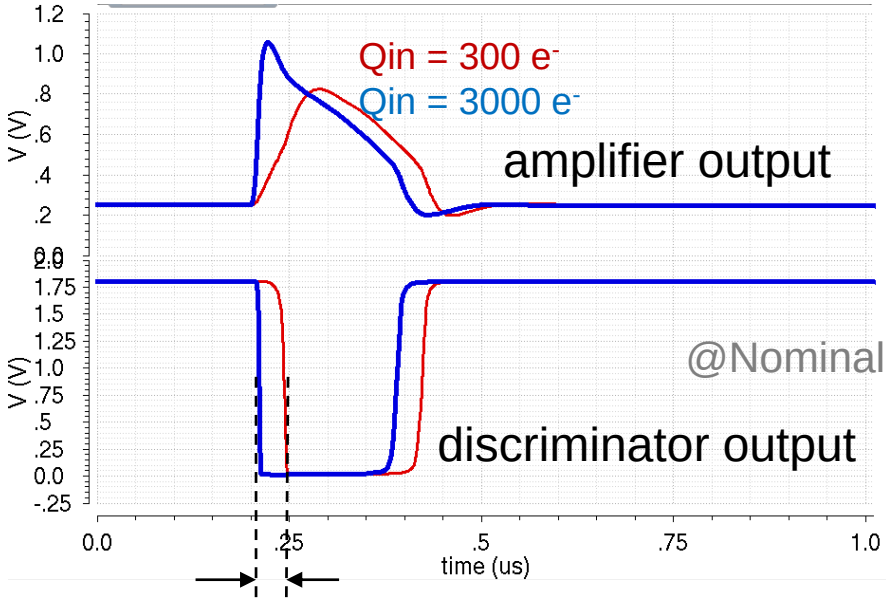
- **Modification for fast timing response**
  - at the cost of power consumption
- **Reduction on layout area**
- **Low threshold disp.**

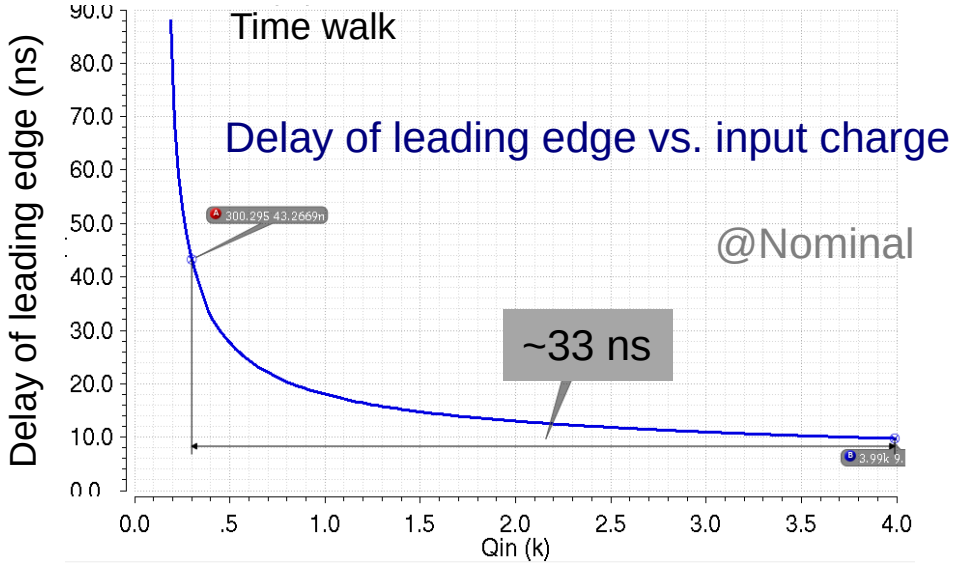


- M2 acts as a source follower to avoid loading the input
- M3 is a cascode transistor to increase the gain on the output node and eliminate the Miller effect for the input node.
- The analog output node is stabilized at low frequencies by active feedback on the transistor M4
- Efficient current usage for the input (the same branch current powers the source follower and the amplification stage)
- M10: clipping of the analog pulse

Front-end simulation result (1)

- **Transient simulation:**
  - Post simulation with parasitic RCC of the front-end
  - Analog power consumption 130 mW/cm^2
  - Duration time (discriminator output) < 200 ns
  - Time walk: time difference between time over threshold
    - ~33 ns @ 300e – 4 ke-

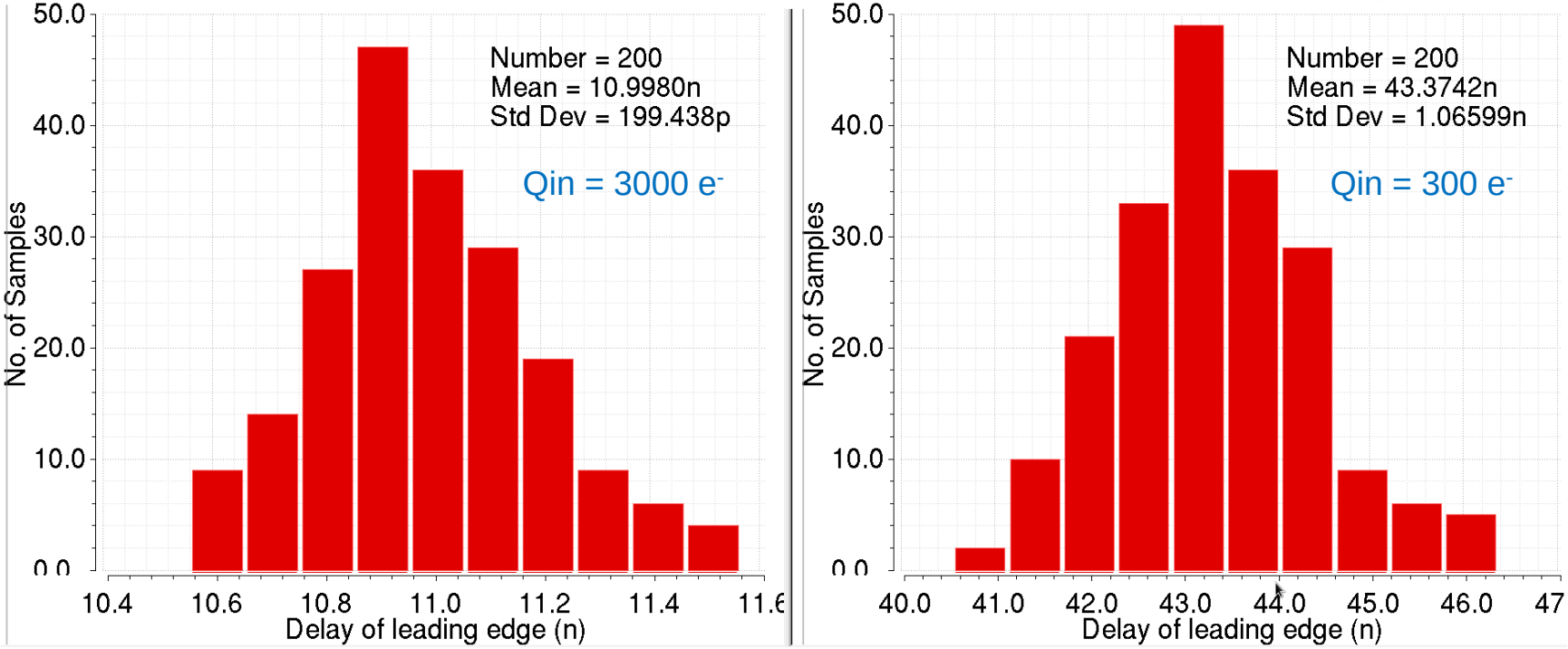




Front-end simulation result (2)

- **Time walk with Monte Carlo mismatch:**
  - Time walk: 32.4 ns ± 1.1 ns @ 300e – 3 ke-

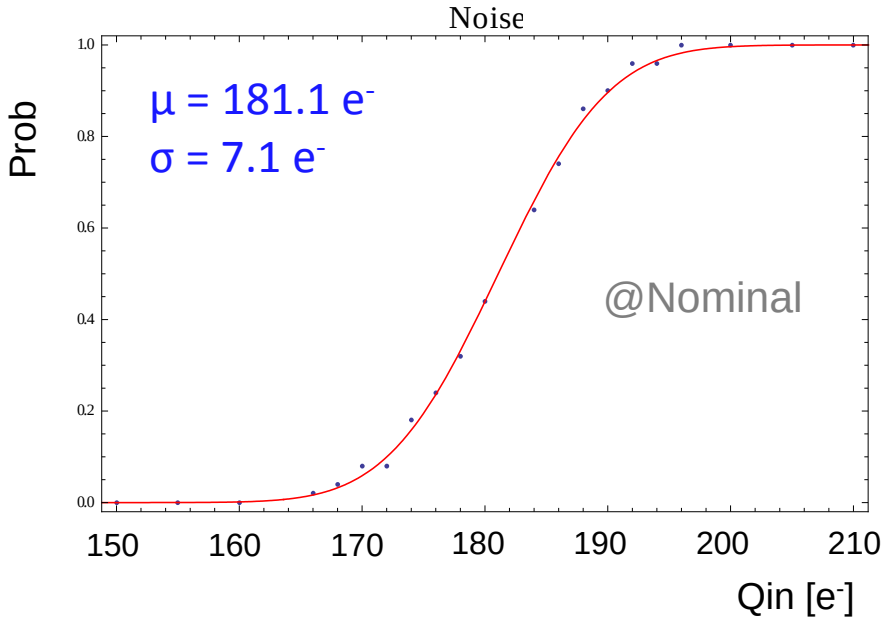
Delay of leading edge of input 300 e- & 3000 e-

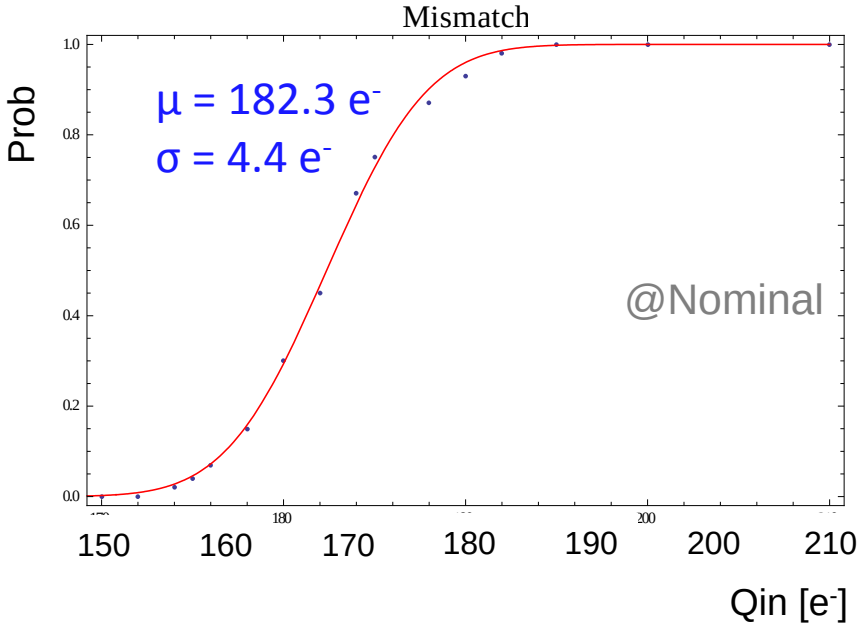


Front-end simulation result (3)

- **Equivalent noise charge and threshold dispersion:**
  - Transient noise simulation with different input charges, 50 runs for each input, record number of “hit” → “S curve”

  ➔ Charge threshold 181 e-, Equivalent noise charge: 7.1 e-
- **Threshold dispersion:**
  - Monte Carlo simulation (mismatch) with different input charges, 100 runs for each input ➔ threshold dispersion 4.4 e^-

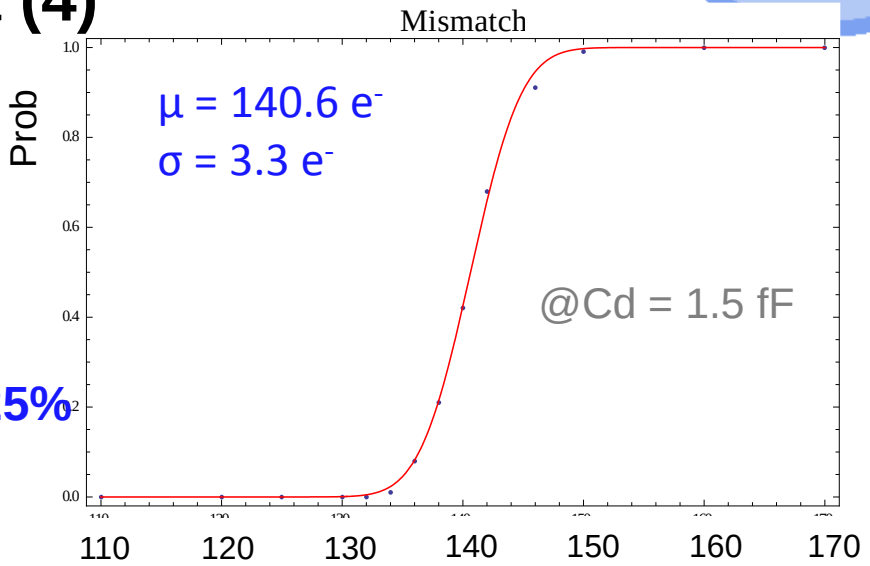


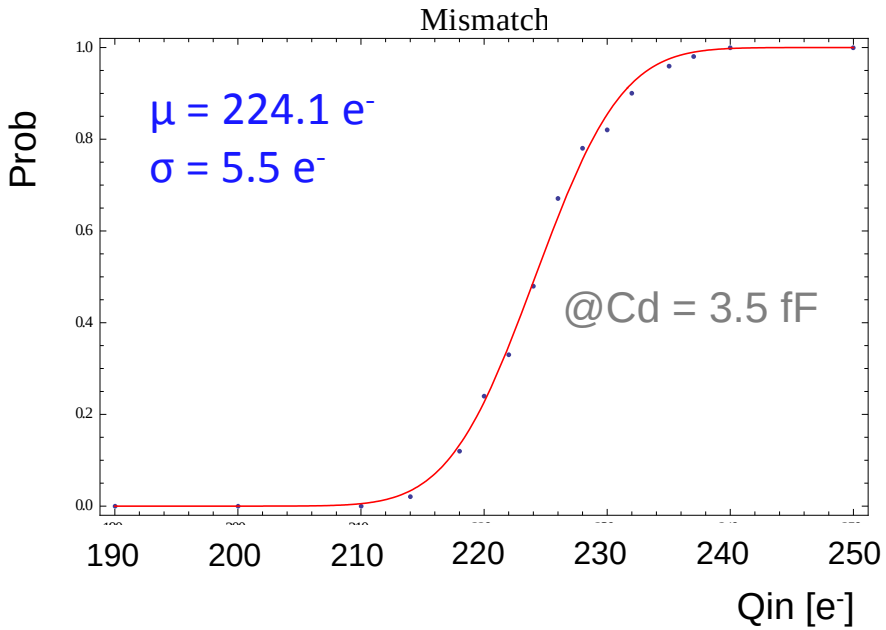


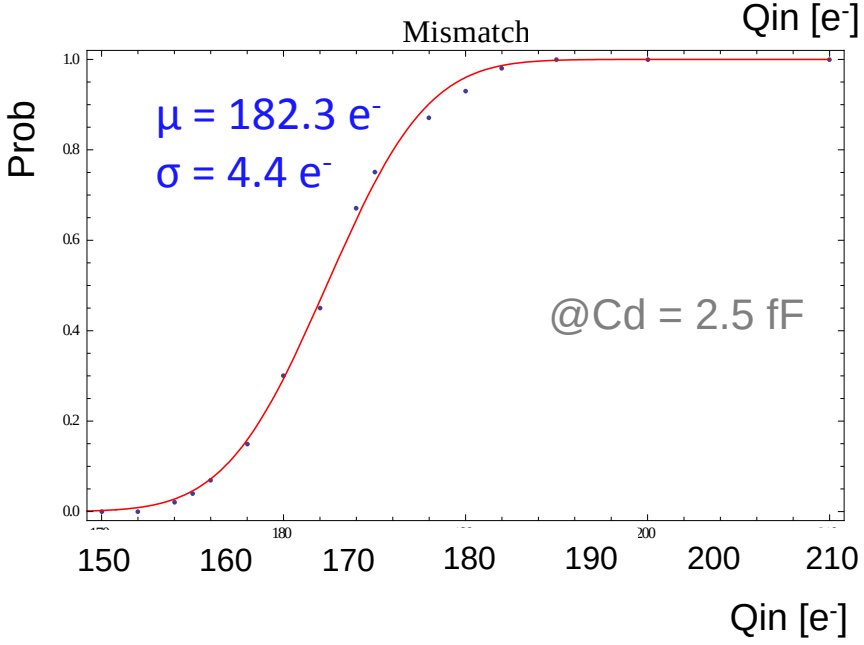
Front-end simulation result (4)

- **Threshold dispersion vs. Cd**
  - Cd: 1.5 fF, 2.5 fF, 3.5 fF
  - σ: 3.3 e-, 4.4 e-, 5.5 e-

Cd ± 40% ➔ threshold dispersion ± 25%





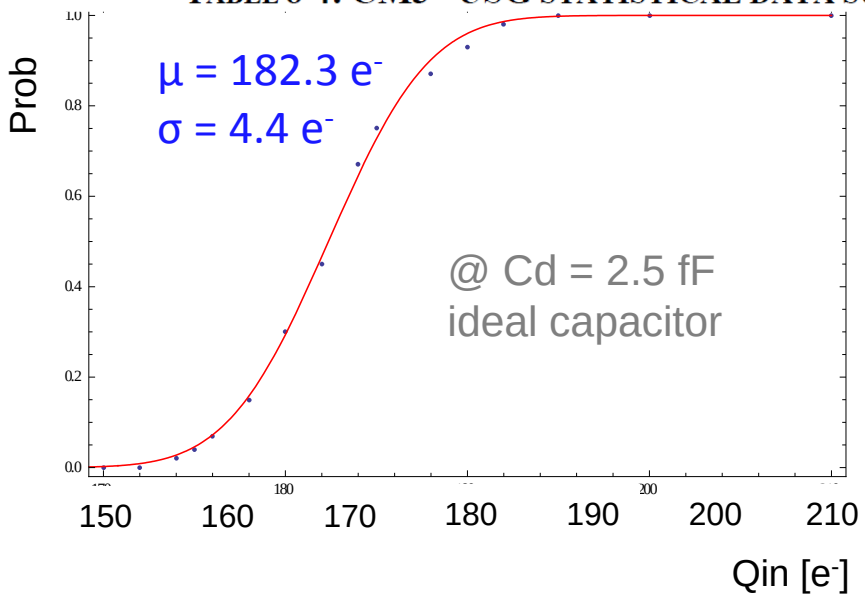


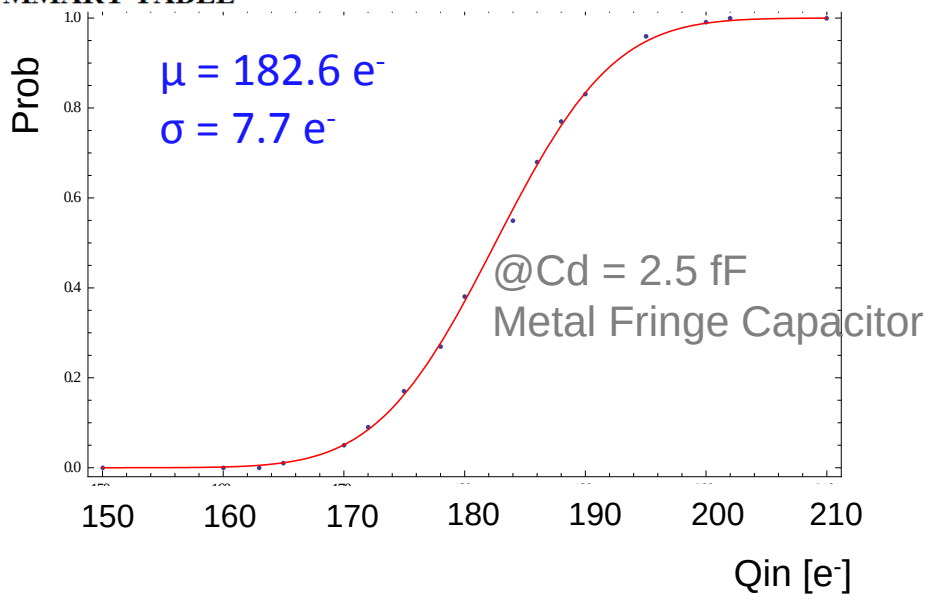
Front-end simulation result (4)

- **Effect of Cd dispersion on the threshold dispersion**
  - Cd: 2.5 fF with ideal capacitor or Metal Fringe Capacitor

Lot, Metal Combo, Type, Wafer, Sites	Min	Avg-3sigma	Avg	Avg+3sigma	Max	Range(%)
T406821.1, 4M1L, USG, W07, 7	0.547	0.534	0.566	0.598	0.579	5.63%
T406821.1, 4M1L, USG, W08, 7	0.547	0.534	0.564	0.593	0.577	5.23%
T406821.1, 4M1L, USG, W09, 7	0.550	0.538	0.569	0.600	0.581	5.39%
T406821.1, 4M1L, USG, W10, 7	0.549	0.536	0.569	0.601	0.582	5.76%
T406821.1, 4M1L, USG, W11, 7	0.551	0.537	0.571	0.604	0.585	5.91%
T406821.1, 4M1L, USG, W12, 7	0.554	0.542	0.571	0.599	0.584	5.23%

TABLE 8-4: CM3 –USG STATISTICAL DATA SUMMARY TABLE

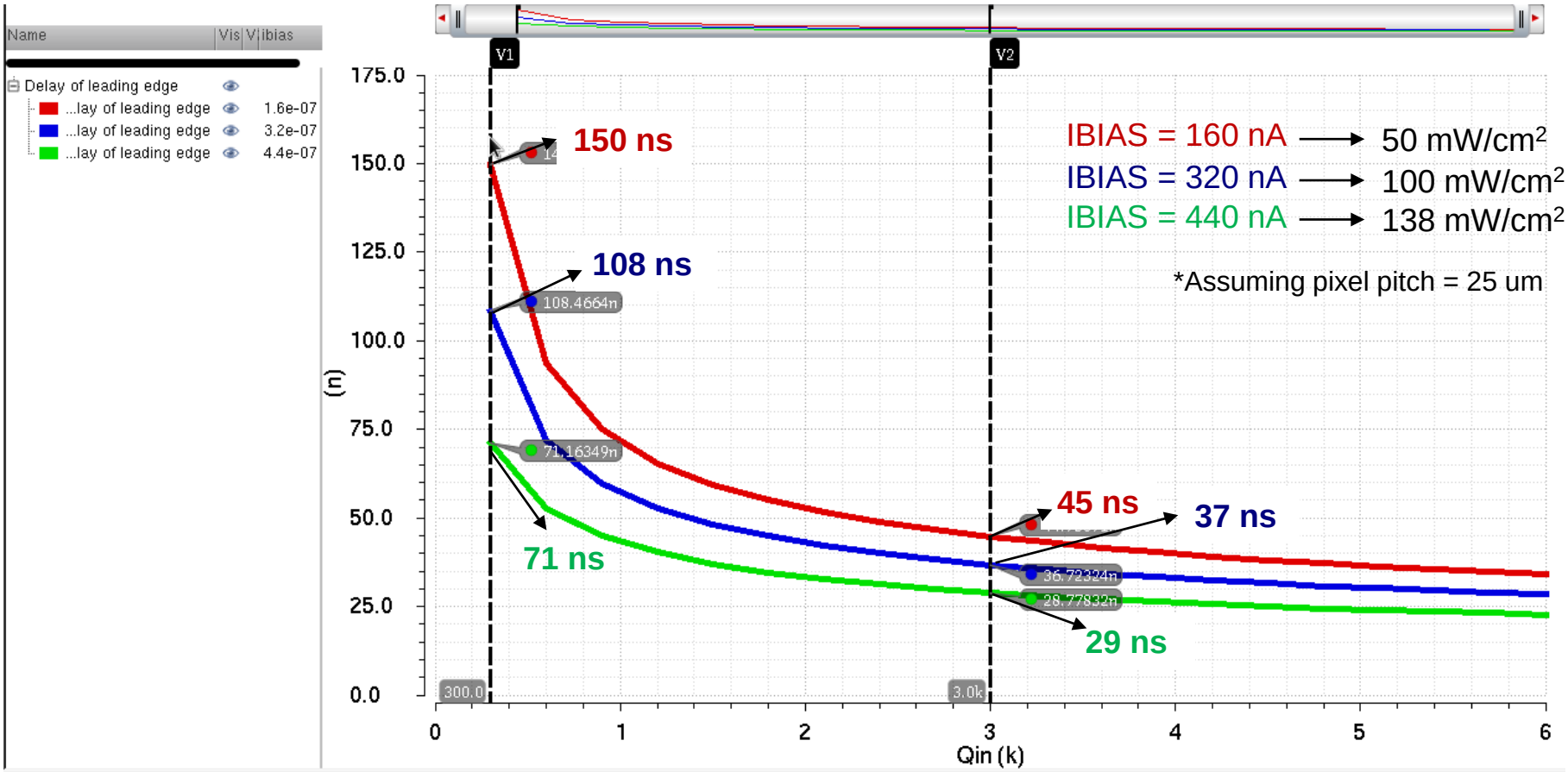




Thanks for your attention !

Time walk vs. power consumption

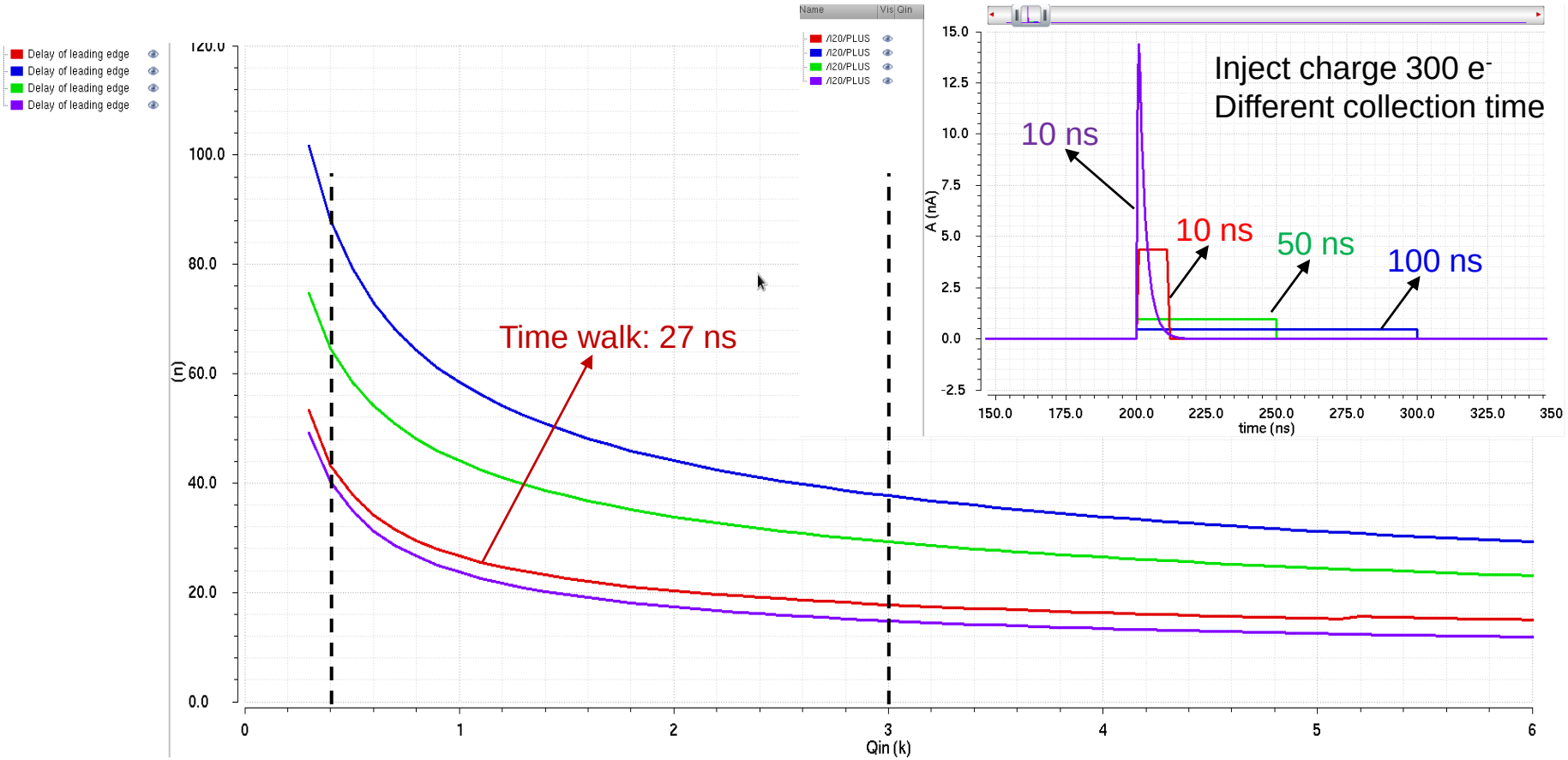
Delay of leading edge vs. input charge



Front-end simulation

Simulation condition: Cd = 2.5 fF, IBIAS = 440 nA

Delay of leading edge vs. input charge vs. charge collection time



Time walk increases with collection time