Status of the Full size pixel chip for high-rate CEPC Vertex Detector

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On behalf of the CEPC MOST2 Vertex detector design team

2019-5-31

Outline

- Motivation of the MOST2 Vertex detector design
- Specification
- Limitation of the existing CMOS sensors towards the high-rate CEPC Vertex Detector
- Key improvement for fast readout
- Design status & schedule
- Issues & concerns

CEPC Vertex Detector Design

Detector Requirements

- Efficient tagging of heavy quarks (b/c) and τ leptons

  $\longrightarrow$ impact parameter resolution

$$\sigma_{r\phi} = 5 \oplus \frac{10}{p(GeV)\sin^{3/2}\theta} \; (\mu m)$$

- Detector system requirements:
  - σ_{SP} near the IP: *<3 μm* $\longrightarrow$ ~16μm pixel pitch
  - material budget: *$\leq$ 0.15%X_0/layer* $\longrightarrow$ power consumption *< 50mW/cm^2*, if air cooling used
  - first layer located at a radius: *~1.6 cm*
  - pixel occupancy: *$\leq$ 1 %* $\longrightarrow$ ~ μs level readout

Target: fine pitch, low power, fast pixel sensor + light structure

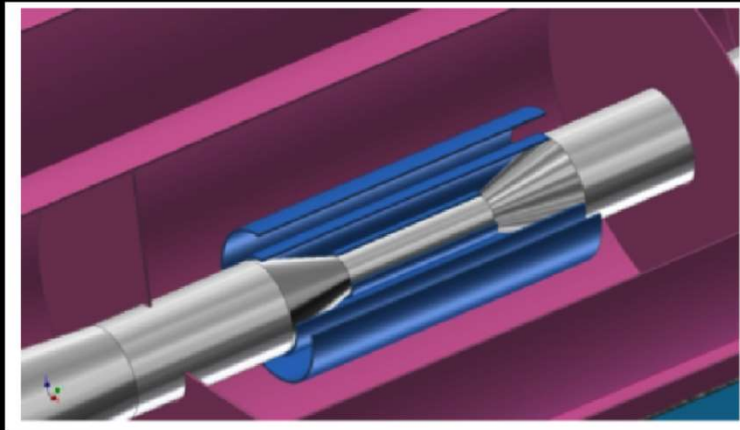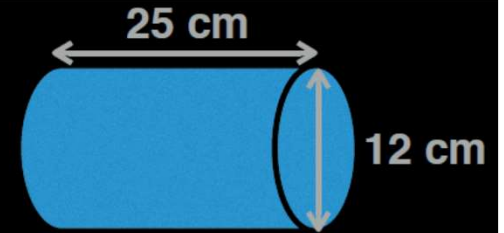Nov.7th, 2017   Status of CEPC vertex detector R&D in China   4

- Ref: Status of vertex detector, Q. Ouyang, International workshop on CEPC, Nov. 7th 2017

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Baseline Vertex Detector design

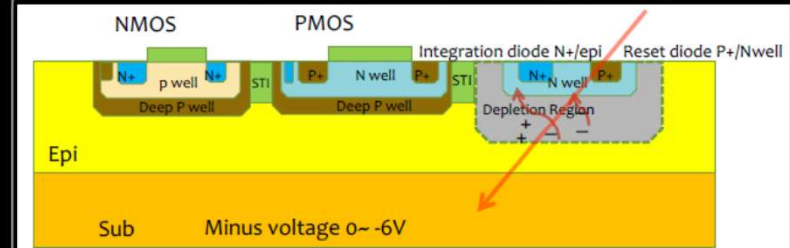## Baseline Pixel Detector Layout

3-layers of **double**-sided pixel sensors

25 cm

12 cm

- ILD-like layout
- Innermost layer: σ_{SP} = 2.8 μm
- Polar angle θ ~ 15 degrees

Implemented in GEANT4 simulation framework (MOKKA)

		$R(mm)$	$|z|(mm)$	$|cos\theta|$	$\sigma(\mu m)$	$Readout\ time(us)$
Ladder 1	Layer 1	16	62.5	0.97	2.8	20
	Layer 2	18	62.5	0.96	6	1-10
Ladder 2	Layer 3	37	125.0	0.96	4	20
	Layer 4	39	125.0	0.95	4	20
Ladder 3	Layer 5	58	125.0	0.91	4	20
	Layer 6	60	125.0	0.90	4	20

CMOS pixel sensor (MAPS)

NMOS   PMOS

Integration diode N+/epi   Reset diode P+/Nwell

N+   p well   N+   P+   N well   P+   N+   N well   P+

STI   Deep P well   STI   Deep P well   Depletion Region

Epi

Sub   Minus voltage 0~ -6V

Integrated sensor and readout electronics on the same silicon bulk with "standard" CMOS process:
- low material budget,
- low power consumption,
- low cost …

- **Ref: Introduction to the Pixel MOST2 Project, Joao Costa, 2018.6**

Ladder Prototype

Silicon Vertex Detector **Prototype** – MOST (2018–2023)

Sensor technology CMOS TowerJazz

- Design sensor with large area and high resolution
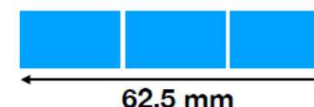- Integration of front-end electronic on sensor chip

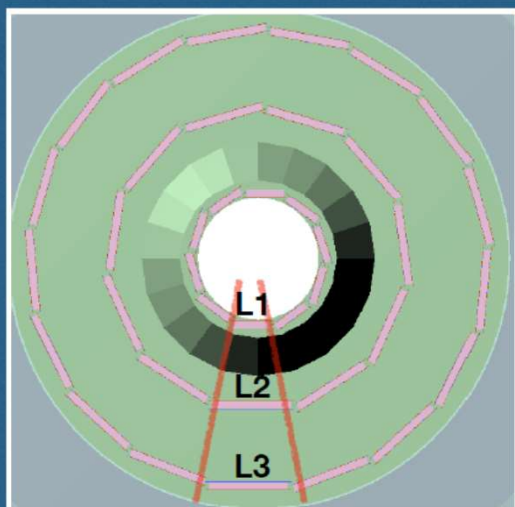Benefit from MOST 1 research program

Double sided ladder Layer 1 (11 mm x 62.5 mm)
Chip size: 11 mm X 20.8 mm

3 X 2 layer = 6 chips

62.5 mm

3-layer sector

L1
L2
L3

Baseline MOST2 goal:
3-layer prototype

Default layout requires different size ladders

Keep it simple for baseline design

L1
L2
L3

3-layers
same size
same chip

Goals:
1 MRad TID
3-5µm SP resolution

Integrate electronics readout

Design and produce light and rigid support structures

- **Ref: Introduction to the Pixel MOST2 Project, Joao Costa, 2018.6**
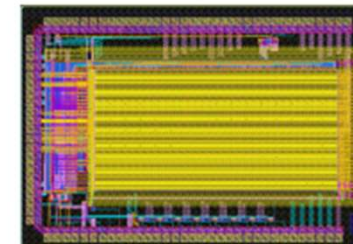
Previous CMOS pixel sensor prototypes

Prototype	Pixel pitch (µm²)	Collection diode bias (V)	In-pixel circuit	Matrix size	R/O architecture	Status
JadePix1	33 × 33 16 × 16	< 1.8	SF/amplifer	96 × 160 192 × 128	Rolling shutter	In measurement
JadePix2	22 × 22	< 10 V	amp., discriminator	128 × 64	Rolling shutter	In measurement
MIC4	25 × 25	reverse bias	amp., discriminator	112 × 96	Asynchronous	In measurement
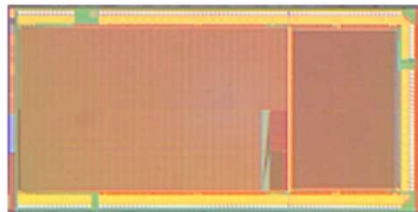
JadePix1 (IHEP)
3.9 × 7.9 mm²
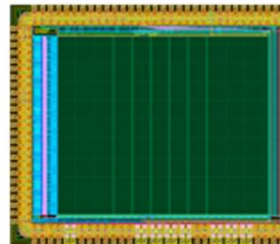
JadePix2 (IHEP)
3 × 3.3 mm²
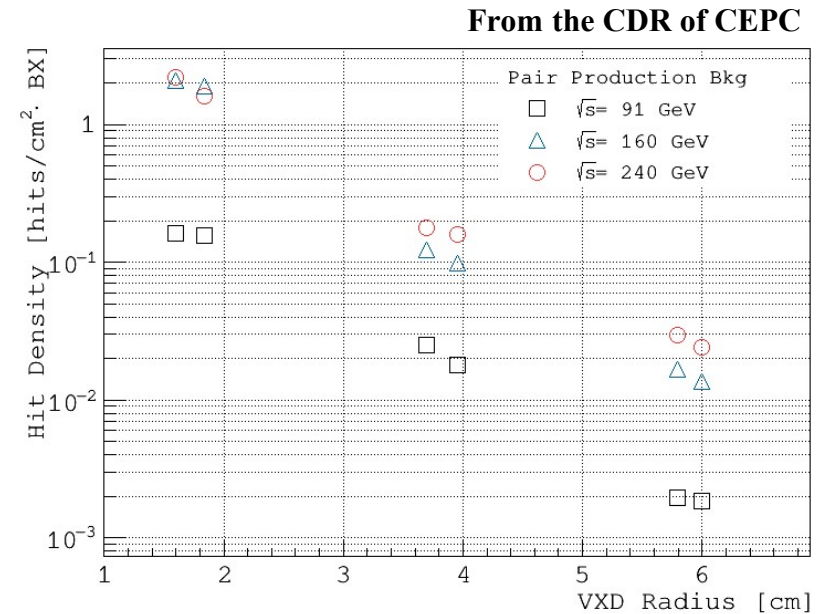
MIC4 (CCNU & IHEP)
3.2 × 3.7 mm²

All prototypes in TowerJazz 180 nm process

- **Slides from Y. Zhang: "IHEP CMOS pixel sensor activities for CEPC", 2018.3**
- **Y.P. Lu, "Pixel design and prototype characterization in China", The 2018 International Workshop on the High Energy Circular Electron Positron Collider**

Main specs of the full size chip for high rate vertex detector

- **Bunch spacing**
  - Higgs: 680ns; W: 210ns; **Z: 25ns**
  - Meaning 40M/s bunches (same as the ATLAS Vertex)

- **Hit density**
  - 2.5hits/bunch/cm^2 for Higgs/W; 0.2hits/bunch/cm^2 for Z

- **Cluster size: 3pixels/hit**
  - Epi- layer thickness：~18μm
  - Pixel size：25μm×25μm

From the CDR of CEPC

Pair Production Bkg
- □ $\sqrt{s}$ = 91 GeV
- △ $\sqrt{s}$ = 160 GeV
- ○ $\sqrt{s}$ = 240 GeV

Hit Density [hits/cm^2. BX] vs VXD Radius [cm]

| For Vertex	Specs	For High rate Vertex	Specs	For Ladder Prototype	Specs
Pixel pitch	<25μm	Hit rate	120MHz/chip	Pixel array	512row×1024col
TID	>1Mrad	Date rate	3.84Gbps --triggerless ~110Mbps --trigger	Power Density	< 200mW/cm^2 (air cooling)
		Dead time	<500ns --for 98% efficiency	Chip size	~1.4cm×2.56cm

Limitation of the existing CMOS sensors

- **None of the existing CMOS sensors can fully satisfy the requirement of high-rate CEPC Vertex Detector**

- **Two major constraints for the CMOS sensor**
  - Pixel size: should be < 25um* 25um, aiming for 16um*16um
  - Readout speed: bunch crossing @ 40MHz

- **TID is also a constraint, but 1Mrad is not so difficult**

	ALPIDE	ATLAS-MAPS (MONOPIX / MALTA)	MIMOSA	JadePix/ MIC4 (MOST1)
Pixel size	✔	X	✔	✔
Readout Speed	X	✔	X	X
TID	X (?)	✔	✔	To be tested

New proposed architecture for MOST2
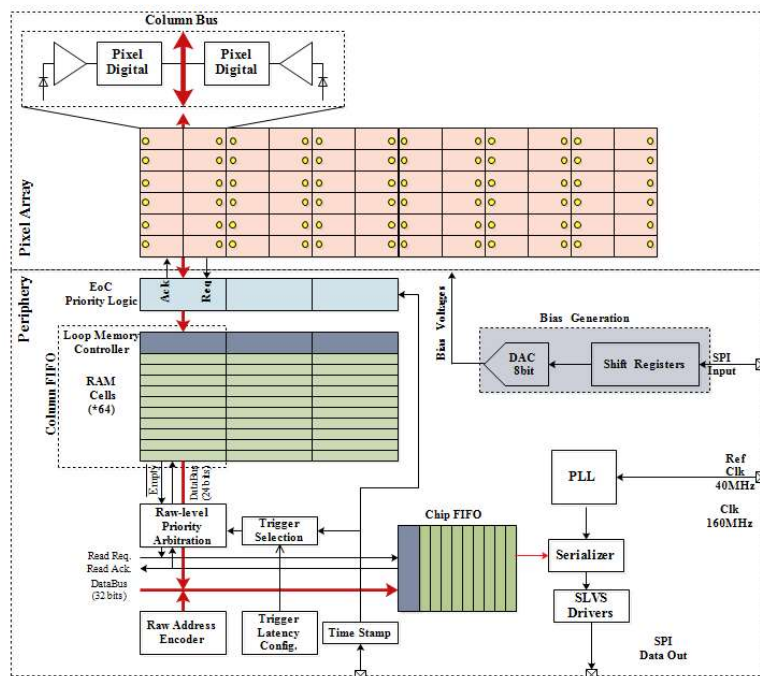
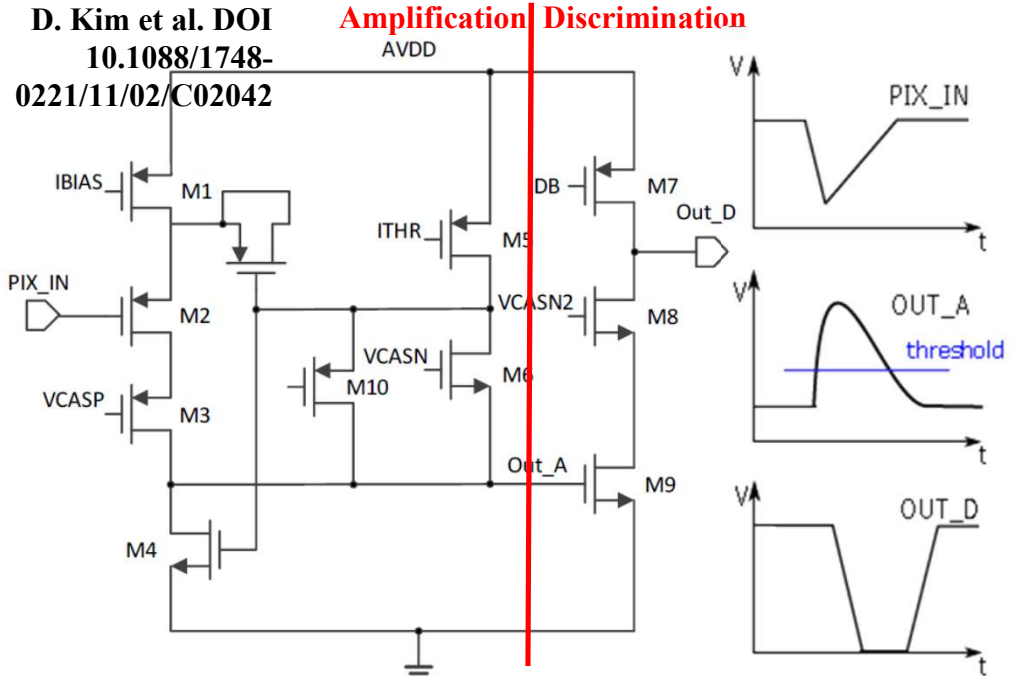From X.M. Wei for the CEPC Vertex MOST2 group meeting
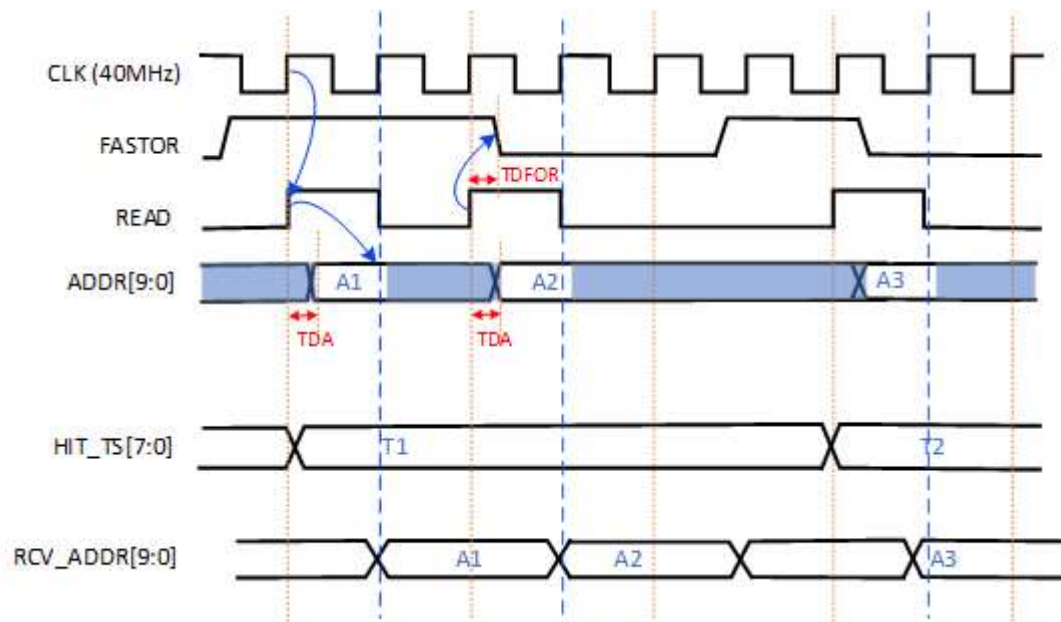
- **Similar to the ATLAS ITK readout architecture: "column-drain" readout**
  – Priority based data driven readout
  – Modification: time stamp is added at EOC whenever a new fast-or busy signal is received
  – Dead time: 2 clk for each pixel (50ns @40MHz clk), negligible compared to the average hit rate
- **2-level FIFO architecture**
  – L1 FIFO: In column level, to de-randomize the injecting charge
  – L2 FIFO: Chip level, to match the in/out data rate between the core and interface
- **Trigger readout**
  – Make the data rate in a reasonable range
  – Data coincidence by time stamp, only the matched event will be readout
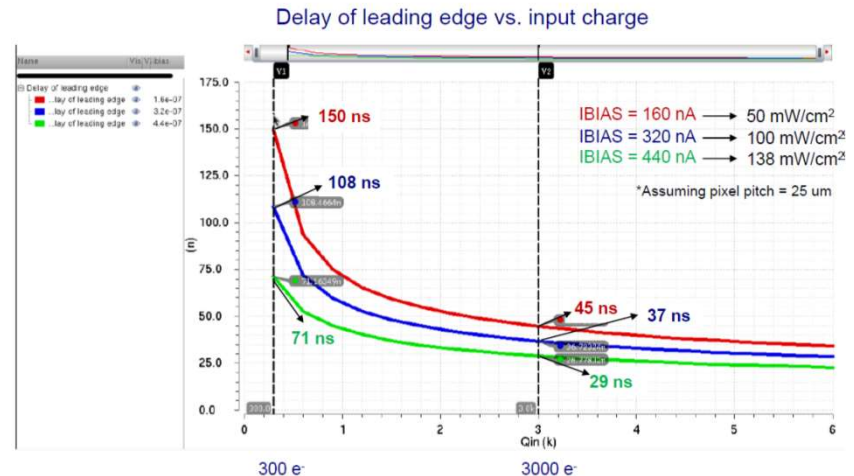
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Pixel architecture – Analog

Y. Zhang for the CEPC Vertex MOST2 group meeting

- **Digital-in-Pixel scheme: in pixel discrimination & register**

- **Pixel analog is derived from ALPIDE (and benefit from MIC4 for MOST1)**
  - **As most of ATLAS-MAPS sensors' scheme**

- **Biasing current has to be increased, for a peaking time of ~25ns**
  - **Now in MOST1 ~2us peaking time was designed, too slow for 40MHz BX**

- **Consequence:**
  - **Power dissipation increased**
  - **Modified TJ process for ATLAS has to be used**
    - ➢ **With faster charge collection time, otherwise only fast electronics is of no meaning**

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Pixel architecture – parallel digital schemes


P.Yang et al.
Nucl.Instrum.Meth.A785(2015)61
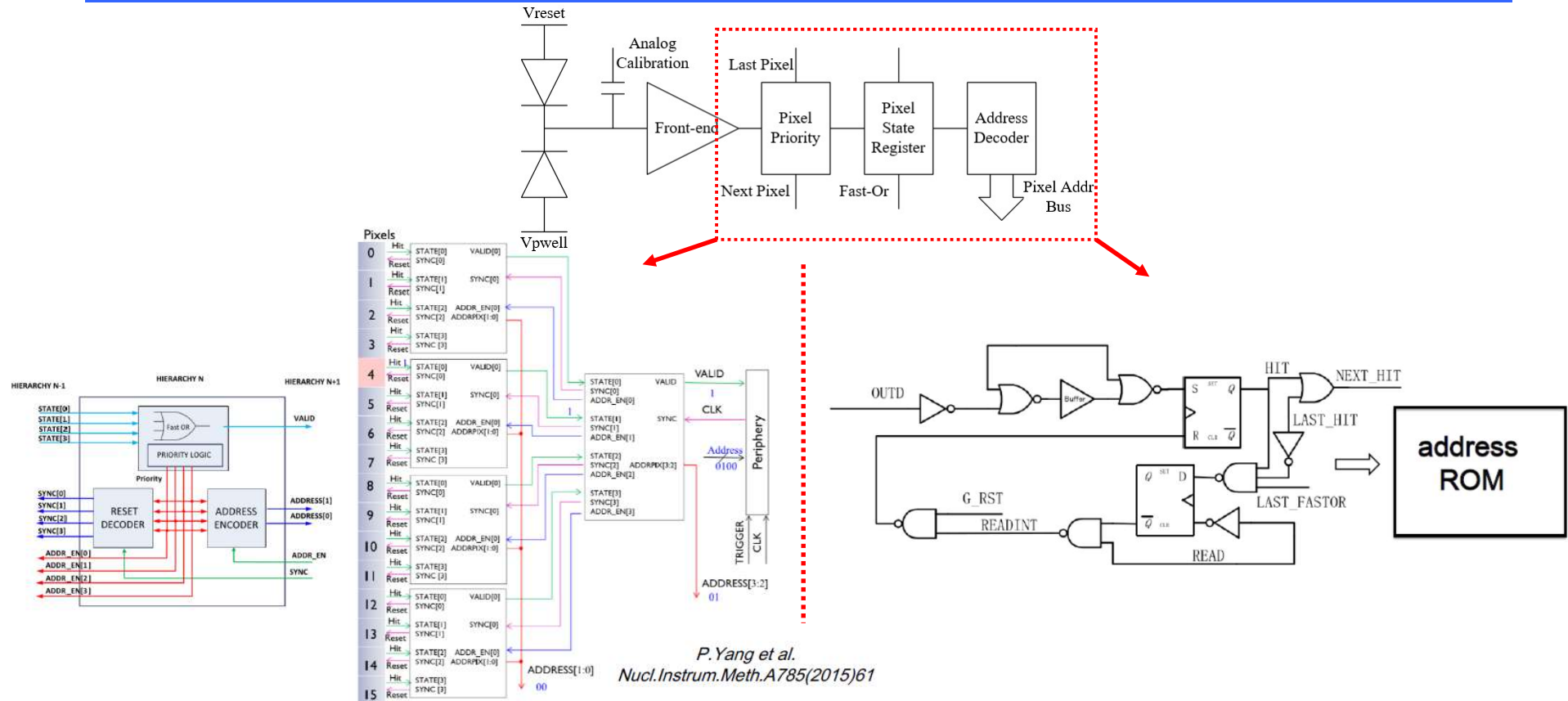
- **Two parallel digital readout architectures were designed:**
  - Scheme 1：ALPIDE-like: benefit from the proved digital readout in small pixel size
  - Scheme 2：FE-I3-like: benefit from the proved fast readout @40MHz BX (ATLAS)

Design effort aiming for 40MHz BX on digital

- ## ALPIDE-like scheme：
  - Fast-Or bus added to record the column hit time stamp
  - Boosting speed of the AERD (Address-Encoder & Reset-Decoder）
    - To shift the Fast-Or by a half of the clock cycle
      - More margin in the timing constraint of the periphery circuit
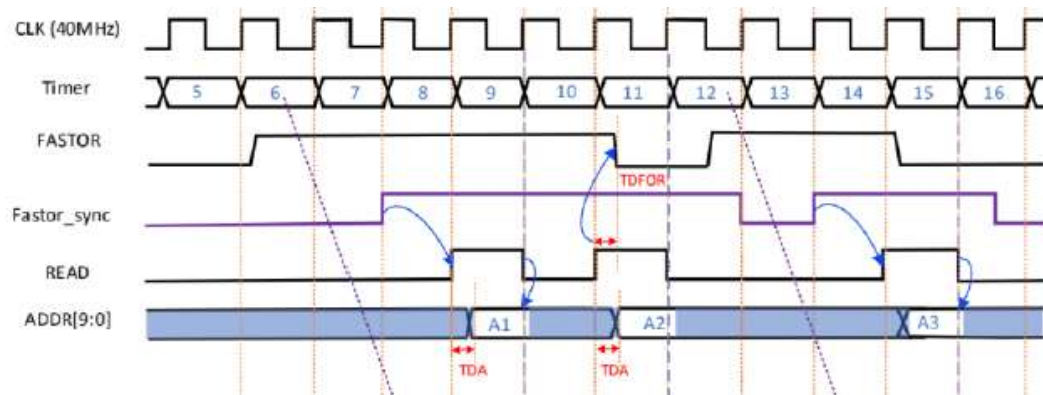
Normal AERD

SS ; 1.6V ; 50℃

Signal	Delay
FASTOR	14.3ns
READ	14.3ns
TDA	28ns
TDFOR	1.3ns

Boost AERD

SS ; 1.6V ; 50℃

Signal	Delay
FASTOR	14.3ns
READ	14.3ns
TDA	25.5ns
TDFOR	1.3ns

TY. Wu for the CEPC Vertex MOST2 group meeting

- ## FE-I3-like scheme：
  - Simplify the pixel cell logic
  - All the logic gates were re-designed with fully customized layout
    - For smaller pixel size

Full chip periphery logic design

From X.M. Wei for the CEPC Vertex MOST2 group meeting
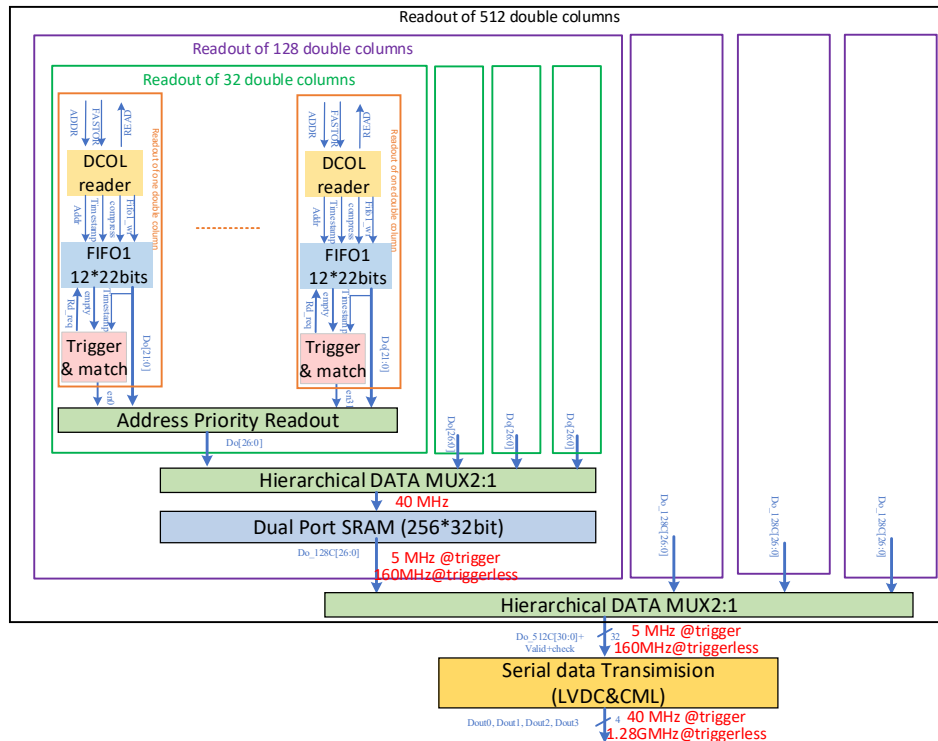
- ## Main Functionality:
  - ### Trigger/Triggerless readout mode compatible
    - ➢ **Data coincidence and trigger window logic**
  - ### Two level FIFOs for hit derandomization
  - ### High speed serialization for data readout
    - ➢ **4Gbps data rate capability**

- ## Other necessary blocks
  - ### Slow control of the pixel array and full chip via SPI interface
  - ### Bias generation by current- and voltage- DACs
  - ### Clock management: Phase Lock Loop and serializer
  - ### Power management: LDOs for on-chip low ripple power supply
  - ### High speed interface: CML & LVDS Drivers
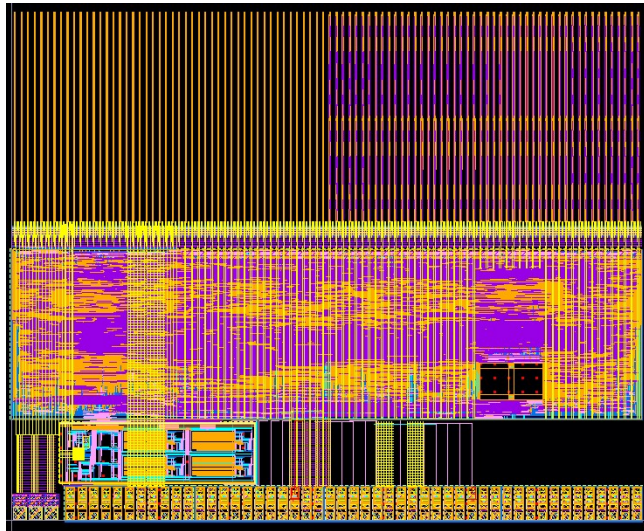
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Team organization

- **Design team:**
  - **IHEP, SDU, NWPU, IFAE & CCNU**
  - **Biweekly/weekly video design meeting on chip design (convened by IHEP)**

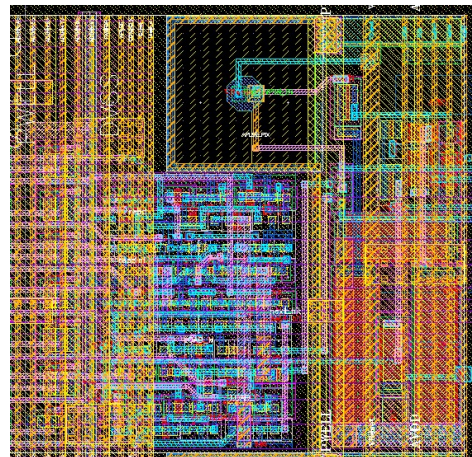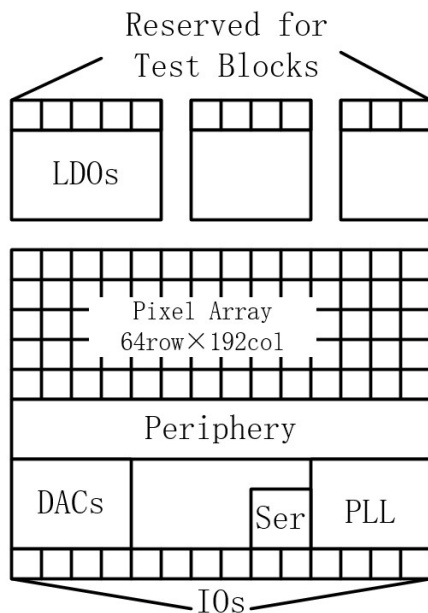| Institutes	Tasks	Designers
IHEP	Full chip modeling & simulation Pixel Analog, TCAD simulation High speed interface: PLL + Serializer	Wei Wei, Ying Zhang Xiaoting Li, Weiguo Lu, Mei Zhao
CCNU/IFAE	Pixel Digital	Tianya Wu, Raimon Casanova
NWPU	Periphery Logic, LDO	Xiaomin Wei, Jia Wang
SDU	Bias generation	Liang Zhang

- **Chip characterization**
  - **Test system development: SDU & + other interested parties**
  - **Electrical test: all designers supposed to be involved in the related module + other interested parties**
  - **Irradiation test: X-ray irradiator + beam line**

Current Status and recent schedule

Reserved for Test Blocks

LDOs

Pixel Array
64row×192col

Periphery

DACs   Ser   PLL

IOs

Chip size：5mm×5mm
Pixel size：25μm×25μm

- **Design Status**
  - **The design and layout of the first MPW1 is almost finished**
  - **Will be submitted in June**

- **An internal review for the chip design was organized on April 30**

- **First MPW tapeout**
  - **Shuttle booked for May 13th via IFAE**
    - ➢ **One block for 5mm×5mm**
  - **Organized with a full functional pixel array (small scale), plus other test blocks (less critical)**
    - ➢ **A 64×192 Pixel array + Periphery + PLL + Serializer**
    - ➢ **Bias generation included**
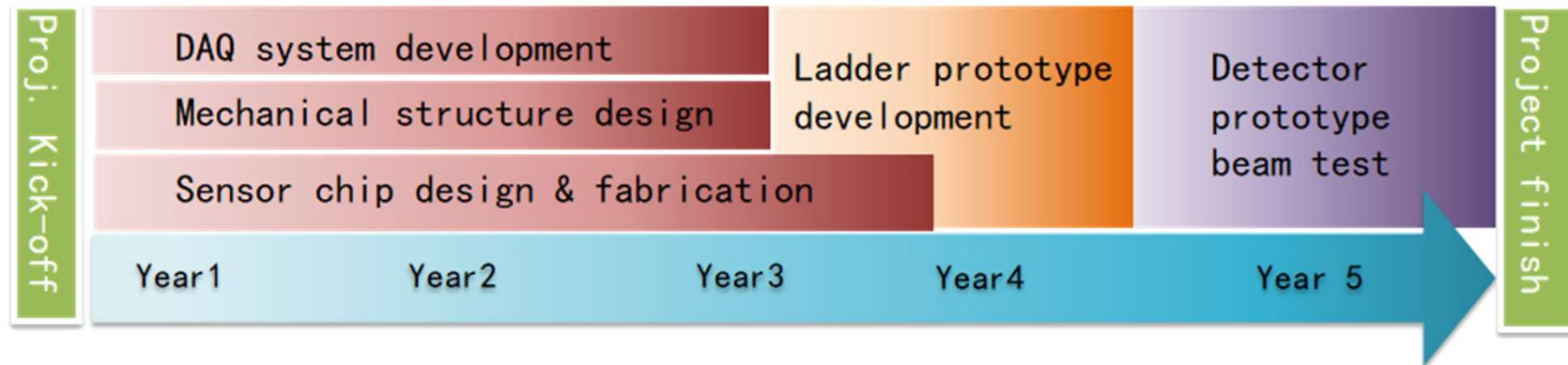   - ➢ **I/O arranged in one edge, as the final chip**

Chip design schedule

- **MOST2 project: May 2018 ~ April 2023 (5 years)**

- **Chip design plan (3 MPW & 1 engineering run in 3 years)**

  - **Year 1: complete the preliminary design of the main functional modules of the sensor chip, submit the 1st MPW prototype, complete the design of all the functional modules**

  - **Year 2: test the first prototype, integrate all the modules in a fully functionality chip, submit the 2nd MPW prototype, complete the 2nd prototype test**

  - **Year 3: solve the detected bugs and finish circuit modification & improvement, fabricate and test the 3rd MPW prototype, complete the full size chip design and tapeout (engineering run)**

- **Slides from Y. Zhang, Satellite meeting of MOST2 in Oxford, 2019.4**

- **Process Issues**
  - **Uncertainty of using Modified TJ process for fast timing**
    - ➢ Mod TJ is necessary for fast timing from sensor side, otherwise only a fast electronics is meaningless
    - ➢ Mod TJ is somewhat protected by CERN, even not available from Strasbourg IPHC
    - ➢ Recently saw some chance for availability from IFAE, still in contact
  - Non-stable schedule of MPW shuttle
    - ➢ Not easy to get access
      - No way to get access by ourselves from Chinese ICC agent
        - » Internal permission is required from TJ
      - Have to share the area & schedule with others (CERN, IPHC), if via IPHC as the past
        - » Then we cannot fully control the project schedule
    - ➢ Partially solved by the help of IFAE
      - as a regular customer under the name of IFAE
      - not sure about the stability of the tunnel
        - » still get impact from other big customers (maybe CERN), the shuttle in May was cancelled

Issues & concerns for the CMOS Sensor for CEPC

- **Concerns on the MOST2 project**
  - **Schedule is very tight**
    - ➤ **4.5 years to get a ladder, less than 3 years for a full size ASIC (Engineering run)**
      - 1 year had passed
  - **Project budget is limited for a second engineering run**
    - ➤ **Only 3 MPW and 1 engineering run was scheduled in budget**
  - **Not a best schedule but we have to:**
    - ➤ All blocks ready in 1st MPW → all functionality in 2nd → full size engineering run (and have to be successfully designed!!)
      - Every MPW should be mostly successful for the next
      - Some design have to go in parallel before the test results are achieved
    - ➤ Actually not enough time for the 3rd MPW
    - ➤ High risk and great challenge for ASIC design
      - Especially with challenging requirements from specs
      - Only 1 engineering run before the assembly is also very challenge, not the usual way as other ASICs
        - » One example is MIMOSA have > 30 versions
        - » One more engineering run from somewhere else may greatly help to get a reliable ladder

- **Few steps in advance may help for the future:**
  - To find a Chinese domestic foundry to begin a co-design CIS process
    - Reliable tunnel, regular MPW shuttle
      - Then fully controllable and speed-up-able R&D schedule
      - Especially in the current international circumstances
    - all parameters can be accessible
      - Can do precise and full TCAD simulation
      - Now all parameter are based on experience (and guess)
    - Process can be self-customized
  - CCNU is collaborating with GSMC(上海宏力）
    - We are not very involved, due to the limited man-power & budget
    - We have doubt on GSMC
    - We are trying to recover with (and aiming at) SMIC
  - Maybe good to try other design approaches
    - HVCMOS approach is also worth to try (and we have some early attempts)
    - But man-power is always a question…

Summary

- **Challenge considering the real CEPC's requirement**
  - Pixel size
  - High rate & power dissipation
  - None existing chip can fully satisfy the CEPC Vertex
- **New proposed architecture**
  - Modified column-drain readout with time stamp for each hit
  - Parallel verification with modified ALPIDE readout
  - Trigger/Triggerless mode compatible
- **Chip design for MOST2 Vertex detector is progressing almost as scheduled**
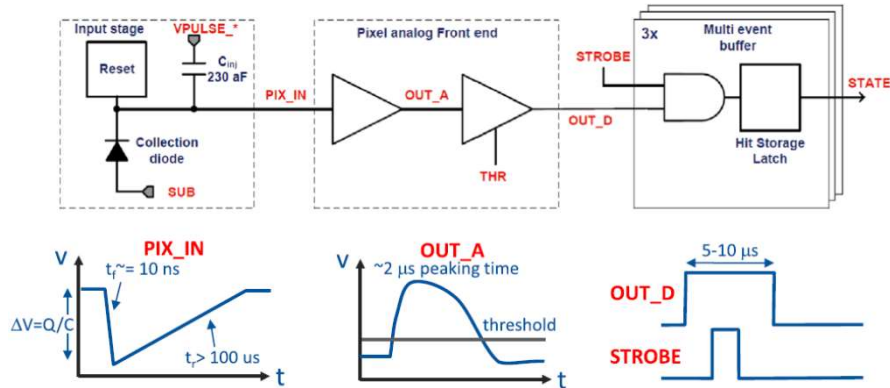 - First chip submission will be delivered very soon

Thank you !

Fig. 2. Block diagram of the ALPIDE pixel cell.

Table 1

General requirements for the pixel sensor chip for the Upgrade of the ALICE Inner Tracking System. In parentheses: ALPIDE performance figure where above requirements.

Parameter	Inner barrel	Outer barrel
Chip dimensions (mm × mm)	15×30	
Silicon thickness (μm)	50	100
Spatial resolution (μm)	5	10 (5)
Detection efficiency	>99%	
Fake hit probability (evt^{-1} pixel^{-1})	$<10^{-5}$ ($\ll 10^{-5}$)	
Integration time (μs)	<30(10)	
Power density (mW/cm^2)	$<300(\sim 35)$	$<100(\sim 20)$
TID radiation hardness[a] (krad)	2700	100
NIEL radiation hardness[a] (1 MeV n$_{eq}$/cm^2)	1.7×10^{13}	1×10^{12}
Readout rate, Pb–Pb interactions (kHz)	100	

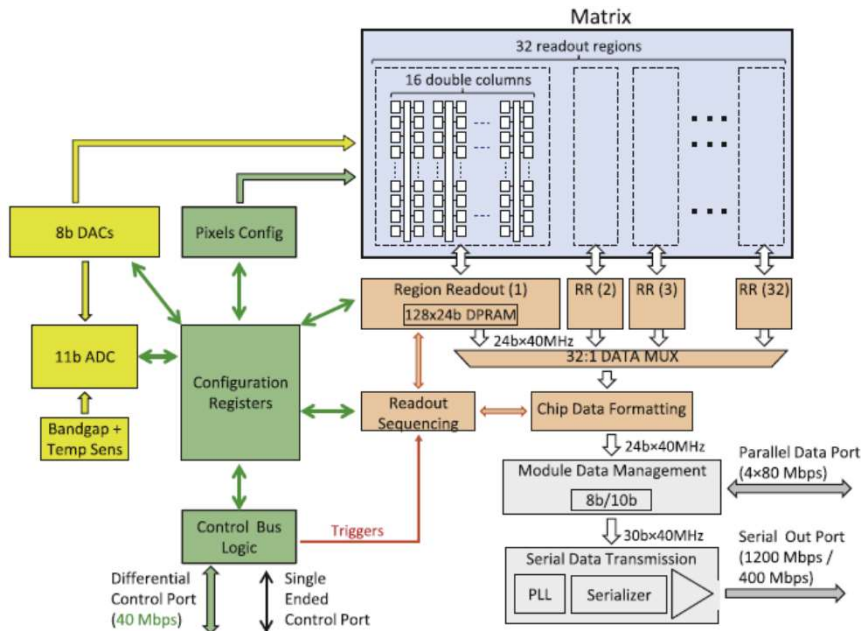[a] 10 × the radiation load integrated over the approved program (6 years of operation).

Fig. 3. Block diagram of the ALPIDE chip.

G. Aglieri Rinella et al. NIM. A 845 (2017) 583–587

- **The ALPIDE architecture, as MOST1 referenced, uses strobe signal as the "trigger"**
- **However, the readout rate is only ~100kHz, and more like frame readout**

Discussion on ALPIDE – analysis & conclusion

- **ALPIDE is not fully compatible with CEPC vertex & other high hit rate, high bunch crossing applications (like ATLAS)**

1. **Bunch crossing too high**
   - Now bunch crossing at 100~200kHz (i.g. frame rate)
   - While CEPC 1.5MHz (Higgs) ~ 40MHz(Z pole)
     - Not possible for the chip level frame-like readout, because:
       - At least 120MHz clk has to run at periphery-column level (3pixel per hit)
       - ALPIDE is "triggerless", no further data reduction, data rate too high (*32bits per hit)

2. **Pixel analog should be (much) faster**
   - now 2us peaking, 10us duration
   - CEPC: "Hit rate: 120MHz/chip, or 225Hz/pixel (average), 120kHz/col (ave)", Meaning every 8.3us, the column will be hit, however, very unlikely to be at the same pixel
   - For CEPC, peaking time should be much faster (25ns level)
     - Otherwise leads to too large delay for the arrival time stamp (although can be covered by the configurable trigger match error)
   - For CEPC, duration should also be faster
     - Better ends earlier than 8.3us, avoiding continuous hit in the same pixel
   - Larger power expected than ALPIDE

From vertex detector MOST1 projects towards MOST2

- **To build a prototype ladder** mounted with silicon pixel sensors
  - Spatial resolution 3-5 μm
  - TID 1 Mrad
- Compared with MOST1 project target:
  - **Pixel sensor prototype design**
  - Spatial resolution 3-5 μm
  - Power consumption <100 mW/cm2
  - Integration time 100 μs
- MOST1 focused on key performance, however we should focus more on **a full function chip** that can work in a prototype system
- Baseline design for MOST2:
  - Reuse the pixel design from MOST1, with necessary modification
  - Focus on full chip readout architecture design, esp. fast readout and full data readout chain

The full size chip for high rate vertex detector

- **Bunch spacing**
  - Higgs: 680ns; W: 210ns; **Z: 25ns**
  - Meaning 40M/s bunches (same as the ATLAS Vertex)

- **Hit density**
  - 2.5hits/bunch/cm^2 for Higgs/W; 0.2hits/bunch/cm^2 for Z

- **Cluster size: 3pixels/hit**

- The hit rate: Higgs 11 MHz/cm^2, W 36MHz/cm^2, Z 24 MHz/cm^2

- The chip should be capable with **36MHz/cm^2 hit rate**

- Suppose the pixel array size is 512rows*1024cols (ALPIDE), 25um*25um pixel size, and 1.28cm*2.56cm pixel array area

- **→ Hit rate: 120MHz/chip, or 225Hz/pixel (average), 120kHz/col (ave)**
  - Meaning every 8.3us, the column will be hit, however, very unlikely to be at the same pixel

- **In order to readout without data loss, time stamp has to be added for every hit**
  - According to the readout speed of MOST1(10~100us), it is not capable for this large hit rate
  - Also MOST1 chip design (MIC4) is currently base on ALPIDE readout architecture, which is still more or less frame-based, not fully capable with trigger readout
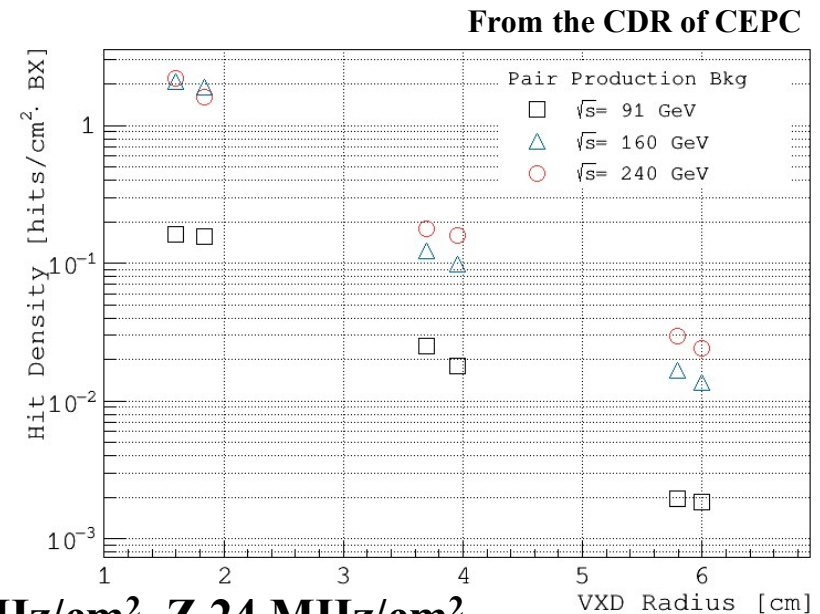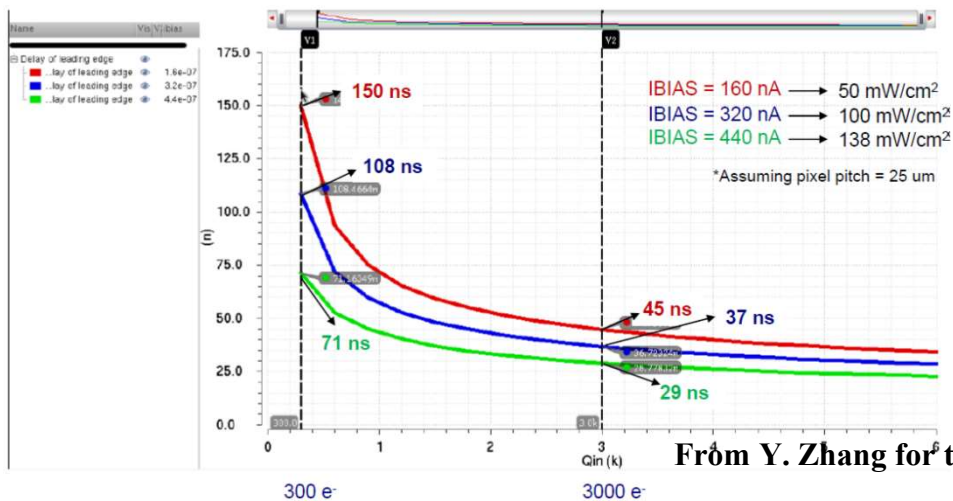
Increased data rate as for the real CEPC

- Every hit has 27~32bits (async): col addr 9bits (512), row addr 10bits (1024), time stamp ~8bits (suppose 40MHz clock, covers 6.4us time region)
- If triggerless, all the raw hit data should be sent off chip
  - **The data rate: ~32bits*120MHz= 3.84Gbps**, possible, but risk too high in the current stage
- If trigger, on-chip buffer should be designed
  - Suppose trigger latency 3us. Trigger rate was said 20kHz~50kHz
  - Triggered data rate:
    - 2.5/hits/bunch/cm^2*3pixels/hit*1.28cm*2.56cm*32bit=786bit/bunch/chip
    - W@20kHz trigger rate -> 15.7Mbps/chip as the triggered data rate
  - In order to cover any trigger error(mismatch of the edge in different column, time walk of the hit peaking…)
    - A trigger window can be set, so that the data within the $\pm\sigma$ of the trigger time stamp can all be read out
    - In this way, the readout data rate will be (suppose trigger window of $\pm$3LSB time stamp):
      - 15.7Mbps * 7 ~ 110Mbps
      - Can still be read out by a single LVDS interface

Other necessary modification for the pixel cell
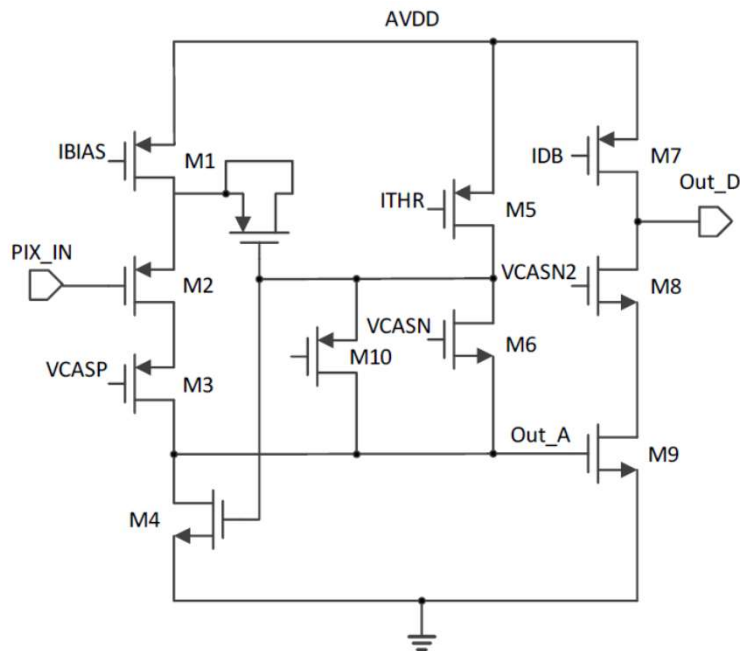
Simulation condition: Cd = 2.5 fF, Qin = 50 e⁻ – 6k e⁻, 3 different IBIAS

Delay of leading edge vs. input charge

IBIAS = 160 nA → 50 mW/cm²
IBIAS = 320 nA → 100 mW/cm²
IBIAS = 440 nA → 138 mW/cm²

*Assuming pixel pitch = 25 um

150 ns
108 ns
71 ns
45 ns 37 ns
29 ns

300 e⁻   3000 e⁻

- Pixel analog in the same architecture as ALPIDE (and benefit from MIC4 for MOST1) but with different parameters
  - Aiming especially for fast readout
- Biasing current has to be increased, in order to achieve a peaking time of ~25ns
  - Otherwise there will be timing error for the event, and has to open a trigger window in this case
  - Now in MOST1 ~2us peaking time was designed, which is too slow for 40MHz BX
- **Consequence:**
  - Power dissipation increased:
    - ➢ bias@440nA with peaking time 29ns, but 138mW/cm² for analog
    - ➢ Total power density may exceed 200mW/cm²
  - Modified TJ process for ATLAS has to be used
    - ➢ With faster charge collection time, otherwise only fast electronics is of no meaning

From Y. Zhang for the group meeting

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