

# Status of digital pixel

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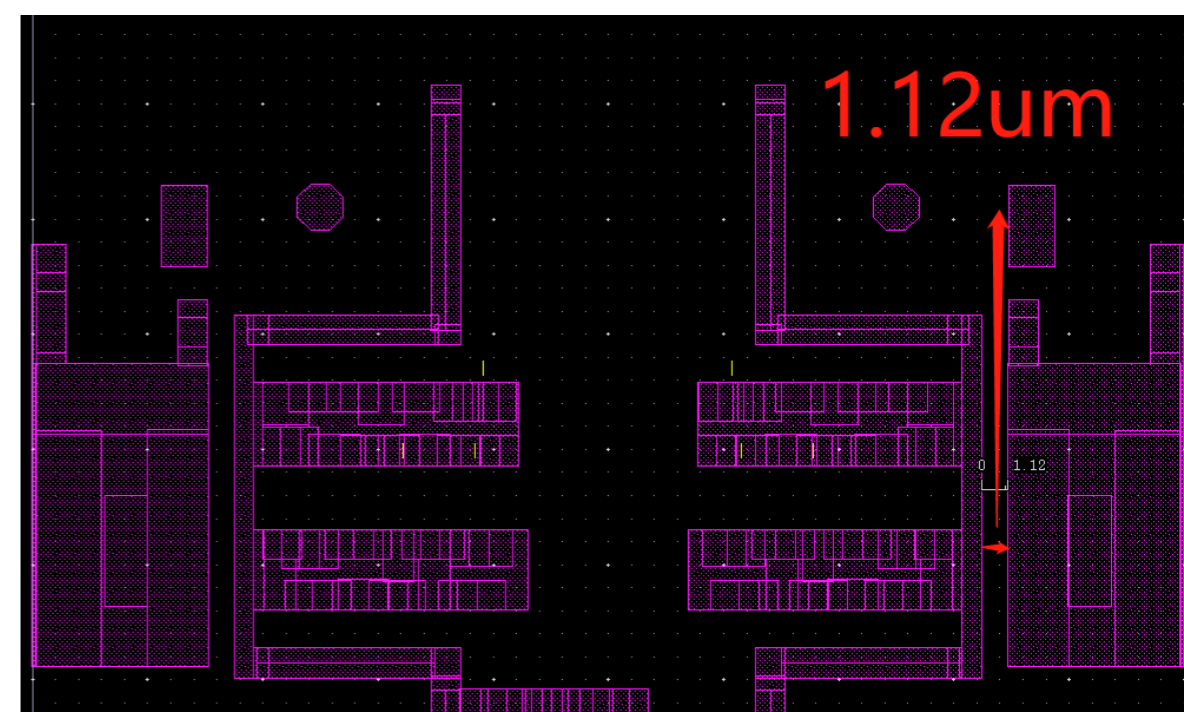
# The rules violation of Scheme 1 layout

WN.S.5	For Image sensor using Epi process only: Space between two WN's having different potential. DRC will check this rule if EPI flag is invoked in the run set	min	2.8
VNN.D.2	Distance from VNN (outside WN) to WN edge	min	1.66
VNN.N.1	VNN inside or cross over WN is not allowed (VNN interact WN is not allowed)		

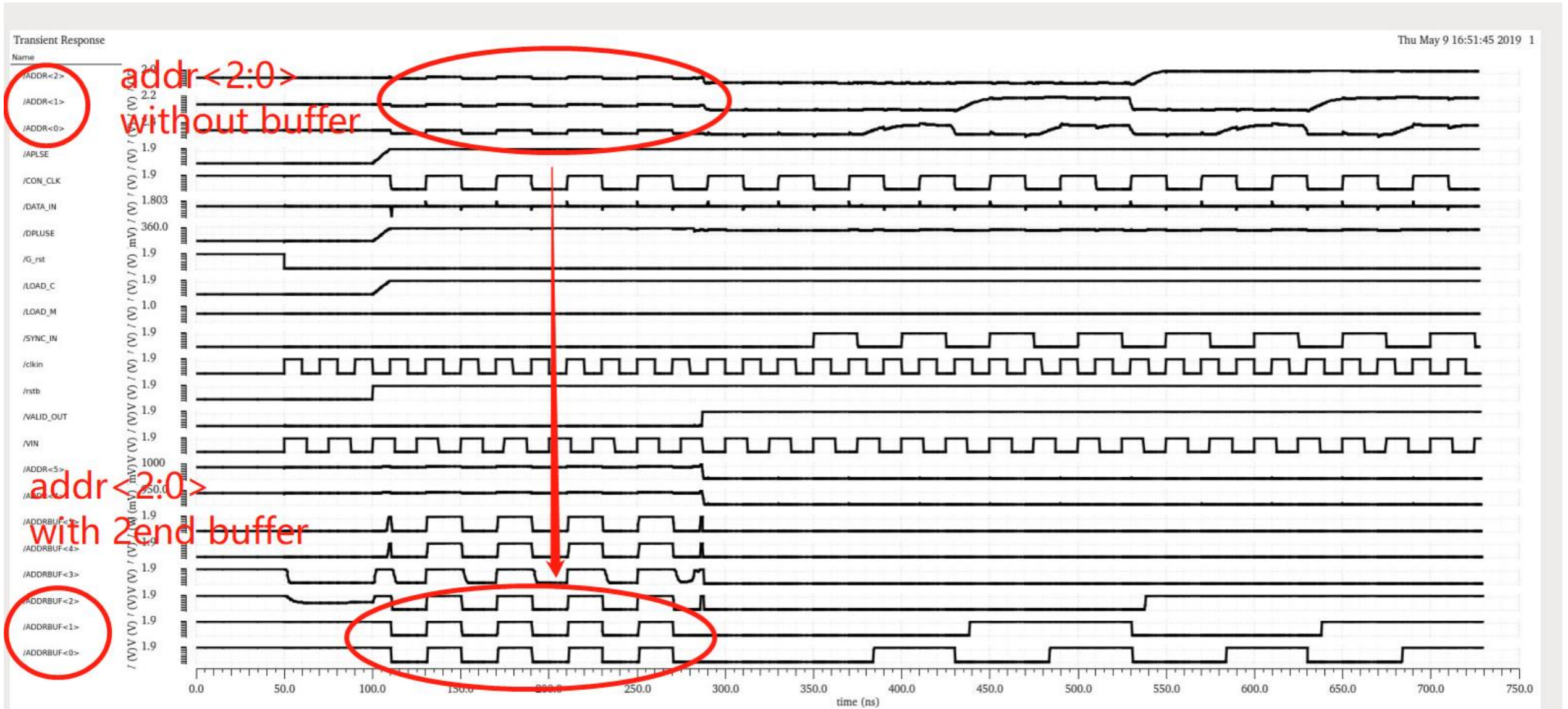


WN.S.1	Space between two WN's having the same potential. That is: 1.8V ~ 1.8V, 3.3V ~ 3.3V or 1.8V ~ 3.3V. Merge if space under this value	min	0.6
WN.S.3	Space between two WN's having different potentials. That is: 1.8V ~ 1.8V, 3.3V ~ 3.3V or 1.8V ~ 3.3V.	min	1.4

The WN space between the DVDD and AVDD, we use the rule WN.S.1, which minimum space is 0.6 um, our space is 1.12um but not reach to 1.4 um.

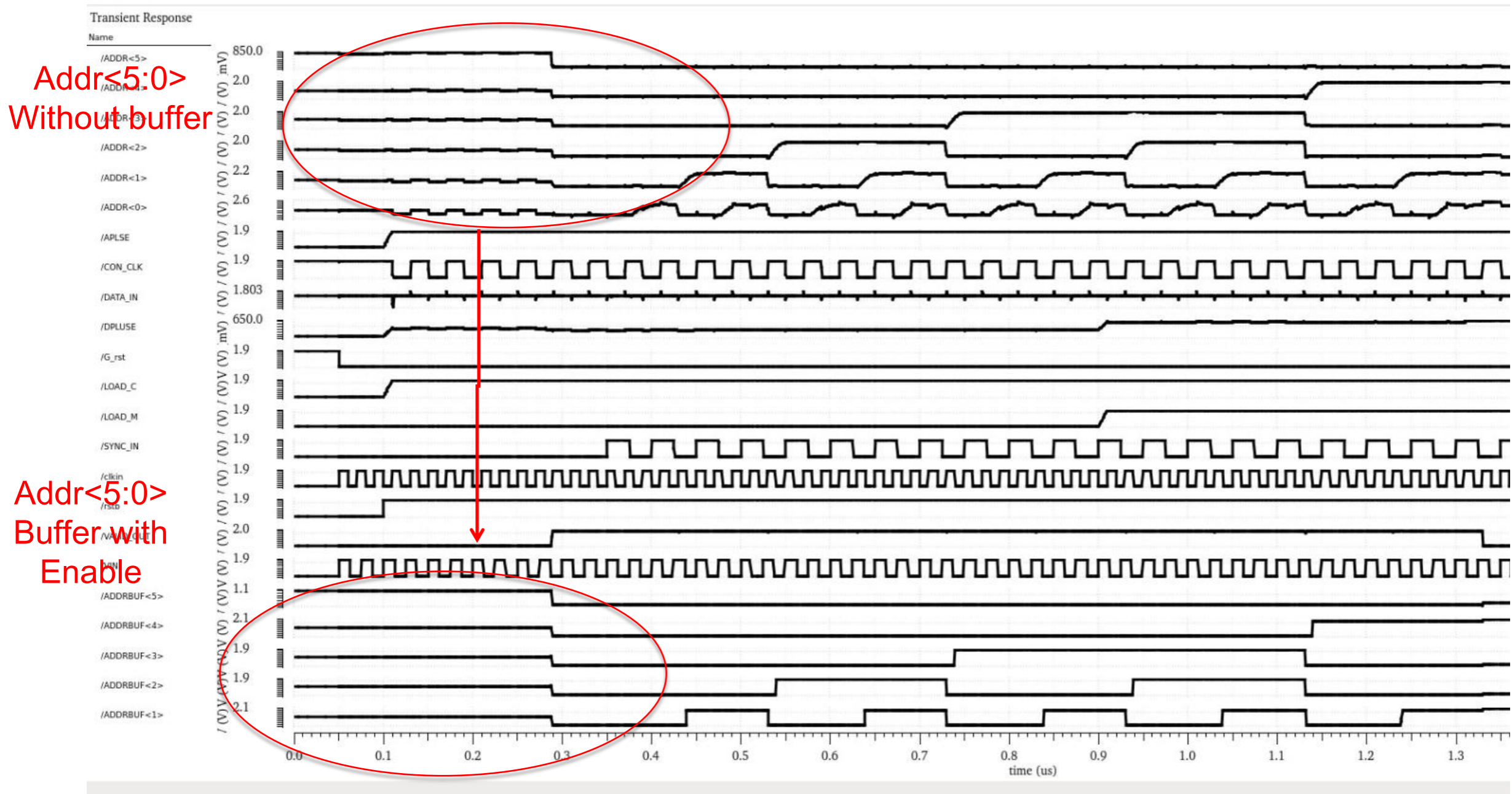


# The post simulation of 64 pixels



If we use the 2 end buffer , the ripple will be amplified. It will increase the power dissipation

# The post simulation of 64 pixels



If we use the 3 end buffer , the buffer will be enabled by the “ fastor”, then it works fine, but there still exist the high impedance.



Thanks for your attention.