CEPC Silicon Tracker R&D Discussion

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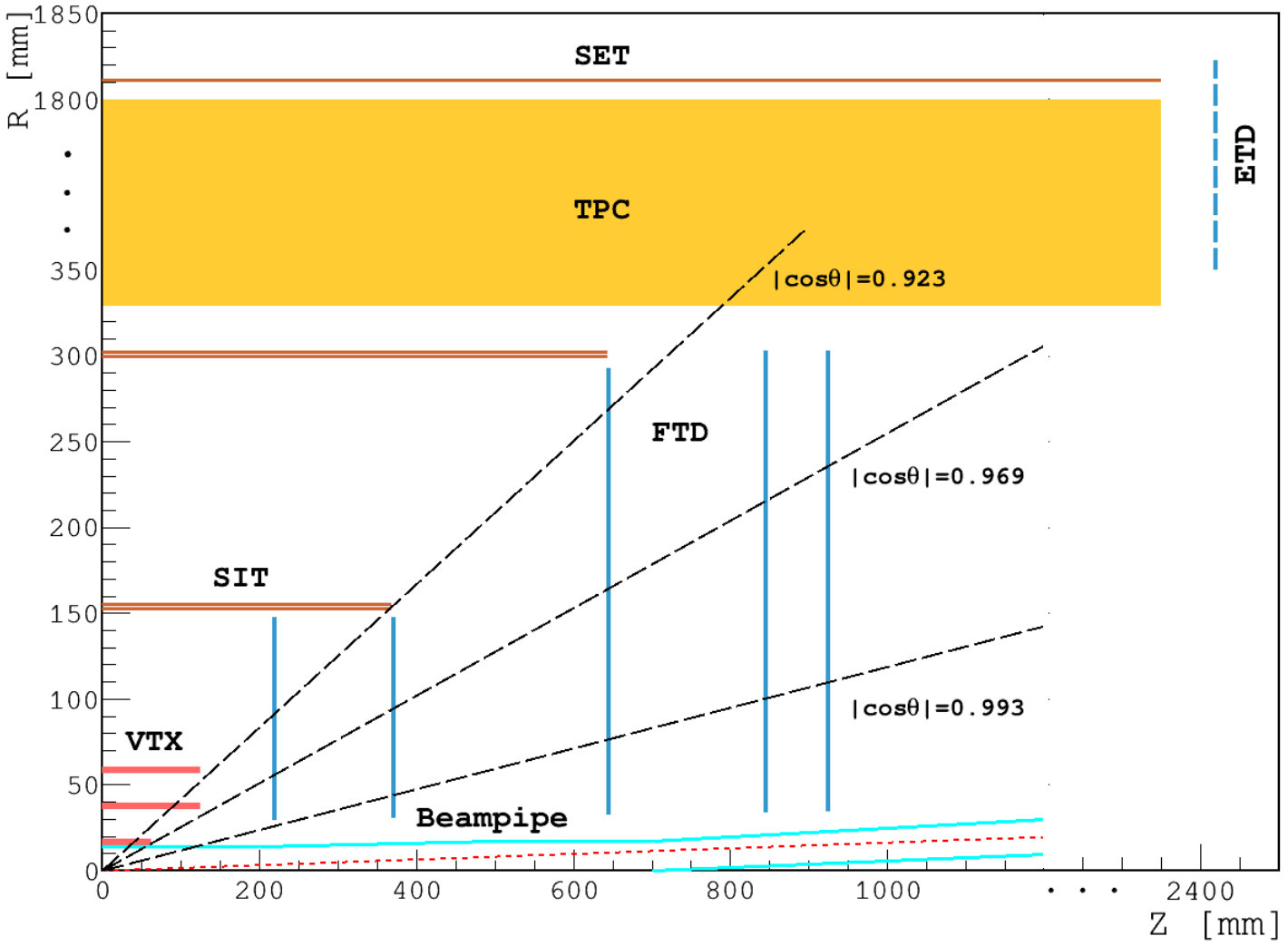
5 June 2019

TRACKER LAYOUT



General Requirements

Detector		Radius R [mm]		$\pm z$ [mm]	Material budget [X_0]
SIT	Layer 1	153		371.3	0.65%
	Layer 2	300		664.9	0.65%
SET	Layer 3	1811		2350	0.65%
		R_{in}	R_{out}		
FTD	Disk 1	39	151.9	220	0.50%
	Disk 2	49.6	151.9	371.3	0.50%
	Disk 3	70.1	298.9	644.9	0.65%
	Disk 4	79.3	309	846	0.65%
	Disk 5	92.7	309	1057.5	0.65%
ETD	Disk	419.3	1822.7	2420	0.65%

***Note**: positions do not match the geometry in simulation.*

- Spatial resolution: $\sigma_{r\varphi} \sim 7\ \mu m$, time resolution: $\sigma_t \sim 10\ ns$ (to separate bunching crossings), low material budget

SENSOR TECHNOLOGIES

- Conventional silicon microstrip sensor with fine pitch

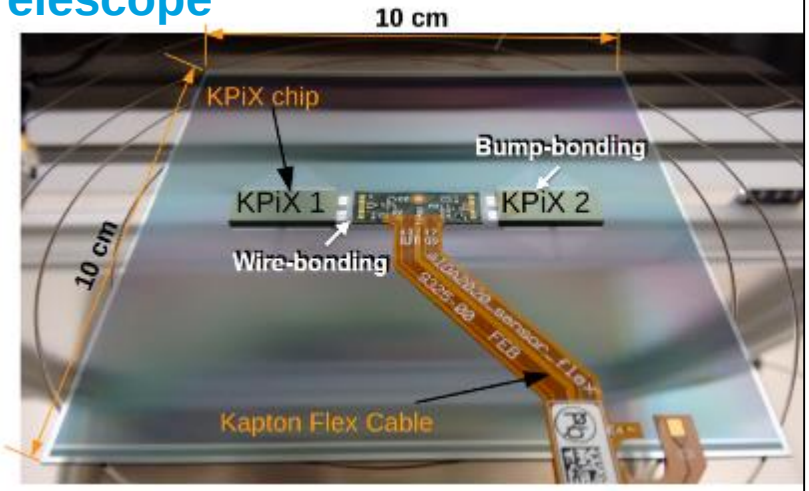
Strip Silicon Sensor

- Size of **10 x 10 cm²**;
- Thickness of 320 µm → **0.3% X_0**;
- Pitch of **25 µm**, thus hit resolution **~7.2 µm**;
- Alternate strips readout.

Readout & way to power

- An integrated (bump-bonding) pitch adapter and digital readout ASIC: **KPiX**;
- A Kapton Flex Cable glued (Araldite2011) + wire-bonded to the sensor
  - Provide **bias** voltage to the sensor;
  - KPiX is **communicated/powered** via it.

LYCORIS Telescope

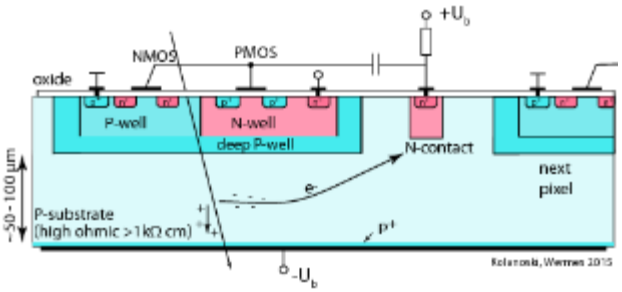


- **Monolithic CMOS pixel/strip sensors** → integrated detection element and readout electronics on the same silicon substrate

ATLAS CMOS Pixel/Strip Sensors

- Not intended to start sensor design from scratch → limited R&D time and no need to re-invent the wheel
- CMOS pixel sensors proposed for **the ATLAS outer most pixel layer** (and strip) but not matured enough for construction → *opportunity to carry it on for the CEPC tracker*

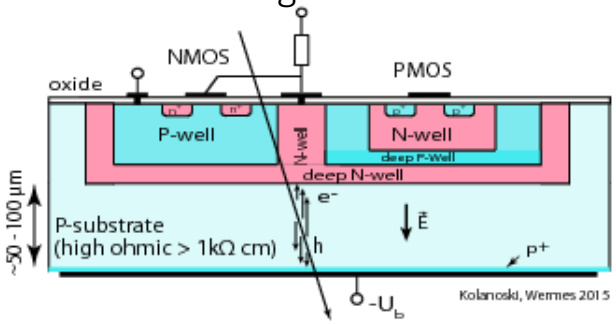
Small fill factor



TJ MALTA/MonoPix (TJ HR-CMOS 0.18 um)

OverMOS (TJ HR-CMOS 0.18 um)

Large fill factor



ATLASPix (AMS/TSI HV-CMOS 0.18 um)

LF-MonoPix (LFoundry HV-CMOS 0.15 um)

CHESS 2 (AMS HV-CMOS 0.35 um)

APPLICABLE CMOS TECHNOLOGIES

0.18 HV-CMOS support ceased

0.18 CIS, Used for JadePix development, modified process required for fast charge collection

0.15 um HV-CMOS, NDA signed

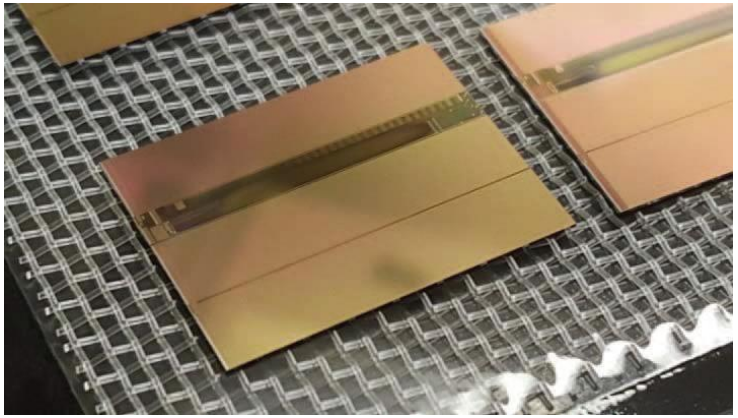
0.2 um SOI, used for sensor development

Accessible 0.18 um SOI HV-CMOS

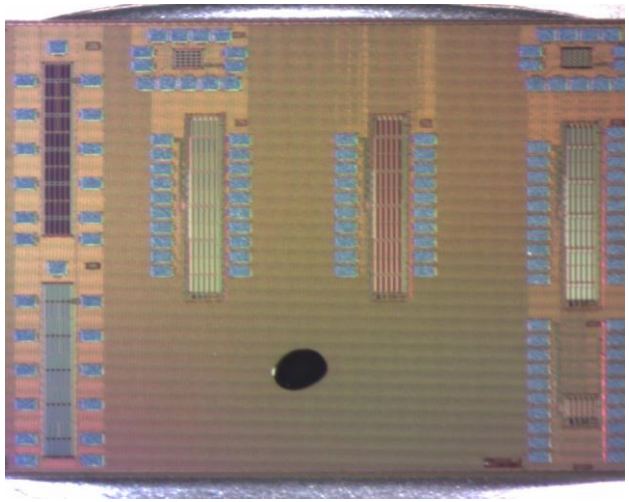
Accessible 0.13 um BCDLite

CMOS Strip Sensors

CHESS (CMOS HV Evaluation for Strip Sensors)



OverMOS



- Have spent much time and effort to characterize the two variants, CHESS 2 (HV-CMOS) and OverMOS1/1.1 (HR-CMOS)
  - Part of the ATLAS ITk-Strip project funded via MOST, experience and more lessons learnt
- In general, sensor design not successful; R&D project ceased two years ago

LANCASTER DISCUSSION

- Had nearly a full day discussion in March with
  - Daresbury: John Dainton (Liverpool Emirate Professor), Roy Lemmon(ALICE group leader), Marcello Borri（Detector System group leader）
  - Lancaster: Harald Fox, Daniel Muenstermann
  - Edinburgh: Yanyan Gao

A proposal presented at the Oxford workshop.

Step 1: ATLASPix + ALICE/ATLAS stave core for demonstration

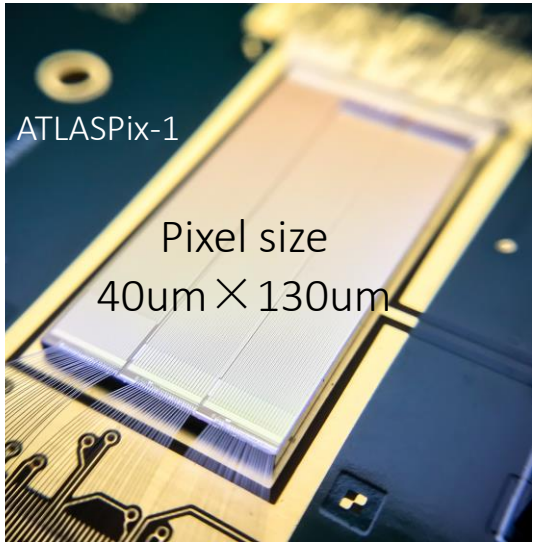
Step 2: CMOS pixel sensor with new process, and R&D on stave core

  - Link to Daniel Muenstermann's talk

- Following-up actions:
  - Applying for funding to support the UK R&D efforts, e.g. GCRF award (Lancaster) and STFC special fund

ATLASPIX PERFORMANCE

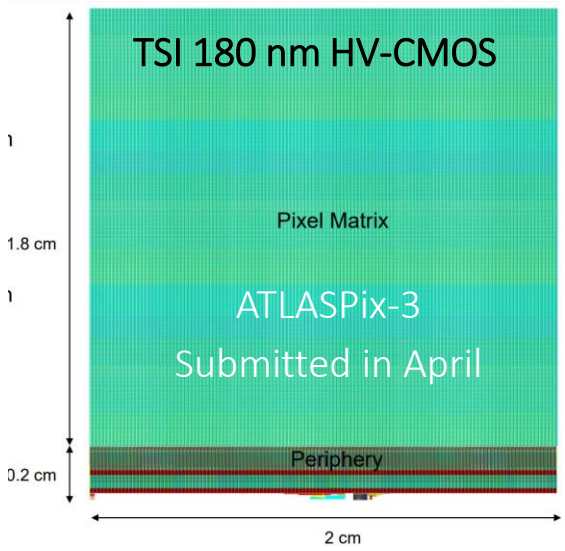
- Fully integrated readout
- Fast charge collection
- Low material budget



AMS 180 nm HV-CMOS, substrate resistivity 20 – 1000 Ω, 100 um thick (can be thinned to 50 um)

ATLASPix-1

Parameter	Measured	Requirement
Material budget	100 um (50 um possible)	100 um
Spatial resolution	$\sigma_{x/y}$ = 11.3/37.0 um	7/X um
Time resolution	6.8 ns	10 ns
Efficiency	>99.7%	99.5% or higher
Power consumption	2-300 mW/cm^2	200 mW/cm^2



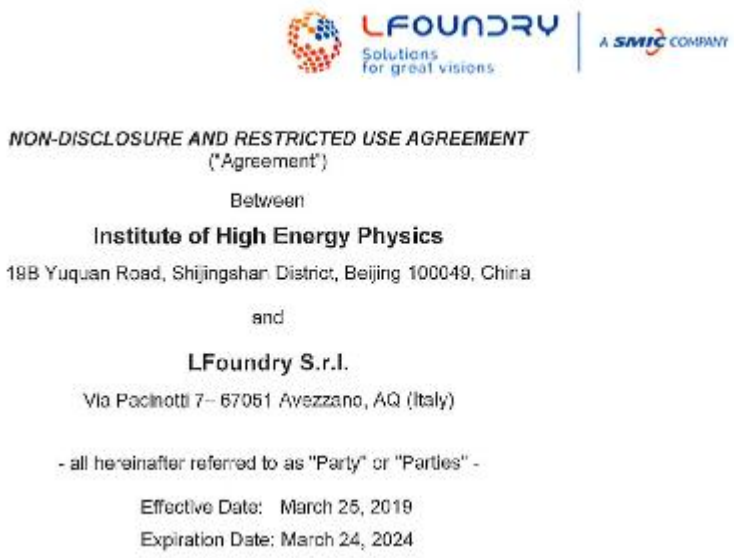
ATLAS CMOS COLLABORATION

Most of the efforts not necessarily related to ATLAS ITk-Pixel (e.g. generic R&D funding) → opportunity to invite them to work on CEPC?

Chip design remains the most critical challenge!

ACCESSIBLE CMOS TECHNOLOGIES

1. **TowerJazz 0.18 um CIS** (already used for JadePix, modified process required for fast charge collection)
2. **LFoundry 0.15 um HV-CMOS** (NDA signed)
3. **SMIC HV-CMOS processes** New



LFOUNDRY Solutions for great visions | A SMIC COMPANY

NON-DISCLOSURE AND RESTRICTED USE AGREEMENT
("Agreement")

Between

Institute of High Energy Physics

19B Yuquan Road, Shijingshan District, Beijing 100049, China

and

LFoundry S.r.l.

Via Paolnotti 7– 67051 Avezzano, AQ (Italy)

- all hereinafter referred to as "Party" or "Parties" -

Effective Date: March 25, 2019

Expiration Date: March 24, 2024

SMIC

Semiconductor Manufacturing International Corporation
中芯國際集成電路製造有限公司*

(incorporated in the Cayman Islands with limited liability)

(Stock Code: 981)

DISCLOSEABLE TRANSACTION
DISPOSAL OF SUBSIDIARY

On 29 March 2019 (after trading hours), the Vendor and the Target Company entered into the Share Purchase Agreement with the Purchaser, pursuant to which, among other things, the Vendor agreed to sell and the Purchaser agreed to purchase the Sale Shares at the Consideration in accordance with the terms and conditions of the Share Purchase Agreement.

As certain of the applicable percentage ratios under Chapter 14 of the Listing Rules for the Transaction exceed 5% but are less than 25%, the Transaction constitutes as a discloseable transaction of the Company, and is therefore subject to the relevant reporting and announcement requirements under Chapter 14 of the Listing Rules.

As the Closing is subject to the satisfaction and/or of terms and conditions set out in the Share Purchase Agreement, the Transaction may or may not proceed. Shareholders and potential investors should exercise caution when dealing in the Shares.

SMIC sold LFoundry to JIANGSU CAS-IGBT Co. LTD.

SMIC HV-CMOS PROCESSES

Tech Node	IO Voltage/Tech Type/Char	RF	2019 MPW Booking Cut-Off Date											
			Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
28nm	IO=1.8V | IO=2.5V CMOS Logic (HP)	Y	8 Q4S (Fab8)		5 Q58 (Fab2)			18 Q5K (Fab2)			3 Q5Q (Fab2)			
40nm	IO=1.8/2.5V| IO=1.8V| IO=2.5V CMOS Logic (LL|UP)	Y		12 Q55 (Fab2)		2 Q62 (Fab2)		4 Q5J (Fab2)			10 Q5R (Fab2)			10 Q5Z (Fab2)
	IO=8/32V CMOS High Voltage (HV) *													
55nm	IO=2.5/5V | IO=2.5V Adv. Emb-Flash (Cu-BEOL) (LL)						14 Q5G (Fab2)						19 Q5X (Fab2)	
	IO=1.8/2.5V | IO=1.8V| IO=2.5V CMOS Logic (LL)	Y		19 Q56 (Fab2)		2 Q5E (Fab2)			16 Q5M (Fab2)			22 Q5W (Fab2)		
	IO=6/32V | IO=8/32V CMOS High Voltage (HV) *													
0.11/0.13um	IO=3.3V CMOS Logic (GE)|Mixed Signal (GE)	Y	15 Q54 (Fab1)		19 Q59 (Fab1)		28 Q5H (Fab1)			6 Q5N (Fab1)		15 Q5V (Fab1)		17 Q5Y (Fab1)
0.13um	IO=3.3/5V| IO=5V Adv. Emb-EEPROM (Cu-BEOL) (LL)			26 Q57 (Fab1)						27 Q5P (Fab1)				
0.15um	IO=18V CMOS High Voltage (HV) *												5 Q61 (Fab1)	
0.153um	IO=3.3V CMOS Logic (GE)|Mixed Signal (GE)	Y			12 Q5C (Fab1)									
0.18um	IO=5/6/9/12/16/20/24/30/35/40 BCD V3E (EP) *	Y									10 Q5T (Fab1)			
	IO=3.3V CMOS Logic (GE)|Mixed Signal (GE)	Y	8 Q53 (Fab1)				7 Q5F (Fab1)				3 Q5S (Fab1)			
0.18um	IO=3.3V CMOS Logic (GE)|Mixed Signal (GE) IO=5/6/9/12/16/20/24/30/35/40V BCDM*	Y			5 Q5B (Fab7)				9 Q5L (Fab7)				12 Q60 (Fab1)	
	IO=3.3/5V| IO=5V EEPROM Embedded (GE)					9 Q5D (Fab1)						8 Q5U (Fab7)		

* 2019 new offered feature: 40nm/55nm/0.15um HV & 0.18um BCD

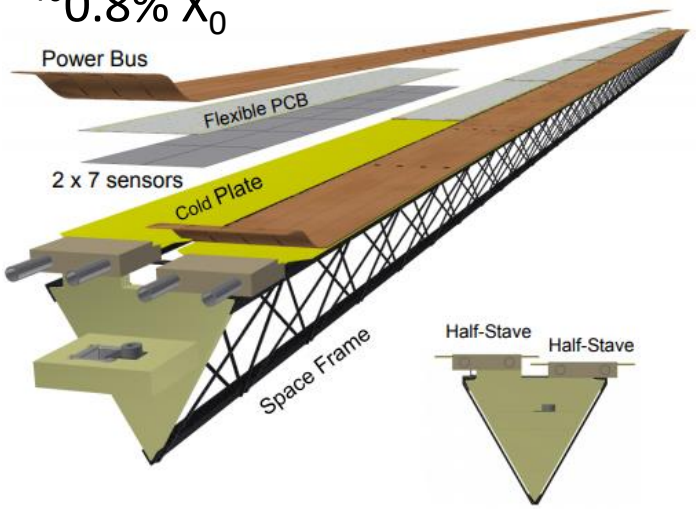
Version: 4.3 Update Date: 2019-1-21

Note: Please login SMIC-Now to find the most updated MPW schedule. (请登录Smic-Now以查阅最新MPW Schedule.)

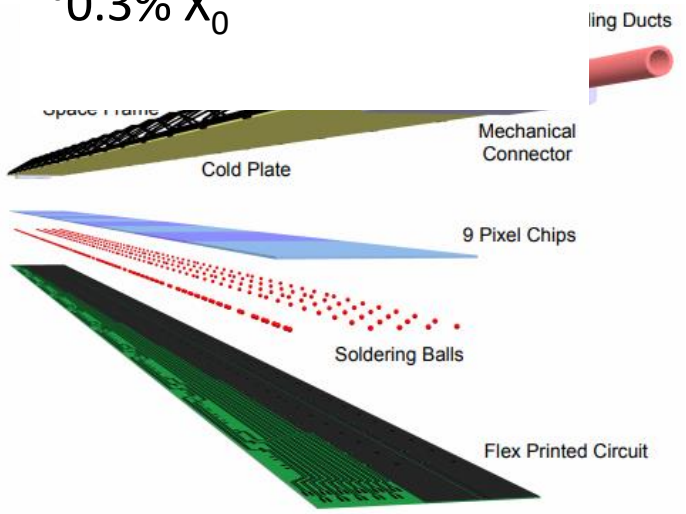
New processes to be tried out (test structures to be submitted) … long term collaboration with SMIC to be established

SUPPORTING STRUCTURE

ALICE Outer Layer Stave
~0.8% X_0

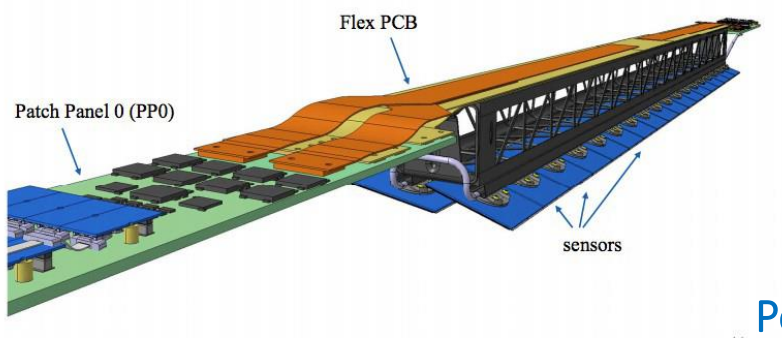


ALICE Inner Layer Stave
~0.3% X_0



ATLAS-ITK: 0.5% X_0 ITK alpine stave (+module)

ATLAS IBL: 0.7% X_0 IBL stave, (+module)



CEPC design target:

0.65% X_0 for stave + modules

Crucial elements:

- Light-weighted carbon truss structure
- Al based flex (prototype with Cu)

Possibility to produce them in China to be explored

DEMONSTRATOR MATERIAL BUDGET

Stavelet Demonstrator

Stave el	Comp	Material	Thick [um]	X0 [cm]	X0[%]
Module	FPC metal	Al (Cu)	50	8.896 (1.435)	0.056 (0.348)
	FPC insulat	Polyimide	100	28.41	0.035
	ASIC	Silicon	100 (150)	9.369	0.106 (0.160)
	Glue	Eccobond 45	100	44.37	0.023
	Total (Al and Si 100um) Total (Al and Si 150um) Total (Cu and Si 150um)				0.22 0.274 0.566
Everything else	Total				0.6
Total (Module Al and Si 100um) Total (Module Al and Si 150um) Total (Module Cu and Si 150um)					0.82 0.874 1.166

ALICE Outer Layer Stave

Table 4.2: Estimated contributions of the Outer Layer Stave to the material budget.

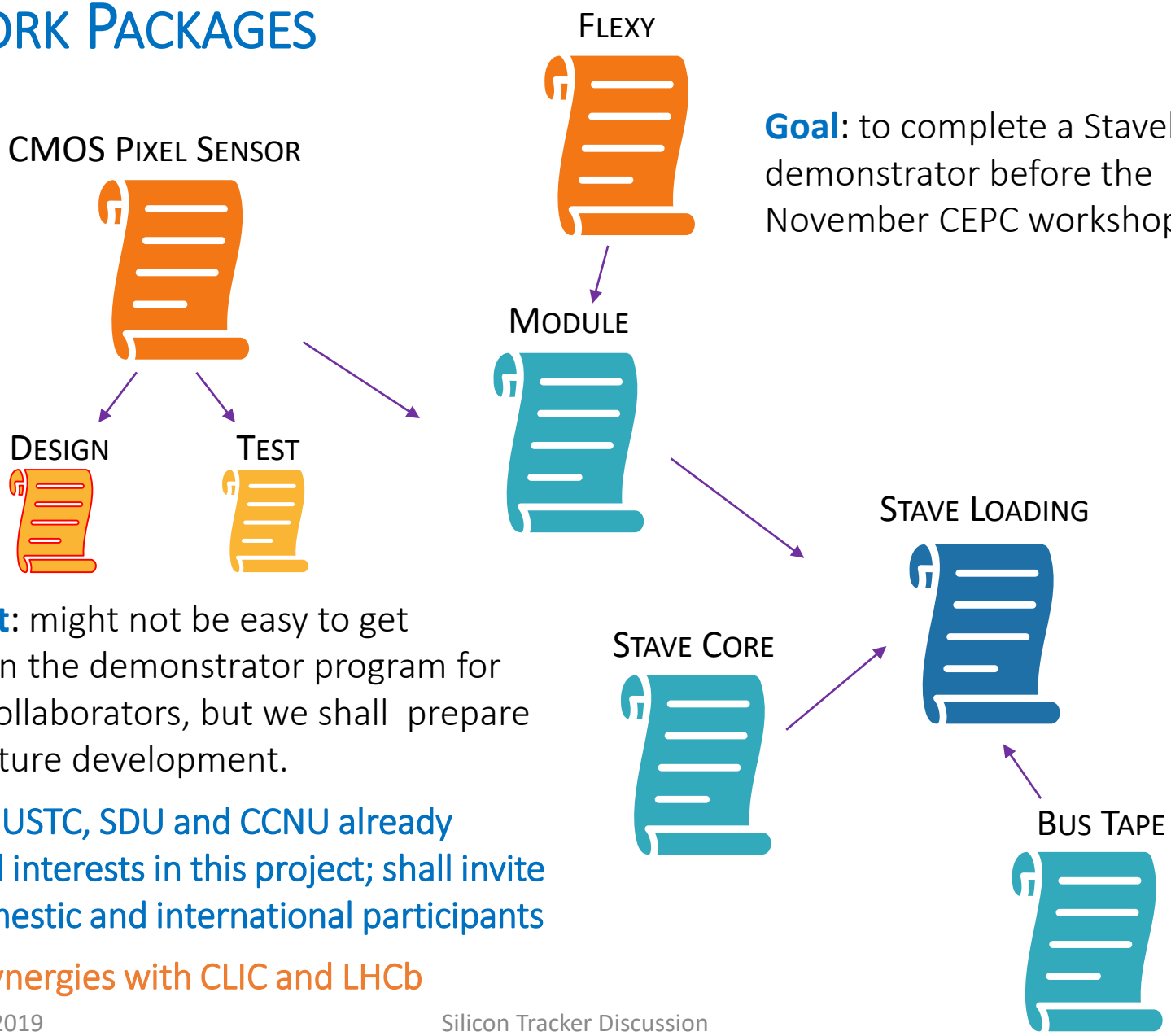
Stave element	Component	Material	Thickness (µm)	X_0 (cm)	X_0 (%)
Module	FPC Metal layers	Aluminium	50	8.896	0.056
	FPC Insulating layers	Polyimide	100	28.41	0.035
	Module plate	Carbon fibre	120	26.08	0.046
	Pixel Chip	Silicon	50	9.369	0.053
	Glue	Eccobond 45	100	44.37	0.023
Power Bus	Metal layers	Aluminium	200	8.896	0.225
	Insulating layers	Polyimide	200	28.41	0.070
	Glue	Eccobond 45	100	44.37	0.023
Cold Plate		Carbon fleece	40	106.80	0.004
		Carbon paper	30	26.56	0.011
	Cooling tube wall	Polyimide	64	28.41	0.013
	Cooling fluid	Water		35.76	0.105
	Carbon plate	Carbon fibre	120	26.08	0.046
	Glue	Eccobond 45	100	44.37	0.023
Space Frame		Carbon rowing			0.080
Total					**0.813**

ALICE Inner Layer Stave

Table 4.1: Estimated contributions of the Inner Layer Stave to the material budget.

Stave element	Component	Material	Thickness (µm)	X_0 (cm)	X_0 (%)
HIC	FPC Metal layers	Aluminium	50	8.896	0.056
	FPC Insulating layers	Polyimide	100	28.41	0.035
	Pixel Chip	Silicon	50	9.369	0.053
Cold Plate		Carbon fleece	40	106.80	0.004
		Carbon paper	30	26.56	0.011
	Cooling tube wall	Polyimide	25	28.41	0.003
	Cooling fluid	Water		35.76	0.032
	Carbon plate	Carbon fibre	70	26.08	0.027
	Glue	Eccobond 45	100	44.37	0.023
Space Frame		Carbon rowing			0.018
Total					**0.262**

Work Packages



Goal: to complete a Stavelet demonstrator before the November CEPC workshop

Comment: might not be easy to get involved in the demonstrator program for non-UK collaborators, but we shall prepare for the future development.

Tsinghua, USTC, SDU and CCNU already expressed interests in this project; shall invite more domestic and international participants

Explore synergies with CLIC and LHCb

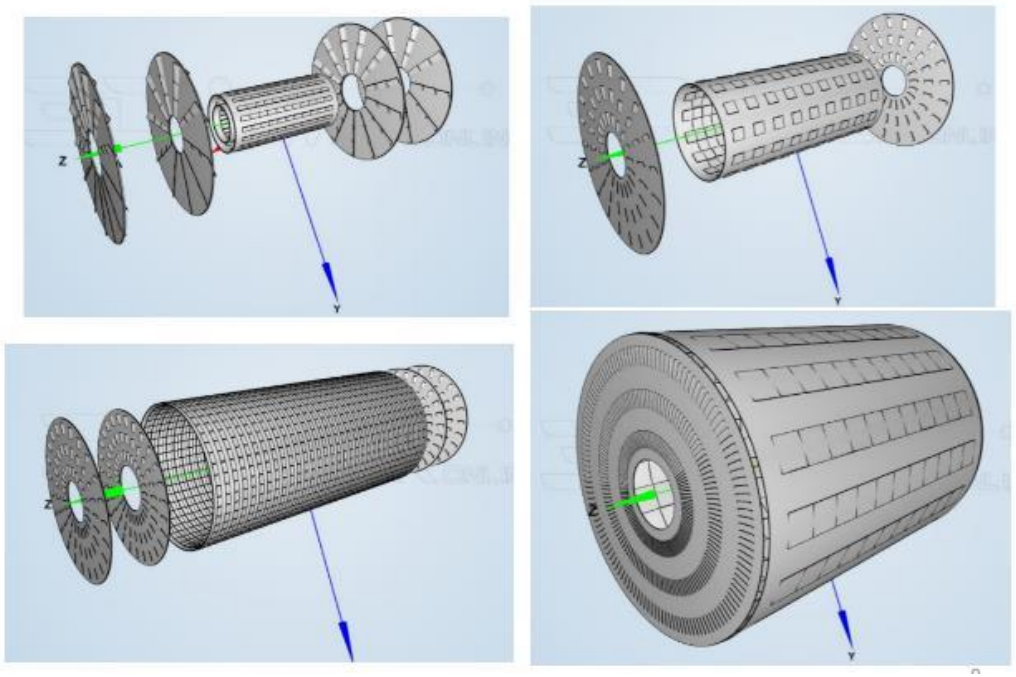
BEYOND DEMONSTRATOR

- Pixel sensor design optimization toward the requirements of the CEPC silicon tracker
  - Pixel size: 50×150, 25 ×300
  - Lower power consumption: less demanding if active cooling applied
  - Powering scheme: serial powering to save material budget ?
  - Other functionalities to be discussed
  - Migrate to SMIC or other foundry that we have access to
- Light weighted support structure (stave core)
  - Improved design inspired by ALICE/ATLAS truss structure, longer extension and higher rigidity/stability (challenging to align detector elements with less tracks)
- Tracking system design
  - Not much discussed yet but definitely needed

Organization, funding support, etc. subject to further discussion

Other Items: Tracking & Tracker Layout

- Have started working on the new tracking software of **ACTS**, which is a generic framework being developed by ATLAS
- Migrate ACTS to **SNIPER or any framework chosen for CEPC**
  - CEPC also listed as a sub-project in ACTS development



CEPC baseline tracker geometry in ACTS

Next step: tracking performance (re-)evaluation (the CDR design, different pixel sizes)

Tracker layout optimization

Depletion Depth