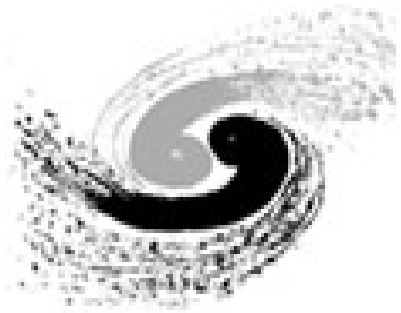
HGTD DAQ AND ELECTRONICS

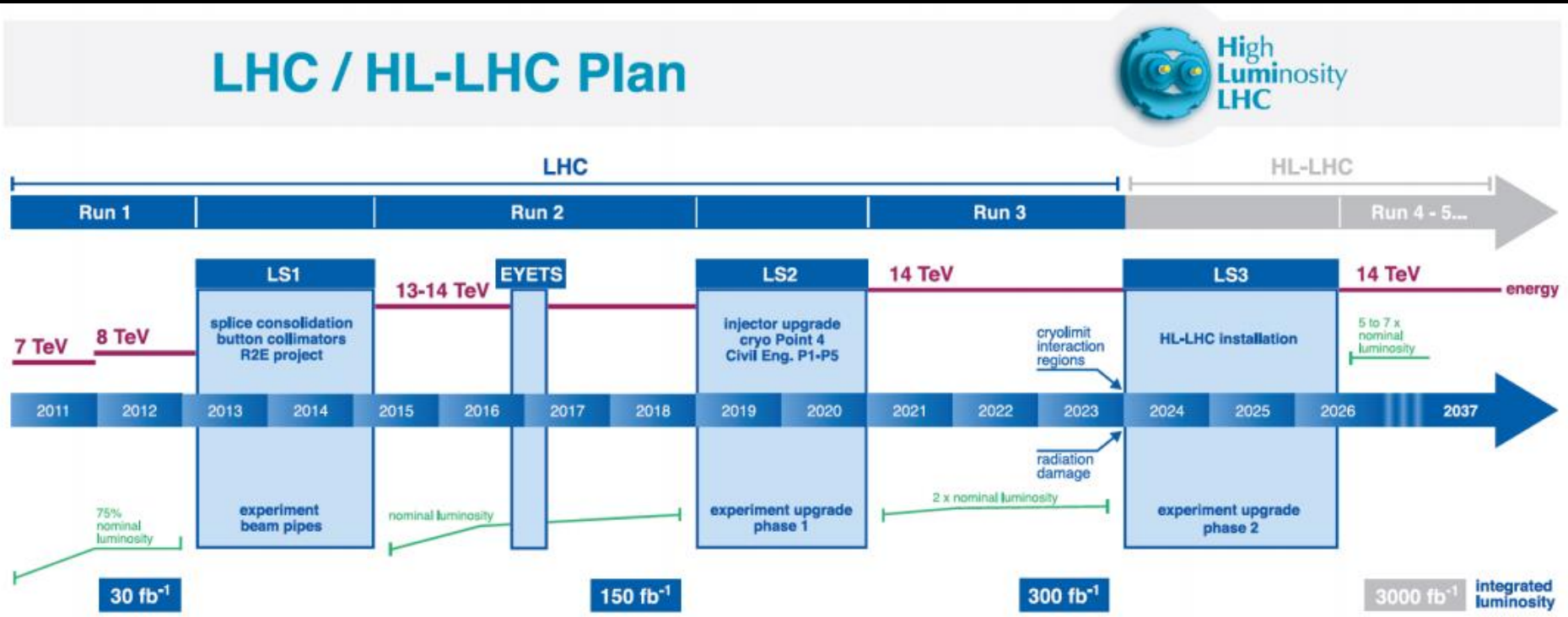
JuanAn García
Institute of High Energy Physics
HGTD IHEP Workshop
June 2019



OUTLOOK

- HGTD requirements
- HGTD readout system
  - On detector electronics
  - Off detector electronics
- DAQ and Luminosity
- Demonstrator
- TO-DO list

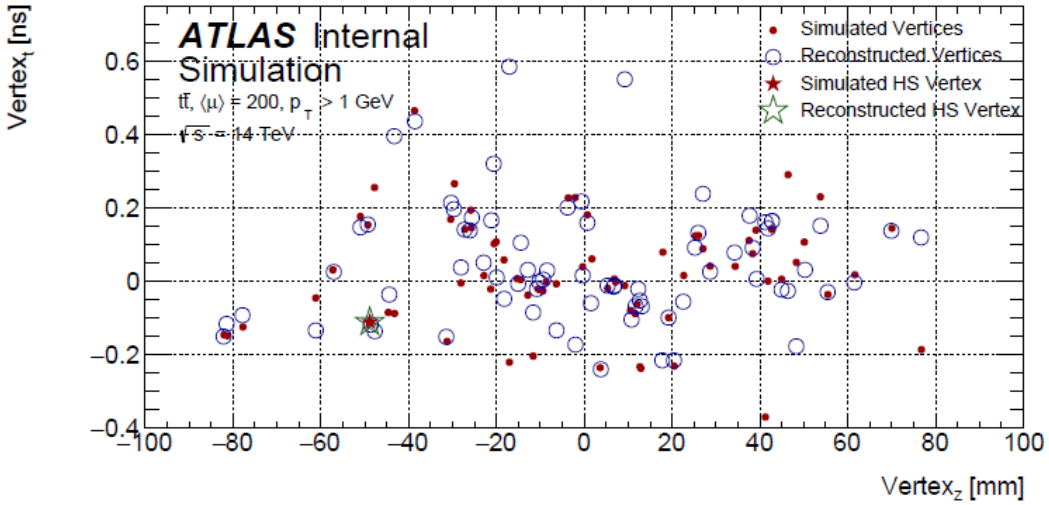
HGTD REQUIREMENTS



$L = 7.5 \times 10^{34}\ cm^{-2}\ s^{-1}$

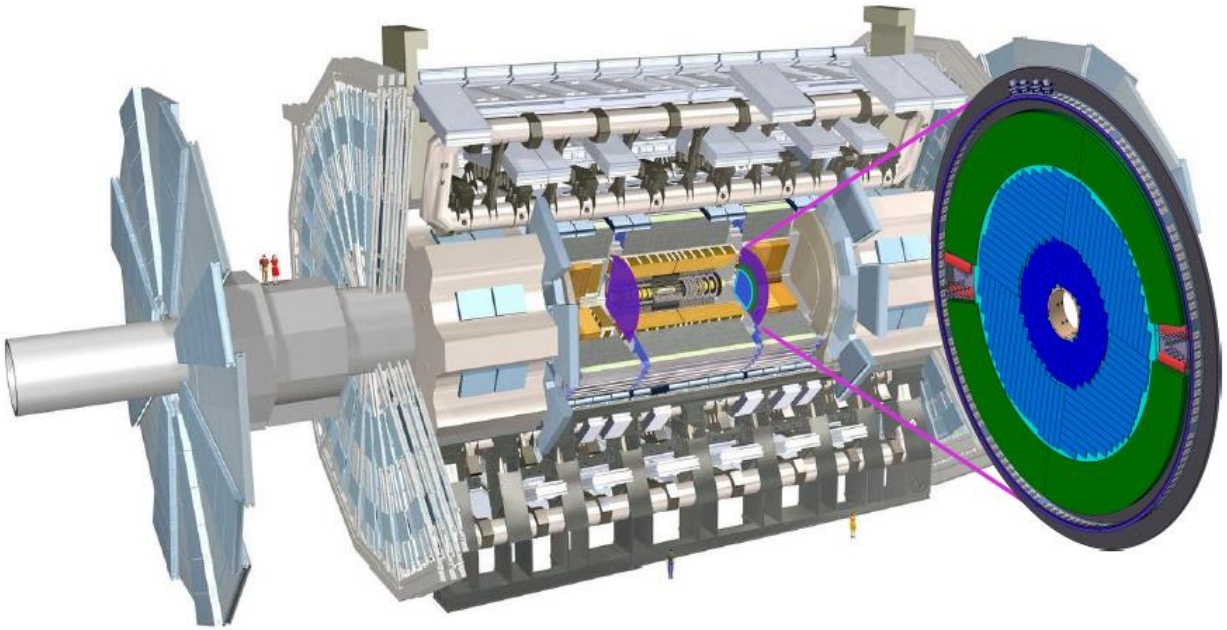
Pile-up of $\mu \approx 200$

High Granularity Timing Detector will provide time resolution at a high pile-up



HGTD REQUIREMENTS

HGTD will be situated between ITK inner detector and the endcap calorimeters (current MBTS region)

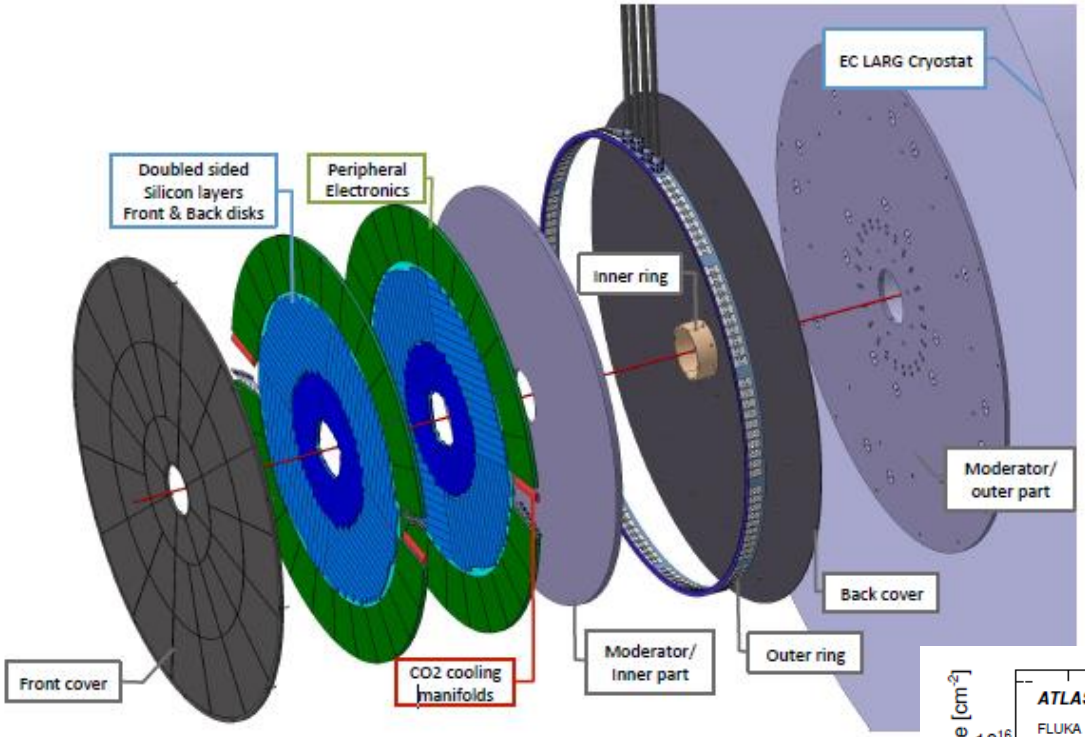


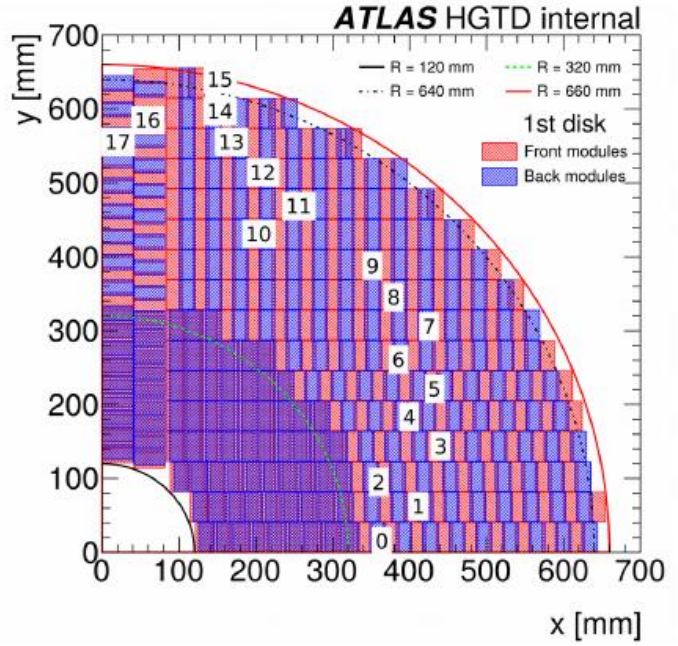
Pseudo-rapidity coverage	$2.4 < \|\eta\| < 4.0$
Thickness in z	75 mm (+50 mm moderator)
Position of active layers in z	$z = \pm 3.5$ m
Radial extension:	
Total	110 mm $< r <$ 1000 mm
Active area	120 mm $< r <$ 640 mm
Pad size	1.3 mm × 1.3 mm
Active sensor thickness	50 µm
Number of channels	3.59 M
Active area	6.4 m^2
Average number of hits per track	
$2.4 < \|\eta\| < 3.1$	≈2
$3.1 < \|\eta\| < 4.0$	≈3
Collected charge per hit	> 2.5 fC
Average time resolution per hit (start and end of operational lifetime)	
$2.4 < \|\eta\| < 3.1$	≈ 40 ps (start) ≈ 70 ps (end)
$3.1 < \|\eta\| < 4.0$	≈ 40 ps (start) ≈ 85 ps (end)
Average time resolution per track (start and end of operational lifetime)	≈ 30 ps (start) ≈ 50 ps (end)

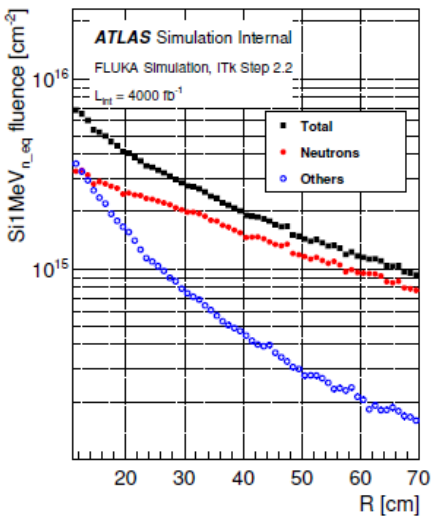
~40 ps time resolution is required!

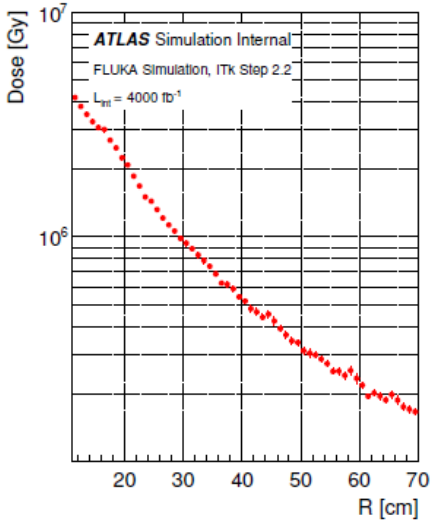
HGTD REQUIREMENTS

Detector layout and radiation hardness:









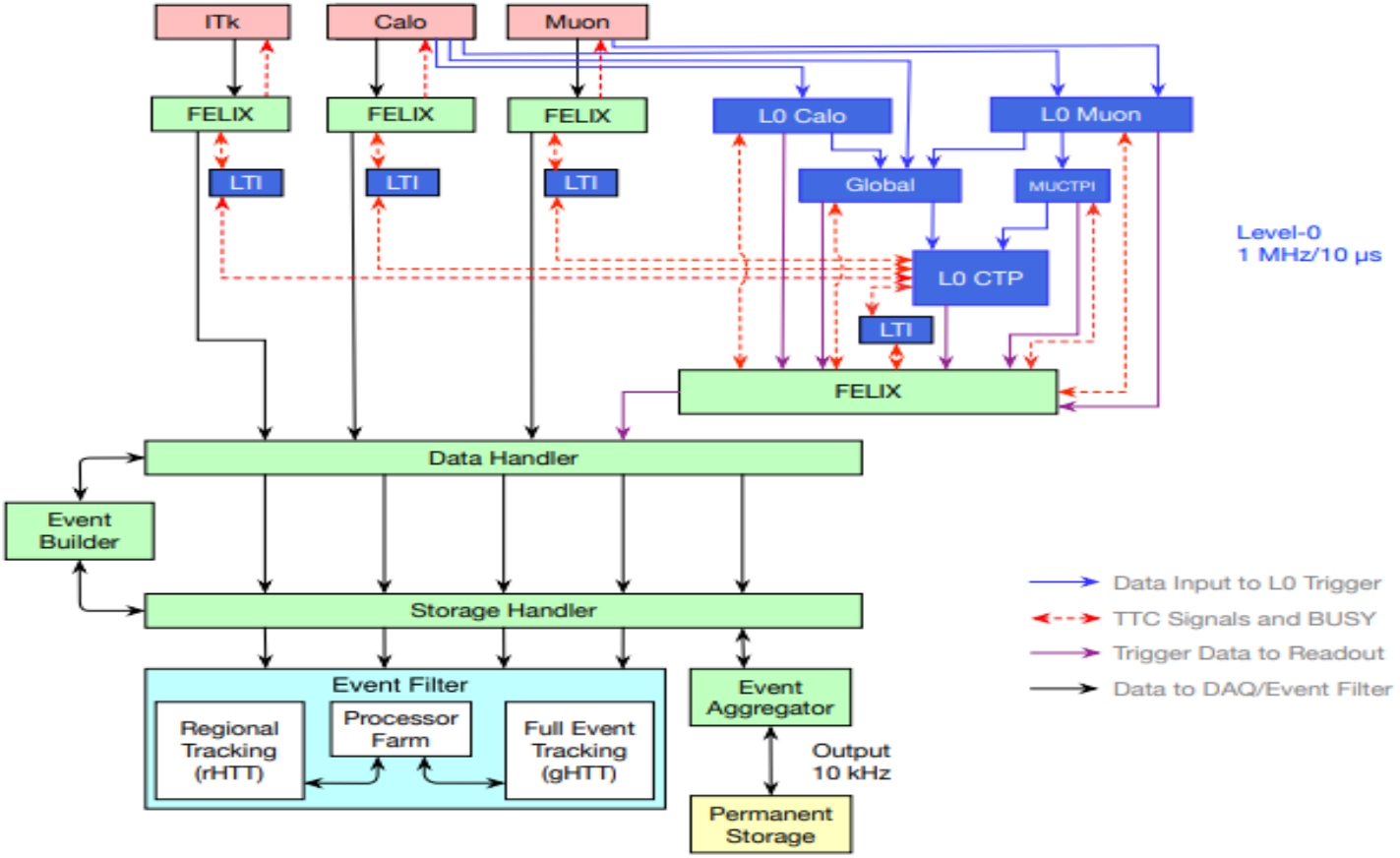
Radiation hard is required for all the components:

- Sensor
- On-detector electronics

HGTD REQUIREMENTS

TDAQ/trigger requirements:

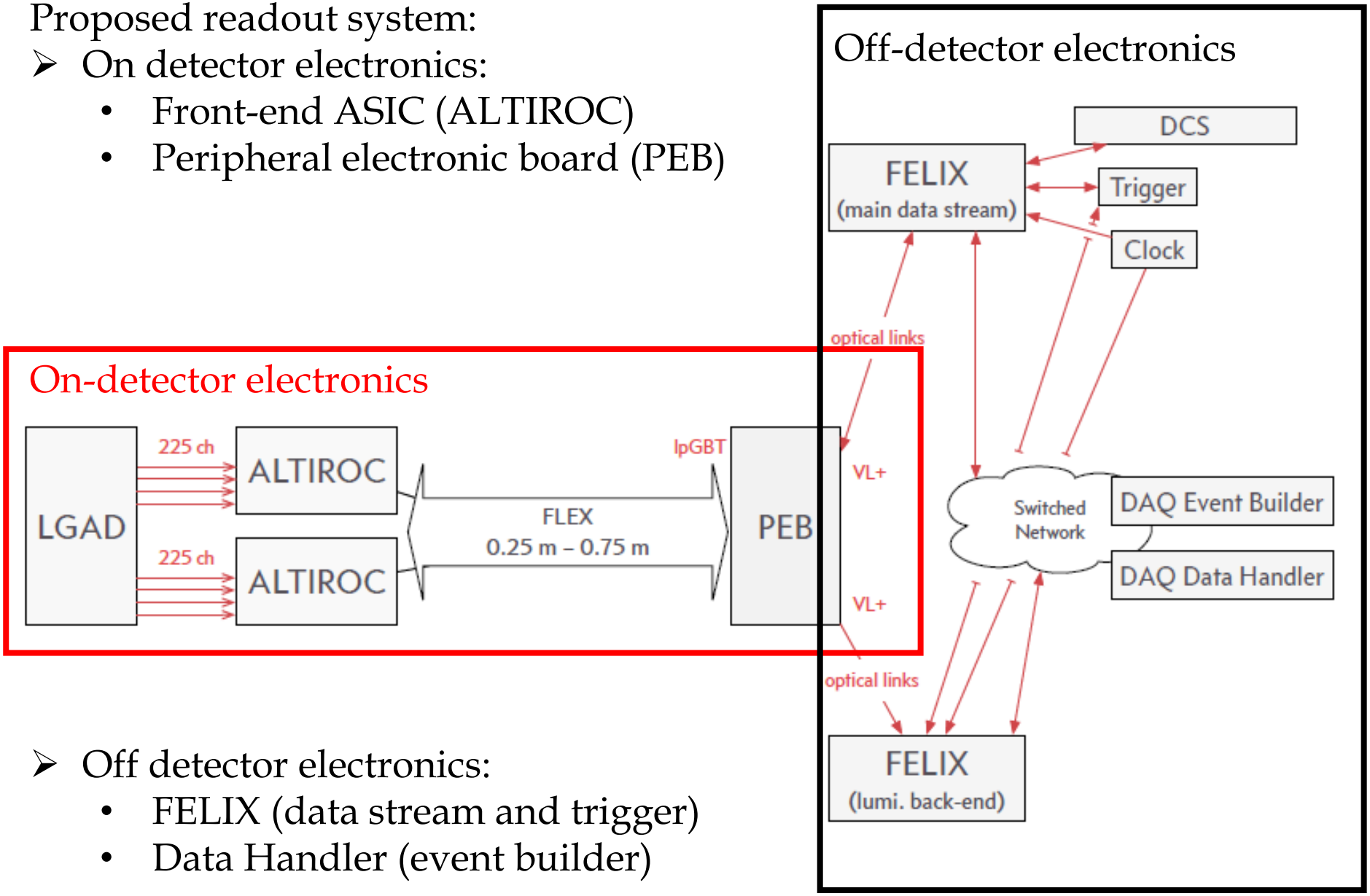
- Two level triggers are foreseen for ATLAS phase II:
  - Level 0 (L0): up to 4 MHz with 10 μs latency.
  - Level 1 (L1): up to 1 MHz with 35 μs latency.
- Consecutive triggers: At most four (4) L0A in five (5) consecutive BCs. No simple dead time!



HGTD READOUT SYSTEM

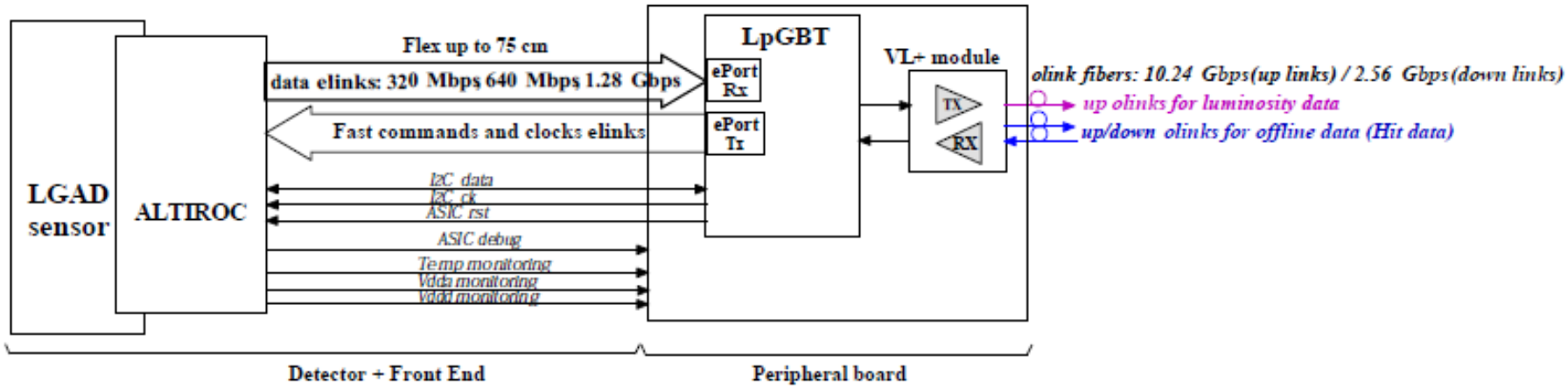
Proposed readout system:

- On detector electronics:
  - Front-end ASIC (ALTIROC)
  - Peripheral electronic board (PEB)



- Off detector electronics:
  - FELIX (data stream and trigger)
  - Data Handler (event builder)

ON DETECTOR ELECTRONICS



Different data and control lines between ALTIROC and peripheral electronics through the flex (~25 to 75 cm length):

- Data transfer:
  - Downlink (readout data): 320, 640 and 1280 Mbps
  - Uplink (fast commands/configuration): 80, 160 and 320 Mbps
  - Clock 320 MHz
- Control lines: I^2C bus for Detector Control System (DCS)
  - Analog current
  - Digital current
  - Temperature
- Low voltage supply
- High voltages

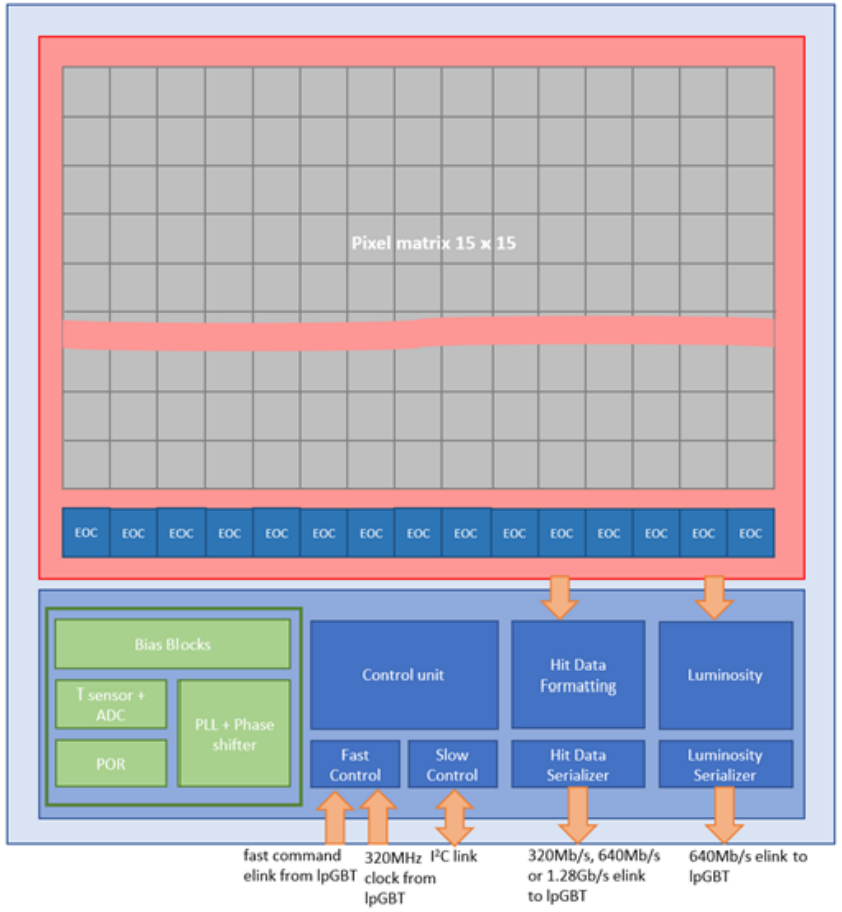
ON DETECTOR ELECTRONICS

Front-end ASIC (ALTIROC) requirements:

- Radiation hardness ~5 MGy
- Clock jitter <25 ps
- Time over threshold (ToT) and Time of Arrival (ToA) information
- Latency up to 35 µs @ 40 MHz
- Low power dissipation

Readout architecture:

- 130 nm CMOS technology
- Analog and digital architecture (digital on top)
- End of column (EOC) logic
- 225 channels (pixels)
- I²C link for slow control
- PLL and phase shifter
- DAQ stream 320, 640 and 1280 Mbps
- Luminosity stream 640 Mbps



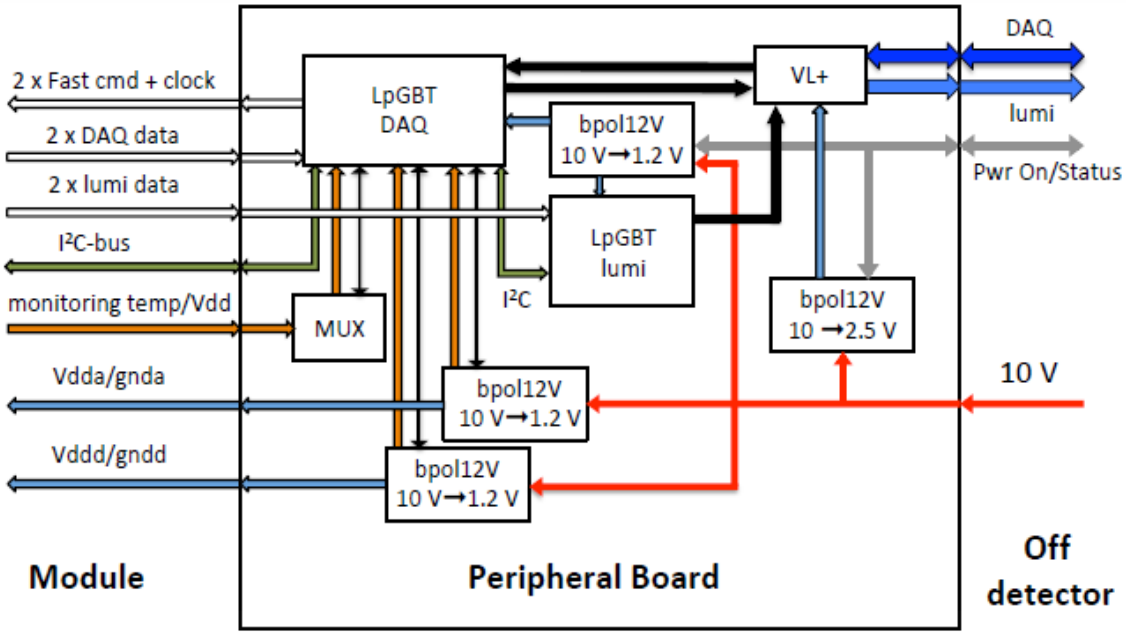
ALTIROC v2 under design:

- See Jie Zhang talk about the data format

ON DETECTOR ELECTRONICS

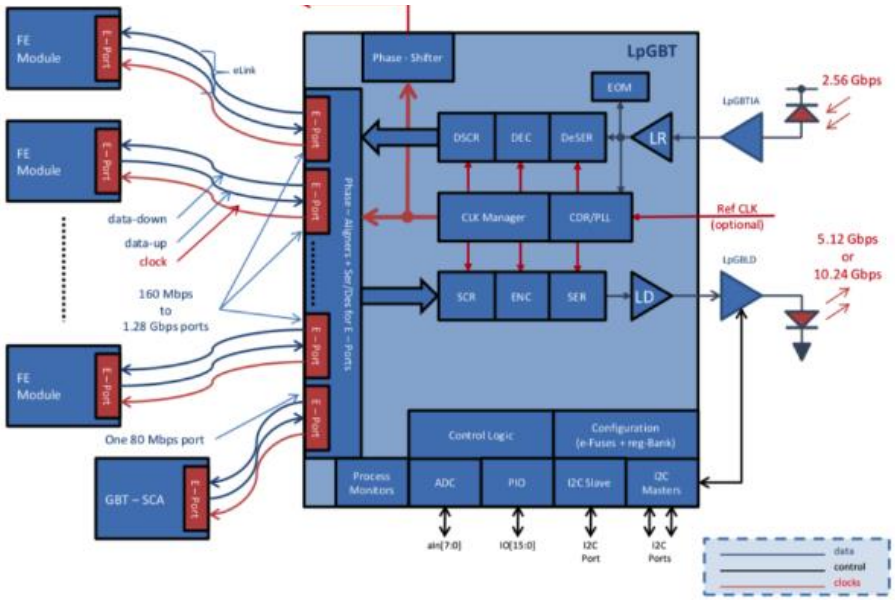
Peripheral electronic board:

- 10 V to 1.2 V DC-DC converter
- Low power GigaBit Transciver (lpGBT)
- Services (LV and HV)
- Versatile link Plus: 2.56 and 10.24 Gbps (up/down-link)



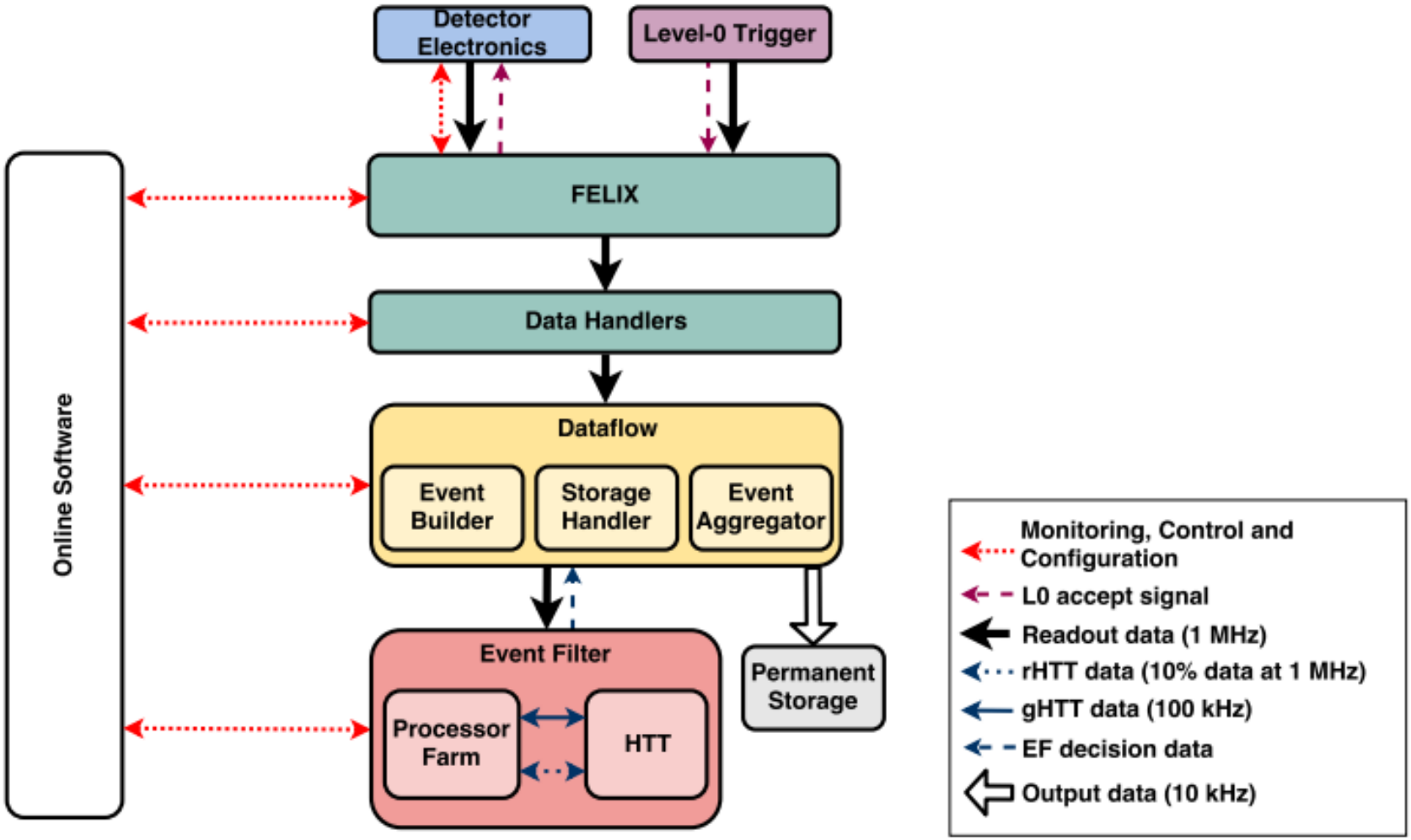
lpGBT:

- Radiation hard
- Low power dissipation
- Clock jitter <2 ps
- I²C bus
- E-link data stream 320, 640 and 1280 Mbps
- E-link data up 80, 160 and 320 Mbps



OFF DETECTOR ELECTRONICS

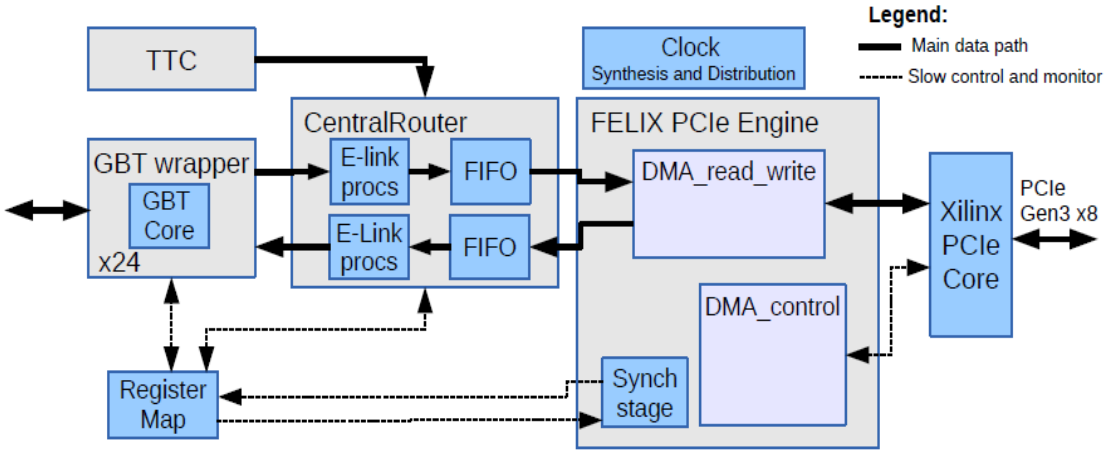
ATLAS phase II readout architecture:

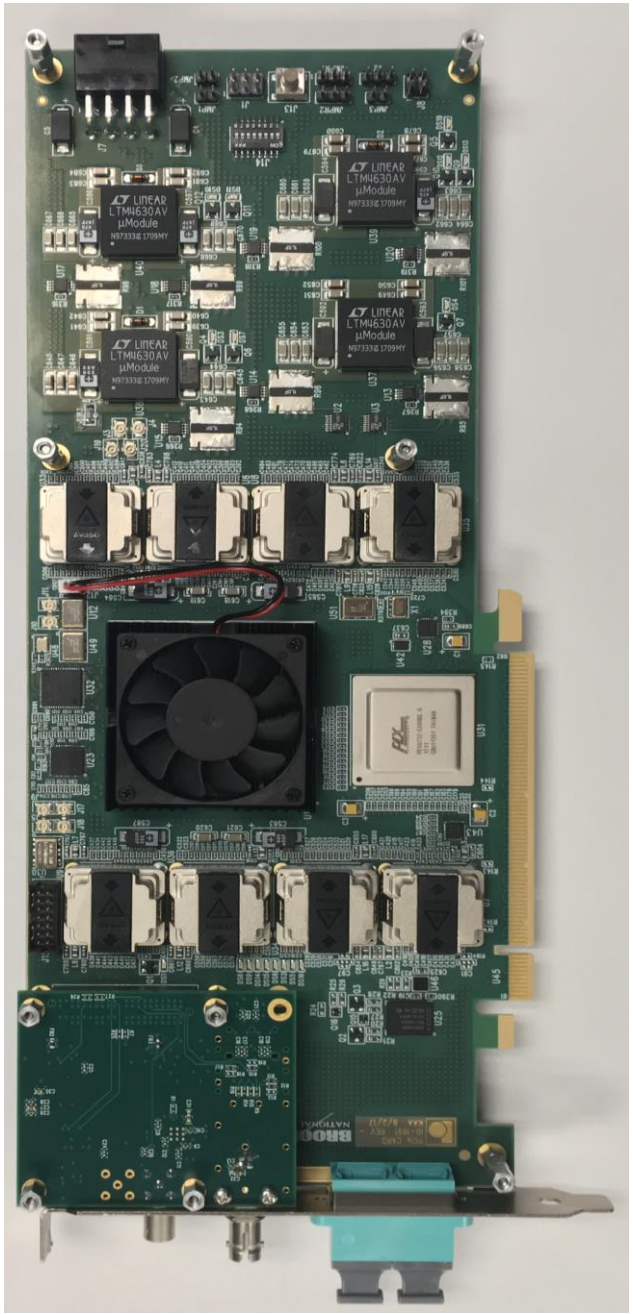


OFF DETECTOR ELECTRONICS

The FELIX (Front End LInk Exchange) board:

- Detector independent (common to all ATLAS detectors).
- Support standard GBT protocol.
- Distribute TTC (Timing, Trigger and Control) signals via fixed latency optical links.
- Route data from different links to configurable network end-points
- Support control, calibration and monitoring of sub-detectors.

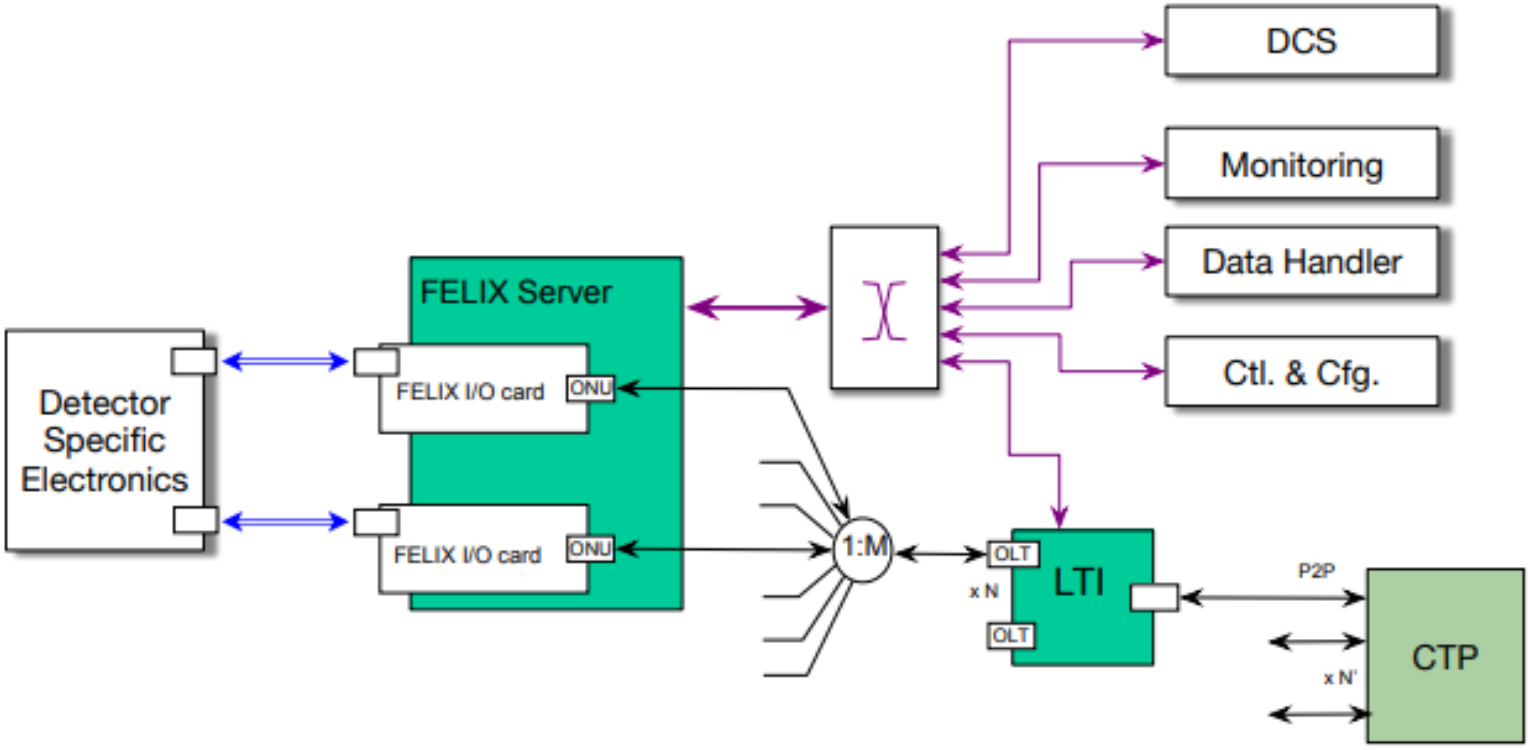




OFF DETECTOR ELECTRONICS

FELIX will interface with most of the ATLAS systems:

- Data handler → Event builder
- Detector Control System (DCS): LV current, temperature,...
- On-line monitoring
- Control and configuration of the FE ASIC



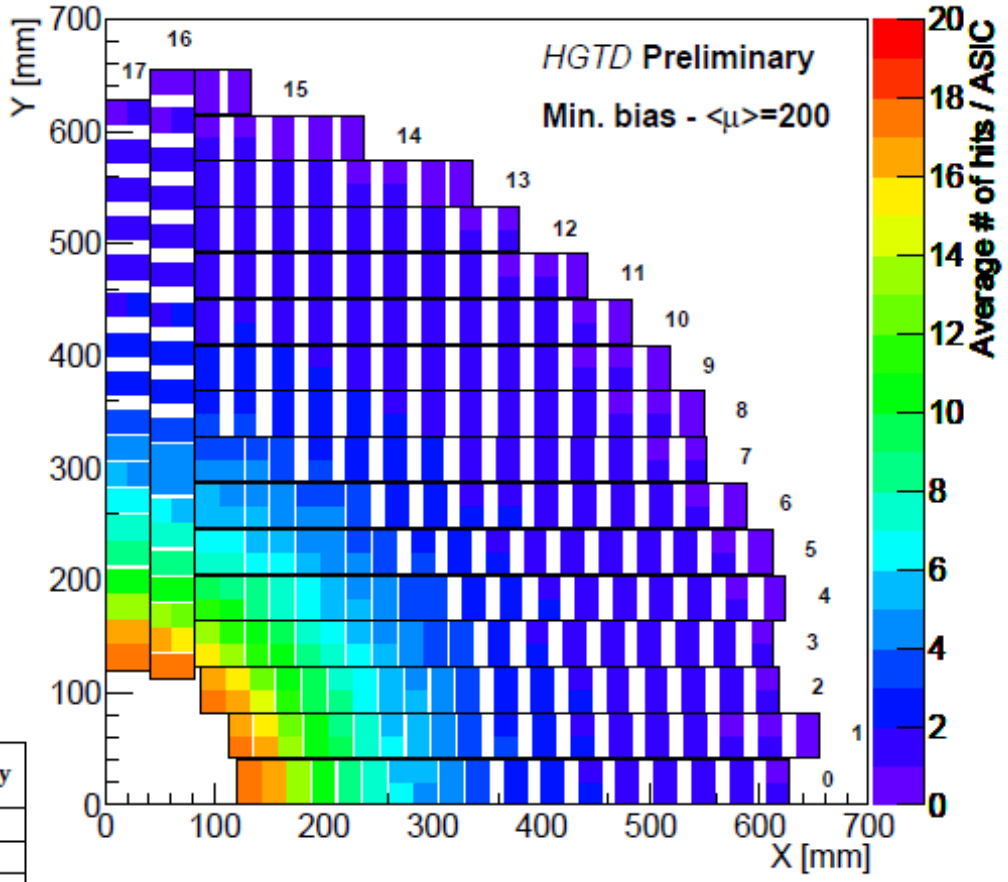
FELIX is going to be used in ATLAS during LHC Run3 (LAr and Small Wheel)

DAQ AND LUMINOSITY

Readout layout:

- Readout layout scales with HGTD occupancy:
  - r < 200 mm: Max occ = 20 hits → readout speed = 1280 Mbps
  - 200 < r < 320 mm: Max occ = 10 hits → readout speed = 640 Mbps
  - r > 320 mm: Max occ = 4 hits → readout speed = 320 Mbps

Peripheral board	Read out rows	Nb of modules	1.28 Gb/s	640 Mb/s	320 Mb/s	Luminosity
Front						
0	0-2	56	24	24	64	56
1	3-5	56	8	32	72	66
2	6-9	59	0	2	116	110
3	10-14	45	0	0	90	90
4	15-17	39	16	16	46	42
Back						
0	0-2	55	20	26	64	56
1	3-5	54	6	34	68	62
2	6-9	56	0	4	108	104
3	10-14	42	0	0	84	84
4	15-17	37	12	18	44	38

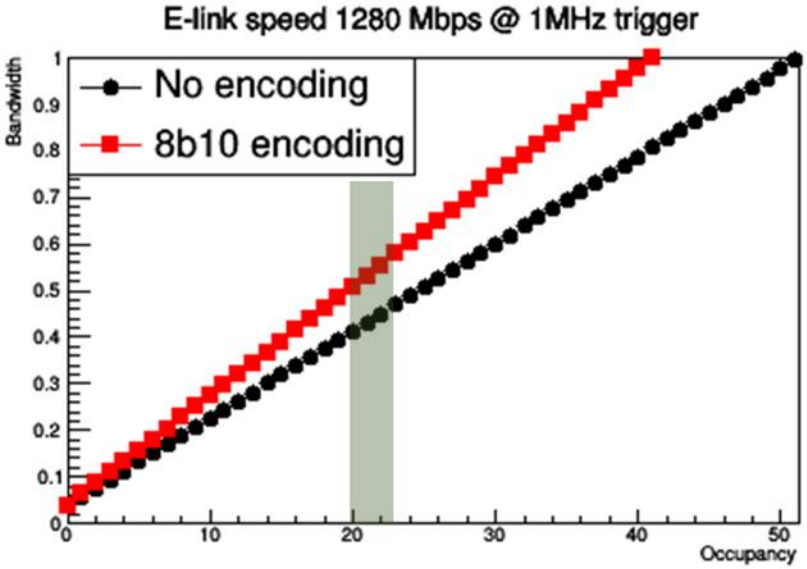


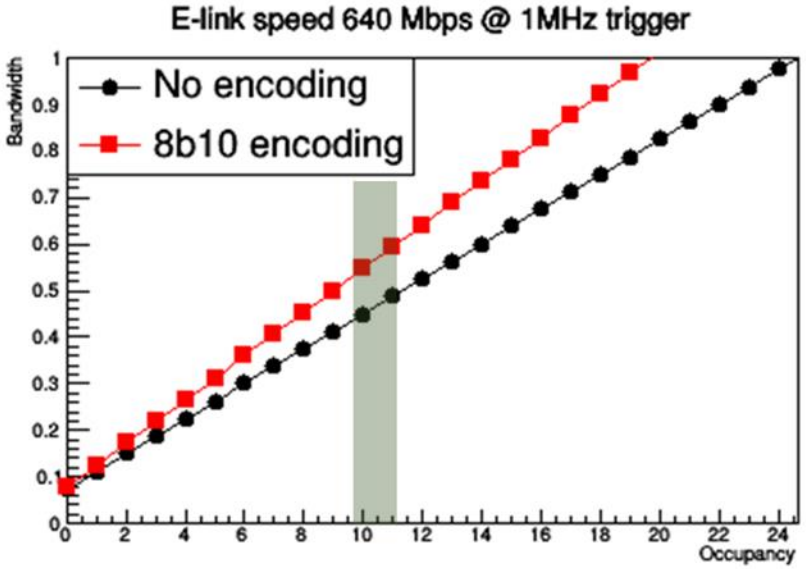
lpGBT #links/readout speed:

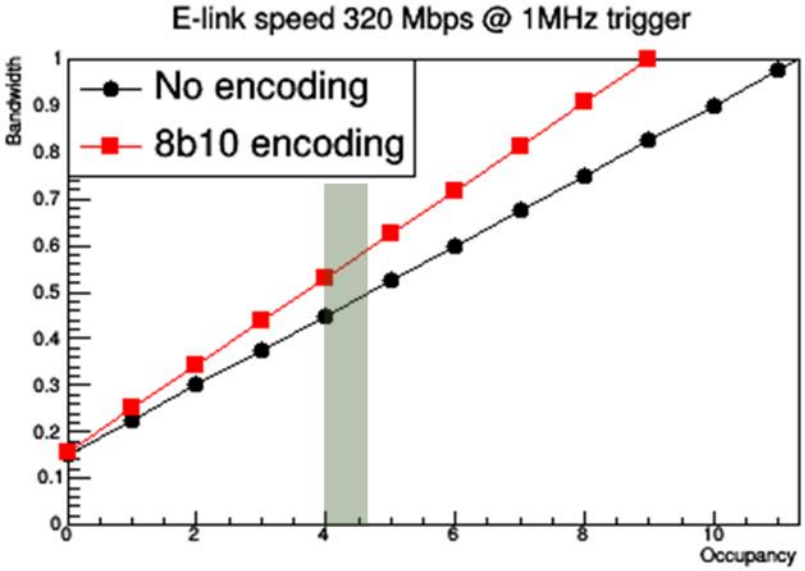
- 1280 Mbps → 6 links
- 640 Mbps → 12 links
- 320 Mbps → 24 links

DAQ AND LUMINOSITY

Expected link usage at different link speeds:





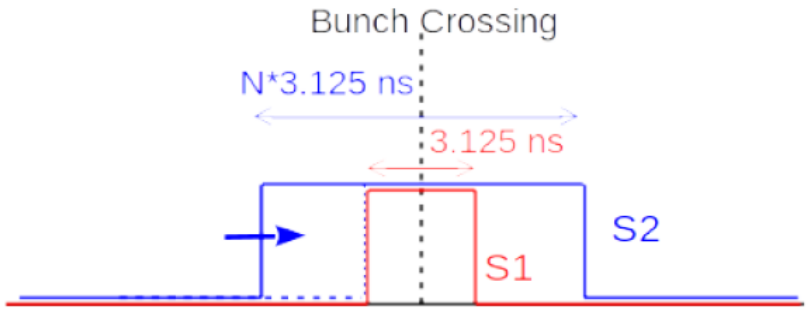


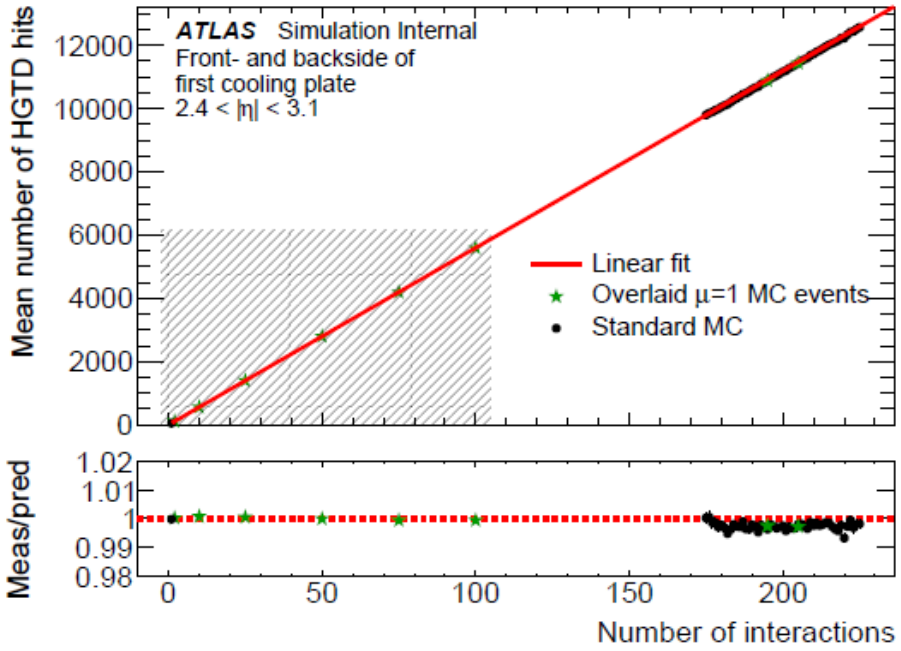
Upper limit on the number of hits/ASIC driven by the bandwidth
→ This is linked with the ALTIROC data format (see Jie Zhang talk)

DAQ AND LUMINOSITY

HGTD as luminometer:

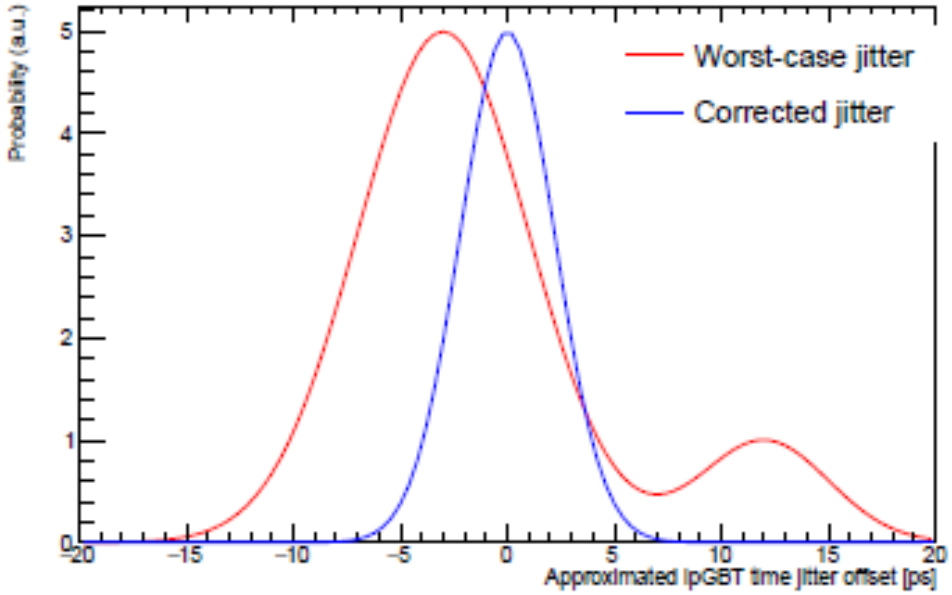
- Bunch by bunch information at 40 MHz
- Sum of the hits between two different time Windows (S1 and S2)
- Dedicated luminosity stream at 640 Mbps.
- Only a sub-sample of modules will be used for luminosity measurements 200 < r < 320 mm
- Luminosity data format still under discussion.
- Off detector readout: Dedicated FELIX lumi boards.





T0 calibration:

- Particularly challenging:
  - Bunch by bunch inhomogeneities in t0
  - Different sources of clock jitter: LHC, FELIX, lpGBT, ALTIROC,...
  - Dynamic contributions: Noise from the flex, day/night temperature changes,...
- A t0 calibration procedure is under study

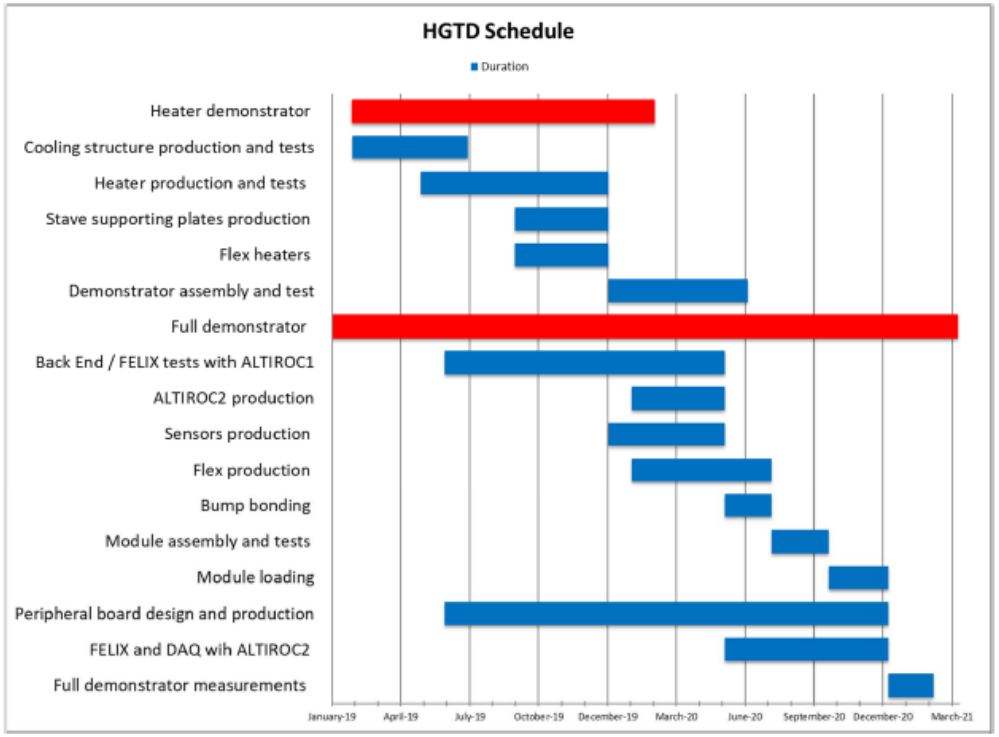


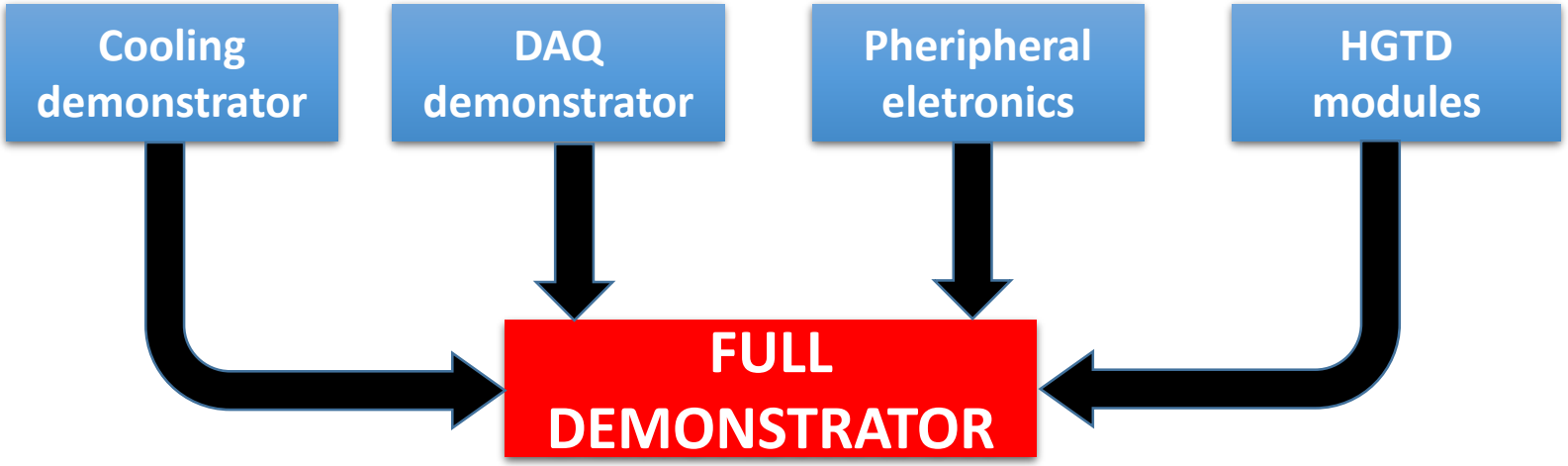
See Ludovica's talk on the t0 calibration

HGTD DEMONSTRATOR

Proof of concept:

- Cooling demonstrator with heaters → Validate termal model and loading procedure
- Mechanical structure and services
- HGTD modules
- DAQ/Luminosity demonstrator (FELIX+GBT)
- Peripheral electronics





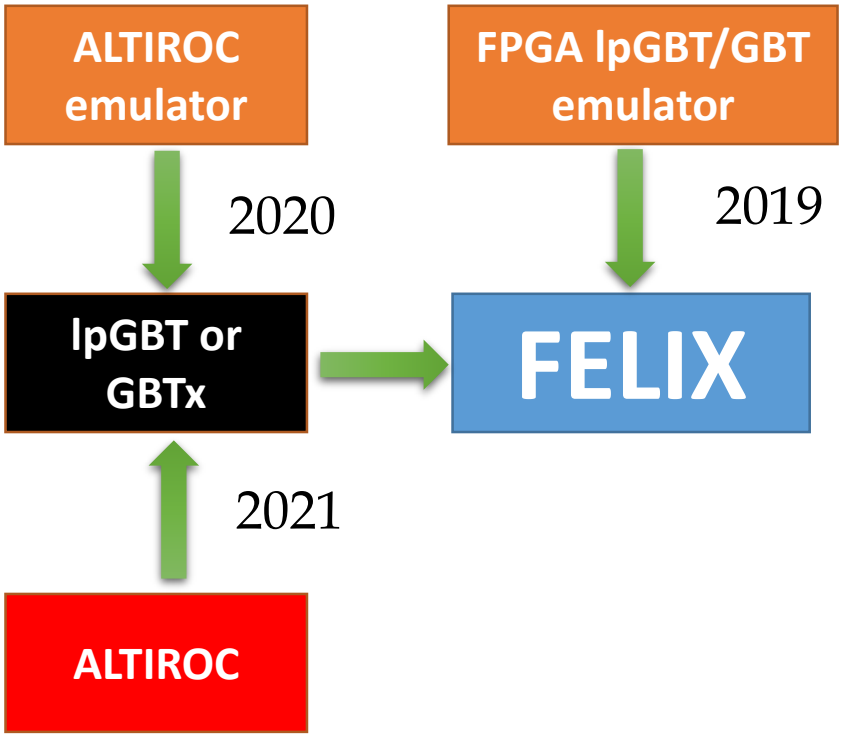
HGTD DEMONSTRATOR

DAQ demonstrator:

- 2019: Validation of FELIX readout with FPGA emulator
- 2020: Validation of lpGBT + ALTIROC emulator
- 2021: First test with ALTIROC modules

Further test:

- Measurement of clock jitter: FELIX+lpGBT+FLEX+ALTIROC
- Validate services (LV,HV,...)
- Develop a calibration procedure: FELIX + YARR (Yet Another Rapid Readout): Generic PCI SW and FW meant for calibrations.



FELIX board will arrive in July 2019 for first test

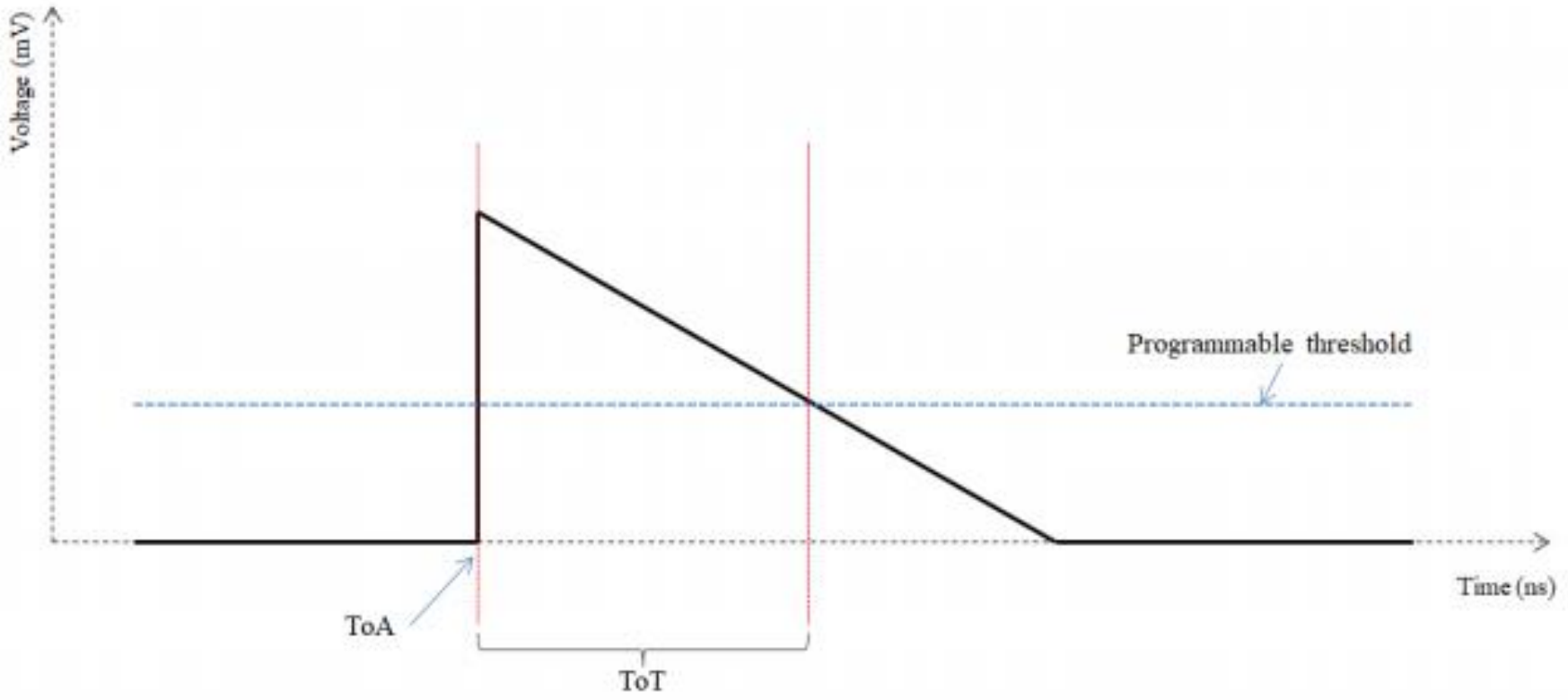
TO-DO LIST

- Front-end ATLIROC
  - Data format (Jie Zhang)
  - Command decoder: Fast command and configuration
  - Register readback
- Peripheral electronics:
  - PCB design and construction
  - Integration of lpGBT and Versatile link
- T0 calibration (Ludovica)
  - Study of bunch by bunch t0 drift
  - Measurement of the jitter performance after the FLEX
- DAQ demonstrator (myself):
  - FPGA lpGBT/GBT emulator
  - ALTIROC emulator
  - Interface with FELIX
  - Proof of concept of peripheral boards
  - Calibration procedure

WE WANT YOU!

BACKUP

ToA and ToT



BACKUP

Useful links:

- TDAQ requirements phase II: https://edms.cern.ch/ui/file/1563801/1/RequirementsPhaseII_v1.1.0.pdf
- lpGBT: https://espace.cern.ch/GBT-Project/LpGBT/default.aspx
- FELIX: https://atlas-project-felix.web.cern.ch/atlas-project-felix/
- HGTD: https://cds.cern.ch/record/2623663/files/LHCC-P-012.pdf
- YARR: https://yarr.readthedocs.io/en/latest/